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Benchmarking of FinFET, Nanosheet, and Nanowire FET Architectures for Future Technology Nodes

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ABSTRACT Nanosheet (NS) and nanowire (NW) FET architectures scaled to a gate length (L_G) of 16 nm and below are benchmarked against equivalent FinFETs. The device performance is predicted using a 3D finite element drift-diffusion/Monte Carlo simulation toolbox with integrated 2D Schrödinger equation based quantum corrections. The NS FET is a viable replacement for the FinFET in high performance (HP) applications when scaled down to L_G of 16 nm offering a larger on-current (I_{ON}) and slightly better sub-threshold characteristics. Below L_G of 16 nm, the NW FET becomes the most promising architecture offering an almost ideal sub-threshold swing, the smallest off-current (I_{OFF}), and the largest I_{ON}/I_{OFF} ratio out of the three architectures. However, the NW FET suffers from early I_{ON} saturation with the increasing gate bias that can be tackled by minimizing interface roughness and/or by optimisation of a doping profile in the device body.

INDEX TERMS Monte Carlo, Schrödinger quantum correction, FinFET, nanowire, nanosheet.

I. INTRODUCTION

Fin field effect transistor (FinFET) technology is the leading architecture for high performance (HP) applications. However, FinFETs will struggle to keep control of device electrostatics in future generations of complementary metal-oxide-semiconductor (CMOS) technology [1]. The eventual changeover to different architectures like nanosheet (NS) [2]–[5] or nanowire (NW) FETs [6], [7], and/or to different channel materials like Ge or III-Vs [8]–[10] requires thorough ground work. Therefore, physically-based 3D simulations play an essential role to benchmark the most promising candidates. Although many works already compared FinFET and NW FET architectures [2], [10]–[12], there are fewer that include a predictive physically based comparison of FinFET, NS and NW FETs [6], [13], [14]. These works use either drift-diffusion simulations [6] that cannot capture non-equilibrium carrier transport, or employ a quantum corrected Monte Carlo (MC) technique via a density gradient approach that requires calibration [7].

In this work, we will benchmark *n*-MOS transistors from the FinFET technology against the NS and NW FET solutions using VENDES, a 3D finite element (FE) quantum corrected MC and drift-diffusion (DD) toolbox with integrated 2D FE Schrödinger equation solver [15], [16]. The transistor dimensions and their shapes are precisely described by a simulation domain using FEs which assures that the accurate quantum mechanical confinement is considered in the carrier channel transport [17]. The three compared architectures of *n*-MOS transistors are assumed to have the same principal characteristics like the gate length, equivalent oxide thickness (EOT) of a high-κ dielectric layer, and *n*-type doping in the source/drain and *p*-type doping in the channel having its optimal orientation in the ⟨110⟩ crystallographic orientation

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(on the (100) Si substrate) [18], [19]. Their particular designs follow the ITRS 2.0 prescriptions [20] and experimental transistors reported for the FinFET [21], NW FET [12], [22], and NS FET [23]. The objective is to show how these different architectures measure up against each other analysing the influence of doping, the gate length (L_G) and the interface roughness (IR) in device performance via the main figures of merit: threshold voltage (V_T), sub-threshold swing (SS), off-current (I_{OFF}), on-current (I_{ON}), and I_{ON}/I_{OFF} ratio.

II. METHODOLOGY AND DESCRIPTION OF DEVICES

VENDES is a 3D FE physically-based simulation toolbox for nanoscaled devices [17], [24], [25] that integrates a 2D Schrödinger equation (SCH) based quantum corrected 3D DD method (SCH-DD) to study the sub-threshold region, and a 2D SCH quantum corrected 3D MC (SCH-MC) to study the transistor on-region. One advantage of using SCH based quantum corrections is that they do not require calibration unlike density-gradient (DG) based corrections [25]. The SCH quantum corrections do not include the source-to-drain tunnelling [26]. However, the source-to-drain tunnelling is negligible for the gate length of the study, 12 nm [7], [27]. The SCH-DD technique is beneficial at gate biases below the threshold voltage (V_T) because the current obtained from the SCH-MC is too noisy there. However, at larger gate biases, the SCH-MC is needed because non-equilibrium transport plays a major role in carrier transport. The SCH-MC simulations account for the following Si related electron scattering mechanisms: electron interaction with acoustic and non-polar optical phonons (intra- and inter-valley) [28], electron interaction with ionised impurity scattering using the third-body exclusion [29] with static screening and Fermi-Dirac statistics [30], and electron scattering with the IR using Ando's model [31] in which the effective electric field is obtained in a real space device domain [32]. The IR scattering, which is sometimes inaccurately called a surface roughness scattering, refers to the carrier scattering on a potential induced by the interface between semiconductor and dielectric material. The IR between the semiconductor and the dielectric is typically characterised by a root mean square height (RMS_{height}) of the roughness and the correlation length (λ_c) at which a roughness pattern re-occurs. The static screening model in the ionised impurity scattering uses Fermi energy and electron temperature self-consistently calculated from the electron density and the electron kinetic energy in the real space domain of a transistor [30], [33].

Fig. 1 shows the three device architectures (FinFET, NS and NW FETs) and their physical dimensions. The FinFET is designed using silicon-on-insulator (SOI) technology to minimise leakage current. The FinFET design aims to have a narrow width and a large height of its silicon body in order to achieve a large density of parallel transistors on the area of a chip. The gate-all-around (GAA) NW FET architecture is designed to have a tight gate control of electron transport through its silicon body to minimise the leakage current at very short gate lengths while still delivering the required drive

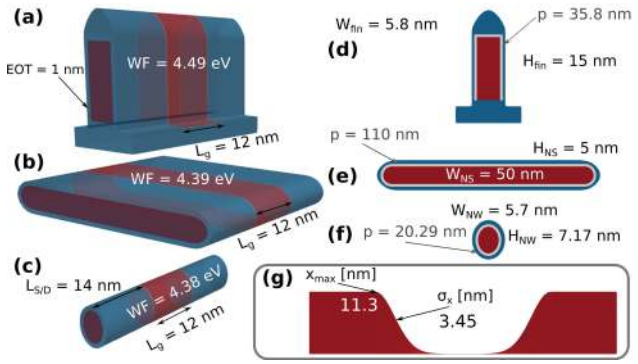

FIGURE 1. Schematics of the 12 nm gate length (a, d) FinFET, (b, e) NS and (c, f) NW FETs with device dimensions: physical gate length (L_G), physical source/drain length ($L_{S/D}$), channel width/height ($W_{\langle dev\rangle}$, $H_{\langle dev\rangle}$; $\langle dev\rangle$ = fin, NW, NS), effective oxide thickness (EOT), work function (WF), effective perimeter (p), and (g) Gaussian doping profile: lateral straggle (σ_x) and the end of maximum doping (x_{max}).

current using stacked NWs. The NS FET architecture aims to reuse, with minimal changes that are explained in detail in [23], the FinFET fabrication process by turning a high thin fin horizontally into a nanoscale sheet, because lateral epitaxial material growth can deliver smoother interfaces at the top and bottom of NS body.

The SOI FinFET and the NW FET in this benchmarking study are based on larger experimental devices with gate lengths of 25 nm [21] and 22 nm [22], respectively, which were scaled following the ITRS guidelines [20] as detailed in [17], [34]. The NS FET is based on an experimental device with a gate length of 12 nm and 44/48 nm contacted poly pitch (CPP) ground rules [23]. The transistor doping profile, essential to simulate the nanoscale transistors, is very challenging to acquire from experimental work. Therefore, we reversed engineered the *n*-type and *p*-type doping profiles in the 12 nm gate length NS FET. We assumed a uniform *p*-type doping (1.0×10^{15} cm^{-3}) in the device channel and a *n*-type Gaussian doping profile in the source/drain (S/D) regions (see Fig. 1 (g)). Three parameters were adjusted: (i) the maximum source/drain doping ($N_{S/D}$), (ii) the position (X_{max}) where the doping starts to decay from $N_{S/D}$, and (iii) the Gaussian lateral straggle (σ_{max}). This process is repeated until a good agreement is achieved in I_D-V_G characteristics between the experimental and the simulated data in the sub-threshold region obtained from the 3D SCH-DD. Further details on the reverse engineering process of doping profiles can be found in [34]. The best match was found for $N_{S/D}$ of 5.0×10^{19} cm^{-3}, X_{max} of 11.3 nm and σ_{max} of 3.45 nm. The comparison of our simulated I_D-V_G characteristics against the experimental data of the 12 nm gate length NS FET showed a very good agreement at a low drain bias of 0.05 V (see the results in [35]).

The SCH-MC simulations are then employed to verify the experimentally observed I_D-V_G characteristics in the on-region. Fig. 2 compares I_D-V_G characteristics of the simulated and the experimentally measured 12 nm gate length NS FET at a high drain bias of 0.7 V. These SCH-MC

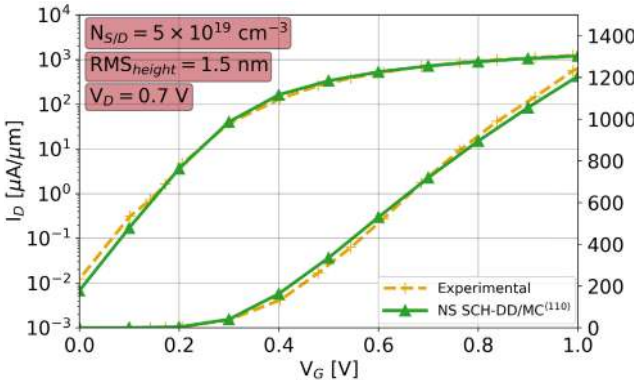

FIGURE 2. Simulated versus experimental [23] I_D-V_G characteristics, on both logarithmic (left) and linear (right) scales, for the 12 nm gate length NS FET at $V_D = 0.7$ V with a channel orientation of ⟨110⟩ assuming $RMS_{height} = 1.5$ nm in the IR scattering ($\lambda_c = 1.7$ nm). The $N_{S/D}$ is 5×10^{19} cm^{-3}.

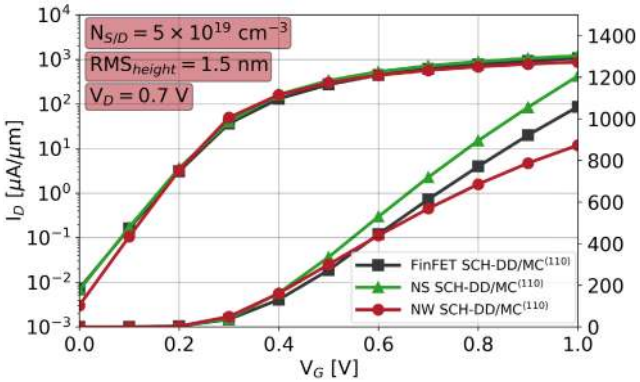

FIGURE 3. Simulated I_D-V_G characteristics, on both logarithmic (left) and linear (right) scales, for the 12 nm gate length FinFET, NS and NW FETs at $V_D = 0.7$ V with a channel orientation of ⟨110⟩ assuming $RMS_{height} = 1.5$ nm in the IR scattering ($\lambda_c = 1.7$ nm). The $N_{S/D}$ is 5×10^{19} cm^{-3}.

simulations assume that RMS_{height} is 1.5 nm and the λ_c is 1.7 nm in electron scattering with the IR induced potential. These parameters which specify the quality of the interface between the silicon channel and dielectric layer, the λ_c and mean square root of the height RMS_{height}, are typically not available from experimental work but the IR scattering has a great influence on the drain current in the on-region. Therefore, we have increased RMS_{height} in 0.5 nm steps as shown by I_D-V_G characteristics in Figs. 3, 4 and 5 until a good agreement is achieved by comparing the on-current against experimental data at $V_D = 0.7$ V (Fig. 2). The λ_c is assumed to be the same as for a nanoscale FinFET [17].

The benchmarking study considers that all three multi-gate architectures (FinFET, NS and NW FETs) are on the (100) Si substrate with the ⟨110⟩ channel orientation [19]. All the transistors have the same *n*-type and *p*-type doping profiles and their work functions were adjusted to provide the same threshold voltages when L_G is 12 nm. Finally, the simulated I_D-V_G characteristics at low and high drain biases from the MC simulations are in a very good agreement with the experimental characteristics, without further need to include access resistance in any additional

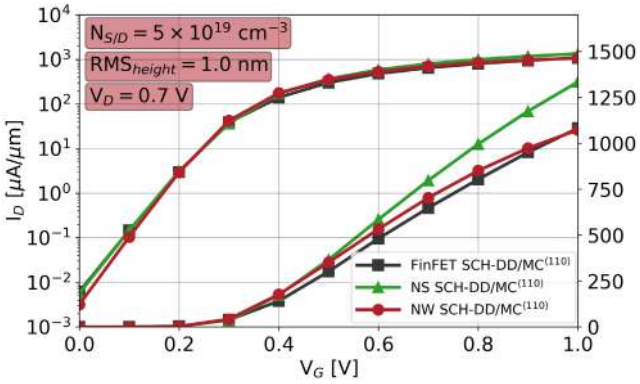

FIGURE 4. Simulated I_D-V_G characteristics at $V_D = 0.7$ V, on both logarithmic and linear scales, for the 12 nm gate length FinFET, NS and NW FETs with a channel orientation of ⟨110⟩ assuming $RMS_{height} = 1.0$ nm in the IR scattering ($\lambda_c = 1.7$ nm). The $N_{S/D}$ is 5×10^{19} cm^{-3}.

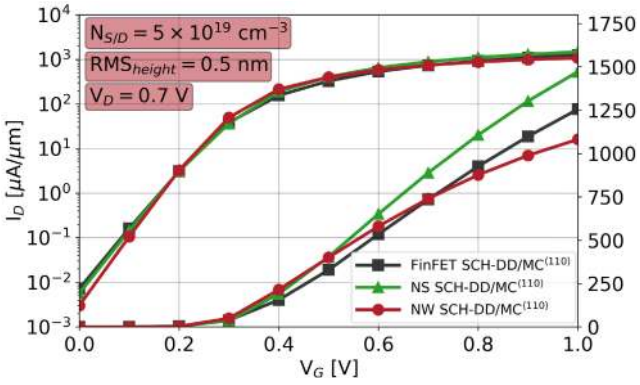

FIGURE 5. Simulated I_D-V_G characteristics at $V_D = 0.7$ V, on both logarithmic and linear scales, for the 12 nm gate length FinFET, NS and NW FETs with a channel orientation of ⟨110⟩ assuming $RMS_{height} = 0.5$ nm in the IR scattering ($\lambda_c = 1.7$ nm). The $N_{S/D}$ is 5×10^{19} cm^{-3}.

post-processing [17], [34]. The characteristics are directly obtained by time consuming SCH-MC simulations of electron transport in the transistor domain including electrons in the heavily doped source/drain that provides a correct electron distribution for their injection into device channel [17], [33], [36]. These accurate simulations of electron transport in the heavily *n*-type doped source/drain of multi-gate nanoscale transistors with governing electron-ionised impurity interaction use the static screening with self-consistent calculations of Fermi energy and electron temperature [30] in the real-space device domain [17], [34].

III. BENCHMARKS

A comparison of the 12 nm gate length FinFET, NS and NW FETs I_D-V_G characteristics is shown in Figs. 3, 4 and 5 at a drive bias (V_{DD}) of 0.7 V for the ⟨110⟩ channel orientation assuming an RMS_{height} of 1.5, 1.0 and 0.5 nm, respectively, and a λ_c of 1.7 nm. The figures of merit (FoM), summarised in Table 1, are extracted using FoMPy module [37], [38]. The V_T values are obtained using the constant current method set to $I_D = 2.0$ μA/μm. The off-current (I_{OFF}) is taken at $V_G = 0.0$ V, and the drive current (I_{ON}) at $V_G = V_{DD}$. Comparing the three architectures and assuming that the

TABLE 1. Threshold voltage (V_T), sub-threshold slope (SS), off-current (I_{OFF}), on-current (I_{ON}), and ON/OFF ratio (I_{ON}/I_{OFF}) for FinFET, NS and NW FETs with the same 12 nm gate length assuming IR scattering with a RMS_{height} of 1.5 nm and λ_c of 1.7 nm.

	$N_{S/D} = 5.0 \times 10^{19}$ cm^{-3}			$N_{S/D} = 1.0 \times 10^{20}$ cm^{-3}			$N_{S/D} = 1.5 \times 10^{20}$ cm^{-3}		
FoM	FinFET	NS	NW	FinFET	NS	NW	FinFET	NS	NW
V_T [V]	0.185	0.185	0.185	0.158	0.164	0.176	0.140	0.149	0.169
SS [mV/dec]	74	71	65	77	74	66	80	76	67
I_{OFF} [nA/μm]	7.0	5.7	3.0	19.0	13.3	4.6	36.1	23.5	6.2
$I_{ON}^{\langle 110\rangle}$ [μA/μm]	612	699	568	724	832	732	777	893	819
$\frac{I_{ON}}{I_{OFF}}(\times 10^5)$ $\langle 110\rangle$	0.87	1.2	1.9	0.38	0.63	1.6	0.21	0.38	1.3

maximum *n*-type S/D doping is $N_{S/D} = 5 \times 10^{19}$ cm^{-3}, the NW FET has the lowest SS and I_{OFF} which indicates excellent control by the gate. In the on-region, a saturation of the drive current in the NW FET starts at V_G of 0.6 V, leading to the lowest I_{ON} for the three compared devices. Despite this, the NW FET still delivers the highest I_{ON}/I_{OFF} ratio. These NW FET characteristics, together with the possibility of stacking them vertically [3], [6], [7], suggest that the NW architecture makes an excellent candidate for low power applications. The NS FET has an I_{ON}/I_{OFF} ratio 37% smaller than the ratio of the NW FET and delivers a slightly better performance in the sub-threshold than that of the FinFET. The NS architecture also has the highest I_{ON} indicating that the NS FET is a viable replacement for the FinFET in HP applications. The FinFET has an I_{ON}/I_{OFF} ratio 27% and 54% smaller than those of the NS and NW FETs, respectively. The FinFET has the largest SS and I_{OFF} due to a weaker control by the gate. However, previous works have shown that the FinFET architecture is more resilient to intrinsic variability than the NW FET one [36].

A. SOURCE/DRAIN DOPING

The drive current can be incremented by increasing the *n*-type S/D doping of $N_{S/D} = 5 \times 10^{19}$ cm^{-3} to 1×10^{20} cm^{-3} and 1.5×10^{20} cm^{-3} but with detrimental impact on the sub-threshold region related FoM (see Table 1). Increased S/D doping results in a lower V_T value, for all three devices. On the other hand the SS, along with I_{OFF}, increases for all the architectures. The NW FET is the most resistant against sub-threshold deterioration as the S/D doping is increased. The V_T decreases by 16 (−8.6%), 26 (−19.5%) and 35 (−24%) mV for the NW FET, NS FET and FinFET, respectively, as the $N_{S/D}$ is increased from 5×10^{19} cm^{-3} to 1.5×10^{20} cm^{-3}. The same change in $N_{S/D}$ results in an increase of SS by 3%, 7% and 8% for the NW FET, NS FET and FinFET, respectively. Finally, the I_{OFF} is increased by 2.1, 4.1 and 5.2 times for the NW FET, NS FET and FinFET, respectively. In case of the on-region, the I_{ON} is increased by 44%, 28% and 27% for the NW FET, NS FET and FinFET, respectively. Moreover, the I_{ON} saturation in the NW FET occurs at larger applied biases due to a reduction of series resistance in the S/D region, opening a possibility of *n*-type S/D doping engineering of NWs to achieve a better I_{ON} with only a slight deterioration in the sub-threshold characteristics. The overall performance enhancement is compared through the I_{ON}/I_{OFF} ratio and we found that it decreases by −32%, −68% and −76% for the NW FET, NS FET and FinFET, respectively, as we increased the $N_{S/D}$ from 5×10^{19} cm^{-3} to 1.5×10^{20} cm^{-3}.

With an increase in the *n*-type S/D doping, the NW FETs still provide the largest I_{ON}/I_{OFF} ratio among the three compared architectures, although the NS FETs still deliver the largest I_{ON}. An increase in $N_{S/D}$ affects the performance of the FinFET the most, leading to the worst sub-threshold characteristics and the lowest I_{ON}.

B. INTERFACE ROUGHNESS

Further improvement of device performance can be achieved through fabrication processes that reduce the IR [39] by either making the λ_c longer or minimising the RMS_{height}. One advantage of reducing the RMS_{height} is the increase in I_{ON} without deterioration in the sub-threshold characteristics. Therefore, we study the effect of decreasing the RMS_{height} from 1.5 nm (see Fig. 3) to 1.0 nm (see Fig. 4) and to 0.5 nm (see Fig. 5) for a maximum *n*-type S/D doping of $N_{S/D} = 5 \times 10^{19}$ cm^{-3}. The NW FET shows the largest increase in I_{ON}, 15.8% (30.1%), for the RMS_{height} of 1.0 nm (0.5 nm). The NS FET increases its I_{ON} by 14.2% (27.3%) for the RMS_{height} of 1.0 nm (0.5 nm). The FinFET shows the smallest increase in I_{ON} of the three devices, 10.1% and 19.9%, for the 1.0 and 0.5 nm RMS_{height}, respectively. The NW FET cross-section (perpendicular to the transport direction) has a larger perimeter-conduction area ratio in the semiconductor than that of the other two architectures. This, together with the fact that this architecture is more affected by volume inversion [40], explains why the NW FET is more sensitive to IR scattering.

The average electron velocity along the channel from the source to the drain at $V_G = 0.7$ V and $V_D = 0.7$ V for the three studied transistor architectures, looking into two possible RMS_{height} of 1.5 nm and 0.5 nm, is shown in Fig. 6. The largest average electron velocity is observed in the NS

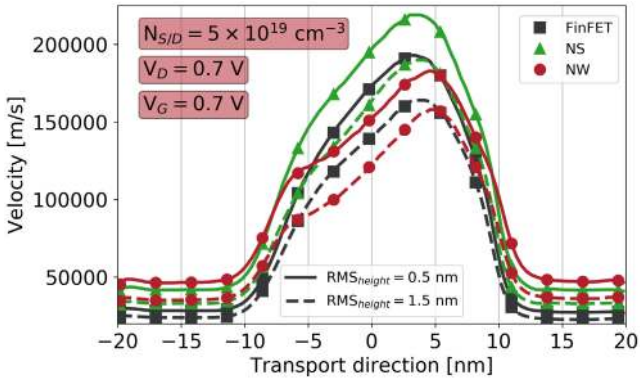

FIGURE 6. Average electron velocity in the transport direction at $V_G = 0.7$ V and $V_D = 0.7$ V for the 12 nm gate length FinFET, NS and NW FETs with $RMS_{height} = 0.5$ and 1.5 nm and a fixed λ_c of 1.7 nm.

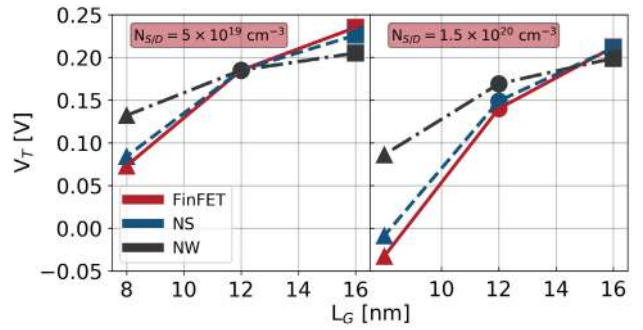

FIGURE 7. Threshold voltage (V_T) vs. gate length (L_G) for the Fin, NS and NW FETs at fixed gate metal workfunctions. The gate metal workfunctions of the three transistors are adjusted to provide the same V_T at the 12 nm gate length with $N_{S/D} = 5 \times 10^{19}$ cm^{-3}. The results are for $N_{S/D} = 5 \times 10^{19}$ cm^{-3} (left) and $N_{S/D} = 1.5 \times 10^{20}$ cm^{-3} (right).

FET, followed by the FinFET and the NW FET. The reduction in the RMS_{height} from 1.5 nm to 0.5 nm can result in an increase of the maximum electron velocity by about 12% in the 12 nm gate length NS FET and FinFET and by 10% in the equivalent NW FET.

C. GATE LENGTH

Finally, we study the effect of the L_G in the three device architectures. Fig. 7 shows threshold voltage vs. gate length for the three studied multi-gate architectures at two different maximum S/D dopings assuming fixed gate metal workfunctions. All three transistors have identical V_T at the 12 nm gate length for $N_{S/D} = 5 \times 10^{19}$ cm^{-3} as seen in Fig. 7 (left). The threshold voltage of the scaled FinFETs and NS FETs are very close because the two architectures have very similar quantum-mechanical confinement, providing them with comparable quantum gate capacitance. The NW FET has the strongest quantum-mechanical confinement in the body which makes this architecture more resilient to the gate length scaling. The negative V_T observed for the 8 nm gate length Fin and NS FETs are a result of the fixed metal gate workfunctions adjusted to provide the same V_T for the 12 nm gate length transistors (at a $N_{S/D} = 5 \times 10^{19}$ cm^{-3}) and can be mitigated by metal gate workfunction engineering. Furthermore, as L_G is scaled down, the SS increases

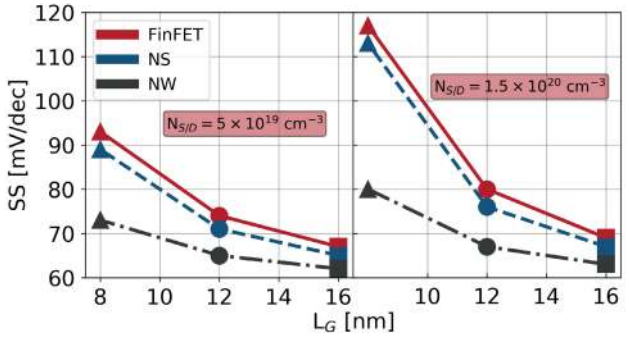

FIGURE 8. Sub-threshold swing (SS) vs. gate length (L_G) for the Fin, NS and NW FETs. The results are for $N_{S/D} = 5 \times 10^{19}$ cm^{-3} (left) and $N_{S/D} = 1.5 \times 10^{20}$ cm^{-3} (right).

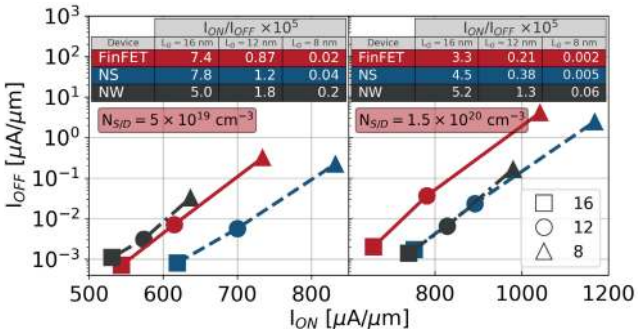

FIGURE 9. Off-current (I_{ON}) vs. on-current (I_{OFF}) for the 16, 12 and 8 nm gate length Fin, NS and NW FETs for $N_{S/D} = 5 \times 10^{19}$ cm^{-3} (left) and $N_{S/D} = 1.5 \times 10^{20}$ cm^{-3} (right). The I_{ON}/I_{OFF} ratios are also shown.

more dramatically in the FinFETs and NS FETs than in the NW FETs due to a weaker gate control over electron transport along the channel (see Fig. 8). The SS itself and its relative increase following the scaling down is more pronounced as the maximum n-type S/D doping is increased to 1.5×10^{20} cm^{-3}. Fig. 9 shows the I_{OFF} vs. I_{ON} for the two extreme dopings. For the three devices, both the I_{ON} and I_{OFF} increase following a linear trend when L_G is reduced. At the lower S/D doping of 5.0×10^{19} cm^{-3}, the 16 nm gate length NS FET has a 36% better I_{ON}/I_{OFF} ratio than the same gate length NW FET and the I_{ON}/I_{OFF} ratio of the 16 nm gate length FinFET is slightly lower (−5%) than that of the equivalent gate length NS FET. However, the NW FET has the largest I_{ON}/I_{OFF} ratio as the L_G is scaled below 16 nm (see Fig. 9). As the S/D doping is increased, the NW FET has also the highest I_{ON}/I_{OFF} ratio for all the investigated L_Gs.

IV. CONCLUSION

We have benchmarked the FinFET architecture against two possible alternatives, NS and NW FETs, to provide guidance towards the development of future multi-gate silicon technology nodes. The NS FET can be an excellent alternative to the FinFET for various digital applications because it offers a higher I_{ON} and slightly better sub-threshold region characteristics while reusing a similar fabrication process. However, sub-threshold characteristics of the NS FET and the FinFET deteriorate more than those of the NW FET for L_G scaled below 16 nm, so a change of transistor architecture to the NW

will be essential. The NW FET offers reduced I_{OFF}, a nearly ideal SS, and a much better I_{ON}/I_{OFF} ratio than those of the NS FET and the FinFET at L_G of 12 nm and 8 nm. However, the NW FET provides a much lower I_{ON} with respect to the on-current in the NS FET but the I_{ON} can be substantially increased by a reduction in the IR scattering (by decreasing RMS_{height} or by increasing the λ_c of the IR), and/or by an increase in the *n*-type S/D doping. Finally, both the NS and NW FETs are stackable thus offering the same or even larger density of transistors on the same die area when compared to the side-by-side placement of FinFETs.

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