Bending induced electrical response variations in ultra-thin flexible chips and device modeling

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APPLIED PHYSICS REVIEWS—FOCUSED REVIEW

Bending induced electrical response variations in ultra-thin flexible chips and device modeling

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Electronics that conform to 3D surfaces are attracting wider attention from both academia and industry. The research in the field has, thus far, focused primarily on showcasing the efficacy of various materials and fabrication methods for electronic/sensing devices on flexible substrates. As the device response changes are bound to change with stresses induced by bending, the next step will be to develop the capacity to predict the response of flexible systems under various bending conditions. This paper comprehensively reviews the effects of bending on the response of devices on ultra-thin chips in terms of variations in electrical parameters such as mobility, threshold voltage, and device performance (static and dynamic). The discussion also includes variations in the device response due to crystal orientation, applied mechanics, band structure, and fabrication processes. Further, strategies for compensating or minimizing these bending-induced variations have been presented. Following the in-depth analysis, this paper proposes new mathematical relations to simulate and predict the device response under various bending conditions. These mathematical relations have also been used to develop new compact models that have been verified by comparing simulation results with the experimental values reported in the recent literature. These advances will enable next generation computer-aided-design tools to meet the future design needs in flexible electronics.
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I. INTRODUCTION

The last decade has witnessed tremendous advances in flexible and conformable electronics. Many applications have benefited and numerous new applications will arise from electronics that can bend and conform to three-dimensional curvilinear shapes. For example, vital medical devices (e.g., retinal implants, pacemakers, and prostheses), intelligent clothing, flexible displays, robotics, and numerous wearable gadgets, which are needed to enable advances in emerging fields such as Internet of Things, robotics, and healthcare, will all require bendable and conformable electronics.[1–11] As for any new technology, the electronics over bendable substrates has its own share of challenges, a few of which (e.g., related to fabrication over large areas and integration on diverse flexible substrates[12]) have already received significant attention. With the field advancing

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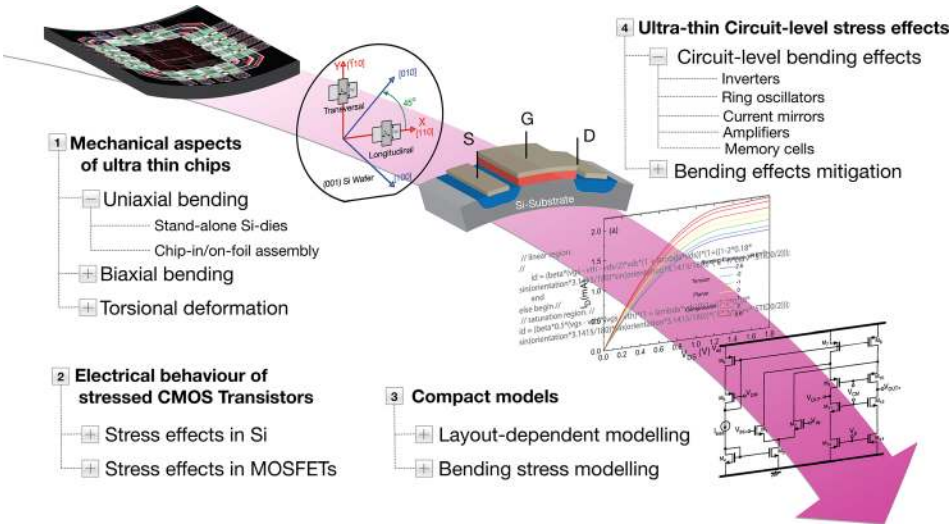

FIG. 1. Graphical overview of this review.

towards circuits and systems, the new set of challenges that require attention are related to reliable and uniform operation of flexible integrated circuits (ICs) under various bending states. Numerous parameters such as the crystal structure of the electronic substrate, the design of devices and circuits and their layout with respect to various crystal axes, and the energy band structure are affected by bending induced stresses and strains through variations in electrical parameters such as charge carrier mobility and threshold voltage. The bending induced effects can bring significant deviation in the response of flexible electronics from their designed values and may influence their effective use in the target application. Therefore, it is critical to understand the behavior of devices and circuits under different bending conditions and the interplay between mechanics, solid-state physics, and electrical and electronic inputs. A few articles have reported some of the stress-induced effects,[13] but the modelling of such variations, for example, to enable future computer aided design (CAD) tools, has not been reviewed so far. This paper will fill this gap by using studies related to electronic devices on ultra-thin chips (UTCs) made from silicon (Si). The goals of this survey paper are to: (1) review various types of bending and related induced stresses experienced by the UTCs and their analytical relationships. Various deformation types, modes of stresses (static and dynamic), surface orientations, device channel directions, and gate electric fields are considered. While the primary focus is on the bending-induced stress, the fabrication process-induced effects are also discussed for the sake of completeness; (2) review the impact of different types of stresses on the DC behavior of electronic devices and gain insights into energy band structure and transport properties; (3) correlate the bending induced stress with the variations in the output of devices and circuits; and (4) advance CAD tools by presenting new compact models. The proposed device models follow the comprehensive studies based on changes in the electrical parameters of strained transistors. The challenges in circuit simulation and implementation have been identified. As flexible electronic systems are often unconstrained during bending, the terms stress and strain are used interchangeably throughout this paper.

A visual summary of this paper is given in Fig. 1. The paper is organized as follows: Sec. II presents a historical perspective of the field. The mechanical aspects of various types of bending, including uniaxial, biaxial, and torsional deformations, experienced by UTCs are presented in Sec. III. Section IV describes the electrical behavior of Si resistors and transistors during bending and the effect of bending-induced stress on electrical parameters of devices on UTCs. A survey of compact modeling of stress effects on complementary metal-oxide-semiconductor (CMOS) is given in Sec. V followed by a detailed analysis of the stress effects at the circuit-level given in Sec. VI. Finally, outlook and concluding remarks are put forward in Sec. VII.

II. HISTORICAL PERSPECTIVE

From the historical perspective, the field of flexible electronics has grown exponentially as evidenced by the trend in Fig. 2, which is based on the number of publications in this

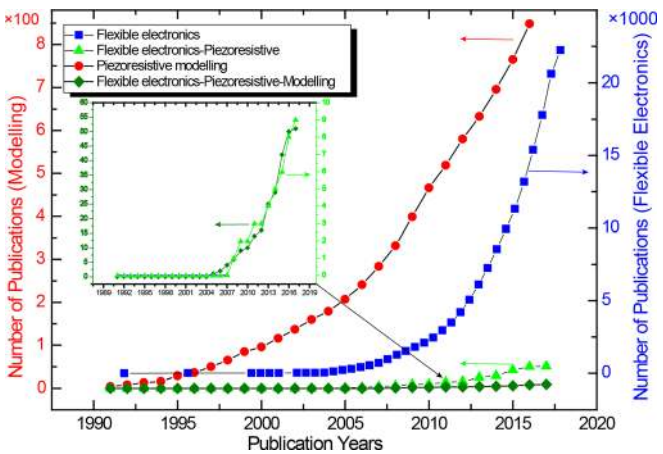

FIG. 2. Plots showing publications since 1991 in the field of flexible electronics (y-axis on the right side), piezoresistive effects in all types of devices, i.e., planar as well and non-planar (y-axis on left side), modeling of devices responses in all types of devices after considering the piezoresistive effect (y-axis on the left side), and the modeling of device responses in all flexible electronic devices after considering the piezorsistive effect (y-axis on the left side). The data were extracted from Web of Science by searching keywords such as flexible electronics and modelling.

field since the early 1990s. The stress/strain or the piezoresistive effect related modeling of the response of devices based on various semiconducting materials also has a similar trend over the same period. However, until about 2005 the piezoresistive effect related studies were mainly based on electronics on planar and non-flexible substrates and they were carried out for different motivations—ranging from optimization of the fabrication process to enhancing the performance. For example, substrate-induced (global) or process-induced (local) uniaxial straining of Si, Ge-, and III-V (e.g., GaAs) alters the band structure so as to enhance the performance of metal-oxide-semiconductor field-effect-transistors (MOSFETs).[14–22] A few review articles have covered aspects such as uniaxial and biaxial strain on carrier mobility in MOSFETs,[23–26] with a theoretical analysis of the physics of strained MOSFETs for different wafer surface orientations, channel directions, gate electric fields, and materials.[23,24,26] These studies have positive implications for similar investigations in bendable or flexible electronics. For example, they tell us that the mechanical stresses are not always detrimental, as conventionally considered. When applied in a controlled manner, the stresses or strain can also enhance the device performance as happened during the transition from micro to nanotechnology when straining of Si became an effective tool to attain improved device performance.[23,27–32] In fact, as explained in Sec. IV, the gains from studies on stress related variations can be higher in the case of flexible electronics as the stress-induced variations in device performances could be exploited to predict more than the just the response of devices under various bending conditions. For example, the responses of devices spread on flexible substrates carry a signature of the shape of the substrate, and mapping these variations during bending could be exploited to obtain more information about UTCs than just getting the electrical responses. A combined outcome of these wide range of studies on stress/strain or piezoresistive effects has been a number of methods that are either used to minimize or compensate (e.g., when stress/strain is considered detrimental) the thermo-mechanical stresses during the chip fabrication assembly and packaging operations[33–35] or methods to improve performance or obtain more information about electronic substrate (e.g., when stress/strain adds value).

The modeling of piezoresistive and bending induced effects in flexible electronics is relatively a new development,[36] as can be noted from Fig. 2. A few papers have reported limited analysis related to the effects of externally applied stresses on device modeling and simulation.[37] These include studies based on limited types of bending such as uniaxial stress-induced effects and using them to propose compact models and SPICE simulations.[38,39] However, many other stress effects such as those related to external applied biaxial and shear stress are yet to be investigated. An in-depth analysis of such effects and their modeling, as presented in this review article, will consolidate the field and potentially boost the research on this topic, which, at the current rate, is expected to yield about 100 publications by the year 2020 (Fig. 2). A general theory about the effects of bending will also enable new CAD tools which are needed to analyze bendable ICs prior to the manufacture and to develop mitigation strategies. The optimum IC design for flexible electronics requires complete understanding and accurate compact modeling of external-induced stress effects in complementary metal-oxide-semiconductor (CMOS) devices.[23]

III. ULTRA-THIN CHIPS AND MECHANICAL BENDING

To understand the limits of reliable operation of UTCs, it is important to examine their mechanical properties in terms of bending strength, bending direction, thickness, and defect formation and failure. UTCs with thicknesses $<20\,\mu$m have been explored by many groups to obtain a compact high-performance flexible electronics by using techniques such as post-process wafer thinning by grinding or chemical etching[30,40] (e.g., Circonflex process[41]) and porous Si (e.g., Chipfilm™ technology[42]). The strength of UTCs varies with the methods adopted to obtain them.[30,43] For example, the 15–20 μm thick plasma treated UTCs have the highest strength of 2.34 GPa and can bend to $R_{min} = 2.5$ mm. On the other hand, the UTCs obtained by grinding and polishing can be deformed up to $R_{min} = 33$ mm. The UTCs obtained with the Dicing-by-Thinning process show the mechanical strengths ranging between 1.5 and 1.9 GPa for 70 μm thick samples (and between 1.6 and 2.7 GPa for 48 μm thick die).[44] The flexible electronic systems are fabricated either (i) directly on flexible substrates (e.g., glass, steel, polyimide)[45–49] by processing methods such as batch[50] and roll-to-roll[46,51–57] or (ii) first on rigid substrates using the existing planar Si fabrication process and then transferred onto mechanically compliant substrates such as flexible plastic/polyimide foils.[30,42] As mechanical properties of various materials are different, the role they play in the variation of device performance during bending could vary and this needs to be considered as well.

The mechanical strength of UTCs could also vary with the packaging type or with the degree of electronics present on them. For example, the UTCs mounted on compliant polymers with epoxy glue or encapsulated between polymeric layers can undergo multiple reversible bending and stretching.[58–61] The 3-point bending [3PB, shown in Fig. 4(a)] tests (initially developed to test thick samples for fracture strength[62–65]) on 8 μm thick UTCs reveal a mechanical strength of ~3 GPa.[66] Similar tests on UTCs embedded in flexible foil substrates[67] show an increase in fracture strength of up to ~190% and a higher curvature of bending—which is up to ~85% more than the UTCs which are not embedded in flexible substrates.[67] Similarly, the mechanical strength of UTCs varies with the degree of electronics present on them. For example, 4-point bending [4PB, shown in Fig. 4(b)] tests have revealed that the blank (i.e., without active electronics) UTCs are mechanically stronger than those with CMOS circuitry.[43,53,55,56]

UTCs can experience different types of deformations such as tension (the body is subjected to pull), compressive (the body is under compression), shearing (when the external load tends to make a part of the body to slide on the other one), and torsional (when the external load tends to twist the body around an axis).[68] These deformation can be quantified in terms of stresses and strains having components such as

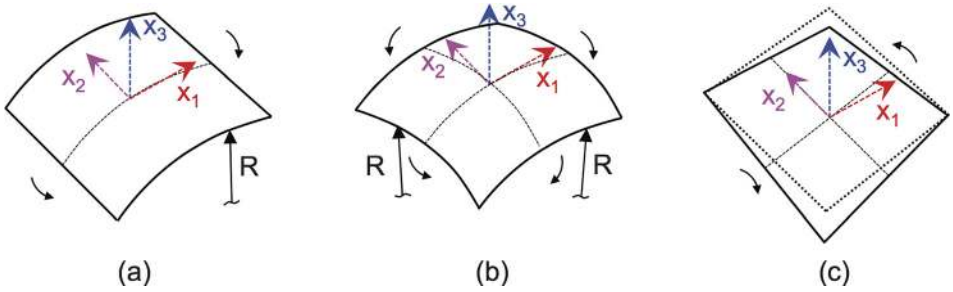

FIG. 3. Distortion of the central-surface of an ultra-thin chip because (a) uniaxial bending along x_2, (b) biaxial bending with respect to the x_1 and x_2, and (c) torsion with respect to x_1. (x_1; x_2; x_3) is the Cartesian coordinate system and R is the radius of curvature.

uniaxial, biaxial, and torsional, as shown in Fig. 3.[68] Their analysis in UTCs is essential to: (a) understand the strength (the capacity to withstand strain and stress without breaking), stiffness (how much the system deforms and how is the load transferred within it), failure (mechanisms, causes, and modes), and stability (reliability of the equilibrium) limits, (b) design of multilayered structures such as 3D ICs, and (c) accurately characterize the CMOS devices. Assuming plane stresses, for a (x_1, x_2) plane the stress tensor can be expressed as (engineering notation) as[69]

$$\boldsymbol{\sigma} = \begin{bmatrix} \sigma_{11} & \tau_{12} \\ \tau_{21} & \sigma_{22} \end{bmatrix}, \tag{1}$$

where σ_{ij} (i = j) are the normal stress components and τ_{ij} (i ≠ j) denote the shear stress components. These components depend on the coordinate system and vary from point to point inside the material.

In addition, residual internal stresses, developed during fabrication, are also present as evident from the warpage in UTCs.[66,70,71] The mechanical properties of UTCs differ from their bulk counterparts due to differences in processing, size, material composition, and microstructure.[72–74] A comparison of Young's modulus E and the Poisson's ratio ν[68] of several materials frequently used in flexible electronics [e.g., single-crystal Si, hydrogenated amorphous (a-Si:H), hydrogenated nanocrystalline Si (nc-Si:H), polycrystalline Si, Kapton®, and polyethylene naphthalate (PEN)] is given in Table I.[75–82] The experimental techniques that have been used to study mechanical aspects of UTCs include (i) direct methods[83,84] such as x-ray diffraction[85,86] and micro-Raman spectroscopy[87,88] and (ii) indirect methods based on measuring the curvature[89] (e.g., optical interferometry,[90] laser scanning,[91,92] and microscope image monitoring in real time[43]). The subsection below presents the uniaxial and biaxial bending in UTCs.

TABLE I. Young's modulus and Poisson's ratio of some materials of interest.

Material	E-Modulus (GPa)	Poisson's ratio ν
$Si_{\langle 110\rangle/(001)}$[75,76]	168.9	0.064
$Si_{<100>/(001)}$[75,76]	130.2	0.279
a-Si[77]	136 ± 9	…
a-Si:H (10% H)[78]	150	0.2
a-Si:H (15% H)[78]	130	0.2
a-Si:H (20% H)[78]	110	0.2
nc-Si:H (SiH_4 4sccm/10sccm)	25–45/55–70	…
Poly-Si[76,79]	158 ± 10	0.22 ± 0.01
Epoxy Epotek 301-2[80]	3.66 ± 0.04	0.358
Polyimide Kapton[81]	5.37	0.320
PEN[221]	5–6	0.3–0.4

A. Uniaxial bending of UTCs

Uniaxial deformation occurs when the applied bending moment(s) deforms the UTC sample along an in-plane axis [e.g., x_1, as shown in Fig. 3(a)]. In the 3PB test, an external load (uniformly distributed force **F**) is applied transversely along the middle line of the chip [Fig. 4(a)], where the induced uniaxial stress is maximum.[93,94] For small deflections, the maximum uniaxial stress, calculated using beam and plate bending theories, can be expressed as[68,95,96]

$$\sigma_{11}^{max} = \frac{3}{2} \cdot \frac{Fb}{Bh^2}, \tag{2}$$

where F is the applied uniform distributed force, b is the distance between the two internal points (Fig. 4), and h and B are the thickness and width of the plate, respectively. The thinner the chips are the more they deform. The finite element method (FEM) simulations indicate that the load-deflection relationship is non-linear at large deformations.[44,97,98] Not much has been reported in the literature about the analytical models that capture the nonlinear relationship between loading force and maximum stress. The 4PB test is another alternative to characterize the UTCs, which is preferred sometimes because of better load distribution between the supports to prevent the UTCs from failing prematurely.[99] In this case, each point of the cross-section suffers both a rotation around the x_2-axis and a displacement along the x_3-axis.[100] A uniform uniaxial stress σ_{11} is induced within the region between the two supports—tensile and maximum at the top of the sample, compressive and maximum at the bottom surface, and zero at the position of the neutral surface (red dashed line). In the case of UTCs, the curvature becomes very large and non-linear effects also appear. As a result, σ_{11} is calculated as[101]

$$\sigma_{11} = E \cdot x_3 \cdot \frac{1}{R} = E \cdot x_3 \cdot \frac{\partial^2 w / \partial x_1^2}{\left(1 + (\partial w / \partial x_1)^2\right)^{3/2}}, \tag{3}$$

where R is the radius of curvature, E shows the Young's Modulus, and w is the beam displacement. The parameters are measured experimentally[43] or determined theoretically from FEM simulations[102] and x_3 is the coordinate along the out-of-plane direction.

In the case of UTCs packaged or embedded in thin foils,[103] several other factors, including increased thickness and the bonding/embedding, influence the bendability as compared to the blank or stand-alone dies. The controlled bending of such chips during characterization is achieved by

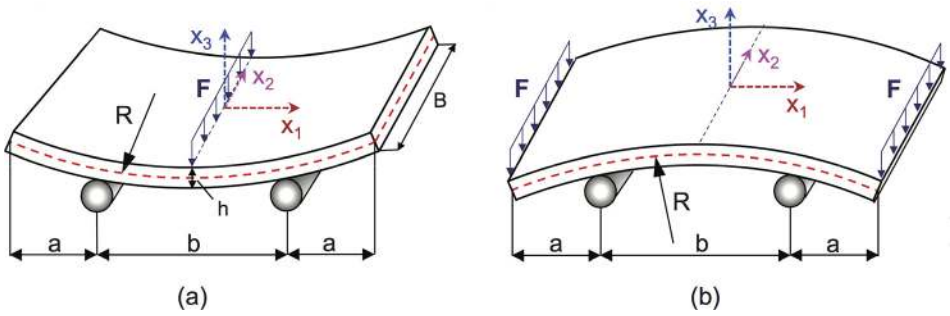

FIG. 4. Classical flexural tests: (a) three-point bending (3PB) and (b) four point bending (4PB). F is the applied uniform distributed force. The neutral surface coincides with the middle plane of the plate and is shown in red.

conforming them to a cylinder and then applying a uniform load, as shown in Fig. 5(a). The induced uniaxial stress in such samples, obtained by applying the load (stretching force **q** and bending moment **M**) to all layers, as shown in Figs. 5(b) and 5(c), is given by

$$|\sigma_{11}| = E \cdot (x_3 - e) \cdot \frac{1}{R}, \tag{4}$$

where e defines the position of the neutral plane. For an m-layer composite structure, e can be determined as[104]

$$e = \frac{\sum_{k=1}^{m} E_k h_k \left[h_k + 2 \sum_{n=0}^{k-1} h_n \right]}{2 \sum_{k=1}^{m} E_k h_k}. \tag{5}$$

For a single layer, Eq. (4) reduces to Eq. (2), and the neutral surface coincides with the middle surface. The analytical expression of strain can be obtained from Eqs. (4) and (5), by considering the Hooke's law.[45,46,68,105] The mechanical deformation of multilayered systems with adhesives (Fig. 5(c)) can be obtained using the theory of lap-joints.[106–108] It can be noticed that Eq. (4) considers only the effect of **M**, and the effect of **q** is ignored. The uniaxial stress at the top of an assembly comprising a 20 μm UTC on 50 μm Kapton foil and conforming to a cylinder of $R = 10$ mm in these samples has been reported to be $|\sigma_{11}|^{\langle 110 \rangle} \cong 212$ MPa and $|\sigma_{11}|^{\langle 100 \rangle} \cong 173$ MPa. The values of E are summarized in Table I. The bending investigations on UTCs (h = 20 μm) with CMOS circuitry encapsulated in a polyimide foil show that 347 MPa uniaxial stress is induced in the chip, for a minimum bending radius R = 5 mm.[109] Likewise, a three-layer system (composed of 20 μm UTC, 10 μm epoxy glue, and 50 μm Kapton foil) bent on a cylinder of $R = 10$ mm experiences uniaxial stress between [200 and 260] MPa, at the top of the chip, for applied **M** and variable $|\mathbf{q}| \in [0, 1]$ MPa mm.[88] The breaking tests performed on UTCs with CMOS circuitry adhesively attached to thin substrates reveal ~60% samples breaking at $R = 6$ mm.[110]

B. Biaxial bending of UTCs

UTCs also experience spherical deformations when bending moments are applied to both in-plane axes x_1 and x_2 [Fig. 3(b)] or by a hydrostatic pressure applied on the entire surface. Biaxial flexural tests on plates, which have been used to evaluate the strength of ceramics for more than 40 years in various configurations such as ball-on-ring,[111,112] uniform pressure,[113] ring-on-ring,[114] or piston-on-three-balls,[115] have been adapted to investigate the biaxial strain effects in UTCs.[116,117,150] Properties such as phonon or electronic deformation potentials[118,119] are measured through these tests to find the fracture strength[96,120–122] or to investigate the 2D strain effects on the electrical behavior of

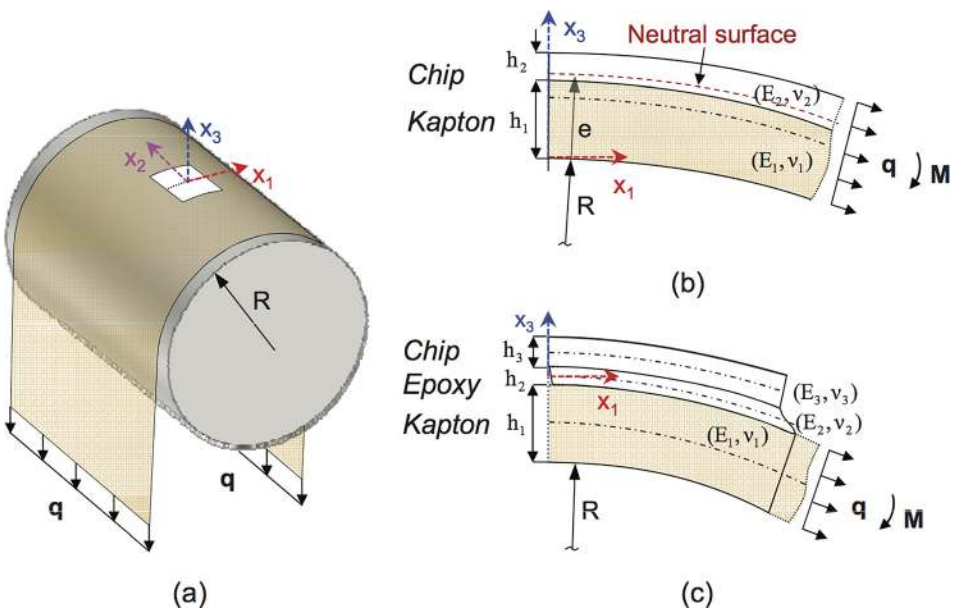

FIG. 5. Schematic representation of the bending of (a) ultra-thin chip in/on foil; (b) ultra-thin multilayered assembly case of chip-in-foil; and (c) ultra-thin assembly of chip adhesively attached to foil.

MOSFETs.[123,124] In the case of thin samples, the fracture strength is influenced by the roughness and morphology of the surface,[125] which in turn are affected by the surface defects introduced through backside grinding, polishing, chemical etching, and edge defects caused by wafer sawing or dicing. In terms of mechanical analysis, the spherical deformation of plates and shells is more complex than the cylindrical or uniaxial deformations. For small deflections, these stresses are expressed analytically,[68,69] and for large deflections (larger than the thickness of the Si-plate), they are usually determined by non-linear FEM calculations.[120] Some examples are presented below.

When a hydrostatic pressure p is applied to a thin Si-wafer (e.g., thickness $h \cong 280\,\mu$m) [Fig. 6(a)], the induced stress can be expressed as a function of the pressure and radius of curvature R as[69,119,126]

$$|\sigma_{biax}| = \frac{R \,.\, p}{h}. \tag{6}$$

The pressure results in spherical deformation of UTCs. The experimental and 3D FEM simulations for UTCs with thicknesses of 15, 25, and 50 μm and an area of (10×10) mm^2 indicate that the induced biaxial stresses are evenly present in the central area of the chip and they increase towards the edge.[117] These studies also indicate that even if the single-crystal Si is anisotropic, its biaxial elastic modulus $\left(\frac{E}{1-\nu}\right) \cong 180.5$GPa (Ref. 127) is invariant for the (001)-Si crystal plane.[128] Spherical deformation using pressure used in the case of islands of a:Si (100 nm grown on top of 400 nm Si_3N_4) circuits fabricated on 50 μm thin Kapton foil[129,130] shows 5% average biaxial strain for every steradian spherical deformation (subtending 66°).

The ball-on-ring test has also been used to investigate the fracture strength of spherically deformed UTCs.[67] In the ball-on-ring method, cylindrical deformation is achieved with a force **F**, applied in the center of the sample with a conical steel punch head of diameter a, as shown in Fig. 6(b).[96,131] The biaxial stress is observed at the central area of the wafer within a concentric circle of diameter d, where the induced radial stress equals the azimuthal (tangential) stress. With this bending method, an applied displacement of ~0.9 mm induces ~0.037% uniform biaxial strain in the center region of 100 mm wafers.[124] The stress

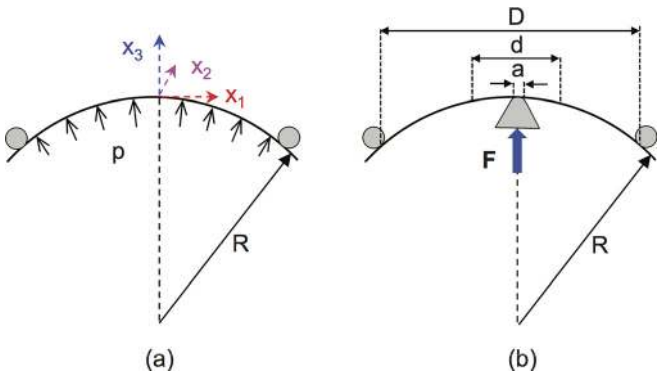

FIG. 6. Schematic representation of two classical biaxial bending tests used in the case of thin samples: (a) hydrostatic pressure; and (b) ball-on-ring.

variation obtained by FEM simulations[124] and the maximum stress is calculated as[96,131]

$$|\sigma_{biax}^{max}| = \frac{3|\boldsymbol{F}|(1+\nu)}{4\pi h^2} \cdot \left(1 + 2\ln\frac{D}{d} + \frac{1-\nu}{1+\nu} \cdot \frac{2D^2 - d^2}{4R^2}\right), \tag{7}$$

where d in turn can be expressed as a function of the thickness h and diameter a.[96,118,131,132]

C. Torsional deformation of ultra-thin Si-chips

The shear stress analysis in UTCs is also important for investigating their torsional fracture strength. A very few publications have reported the investigation of flexible layered Si-structures subjected to torque.[133] Most of these investigations have been carried out by twisting bulk Si-strips around one axis (e.g., ⟨110⟩ or ⟨100⟩) with test setup called torsional bridge.[134] The torsional stiffness of bulk Si has been investigated since 1996 (Refs. 135 and 136) and torsional tests have been used to determine the shear-moduli[137] and failure criteria.[138] The maximum shear stress induced by a torsional moment at the surface of UTC depends on the applied moment, thickness, and the shear coefficients of the material UTC is made of. The rotational angle can also be calculated as a function of applied moment.[134] Both the analytical results and the FEM simulation have been shown to have homogeneous shear stress induced at the surface with edges, thus offering an exception where the shear stress decreases rapidly. The shear stress analysis in UTCs can be described by the beam's theory based on small deformation assumption.[68] The mechanical analysis of UTCs subjected to torque can be explained with Karman's plate theory[69] of large deflections. Since the deformation of such thin systems is accompanied by large rotational angles, the stress analysis often requires 3D FEM simulations. One of the few publications that deal with the torsional deformation of thin multilayer polymer systems used as substrates in flexible electronics is the study by Lee and Liu.[133] Their results indicate that a sample having larger Young's modulus is easier to twist along the twisting direction than along the transverse direction and that the rectangular samples are easier to deform than the square ones.

IV. ELECTRICAL BEHAVIOR OF STRESSED SILICON AND CMOS TRANSISTORS

The effects of uniaxial, biaxial, and shear stress on the electrical behavior of strained Si-resistors and MOSFETs are further summarized in this section. The physical mechanisms by which various types of stress change the electron transport in Si are also highlighted.

A. Stress effects in bulk Si

Stresses change the electrical resistance of Si by significantly changing its resistivity even for small variation in geometry,[139] which is also termed as piezoresistivity.[140] As Si is anisotropic, the variation in its conducting properties[141,142] as a result of stress can be expressed as

$$\frac{dr_{ij}}{r} = \frac{d\rho_{ij}}{\rho} = \Pi_{ijkl} \cdot \sigma_{kl} + \Pi_{ijklmn} \cdot \sigma_{kl} \cdot \sigma_{mn} + \cdots, \quad (\forall)\, i, j, k, l, m, n = \{1, 2, 3\}, \tag{8}$$

where r and ρ are the resistance and resistivity without stress, σ_{kl} and σ_{mn} are the components of stress tensor [Eq. (1)], and Π_{ijkl} and Π_{ijklmn} are the first- and second-order piezoresistive coefficients. The cubic symmetry of Si results in a simplified piezoresistive tensor,[143] which can be evaluated for different Si-surface orientations and for uniaxial and biaxial stress. For the (001) Si-surface (which is prevalent in the microelectronics industry) and in-plane uniaxial stress, the 1st order piezoresistive tensor reduces to three independent piezoresistive coefficients ($\Pi_{11}^{(001)}$, $\Pi_{12}^{(001)}$, $\Pi_{44}^{(001)}$)[144,145] and the 2nd order piezoresistive tensor reduces to nine.[146,147] For low stresses ($\leq$500 MPa), the higher-order terms are usually neglected. $\Pi_{11}^{(001)}$ ($|\theta - \varphi| = 0°$) and $\Pi_{12}^{(001)}$ ($|\theta - \varphi| = 90°$) are the longitudinal and transverse piezoresistive coefficients. The angle θ indicates the current flow direction and the angle φ the stress application direction, as sketched in Fig. 6. These coefficients are determined from measurements along ⟨100⟩-Si fundamental axes, which is also the principal stress axes (no shear stresses act along these directions). $\Pi_{44}^{(001)}$ is the shear coefficient determined from ⟨110⟩ measurements as the uniaxial stress along these axes consists of both hydrostatic and shear components. The axes [$\bar{1}$10] and [110] are parallel and perpendicular to the primary wafer flat and correspond to the orientation of most resistors and transistors in ICs. A general relationship for the (001) Si-plane $\boldsymbol{\Pi^{(001)}}$ ($\Pi_{11}^{(001)}$, $\Pi_{12}^{(001)}$, $\Pi_{44}^{(001)}$, θ, φ) is[39]

$$\Pi^{(001)} = \Pi_{11}^{(001)} \cdot \left(cos^2\theta \cdot cos^2\varphi + sin^2\theta \cdot sin^2\varphi\right) + \Pi_{12}^{(001)} \cdot \left(cos^2\theta \cdot sin^2\varphi + sin^2\theta \cdot cos^2\varphi\right) + 2 \cdot \Pi_{44}^{(001)} \cdot \sin\theta \cdot \cos\theta \cdot \sin\varphi \cdot \cos\varphi. \tag{9}$$

Typical values of piezoresistive coefficients, obtained experimentally for uniaxial stresses up to 174 MPa, are given in Tables II and III.[144,147] The piezoresistance coefficients depend on the impurity type and concentration. In conventional layout (Manhattan style), most transistors are built for $\theta = 45°$. In that case, Eq. (9) becomes

$$\Pi^{(001)}(45°, \varphi) = \frac{\Pi_{11}^{(001)} + \Pi_{12}^{(001)}}{2} + \Pi_{44}^{(001)} \cdot \sin\varphi \cdot \cos\varphi. \tag{10}$$

TABLE II. Piezoresistive coefficients values ($\times 10^{-12}$ Pa^{-1}) for n-type Si of different doping concentrations (cm^{-3}), measured at 300 K.

	n-type Si			
Piezoresistive coefficient	6×10^{14}	4×10^{16}	1×10^{17}	2×10^{18}
Π_{11}	−1022	−840	−770	−650
Π_{12}	534	430	390	330
Π_{44}	−136	−200	−140	−120

TABLE III. Piezoresistive coefficients values ($\times 10^{-12}$ Pa^{-1}) for p-type Si of different doping concentrations (cm^{-3}), measured at 300 K.

	p-type Si			
Piezoresistive coefficient	6×10^{14}	4×10^{16}	1×10^{17}	2×10^{18}
Π_{11}	66	−0.0	−60	−40
Π_{12}	−11	20	10	30
Π_{44}	−1381	1190	1120	970

Sometimes, the longitudinal $\Pi_L^{(001)}$ and transverse $\Pi_T^{(001)}$ coefficients are used instead of the fundamental piezoresistance coefficients. These are

$$\Pi_L^{(001)} = \Pi^{(001)}(45°, 45°/225°) = \frac{\Pi_S^{(001)} + \Pi_{44}^{(001)}}{2}, \tag{11}$$

$$\Pi_T^{(001)} = \Pi^{(001)}(45°, -45°/135°/315°) = \frac{\Pi_S^{(001)} - \Pi_{44}^{(001)}}{2}, \tag{12}$$

where $\Pi_S^{(001)} = \Pi_{11}^{(001)} + \Pi_{12}^{(001)}$. The piezoresistance coefficients for other Si-planes and crystallographic directions can be calculated by applying tensor rotation from the reference to the target Cartesian coordinate systems.[132,141] For the (111)-Si plane, which is another common type of wafer used in IC fabrication, the uniaxial piezoresistive coefficients, for lightly doped n-type Si, with respect to the ([$\bar{1}$10], [$\bar{1}\bar{1}$2], [111]) axes are $\boldsymbol{B}$ (B_1, B_2, B_3) = (−312, 297, 61) ($\times 10^{-12}$ Pa^{-1}).[27] The corresponding values for p-type Si are (718, 228, −448) ($\times 10^{-12}$ Pa^{-1}). In an n-type material, B_1 and B_2 are the largest coefficients whereas B_3 is quite small. On the other hand, in the case of a p-type material B_1 and B_3 have the largest values.

In the biaxial case, the stress is in-plane and symmetric $\sigma_{11} = \sigma_{22}$ and $\sigma_{33} = 0$. The biaxial piezoresistive coefficient of Si is $\Pi_B = \Pi_L + \Pi_T$.[123] The resistors and MOSFETs have been extensively studied to determine the variation of mobility of electrons and holes with biaxial stress and to analyze the electronic band structure of biaxially strained-Si.[148,149] These studies show that the electron mobility increases with tensile biaxial strain and decreases with compressive strain. The hole mobility increases with both tensile and compressive biaxial strain and is more pronounced in the case of compressive strain.[123,148] These observations do not depend on the channel direction. The value of the shear piezocoefficient (Π_{66}) in biaxially strained (001) p-type Si has been shown to increase for compressive biaxial strain and decrease in the case of a tensile strain.[149] These observations are not always independent of dopant densities. For example, in the case of biaxial tensile strain, the decrease in the shear piezoresistive coefficient is more pronounced for low dopant densities, while for densities around 10^{20} cm^{-3}, it remains unaffected. Further, the value of shear piezoresistive coefficients varies linearly with the compressive biaxial strain but is highly nonlinear in the case of tensile strain.[17] The value of the shear piezoresistive coefficients also varies with temperature[150]-decreasing linearly and monotonically with the increase in temperature from −150 °C to +125 °C. The

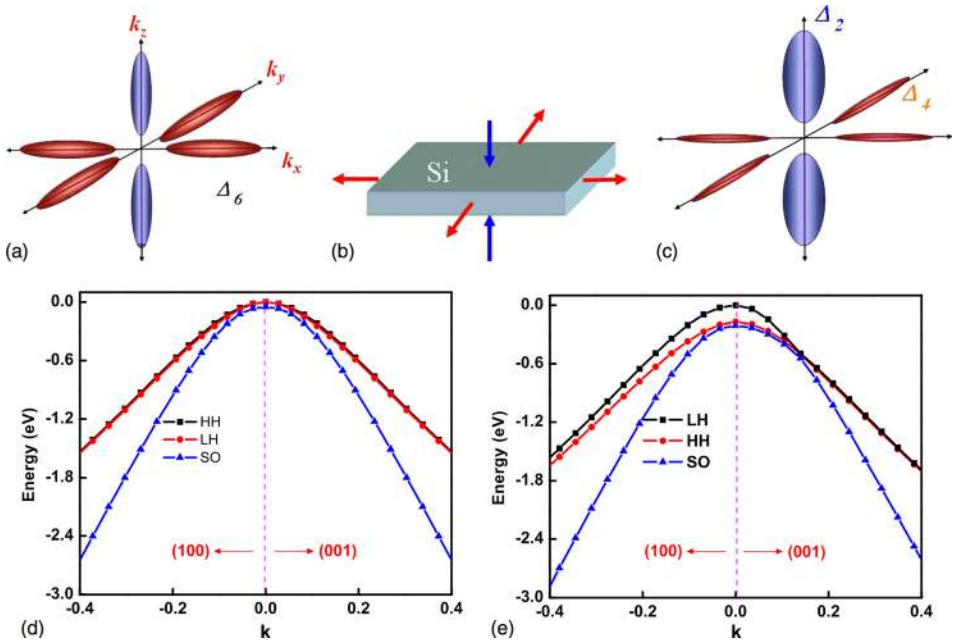

FIG. 7. Si conduction and valence bands as a function of biaxial strain. (a) The six Si conduction band valleys along three different directions are equally populated without strain; (b) schematics of bulk Si under biaxial tensile strain; (c) under tensile strain, the valleys are split into two groups. Electrons tend to populate the lower Δ_2 valleys than the higher Δ_4 valley; (d) and (e) show the three-top valence band near the Γ point for the strain-free and 1.5% biaxial tensile-strained Si, respectively. Reprinted with permission from Yu *et al.*, Phys. Rev. B **78**(24), 245204 (2008). Copyright 2008 American Physical Society.

coefficient value can also change sign for low temperature and low doping as the strain is increased. This means that it may be possible to adjust the temperature dependence for strained-Si with specific doping and biaxial strain. The biaxial elastic modulus of Si often used in such investigations is $B_{001} \cong 181$ GPa.[151]

The effects of strain are also reflected through change in the positions of atoms, bond lengths, and the angles between the bonds.[143] For example, the high cubic symmetry (O_h group) of the Si crystal is lowered with strain, which changes the energy band structure.[152] The effect of changes in the energy band structure on electronics is reflected through variation in the effective mass and hence the mobility, as explained below. The band structure of crystalline Si in the first Brillouin zone consists of six ellipsoidal degenerate energy valleys [Fig. 7(a)], which are also reflected through the cubic symmetry of Si. The ellipsoidal shape of the valleys can be characterized by two effective masses:[153] transverse $m_t = 0.19m_0$ and longitudinal $m_l = 0.91m_0$, where $m_0 = 9.11 \times 10^{-31}$ kg (511 keV) is the free electron rest mass. The electron conductivity effective mass of Si is proportional to the inverse of the sum over the effective masses in the different minima along the equivalent directions and is expressed as

$$m^* = \frac{3}{\frac{1}{m_l} + \frac{1}{m_t} + \frac{1}{m_t}} = 0.26 \cdot m_0. \tag{13}$$

The applied strain lifts the original symmetry determined by band degeneracies and this leads to band warping[154] and changes the transport properties. The carrier mobility ($\mu = \frac{q}{m^*} \cdot \tau$) also changes with resulting variations in the effective mass (m^*) and the scattering rate ($1/\tau$) of phonons and impurities.[143] In the case of *n*-type Si, the stress-induced band splitting causes the electrons to locate in the low-energy valleys. As an example, the biaxial stress splits the conduction-band minimum, as shown in Figs. 7(a)–7(c). This consists of six equivalent Δ_6 valleys in the unstrained state, four in-plane Δ_4 valleys and two out-of-plane Δ_2 valleys.[148] On the other hand, in *p*-type Si the heavy-hole (HH) and light-hole (LH) valence bands minima are degenerated at the Γ point in the absence of stress as shown in Fig. 7(d). The tensile or compressive biaxial strain warps them significantly, with valence bands becoming highly anisotropic as shown in Fig. 7(e).[123,155,156] Such effects change the conductivity and resistivity (ρ) of Si, which is related to the concentration of electrons (n) and holes (p) and their mobility μ_n and μ_p as $\rho = 1/(qn.\mu_n + qp.\mu_p)$, where q is the elementary charge.[157]

B. Stress effects in MOSFETs

Various experiments on MOSFETs presented in the literature indicate that the mobility of charge carriers can vary with various stresses (tensile and compressive), as also explained previously in Section III. These variations can be directional as well as carrier type dependent. Generally, the channel direction differs from the stress direction. In a conventional layout, the MOSFETs are realized on the standard (001)-Si surface with current $\boldsymbol{J}$ flowing along ⟨110⟩ (Fig. 8). However, devices oriented along the principal Si high-symmetry axes ⟨100⟩ or processed on other Si-surfaces such as (110) and (111) are also often encountered. Therefore, the piezoresistive coefficient tensor should be evaluated separately from the channel mobility variation with stress.

Unlike bulk-Si, two aspects are specific to shear piezoresistive coefficients of the MOSFETs: *First*, in addition to the scattering on phonons and impurities, the carriers also experience Coulomb scattering at the oxide-Si interface.[158] As a result, their surface mobility at room temperature is much lower than bulk Si (e.g., $\mu_n \leq 670\,\mathrm{cm^2/V\,s}$ versus $\leq 1400\,\mathrm{cm^2/V\,s}$ for the bulk and $\mu_p \leq 250\,\mathrm{cm^2/V\,s}$ versus $\leq 450\,\mathrm{cm^2/V\,s}$ for the bulk).[159,160] The scattering takes place on the charges trapped at the interface and on the interface roughness.[143] *Second*, the applied vertical electric field creates a potential

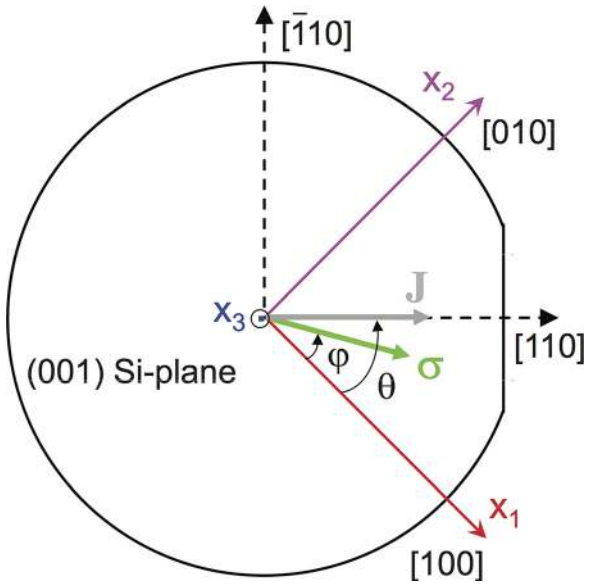

FIG. 8. Common current flow (J) direction on (001) Si-plane. σ is the uniaxial stress. The angle θ indicates the current flow direction and the angle φ the stress application direction, from the principal Si-axis.[100]

well which confines the carriers in the out-of-plane direction, quantizing the energy levels and changing the effective mass in the out-of-plane direction. The degeneracy between in-plane and out-of-plane valleys is removed. In n-type MOSFETs, the conduction band valleys shift and split the minimum into sub-bands Δ_2 and Δ_4.[161] Thus, even in the absence of strain, the energy levels are non-degenerate. The energy difference between the Δ_2 and Δ_4 sub-bands varies with the intensity of the transverse effective field. For example, an effective gate field of 1 MV/cm induces an energy difference $\Delta E_0 = \sim 12$ meV, at $T = 300$ K, for an inversion electron density of 10^{13} cm^2.[143] The confinement field in the p-type MOSFETs shifts the degeneracy of valence band HH and LH sub-bands. A higher split can lead to lower interband scattering. In the case of (001)/⟨110⟩, the 1 MV/cm surface field causes a splitting of ∼25 meV, at $T = 300$ K.[162] For (110)/⟨110⟩, the same field splits more the HH and LH sub-bands and causes a lower inter-band scattering, thus resulting in a higher hole's mobility than (001)/⟨110⟩ Si.

In the presence of stresses, the band splitting is due to the cumulative effect of both confinement-induced and strain-induced band splitting. The strain alters the electrical characteristics of MOSFETs by changing the drain current I_D through the effective carriers mobility μ_{eff}.[163] This is the spatial average of the mobility profile in the inversion layer, which can be modeled by the universal mobility curve.[161] The sensitivity of I_D to stress is reported to have been caused primarily by the strain-induced changes of mobility.[164,165] If the stress-induced threshold voltage variation is low, the I_D variation because of stresses is governed by variations in μ_{eff}. Like Eq. (8), the change in drain current can be expressed as

$$\frac{\Delta I_D}{I_D} = \frac{\Delta \mu_{eff}}{\mu_{eff}} = \Pi_{ijkl} \cdot \sigma_{kl} + \cdots, \quad (\forall)\, i, j, k, l, m, n = \{1, 2, 3\}. \tag{14}$$

For the low stress values (<500 MPa), the piezoresistive coefficients are determined by variations of I_D with stress in the linear or saturation regions of transistor characteristics. The piezoresistive coefficients can be calculated from the slope of mobility variation with respect to stress. These are significantly smaller in UTCs than their bulk counterparts, with values depending on the actual doping density and applied gate voltage. The piezoresistive coefficients also have some dependence on the channel length of MOSFETs. The source-drain parasitic resistances to the drain current also contribute to such variations.[166] For high stresses, the linear response piezo-model fails and the 2nd order terms must be considered. For (001) surface orientation and uniaxial stress, the piezoresistive coefficients are determined from uniaxial stress measurements in three cases: (a) longitudinal (stress ∥ drain current I_D ∥ ⟨110⟩); (b) transverse (stress ⊥ (I_D ∥⟨110⟩)); and (c) diagonal ($\angle(I_D, [110]) = \theta = 45°$) while stress is applied longitudinal and transversal to the channel.[167,168]

For n-type MOSFETs, the experimental results show that ∼100 MPa uniaxial tensile stress applied along ⟨110⟩ leads to ∼5% increase in the electrons μ_{eff} in the longitudinal case and only ∼2% in the transverse case.[39] A few values of the piezoresistive coefficients are given below in Table III. For p-type MOSFETs, the hole mobility depends on the Si surface and channel orientation. The (001)/⟨110⟩ MOSFETs show an inferior surface hole mobility than the (110)/⟨110⟩ MOSFETs.[155] This is due to a higher surface roughness scattering rate in (001)/⟨110⟩ p-type MOSFETs than in (110)/⟨110⟩ p-type MOSFETs. The confinement field shifts the degeneracy of the HH and LH sub-bands. For example, a field of 1 MV/cm in a (001)/⟨110⟩ p-type MOSFET, at $T = 300$ K, induces a splitting between the HH and LH sub-bands as large as ∼25 meV.[162] A tensile uniaxial stress of ∼100 MPa applied along the [110] direction causes an increase of ∼4.5% of the hole's mobility μ_{eff} in the transverse case and a decrease of ∼ −6% in the longitudinal case.[39,166] The absolute values of the piezoresistive coefficients $\Pi_{11}^{(001)}$ and $\Pi_{12}^{(001)}$ of bulk MOSFETs are lower than bulk Si (Table III). However, the values of $\Pi_{44}^{(001)}$ are similar. The differences arise from the presence of the confinement field in MOSFETs. In the case of the (111) Si-plane, the maximum mobility variation is obtained for the longitudinal case and the mobility variation is minimized when in the transverse case.

The studies related to the impact of stress on threshold voltage (V_{TH}) of nanoscale strained-Si and SiGe MOSFETs reveal that V_{TH} decreases with increasing strain in the Si thin film. The V_{TH} roll-off affects the device characteristics and performance. The analyses of V_{TH} shift for uniaxial and biaxial stressed Si NMOS transistors with the ⟨110⟩ channel direction on (001) wafers show a significantly larger linear shift of the V_{TH} (four times larger) for biaxial stress compared to the uniaxial case. This large variation in the biaxial case results from the stress-induced change in the Si electron affinity and bandgap.

The piezoresistive behavior of MOSFETs with similar configurations, under the same environmental conditions and in the presence of the same applied stress type and

magnitude, is expected to be similar for devices on bulk Si and on UTCs. The difference between them arises from the mechanical stiffness (see Sec. III) related to the stress magnitude induced by a certain bending radius R. In this respect, UTCs in/on foils with different CMOS technologies have been reported to investigate the effects of piezoresistive behavior of MOSFETs. For example, short-channel single-crystal-Si MOSFETs in a 0.8 μm CMOS process with 20 μm thickness on a 50 μm thick Kapton foil substrate have been studied by bending on cylinders of radii of curvature down to 10 mm.[88] Smaller radii of curvature (R = 5 mm) have also been reported with mono-crystalline NMOS and P-type Meal Oxide Semiconductor (PMOS) transistors on 20 μm thick UTCs in a 0.35 μm CMOS process embedded into a polyimide foil, corresponding to a uniaxial stress $\sigma_{22} \cong 347$ MPa.[109] Further enhancement in the minimum of radii of curvature (R ϵ [1.6, 70] mm) is achieved in a-Si:H thin-film transistors (TFTs) fabricated on 25 μm thick Kapton foil.[169]

V. COMPACT MODELING OF STRESS EFFECTS IN CMOS DEVICES

As explained earlier, the stress leads to changes in semiconductor material properties such as change in band structure, effective mass, and electron affinity. From device viewpoint, all this is reflected in the changed mobility and threshold voltage, which eventually affect the device performance parameters such as drain current and transconductance. For an effective use of UTCs, an accurate and high-speed simulation of circuits based on a thin substrate is required. Currently, the simulation of the bending stress effects in ultra-thin devices is performed analytically using formulations available for understanding the analog operations. These effects are considered in conventional simulators for the planar architecture. Furthermore, due to the inherently slow simulation in the models based on numerical techniques, they are less desirable for ultra-thin devices. The performance indicators like accuracy, speed, and reliability are strongly connected to the compact models that are used to describe the device behavior, as also explained in Sec. I. This illustrates the importance of an accurate and efficient compact model for ultra-thin CMOS chips, which considers some of the stress/strain related variations discussed in Secs. III and IV. This section reviews the state-of-the-arts in this area.

A. Layout-dependent stress effects modelling

During the process of transistor isolation, it is a standard practice to make a shallow trench by etching the wafer and filling it with silicon oxide to isolate the active areas of MOSFET devices. This process exerts mechanical force, which is a compressive stress applied near to the diffusion areas. This stress is commonly referred to as the shallow trench isolation (STI) stress and termed as the Length of Oxide Diffusion (LOD) effect. Figure 9(a) shows the typical MOSFET layout surrounded by shallow trench isolation. SA and SB are the distances between trench isolation edges to Gate-polySi from the two ends. The LOD is expressed as $LOD = SA + SB + L$. Figure 9(b) shows the stress

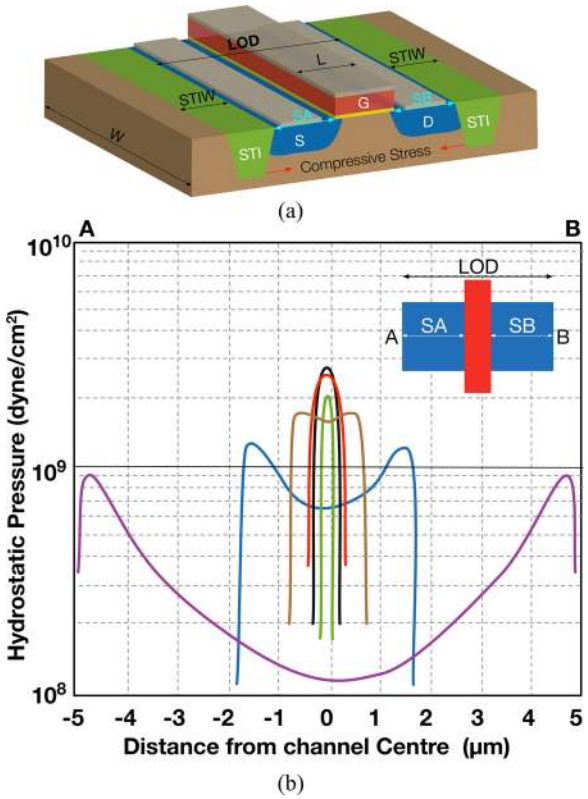

FIG. 9. (a) Illustration of MOSFET device geometry using a STI scheme. (b) Stress distribution within the MOSFET channel. Reproduced from Xi *et al.*, Technical Report No. 94720 (University of California, Berkley, 2003).

distribution along the channel of MOSFET devices induced by the trench isolation. It can be noted that the stress of the central region increases dramatically with shrinking of the LOD.[170] The charge carrier mobility of the device is influenced through the band structure modification, as explained in Sec. IV. Furthermore, the doping profile variation results in V_{th} dependence of the stress effect. Both effects follow the same $1/LOD$ trend but have different L and W scaling influence. This underlined the importance of modifying some parameters in the BSIM model to implement the phenomenological model.

To model the mechanical stress effects impacting MOSFET electrical behavior, Bianchi *et al.*[171] presented a model which accounts for the mobility variations and experimentally evidenced with complex MOSFET geometries. This model proves to be an efficient way to include mechanical stress effects into standard simulation models. In this work, the STI induced mechanical stress has been shown to be the dominant mechanism for stress variation in the channel, which modulates the charge carrier mobility as a function of MOSFET geometry.

Another compact and scalable model about the STI induced mechanical stress effect on MOS electrical performance is given in Ref. 172. This model includes the influence of STI stress on the mobility, saturation velocity, threshold voltage, and other important second-order effects and therefore it could simulate the layout-dependence of MOS performance with greater accuracy and efficiency. The model has been verified with different technologies, different

dimensions, and various layouts of MOS devices. Based on the model, new effective *SA*/*SB* formulas have been derived to improve the simulation efficiency and have also been verified by data from various layouts.

An analytical model to estimate the delay in the presence of process-induced mechanical stress in stacked transistors based inverters and logic gates has been reported by Alam *et al.*[173] Derived using a modified alpha-power law, this model considers the channel length modulation effect. The methodology to incorporate the impact of process-induced mechanical stress effects in the derived delay model has also been presented. The incorporation of stress effects in this model enables estimating the layout-dependent effects of process-induced mechanical stress. The model has also been compared with Technology Computer Aided Design (TCAD) calibrated HSPICE simulation setup using 45-nm Predictive Technology Model. The model derives a stress-aware delay model which is usable in the method of logical blocks like inverter and NAND/NOR gates.

B. Bending stress effect modelling

Several device modeling groups are dealing with the compact modelling of bulk MOSFET and advanced technologies such as double-gate (DG) MOSFET,[174] graphene FET transistors,[175] MoS_2FET,[176] and CNTFET (Carbon NanoTube FET),[177] for analog and mixed circuits. The major goal is to bring simple solutions, which are numerically efficient and are close to device physics. These compact models also extensively explore the capabilities of Verilog-A and VHDL-AMS. However, only very few works have included the effect of stress in MOSFETs.[39,178]

In 2011, the authors reported a method to simulate the effect of uniaxial stress on MOSFETs.[39] To calculate the coefficients for arbitrary directions of current and stress in the (001) silicon (Si) plane, the model implemented a general relation with the fundamental piezoresistive coefficients. This method can perform static and dynamic simulations in linear and saturation regions. It is simulator-independent and does not depend on the source of uniaxial stress. The model is adaptable to other bulk CMOS nodes as well as technologies such as Si-on-insulator (SOI).

The MOSFET device aging has also been studied and implemented with SPICE circuit simulation.[179] For circuit simulation, the age-related degradation has been implemented as stress and associated key MOSFET parameters such as threshold voltage and mobility. The model operates with an optimization loop and starts the sequence with an initial set of parameters in Synopsys HSPICE as an external circuit simulator. It extracts device characteristic parameters including threshold voltage and drain current in the saturation and linear region. Subsequently, with an error function, the measured and simulated values have been compared to adjust the parameters and reach the minimum value of the error function. A compact model which demonstrates the simulations involving elastic deformation of a thin Si chip on a spherical holder is presented in Ref. 117. In this work, the simulation starts with a shell model which is validated through a convergence study and comparison with a 3D model. Following this, the influence of the anisotropic elastic behavior (single crystal) is considered in a bulge test condition and it was noted that isotropic and anisotropic Si simulation gave similar deformations. At the end, the spherical forming is accomplished with a shell model and an anisotropic law.

A deterministic compact model developed by Alagi *et al.* to investigate the parametric instability in elementary devices addresses the device instability, which can be traced back to microscopic reactions obeying the reversible first-order kinetics.[180] The model can describe the response to different periodic stimulus waveforms and is suitable for implementation in commercial electronic circuit simulators (Eldo UDRM). This methodology has been applied to model the negative-bias-temperature threshold voltage instability of a *p*-channel MOSFET. The comparator circuit simulated in this paper for threshold voltage recovery is crucial for circuit design.

A methodology to include parametric shifts induced by mechanical stress from wafer level chip scale package (WLCSP) in an analog circuit simulation flow is given in Ref. 181. Considering that the bending stress is homogeneous with packaging induced mechanical stress, their methodology enables analog system designers to identify circuit blocks with unacceptable sensitivity to WLCSP stress and provides a quantitative route for optimizing system floorplan and/or circuit layout. This is exemplified with an on-chip oscillator circuit suffering from an increased spread and yield loss caused by WLCSP stress variability. This issue has been resolved using a simulation flow which tuned using high-resolution experimental variability data measured on dedicated test chips. The method could be potentially useful for large area flexible electronics also.

Another interesting dimension of mechanical stress is its influence of the thermal behavior of devices. In this regard, the nonlinear model order reduction method is useful as it constructs the one-port dynamic compact models of nonlinear heat diffusion in UTC stacking technology.[182] The method leads to models of small state-space dimensions and allows accurate reconstruction of the time evolution of temperature field due to an arbitrary power waveform of practical interest. This model has not been investigated for MOSFETs, but it helps us gather the information about the thermal behavior of UTCs.

Recently, Ojha *et al.*[183] presented a physics-based compact model for longitudinal and transverse stress profile in the channel of an uniaxially strained bulk MOS transistor. The model predicts the stress profile for linear stress (σ_L), linear thickness (t_L), gate length (L_G), and gate height (h_G). The modeled stress profile is used to calculate the average stress and respective threshold voltage shift (ΔV_{th} $[V_{th}(\sigma_L \neq 0) - V_{th}(\sigma_L \approx 0)]$) for different ($h_G$). The final strain induced V_{th} model has only three fitting parameters and includes both the transverse stress component (S_T, the stress component perpendicular to the direction of carrier flow) and the longitudinal stress component (S_L, the stress component in the direction of carrier flow). Finally, the accuracy of the reported model has been verified by comparing it with the

measured data obtained from devices fabricated using a 28 nm CMOS technology.

Various bending induced effects described in Secs. III and IV can be used to develop a mathematical relation to describe the device model of the MOS transistor as

$$I_{D_{stress}} = I_{D_0}(1 + \Pi_{I_D} \cdot \sigma_{I_D}), \quad (15)$$

$$V_{th_{stress}} = V_{th_0}(1 + \Pi_{V_{th}} \cdot \sigma_{V_{th}}), \quad (16)$$

where $I_{D_{stress}}$ and $V_{th_{stress}}$ are the new effective drain current and threshold voltage parameters including bending stress. I_{D_0} and V_{th_0} are the original drain-current and threshold-voltage of the transistor without stress, respectively. The piezoresistive coefficients proportional to the drain-current and threshold voltage are reflected by Π_{I_D} and $\Pi_{V_{th}}$. σ_{I_D} and $\sigma_{V_{th}}$ are the bending stress proportional to drain-current and threshold-voltage, respectively. The authors reported the implementation of Eqs. (15) and (16) using a language description in the Cadence environment to predict the value and orientation of the bending stress and describe the behavior of the transistor.[184] Based on the three parameters (including drain-current, threshold-voltage, and orientation of the integrated transistor, which vary under the bending stress), a Verilog-A compact model was presented for MOSFETs developed in the standard CMOS technology. Figure 9(a) illustrates the CAD-based simulation flow by authors.[184] It involves different abstract levels for both planar and bent MOSFETs. The labels A, B, C, etc., identify the blocks at various levels of simulation. From this model, one can note that there are significant performance advantages in process-induced uniaxial stressed n-MOSFET, exhibiting a smaller drain-current variation and threshold voltage shift by monitoring the bending stress and changing the supply voltage. The efficiency of this model was demonstrated recently with experimental results on 20 μm thick UTCs having devices and circuit realized in a standard CMOS technology.[185] The measured and simulated transfer and output characteristic curves of NMOS and PMOS 0.35 μm transistors on a linear scale under planar, tensile, and compressive bending conditions are shown in Figs. 10(b)–10(c). The maximum observed percentage difference in drain-current during bending for NMOS was found to be ~5.9%, while the percentage difference of simulated results was 4.4%. For PMOS, it was found to be ~2.4%, while the simulated difference was 2.17%. These results proved >95% accuracy of the proposed model to predict the effect of the bending stress on the devices.

VI. CIRCUIT-LEVEL STRESS EFFECTS

System is more than sum of its parts. In this regard, it is possible that the bending related effects observed in devices may or may not add up at the circuit level. Therefore, taking the discussion forward from devices to circuits, in this section we discuss the works where circuit level bending effects have been studied. We also use some of these circuits to establish the efficacy of Eqs. (15) and (16), which have been proposed to describe the stress induced changes in device response. These results open new avenues to predict the device behavior under various bending conditions and to explore the ways to compensate the bending effect or to take advantage of bending related changes extract more from the overall structure. For example, knowing the responses of

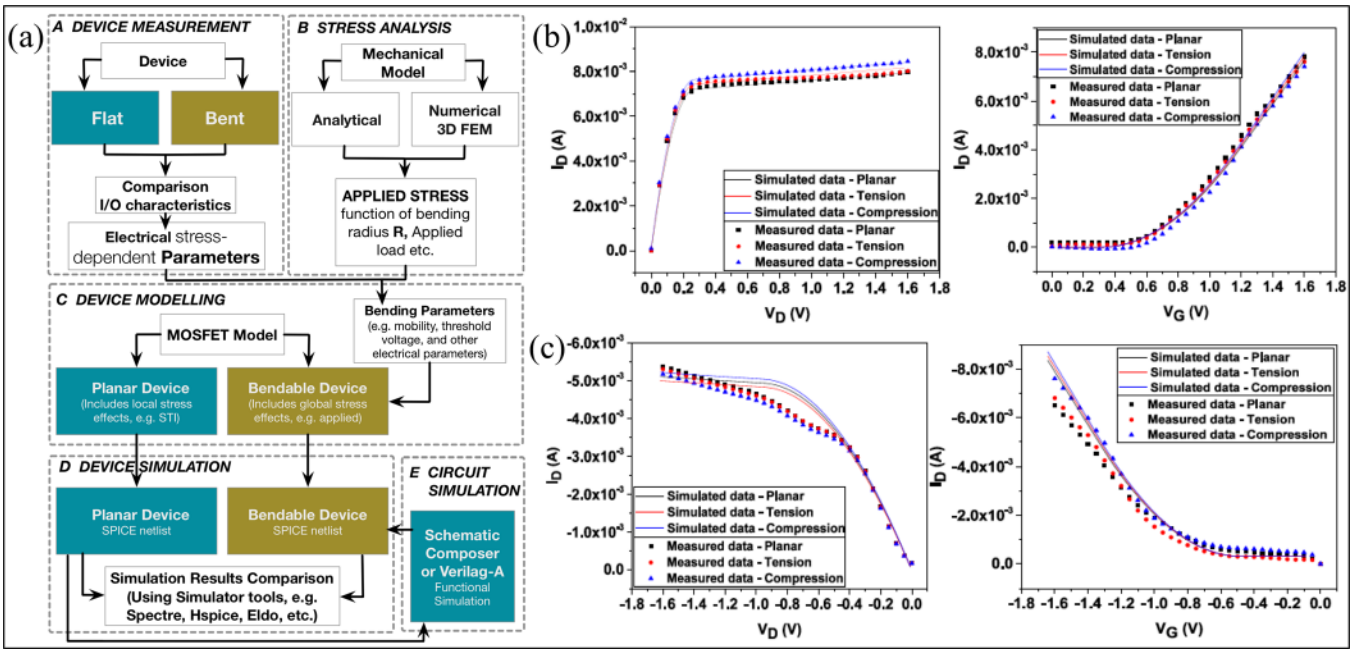

FIG. 10. CAD-based simulation flow to study electrical device characteristics of the bendable CMOS integrated circuit. Reprinted with permission from Heidari *et al.*, in *IEEE International Symposium on Circuits and Systems (ISCAS)* (2016), pp. 1358–1361. Copyright 2016 IEEE. Measured (symbols) and simulated (lines) transfer and output characteristic curves of NMOS and PMOS transistors on a linear scale under planar, tensile, and compressive bending conditions. (b) NMOS 0.35 μm transistor: Output characteristic (ID-VD) and transfer characteristics (ID-VG). (c) PMOS 0.35 μm transistor: output characteristic (ID-VD) and transfer characteristics (ID-VG). Reprinted with permission from Vilouras *et al.*, IEEE Trans. Electron Devices **64**(5), 2038–2046 (2017). Copyright 2017 IEEE.

TABLE IV. Piezoresistive coefficients values of n-type MOSFETs measured along ⟨110⟩ ($\times 10^{-12}$ Pa^{-1}).

References	$\Pi_{11}^{(001)}$	$\Pi_{12}^{(001)}$	$\Pi_{44}^{(001)}$	$\Pi_{L}^{(001)}$	$\Pi_{T}^{(001)}$
Dorda and Eisele[222]	…	…	…	300	200
Canali *et al.*[223]	840	−340	170–200	335	190
Bradley *et al.*[164]	…	…	100	450	350
Gallon *et al.*[166]	…	…	…	485	210
Chu *et al.*[123]	…	…	170	320	150
Wacker *et al.*[39]	…	…	…	480	170
Mahsereci *et al.*[168]	420	260	310	495	185

devices spread over an area one can perform inverse calculations to predict the shape of substrates on which devices are present. This section also presents the methods that have been adopted to minimize or compensate the effects of bending in devices and circuits. Minimizing or mitigating the bending effect by placing devices in a neutral plane is one popular method that has been used in many circuits presented in this section.[186–188] Some of the circuits described in this section also use layout orientation to reduce the stress-induced effects. The mechanics and the electronic behaviors of various integrated circuits have been highlighted below (Tables IV and V).

A. Circuit-level bending stress effects

1. Inverters

CMOS inverters are one of the most widely used circuits. They operate at relatively high speed with very little power. During bending, the inverters on UTCs show deviation from expected response, because of the changes in responses of their constitutive FETs, i.e., PMOS and NMOS and the underlying physics. Some of ultra-thin CMOS inverters reported in the literature are summarized in Table VI.[186,188–191] Only few of them have investigated the effect of bending stress on the performance. The performance of the thinned Si CMOS inverter circuit by Kino *et al.*[191] degrades under bending stress, as shown in Fig. 11(a) with MOSFET currents and CMOS inverter switching behaviors. It was observed [Fig. 11(b)] that the switching threshold point, V_{sp}, slightly increased after bending stress. The V_{sp} increases with an increase in hole mobility or decrease in electron mobility as the β_n/β_p ratio increases under these conditions. Here, β_p and β_n are $C_{ox}W_g/L_g$ and $C_{ox}W_g/L_g$, C_{ox}, W_g, and L_g indicate the hole mobility, electron mobility, gate capacitance, gate width and gate length, respectively. The increase of V_{sp} after bending shows that the compressive stress increases with V_{sp}. Thus, local bending stress induced stress affects the CMOS inverter, leading to the circuit performance fluctuations in the Si chip. Another example by Sevilla *et al.*[189] reports thin (40 μm) and flexible (1.5 cm bending radius) Si based functional CMOS inverters whose characteristics show reduced performance for bending radii higher than 1.5 cm as shown in Figs. 11(c) and 11(d). A comparison of these experimental results with the simulated output based on the compact model presented in Sec. IV B is shown in Figs. 11(e) and 11(f). The good agreement of simulation results with the experimental characterization shows that the model presented in this paper through Eqs. (15) and (16) could be the starting point for analyzing device behavior under bending conditions. The effects of circuit-level stress on inverter performance investigated by Shahrjerdi and Bedell[205] show that the electron mobility increases with tensile strain and decreases with compressive strain. On the other hand, the hole mobility increases with both tensile and compressive strain but the effect is more significant for compressive strain because the hole effective mass decreases with compressive strain but increases with tensile strain.[161,205] Since drain current is directly proportional to carrier mobility, higher drain current of the Si MOSFETs under strain can be attributed to high mobility.[192] Therefore, the local bending stress affects the I–V characteristics of both MOSFETs in the inverter and so the switching behavior of the CMOS inverter.

TABLE V. Piezoresistive coefficients values of p-type MOSFETs measured along ⟨110⟩ ($\times 10^{-12}$ Pa^{-1}).

References	$\Pi_{11}^{(001)}$	$\Pi_{12}^{(001)}$	$\Pi_{44}^{(001)}$	$\Pi_{L}^{(001)}$	$\Pi_{T}^{(001)}$
Colman *et al.*[145]	10	−238	−1278	−753	525
Canali *et al.*[223]	125	−280	(−1050)–(−1150)	−600	500
Bradley *et al.*[164]	…	…	−950	−500	450
Chu *et al.*[123]	…	…	−1030	−710	320
Wacker *et al.*[39]	…	…	…	−620	440
Mahsereci *et al.*[168]	101	−280	−1060	−619	440

TABLE VI. Summarized comparison of flexible CMOS Inverters.

Material	Kim *et al.*[188]	Sevilla *et al.*[189]	Sachid *et al.*[190]	Hwang *et al.*[186]	Kino *et al.*[191]
Thickness (μm)	1.7	40	0.007	0.3	30
L_g[a] (μm)	13	0.25	2	500	0.22
W_N (μm)	300	0.35	3.3	40	0.22
W_P (μm)	100	0.45	5.9	40	0.22
I_{on}/I_{off}	$>10^5$	N/A	$>10^7$	$\sim 10^5$	N/A
V_{sp}[b] (V)	2.5	0.4	−4	N/A	∼0.9
μ_N (cm^2/V s)	290	132	38	400	1450
μ_p (cm^2/V s)	140	80	238	70	300

[a]L_g is the gate length.
[b]V_{sp} is the voltage of the switching threshold point.

2. Ring oscillators (RO)

The ring oscillator (RO) is cascaded combination of delay stages (inverters), connected in a closed loop. The ROs are of great interest to electronic engineers because of numerous useful application and features such as (i) oscillation at low voltage, (ii) high frequency oscillation, and (iii) low power dissipation and many more.[193] Studying the effect of bending on 43-stage RO using a 250-nm process, Yuan *et al.*[194] noticed the speed enhancement under strained conditions. They have studied two types of inverter cell layouts: (i) PMOS channel is perpendicular to the NMOS channel and (ii) PMOS channel is parallel to the NMOS channel. A speed enhancement of ∼7.4% was noticed for uniaxial strain in a direction parallel to NMOS and perpendicular to PMOS. This is due to large current enhancement for both NMOS and PMOS. The speed enhancement for the second type of layout

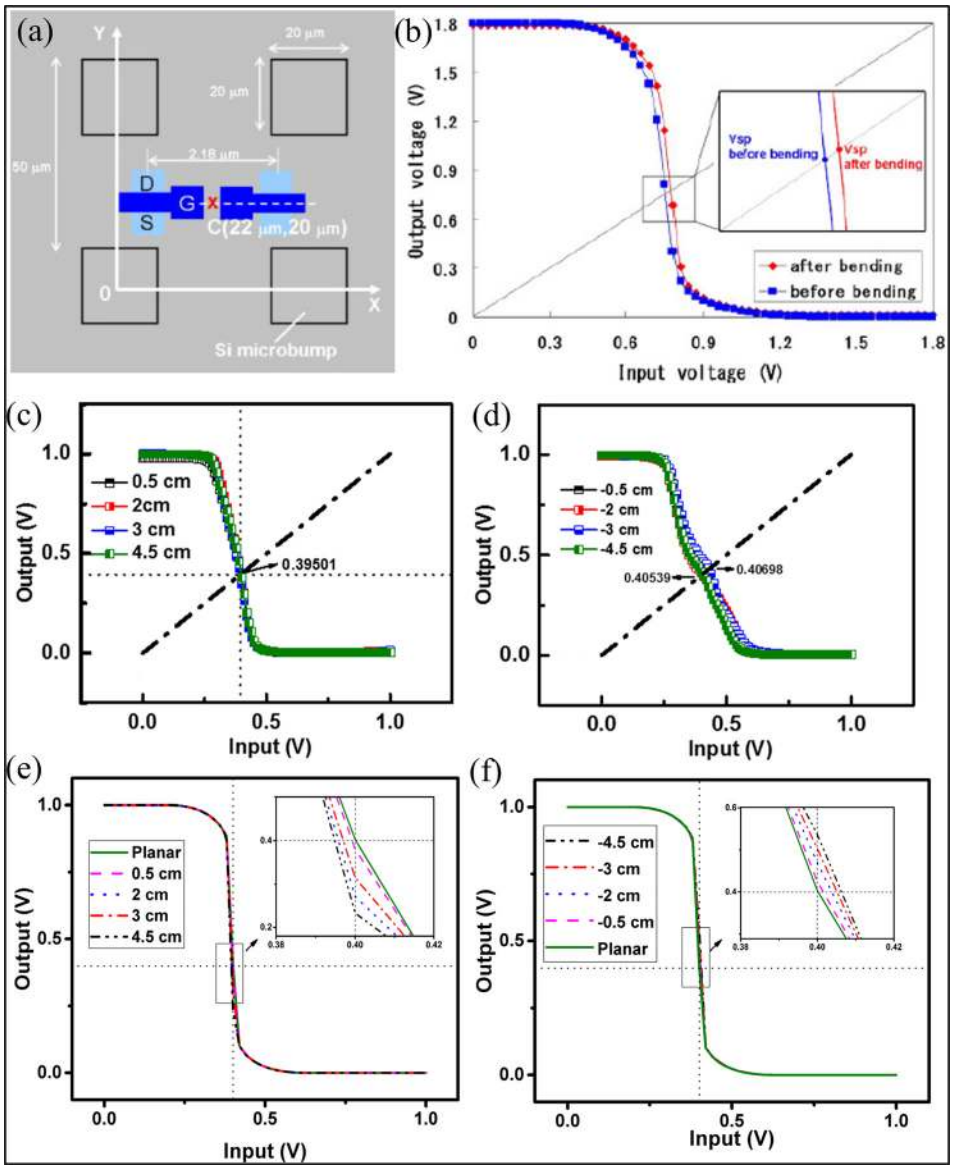

FIG. 11. (a) Layout of Si microbumps and CMOS inverters in the thinned Si chip, and (b) CMOS inverter characteristic before and after bending. Reproduced with permission from Kino *et al.*, Jpn. J. Appl. Phys., Part 1 **52**(4S), 04CB11 (2013). Copyright 2013 The Japan Society of Applied Physics. (c) Voltage transfer curve characteristics of flexible inverters at different bending downward radii and (d) upward radii. Reproduced with permission from J. Appl. Phys. Lett. **108**(9), 094102 (2016). Copyright 2016 AIP Publishing LLC. (e) Simulated results (based on the developed compact model) at different bending downward radii corresponding to the characterizations shown in (c). (f) Simulated results corresponding to the characterizations shown in (d) for different bending upward radii.

where strain is perpendicular to NMOS and parallel to PMOS was found to be only ∼1.5%, as no simultaneous enhancement for both NMOS and PMOS can be achieved. The mechanical study of ROs on the extremely thin flexible Si on insulator (ETSOI) process with a power supply voltage of 0.9 V also indicates a delay of ∼16 ps.[195] The ultra-thin body of the Si channel in ETSOI devices allows aggressive scaling of the channel length into sub-20 nm range without incurring the detrimental short channel effects. Figures 12(c) and 12(d) show the schematic illustration of RO used for a flexible Si solar cell and a flexible 20 μm thick Si, respectively.

3. Current mirrors

The current mirror is an important building block for linear integrated circuits especially amplifiers. In this circuit, the output current depends upon the aspect ratio, mobility, and feed current.[196] There are clearly observable changes in the output current when the current mirror fabricated on thin Si experiences bending. This is because under the strained condition the mismatching between transistors gains prominence. In an attempt to overcome the piezoresistive effects of bending to realize stable circuit, Hassan *et al.*[197] investigated ultra-thin (20 μm) CMOS current mirrors made up of orthogonally oriented transistors. The use of orthogonally configuration demonstrates the output current change ($\Delta I_2/I_2$) related to the transistor's changes of drain current ($\Delta I_D/I_D$) differences and can be written as

$$\frac{\Delta I_2}{I_2} = \frac{\mu_2 - \mu_1}{\mu_2} = \frac{(\mu_0 + \Pi_2 \cdot \sigma) - (\mu_0 + \Pi_1 \cdot \sigma)}{(\mu_0 + \Pi_2 \cdot \sigma)} = (\Pi_2 - \Pi_1) \cdot \sigma, \quad (17)$$

where μ, σ, and Π are the mobility, stress, and corresponding piezoresistive coefficients, respectively. The circuits had a compact layout, fabricated using ChipFilm technology and were placed near the chip edges to reduce the chip warpage.

4. Operational amplifiers

Operational amplifiers (Op-Amps) are the commonly used components in circuit designs for amplification and

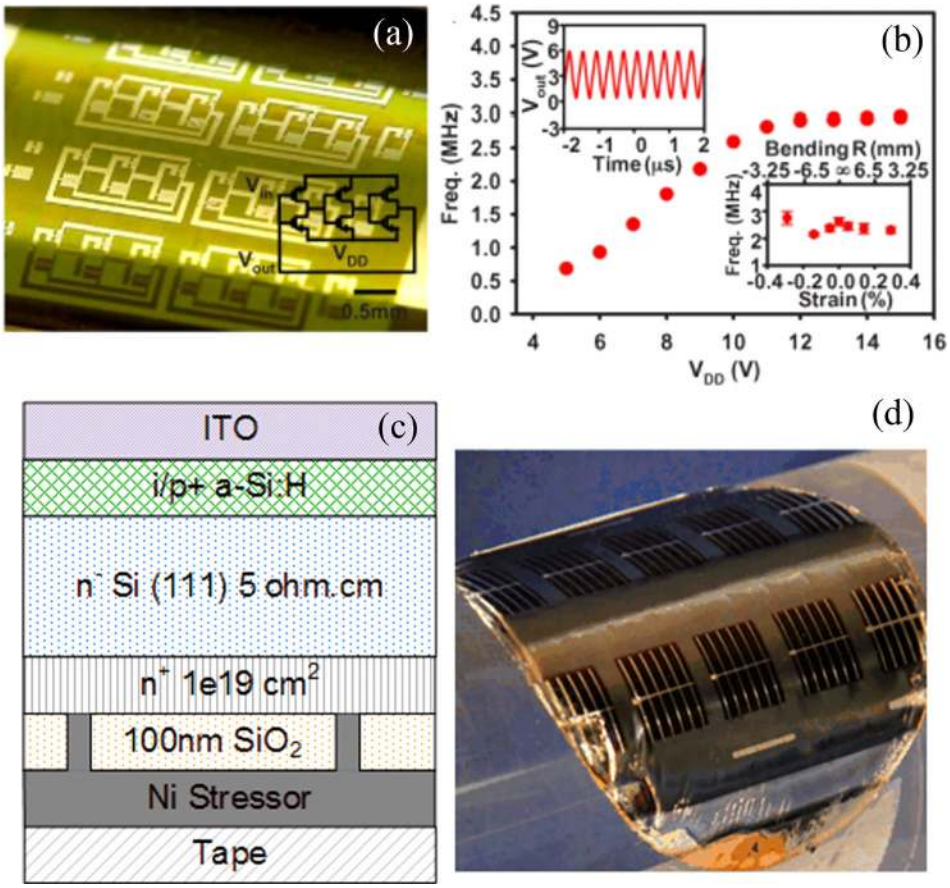

FIG. 12. (a) Image of an array of ring oscillator; the inset on the right bottom shows the circuit diagram. (b) Dependence of the oscillation frequency on the supply voltage (VDD); the upper left inset shows output characteristics of an oscillator evaluated with a 10 V supply (VDD); the lower inset shows the variation in frequency as a function of bending radius and corresponding bending strain. Reprinted with permission from Kim *et al.*, Science **320**(5875), 507–511 (2008). Copyright 2008 AAAS. (c) Schematic illustration of a flexible Si solar cell. (d) Photographs of flexible 20 μm thick silicon. Reprinted with permission from Shahrjerdi *et al.*, Solid-State Electron. **117**, 117–122 (2016). Copyright 2016 Elsevier.

sensor interfaces. Bendable Op-Amp design has become an increasingly interesting subject as many flexible sensors need them as an integrated part. Several Op-Amps, in different semiconductor material classes, have been reported for flexible electronics.[198–201] Many of these have poor performance in comparison to conventional Si technology. For example, an a:Si op-amp[198] as a part of a 4-b digital-to-analog converter on a glass substrate, investigated for threshold instability in a time varying form, shows varying threshold voltage when Op-Amp is stressed. Another example is the non-Si Op-Amp based on IGZO TFTs[200] bent to a radius of 5 mm. The bent amplifiers show the same output behavior as the flat. The high-performance bendable op-amps on the polyimide substrate, realized with printed ribbons of single-crystalline Si, have a voltage gain of 4 dB, a unity-gain frequency of ≈100 kHz, and can be bent to a radius of 6 mm, which corresponds to a strain of 0.23%.[202] Another example is the low noise amplifier (LNA) circuit realized by Kao and Chang[203] in a 0.18 μm technology on a thinned Si substrate of 90 μm. The LNA integrated with active and passive devices on plastic forms the front-end of a receiver. This work investigated the loss mechanisms of the parasitic effect of inductor before and after thinning of Si to 90 μm, but the effects of bending stress on the circuit performance were not provided.

5. Memory cells

The theoretical and physical limits of the traditional information storage technology have driven new generation data storage devices. To fabricate a fully functional flexible memory and prevent unwanted effects due to leakage current paths through adjacent cells, each memory cell must be integrated with a switching component such as a transistor. The high performance UTCs can meet flexible, fast, high- endurance, and scalable memory devices. A nonvolatile resistive random access memory (RRAM) array using a single crystal Si transistor and a memristor on flexible substrates was reported by Kim *et al.*[204] The n-channel MOSFETs transferred from a Si-on-insulator (SOI) wafer were used as a switching element of memory. A static random access memory (SRAM) cell is presented by Shahrjerdi and Bedell[205] as the integral element of system on chip (SoC) integrated circuits. In this work, bending tests were performed using circular cylinders with different radii of curvature (R) from 6.3 to 15.8 mm, shown in Fig. 13(a). The transfer characteristics of n-FET under different tensile bending conditions exhibit slight V_{th} shift to smaller values ($\Delta V_{th} = 35$ mV at R = 6.3 mm). In these experiments, the bending was performed along the direction of the current flow in the (110) channel direction. Adequate stress management of UTCs is required to minimize the effect of bending stress. In this regard, additional enhancement to diminish warpage of UTCs has been investigated with Hybrid Systems-in-Foil (HySiF).[206] The dummy structures for the upper metal interconnect layer have been used to reduce the stress originating from the final nitride/oxide passivation layer [Figs. 13(b) and 13(c)]. Additional enhancement with cancelling of bending stress effects on MOSFET is shown in Fig. 13(d).[207] The achieved current at saturation for this particular device in

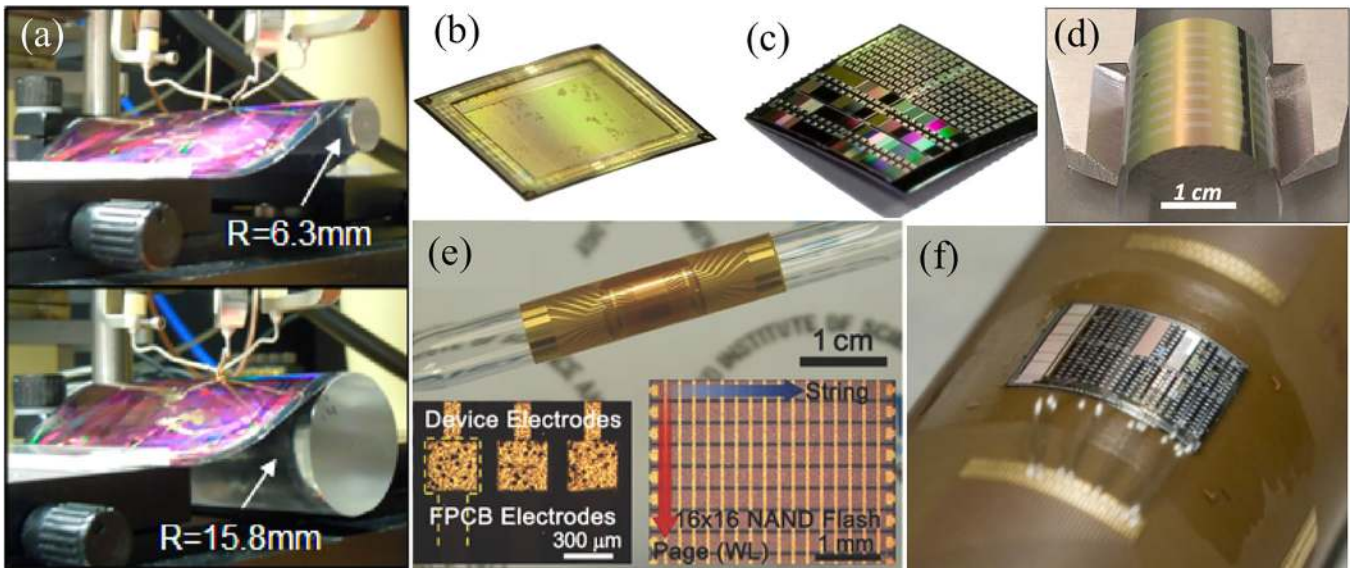

FIG. 13. Bending stability of the flexible circuits. (a) Photograph of a flexible circuit under tensile bending tests at two different radii of curvature. Reprinted with permission from Shahrjerdi and Bedell, Nano Lett. **13**(1), 315–320 (2012). Copyright 2012 American Chemical Society. Photos of two 20 μm thin chips originating from the same wafer: (b) layout-optimized highly integrated IC exhibiting small warpage and (c) coarsely integrated chip showing large warpage. Harendt *et al*., Solid-State Electron. **113**, 101–108 (2015). Copyright 2015 American Chemical Society. (d) MOSFET fabricated with the device- first/release-last approach under bending. Rojas *et al*., ACS Nano **8**(2), 1468–1474 (2014). Copyright 2015 American Chemical Society. (e) Photograph of the highly compliant ACF-packaged f flexible Si NAND flash memory wrapped on a glass rod (diameter of 7 mm). The OM image of the electrode area (left) and the active device area (right) are shown in insets. Reprinted with permission from Kim *et al*., Adv. Mater. **28**(38), 8371–8378 (2016). Copyright 2016 John Wiley and Sons. (f) Bending of the ultra-thin Si-chip on flexible substrate. Wacker *et al*., Semicond. Sci. Technol. **29**(9), 095007 (2014). Copyright 2014 IOP Publishing.

UTCs (<5 μm) was 6.2 μA/μm with an on/off ratio of 3 decades, a threshold voltage of 0.36 V, and a subthreshold swing of 145 mV/dec. This indicates that the competitive metrics and the data for different bending radii can be improved through optimization and more advanced infrastructure. This type of minimization of process-induced stress for cost-efficient means of stress management could be an interesting future direction.

Further improvements have been reported in UTC memory cells with a simultaneous roll transfer and interconnection of Si-based flexible NAND flash memory (f-NAND) based on a highly productive roll-to-plate anisotropic conductive film (ACF) packaging [Fig. 13(e)].[208] In this study, an ultra-thin f-NAND chip is presented on an intermediate transfer substrate by bonding the Si NAND flash on a rigid glass and subsequently removing the handle wafer. They testified high performance specifications such as I_{on}/I_{off} ratio (>102 at V_{read}), reproducible endurance (>103 switching cycles), and long retention (>104 s).

In another report, electromechanical reliability of UTCs, including digital gates, was tested by the FleX^{TM} Silicon-on-Polymer^{TM} process where standard full thickness SOI wafers are transformed into flexible wafers and subsequently ultra-thin physically flexible die.[209] This work advanced the previous effort using single-crystal-Si MOSFETs in a 0.8 μm CMOS process with 20 μm thickness, bending on cylinders of radii of curvature down to 10 mm,[88] as shown in Fig. 13(f).

CMOS compatible metal-insulator-metal capacitors (MIMCAPs) on a mechanically flexible Si (100) fabric with 25 μm thickness have been reported by Rojas *et al*. as key components of dynamic random access memory (DRAM).[210] The bending stress effects reported in this work indicate the mechanical robustness (minimum bending radius of 10 mm at an applied strain of 83.33% and a nominal strain of 0.125%) of devices and their consistent electrical behavior regardless of the applied mechanical stress. Recently, Kim *et al*. demonstrated a wearable and fully multiplexed Si nonvolatile memory array with nanocrystal floating gates.[211] In this study, a deformable charge trap floating gate memory (CTFM) based on single-crystal Si has been fabricated under ambient conditions and process compatibility with conventional CMOS fabrication processes. The presented system measures the heart rates after exercise stress by interfacing with wearable Si amplifiers and on-board electrodes and stored in CTFMs. Accordingly, they used a pseudo-CMOS inverter composed of four n-type MOS transistors to amplify ECG signals and subsequently acquire the heart rate.

B. Circuit-level bending stress effect mitigation

The strategies to mitigate stress effects in flexible electronics or to exploit the new opportunity offered by bending is likely to gain more importance as the flexible electronics research makes way to the market. There have been few attempts to minimize or compensate the effects of bending-induced stress on devices and circuits. The three main approaches which have been reported so far include (1) locating or embedding the device and circuits in the neutral plane, (2) distributed islands of rigid and stiff electronic components on flexible and stretchable substrates, and (3) optimal layout orientation for the circuits, possibly considering the expected bendability during use. A few examples of these methods are discussed below.

For reliable systems able to experience multiple bending during their lifetime, the UTCs are encapsulated between polymeric layers, particularly at the neutral surface in order

to minimize the stress induced by deformation.[68,212,213] The polymeric multilayer structures with simple circuit such as logic gates, inverters, ring oscillators, and differential amplifiers placed in the neutral surface have been reported by Kim *et al.*[188] to obtain flexible electronics with the minimal effect related to compression and tension. The 3-stage ring oscillator they fabricated using the printed single crystalline Si ribbon on the plastic substrate for studying the bending effect is shown in Figs. 12(a) and 12(b). They reported slight but nonsystematic variations in the parallel channel ring oscillator on Si wafers under uniaxial strain. The speed enhancement is insignificant due to the simultaneous strain effect on both NMOS and PMOS. From this, it may be concluded that perpendicular channel ring oscillators prove to be more beneficial because of their high-speed enhancement under bending. A differential amplifier integrated by combining nine transistors (a current source, a differential pair, and a current mirror) to provide a voltage gain of ∼1.4 for a 500 mV peak-to-peak input signal shows that measured gains at various tensile strains vary by less than ∼20%.[188] In this work, the stretchable differential amplifiers undergo tensile strain of 0% and 5%. A stable output is demonstrated with tensile strains up to 5%. Another example of using the neutral surface is reported by Hwang *et al.*,[186] where the active layer is encapsulated by thin polymer layers, thereby placing the metal near the neutral mechanical plane.

The distributed islands of rigid and stiff electronic components involve local modification of the flexible and stretchable substrates to mechanically support devices. Wagner's group at Princeton initiated this approach by integrating stiff islands of Si based devices and connecting them with compliant metallic conductors patterned on a soft substrate.[214,215] The concept was broadened by tuning the local stiffness of a Polydimethylsiloxane (PDMS) substrate by controlling the cross-linking density.[216,217] These elementary technologies led to system-level integration, where macroscopic ICs (mm to cm scale) were directly embedded in an elastomer matrix to allow immediate commercialization.[216–219] Recently, this approach has been improved toward a stretchable electronic substrate by employing multiple soft polymer layers patterned around silicon chips, which act as surrogates for conventional CMOS electronics chips, to create a controllable stiffness gradient.[220]

In terms of the optimal layout configuration to mitigate the stress and strain effects, Yuan *et al.*[194] reported a ring oscillator with different orientation layouts in each inverter cell. The two types of inverter cell layouts presented in this work include (1) the p-channel perpendicular to the n-channel (perpendicular layout) and (2) the p-channel parallel to the n-channel (parallel layout). The measurement results demonstrate a 7.4% speed enhancement of the ring oscillator with the perpendicular configuration under the uniaxial tensile strain to the parallel one. Accommodating the potential bending related changes at the design stage itself will be an interesting future direction.

VII. CONCLUSION

A review of recent progress on studies related to stress-induced effects in flexible electronics and their modeling have been presented in this paper. The focus of the paper was to analyze various stress/strain induced effects on the performance of electronics on flexible substrates and give new mathematical description of these bending induced effects to advance the CAD tools for designing of the next generation flexible electronics. The variations in the electrical parameters such as mobility, threshold voltage, and the device performance (static, dynamic) because of various bending induced stresses have been thoroughly presented. The effects of bending, material, mechanics, crystal axis, and band structure of the devices on UTCs have also been presented along with few strategies to compensate or minimize the effects of bending. The changes in the device and circuit response due to bending have been captured with mathematical relations, and their efficacy has been demonstrated by comparing the device output using these relations with experimental results reported in the literature. These results open new avenues for predicting the device behavior under various bending conditions and to explore the ways to compensate such effects. A few methods that have been adopted to minimize or compensate the effects of bending in devices and circuits have been discussed in Sec. IV. The minimization and mitigation of the bending effect by placing the device in the neural surface of the structure are popular and have been used in many of the circuits reported thus far for flexible electronics. The approach of using the neutral plane is attractive as it allows us to use the conventional planar fabrication and design tools, without worrying about the stress-induced effect, as the devices in neutral surfaces experience minimal or zero strain. However, this is not enough as it is challenging to fabricate all devices in neutral plane. Further for heterogeneous integration and 3D integration on flexible substrates, the neutral plane may not be possible and new methods will be needed to compensate the bending effects. The new knowledge will open avenues for further advances in flexible electronics. For example, with the knowledge of the response of devices spread over an area, one can perform inverse calculations and predict the shape of substrates on which these devices are present. This will be a new direction in the field of flexible electronics as the effects of bending, which were hitherto considered challenges to be overcome through various compensation methods, could be used to extract more information from bendable or conformable systems. Therefore, in addition to reviewing the current state of bending related effects in flexible electronics, this review paper also lays strong foundation for the new directions in flexible and large area electronics.

ACKNOWLEDGMENTS

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