



HAL
open science

BEOL Thermal Resistance Extraction in SiGe HBTs

K. Nidhin, Suresh Balanethiram, Deleep Nair, Rosario d'Esposito, Nihar Mohapatra, Sebastien Fregonese, Thomas Zimmer, Anjan Chakravorty

► **To cite this version:**

K. Nidhin, Suresh Balanethiram, Deleep Nair, Rosario d'Esposito, Nihar Mohapatra, et al.. BEOL Thermal Resistance Extraction in SiGe HBTs. IEEE Transactions on Electron Devices, 2022, pp.1-6. 10.1109/TED.2022.3215715 . hal-03846371

HAL Id: hal-03846371

<https://hal.science/hal-03846371>

Submitted on 10 Nov 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

BEOL Thermal Resistance Extraction in SiGe HBTs

Nidhin K, Suresh Balanethiram, *Member, IEEE*, Deleep R Nair, *Member, IEEE*, Rosario D'Esposito, Nihar R. Mohapatra, *Senior Member, IEEE*, Sebastien Fregonese, Thomas Zimmer, *Senior Member, IEEE*, and Anjan Chakravorty, *Member, IEEE*,

Abstract—A prior estimate of the impact of thermal resistance from the back-end-of-line (BEOL) metallization layers is crucial for an accurate circuit design and thermally aware device design. This paper presents a robust technique to extract the thermal resistance component originating from the BEOL metal layers in silicon germanium heterojunction bipolar transistors (SiGe HBTs). The proposed technique is first tested on data generated using analytical equations and later validated with 3D TCAD simulation. The results clearly show that the exact contribution of the BEOL to the overall thermal resistance is captured in the proposed approach. Finally, we verified the method using measured data obtained from fabricated SiGe HBT structures using Infineon B11HFC technology. The extracted parameters show reasonable accuracy and consistency across different emitter dimensions and BEOL configurations.

Index Terms—SiGe HBTs, self heating, thermal resistance, back-end-of-line (BEOL), parameter extraction, compact models.

I. INTRODUCTION

A serious concern about the modern silicon germanium heterojunction bipolar transistors (SiGe HBTs) is the self-heating induced degradation of high-frequency performance and long-term reliability of the device [1]. This is why a self-heating aware device design has attracted the attention of researchers [2]–[4]. On the other hand, to ensure a reliable circuit design, the transistor model is supposed to accurately predict the electrothermal effect using an appropriate thermal sub-circuit. The static thermal network essentially involves two connected elements, a dependent current source equal to the total dissipated electrical power (P_d) and a thermal resistance (R_{th}). The former is directly obtained from the electrical network, while the latter depends on the transistor structure and material thermal conductivity. Fig. 1 shows a typical transistor structure including the front-end-of-line (FEOL) Si substrate and back-end-of-line (BEOL) metal layers. Since the power dissipation happens mostly at the base-collector junction, the generated heat flows towards both the FEOL

substrate and BEOL stack composed of metal layers and inter-layer dielectrics. Therefore, the overall R_{th} has two components in parallel, the FEOL component (R_s) and the BEOL component (R_m) as shown in Fig. 1. Note that the resistor R_m additionally includes the thin SiGe base as well as mono and poly-emitter portions (part of upward heat flow). As the thermally insulating inter-layer dielectrics constitute bulk of the BEOL portion along with vias and contacts, a small but non-negligible amount of heat flows upwards [5], [6]. Note that for electrical parameter extraction purposes, special test structures are designed where the emitter is grounded leading to a higher amount of upward heat flow. In case of convective boundary at the chip-ambient interface, thermal ground at the top surface in Fig. 1 assumes that the extracted BEOL thermal resistance additionally includes the effect of the convective boundary condition. Also there can be multiple heat flow path through BEOL as elaborated in [7]. Alternatively, the heat can flow to another device via the BEOL metal line. The fraction of the total heat flow through these BEOL paths depends on the actual structure, material properties and the nearby devices' temperature. This results in a different finite values of R_m . From the perspective of device performance, the impact of BEOL design has also been investigated in [8]. While R_m is relatively temperature independent, the variation of R_s with temperature is significant due to the temperature-dependent thermal conductivity ($\kappa(T)$) of Si, which can be expressed as

$$\kappa(T) = \kappa(T_0) \left(\frac{T_0}{T} \right)^\alpha. \quad (1)$$

Here, $\kappa(T_0)$ is the thermal conductivity of Si at the nominal temperature, T_0 . While extracting the thermal resistance parameters for accurate modeling purpose, the parameter α in the Si thermal conductivity model plays a crucial role; and sometimes its value deviates from the physically expected values due to the negligence of a finite R_m component [9], [10]. Also, a proper estimation of the R_m component from characterization data can help us obtain a reliable model for R_m depending on the number of BEOL metal layers and their design configurations. In specific situations, an accurate estimation of R_m can help the modeling engineer to de-embed the effects of huge BEOL metal stacks which may not affect the actual device placed in circuit. Indeed, our test structure (used in section IV) additionally has a very short BEOL thermal path to a heat sink (ground plane) allowing us to identify and correct the contribution of R_m on devices in actual circuit layout configuration.

Different approaches have been reported in the literature to separate the FEOL and BEOL components of thermal resistance [11]–[13]. The work in [11] extracted the FEOL

Nidhin K, D. R Nair, and A. Chakravorty are with the Department of Electrical Engineering, IIT Madras, Chennai 600036 India. email: ee15d030@ee.iitm.ac.in.

S. Balanethiram is with National Institute of technology Puducherry, Karaikal 609609 India. email: sureshbalanethiram@gmail.com.

Nihar R. Mohapatra is with the Department of Electrical Engineering, IIT Gandhinagar, Gandhinagar 382355 India. email: nihar@iitgn.ac.in.

S. Fregonese, and T. Zimmer are with IMS Laboratory, University of Bordeaux, 33400 Talence, France. email: sebastien.fregonese@ims-bordeaux.fr, thomas.zimmer@ims-bordeaux.fr.

R. D'Esposito is with Micron Semiconductor, 67051 Avezzano, Italy.

This work was supported in part by ISRO project ELE/17-18/176/ISRO/ANJA, in part by DST, India, under Project EMR/2016/004726

The authors would like to thank Infineon for providing Silicon hardware. The test-structure designs used in this work were a part of the joint European research project DOTSEVEN.

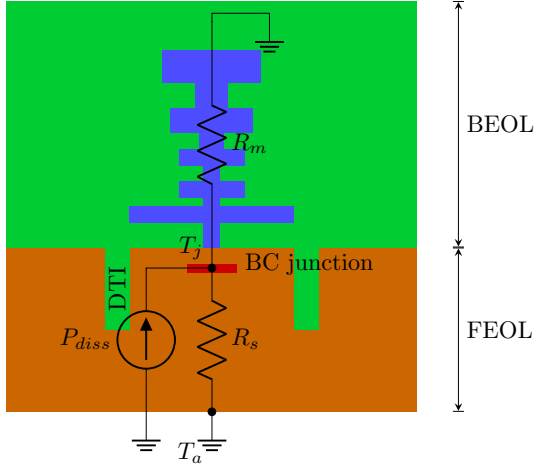


Fig. 1. Schematic representation of a typical transistor cross section including BEOL. The base collector junction is the heat source and is represented as a current source in the equivalent circuit. The total resistance from heat source to ambient in the upward direction is represented by R_m and the same in the downward direction is represented by R_s in the equivalent circuit.

component by de-embedding the BEOL and the pads. The disadvantage of this method is that one requires test structures with multiple M1 bar widths to extract the resistance components. An analytical method to estimate the thermal resistance offered by the BEOL was proposed in [12]. However, this method requires the knowledge of exact geometry and material properties of the BEOL stack. Another analytical technique to extract both the FEOL and BEOL components of the thermal resistance was proposed in [13]. The method extracts these components by choosing three points in the R_{th} vs T_j data. But finding R_m and α from characterization data is essentially an inverse problem; hence not only difficult but also sensitive to the data in use. Therefore, it is not advisable to depend on only certain data points. It is found that application of a smoothing function on the overall available data set ensures an extraction of the thermal parameters that are less sensitive to the measurement noise. This paper presents a reliable methodology to simultaneously extract R_m and α from characterized data sets. Section II elaborates the extraction methodology, while Section III demonstrates the validation of the proposed methodology using analytically generated synthetic data and TCAD simulation of different transistor structures. In section IV, we apply our technique on measured data obtained from different SiGe HBTs fabricated in state-of-the-art B11HFC process from Infineon and analyze the obtained results. Finally, we conclude in Section V.

II. EXTRACTION TECHNIQUE

Let $G_{th}(T_a, P_d)$ be the overall thermal conductivity of the structure as a function of the ambient temperature (T_a) and electrical power dissipation (P_d). This data can be obtained from device characterization [14], [15] and is often presented in the literature using the conventional R_{th} versus T_j plot [16], [17]. $R_{th} = 1/G_{th}$ is the overall thermal resistance of the structure and $T_j = T_a + P_d R_{th}$ is the operating temperature of the device. However, for near-zero P_d the overall thermal

conductance of the structure is mostly a function of T_a alone and is given as

$$G_{th}(T_a) = G_s(T_a) + G_m \quad (2)$$

where $G_m = 1/R_m$ is the temperature-independent BEOL thermal conductance. On the other hand, $G_s = 1/R_s$ is the thermal conductance corresponding to the FEOL substrate component, given as

$$G_s(T_a) = G_{s0} \left(\frac{T_0}{T_a} \right)^\alpha \quad (3)$$

$G_{s0} = G_s(T_0)$ is the FEOL thermal conductance at T_0 . Note that T_a and T_0 (usually $T_0=300$ K) are known quantities. The unknown quantities are G_{s0} , α and G_m . One can begin by eliminating G_m using G_{th} evaluated at T_a and T_0 as

$$G_{th}(T_0) - G_{th}(T_a) = G_{s0} \left[1 - \left(\frac{T_0}{T_a} \right)^\alpha \right] \quad (4)$$

From the characterized data one can obtain the LHS of (4) as a function of T_a and use an iterative curve fitting approach to solve for α and G_{s0} , simultaneously. Using (2) at $T_a = T_0$, one obtains the temperature-independent G_m since $G_{th}(T_0)$ and $G_s(T_0)$ are already known. The robust nature of the extraction approach is due to the fact that the fitting function in the RHS of (4) is simple and involves no differentiation of the actual data. Besides, the estimated value of the parameter α is not influenced by R_m ; hence, it reflects a physically consistent value corresponding to the FEOL substrate material.

III. VALIDATION OF PROPOSED METHODOLOGY

A. Analytically generated synthetic data

First we test the extraction approach on analytically generated synthetic thermal conductance data based on a temperature-dependent G_s and a constant G_m . One can use the well-known analytical model reported in [18] and [19] to generate T_j -dependent G_{th} data for different values of T_a as

$$G_{th}(T_j) = \frac{G_{s0} \cdot T_0^\alpha}{(1 - \alpha)} \cdot \frac{T_j^{1-\alpha} - T_a^{1-\alpha}}{T_j - T_a} + G_m \quad (5)$$

with, α , G_{s0} and, G_m as model parameters.

The G_{th} is evaluated for T_j in the range (T_a , 600 K) with $\alpha = 1.4$, $G_{s0} = 3.357 \times 10^{-4}$ W/K, and $G_m = 0.1$ mW/K in (5). The process is repeated for multiple values of T_a in steps of 30 K between 300 K and 420 K. Subsequently, the electrical power dissipation in the selected range of T_j is calculated, for each T_a , as $P_d(T_j) = G_{th}(T_j) \cdot (T_j - T_a)$. The resulting $T_j(P_d)$ for different T_a values are shown with symbols in Fig. 2a. Similarly, G_{th} is plotted against P_d for multiple T_a values and extrapolated to $P_d = 0$ point to calculate the $G_{th}(T_a)$. Taking $T_0 = 300$ K, $G_{th}(T_0) - G_{th}(T_a)$ is calculated and non linear regression using (4) is done on this data to extract the parameters.

Since there are two parameters in (4), the nonlinear regression is done by fixing one parameter. This makes the equation single-variable and easy to solve. Since the value of G_m is less than G_{s0} , the value of G_{s0} will lie in the range $G_{th}(T_0)/2$ to $G_{th}(T_0)$. G_{s0} is varied in this range, and the

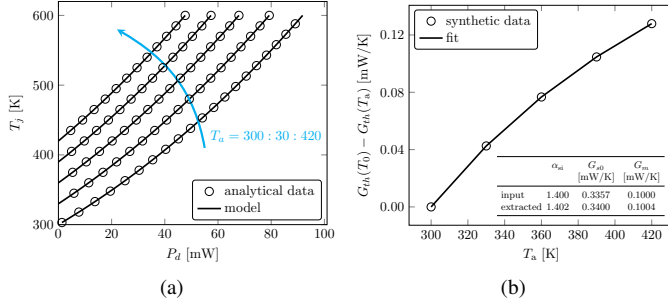


Fig. 2. (a) Dissipated power dependent junction temperature at different ambient temperatures: comparison of analytically generated synthetic data and model using the extracted parameters. (b) Ambient temperature dependent $G_{th}(T_0) - G_{th}(T_a)$: analytical data and fitting by RHS of (4) to extract G_{s0} and α .

corresponding α and mean squared error are recorded. The G_{s0} and corresponding α for which error is minimum are chosen as the extracted values. Fig. 2b shows the data points used for regression (symbols) and the fit to it (line). While generating the synthetic data, we have used $G_m = 0.1$ mW/K which is exactly returned by the extraction scheme. The extracted values, tabulated in Fig. 2b are highly in agreement with the input values used to generate the data; hence, the model evaluated with these extracted values (lines in Fig. 2a) shows an excellent match with the synthetic $T_j(P_d)$ data sets (symbols).

B. TCAD generated data

Using commercially available Synopsys Sentaurus TCAD simulator [20], 3D thermal simulations of an HBT structure are carried out. The structure consisted of a substrate with a heat sink maintained at T_a at the bottom surface and a BEOL structure with only one metal (Copper) layer. A heat sink is also placed on the top surface of BEOL, and a rectangular heat source of area $5 \times 0.2 \mu\text{m}^2$ is placed at the location of base-collector junction, 200 nm below the FEOL-BEOL interface. Here 200 nm is the sum of widths of the emitter and the base regions. Note that we approximate the actual non-uniform heat source with a rectangular uniform heat source. Since the proposed extraction method is independent of the uniformity of the heat source, we adopted this approximation, instead of a more rigorous approach followed in [21]. The heat source injects power at uniform power density, and all other outer surfaces except the heat sinks are assumed to be thermally insulating. The injected power is varied from 0 to 30 mW, and the temperature at the middle of the heat source is recorded as the junction temperature T_j . A constant thermal conductivity is used for BEOL materials to ensure that R_m is temperature independent. The temperature dependence of thermal conductivity in Silicon is included using (1). The simulations are repeated for three different alpha values: 1.3, 1.4 and 1.5, keeping $\kappa(T_0) = 1.702$ W/(cm-K) [22].

Fig. 3a shows the dissipated power-dependent junction temperature at different ambient temperatures obtained from TCAD simulations with $\alpha = 1.4$. Thermal conductance $G_{th} = P_d/(T_j - T_a)$ is calculated from the TCAD data and

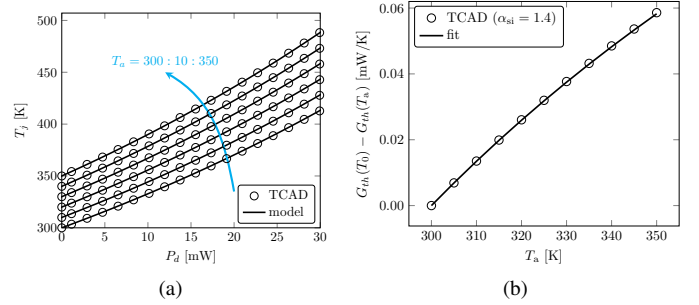


Fig. 3. (a) Dissipated power dependent junction temperature at different ambient temperatures: comparison of 3D TCAD thermal simulation (with $\alpha = 1.4$) and model using the extracted parameters. (b) Ambient temperature dependent $G_{th}(T_0) - G_{th}(T_a)$: TCAD data and fitting by RHS of (4) to extract G_{s0} and α .

TABLE I
PARAMETERS EXTRACTED FROM TCAD DATA.

	α		G_{s0} [mW/K]	G_m [mW/K]
	expected	extracted	extracted	extracted
TCAD1	1.300	1.300	0.3013	0.0252
TCAD2	1.400	1.399	0.3003	0.0262
TCAD3	1.500	1.501	0.2990	0.0275

extrapolated to obtain $G_{th}(T_a)$. The corresponding nonlinear regression plot and the extracted parameters are presented in Fig. 3b and Table I, respectively. The results of three TCAD structures presented in Table I correspond to different α values, but identical geometry and $\kappa(T_0)$ values. One can observe that the extracted α values are in excellent agreement with the expected values. Since the thermal conductivity value at 300 K ($\kappa(T_0)$) and the structure are the same, the extracted G_{s0} and R_m values remain the same across these devices, as expected. The correlation between symbols (TCAD) and lines (model evaluated with extracted parameters) in Fig. 3a re-confirms that the values extracted are accurate.

C. Generating T_a dependent data

The method proposed here requires peak temperature data as a function of dissipated power at many different ambient temperatures. In cases where $T_j(P_d)$ for single T_a is available, one can generate the required data. This subsection explains how the $T_j(P_d)$ data for multiple ambient temperatures can be generated from the data measured at a single T_a . The total dissipated power for a given T_j and T_a can be obtained by multiplying (5) with $T_j - T_a$ on both sides and following simple algebraic steps one obtains

$$\begin{aligned}
 P_d(T_j, T_a) &= \frac{T_j - T_a}{R_m} + G_{s0} \frac{T_j^{1-\alpha} - T_a^{1-\alpha}}{(1-\alpha)T_0^{-\alpha}} \\
 &= \left(\frac{T_j - T'_a}{R_m} + G_{s0} \frac{T_j^{1-\alpha} - T'_a{}^{1-\alpha}}{(1-\alpha)T_0^{-\alpha}} \right) \\
 &\quad + \left(\frac{T'_a - T_a}{R_m} + G_{s0} \frac{T'_a{}^{1-\alpha} - T_a^{1-\alpha}}{(1-\alpha)T_0^{-\alpha}} \right) \\
 &= P_d(T_j, T'_a) + P_d(T_j = T'_a, T_a)
 \end{aligned}$$

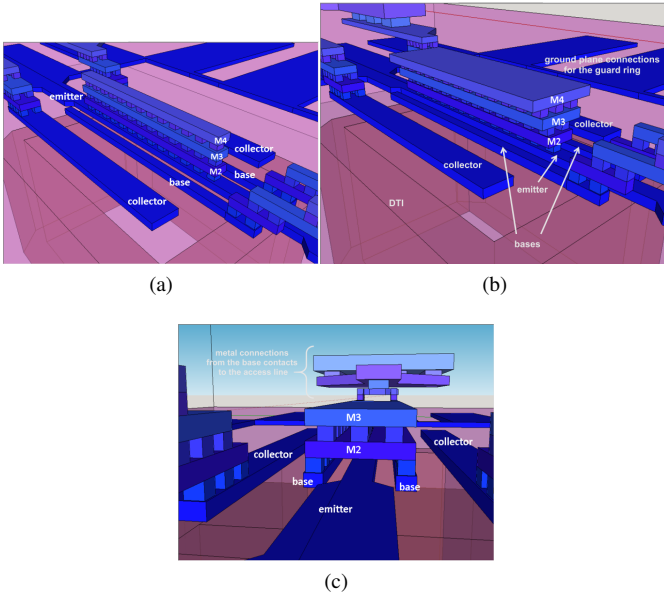


Fig. 4. The test structures considered (a) E4narr - test structure with 4 dummy metal layers of same width and length placed above emitter contact. (b) E4wide - test structure with 4 dummy metal layers placed above emitter contact, whose width increases from first layer to fourth layer. (c) B3- 3 level structure where the stacking of dummy metal layers are done directly above the base contact. The images are taken from [23].

$$= P_d(T_j, T'_a) + \Delta P_d. \quad (6)$$

Since ΔP_d is independent of T_j , formulation (6) signifies that the dissipated power dependent junction temperature data for another ambient temperature T'_a can be obtained just by shifting the original curve along the power axis by ΔP_d . From the $T_j(P_d)$ at a given T_a , one can, therefore, obtain other $T_j(P_d)$ curves for multiple different T'_a values.

Using this methodology, we have regenerated all the curves shown in Figs. 2a and 3a by shifting the lowest curve with $T_a = 300$ K and obtained perfect agreements with the corresponding TCAD generated curves. Thus we have verified the methodology which will be useful in the following section while applying our extraction scheme on actual measured data.

IV. EXTRACTION FROM MEASURED DATA

The state-of-the-art SiGe BiCMOS HBT technology from Infineon (B11HFC) having $f_T = 250$ GHz, $f_{\max} = 370$ GHz and six levels of metallization reported in [23] is used to demonstrate our extraction technique. The experimental data presented in this paper corresponds to a maximum of four metal layers (till M4). The transistors are isolated using deep trench isolations (DTI). The test structures had the same FEOL with an emitter dimension of $0.35 \times 5 \mu\text{m}^2$ but different metallization schemes in the BEOL part. In the first type, we have dummy metal layers of the same width and length directly above the emitter contact but not above the base and collector contacts as shown in Fig. 4a. This test structure will be called E4narr. The number denotes the last layer of the metal stack and E indicates that the metal dummies are on Emitter contact. In the second type, we have two test structures, namely E2wide and E4wide. Here the difference is

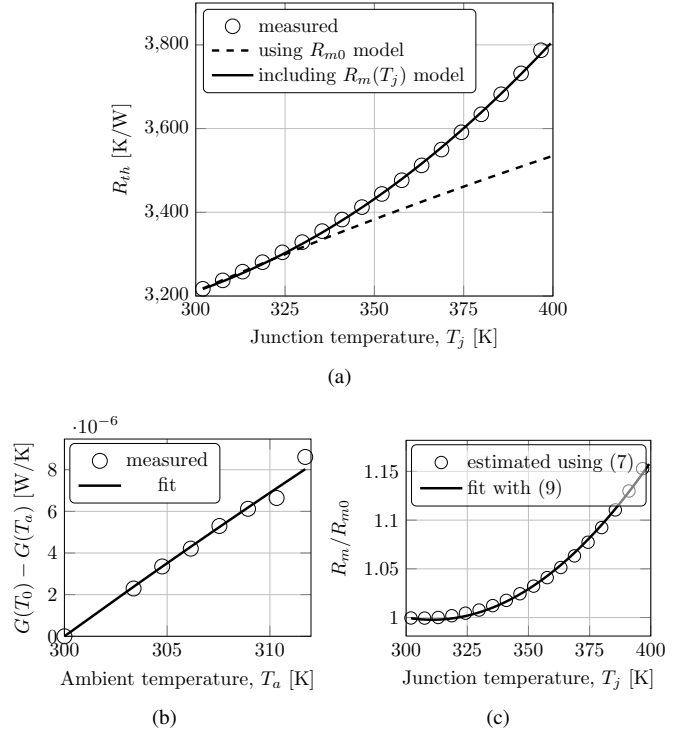


Fig. 5. (a) Junction temperature dependent thermal resistance: comparison of measured data (symbols) and model (lines) using the extracted parameters. Dashed line represent the constant R_{m0} model and solid line represent the model with temperature-dependent R_m . (b) Ambient temperature dependent $G_{th}(T_0) - G_{th}(T_a)$: measured data and fitting by RHS of (4) to extract G_{s0} and α . (c) R_m estimated using (7) with extracted R_{m0} .

that the width of the metal dummies on the emitter contact increases progressively as shown in Fig. 4b. Note that the total volume of metal on top of the emitter contact of E4wide structure is more than E4narr. Lastly, we have two other test structures named B2 and B3, where the metal dummies are placed directly on top of the base contacts but not on the emitter and collector contacts as shown in Fig. 4c. All the test structures considered in the study are listed in Table II.

In section III, for both synthetic and TCAD data, the BEOL thermal conductivity was kept constant. However, the actual BEOL thermal resistance varies with temperature due to the temperature-dependent thermal conductivity of the BEOL components. Since this dependence is significantly weak compared to that of FEOL, one can assume R_m to be independent of temperature especially at temperatures close to T_a . Therefore, for the R_m extraction, we are going to use only those data points which are close to T_a . Since $T_j(P_d)$ data for a single T_a is available for each kind of devices discussed above, required data for multiple T_a values are obtained using the shifting method elaborated in section III-C.

Fig. 5a compares the $R_{th}(T_j)$ data corresponding to the structure B3 obtained from measurement (symbols) and that obtained from (5) (dashed line) using the extracted parameters. Note that the extraction is carried out using the data points ($T_j < 313$ K) close to T_a . The non-linear regression plot for the same is shown in Fig. 5b. The model (dashed line) and the measurements are in excellent agreement in the low-temperature range as shown in Fig. 5a.

TABLE II
PARAMETERS EXTRACTED FROM MEASURED DATA [23].

Test Structure	α	G_{s0} [mW/K]	R_{m0} [K/W]	m_1 [K]	m_2 [K ²]
B2	1.3158	0.1702	7439	-4.46×10^{-4}	2.09×10^{-5}
E2wide	1.3125	0.1622	6855	-4.48×10^{-4}	2.02×10^{-5}
B3	1.3125	0.1636	6765	-4.29×10^{-4}	2.03×10^{-5}
E4narr	1.3125	0.1568	6575	-4.46×10^{-4}	1.85×10^{-5}
E4wide	1.3130	0.1719	6936	-4.84×10^{-4}	2.22×10^{-5}

After extracting α and G_{s0} and $R_m = R_{m0}$ at low temperature, the junction temperature (T_j) dependent R_m can be estimated from the measured $R_{th}(T_j)$ data as

$$\frac{1}{R_m(T_j)} = \frac{1}{R_{th}(T_j)} - \frac{1}{R_s(T_j)} \quad (7)$$

where

$$R_s(T_j) = (1 - \alpha) \cdot \frac{T_0^{-\alpha}}{G_{s0}} \cdot \frac{T_j - T_a}{T_j^{1-\alpha} - T_a^{1-\alpha}} \quad (8)$$

is the FEOL component of thermal resistance evaluated using the parameters extracted from the low temperature data. This temperature dependence of R_m can be captured with simple polynomial functions. Symbols in Fig. 5c shows the normalized variation of $R_m(T_j)$ calculated using (7). The variation of the extracted $R_m(T_j)$ from the measured data is not negligible unlike the ones enforced in the synthetic as well as the TCAD simulation in section III. Possible reasons for such a variation can be as follows. According to our modeling framework, all the regions above the heat source (i.e., the base-collector junction) including the thin SiGe base as well as the mono and poly-emitter portions are considered within the upward heat transfer path contributing to the overall R_m along with the actual BEOL stacks. The thermal conductivity of these base and emitter regions decrease significantly with temperature and contributes to the rise in R_m with temperature. Along with that the thermal conductivity of metals within the BEOL slightly reduces with temperature, causing an increase (although minor) in R_m with temperature. Note that in TCAD simulation (presented in section III), we have placed the heat source at the emitter finger and considered constant thermal conductivity for the metal layers; hence obtained a constant R_m .

It is clear that the FEOL component can be evaluated from the extracted parameters using (8) and subsequently $R_m(T_j)$ can be estimated using (7). Finally, assuming that the temperature-dependence of R_m can be captured with a parabolic function given as

$$R_m(T_j) = R_{m0} (1 + m_1(T_j - T_0) + m_2(T_j - T_0)^2), \quad (9)$$

the parameters m_1 and m_2 are extracted using simple polynomial fit. Fig. 5c presents a simple modeling results for $R_m(T_j)$ (normalized w.r.t. R_{m0}) obtained by using (9). After including this temperature dependent R_m model, the complete model (solid line) and the measured data (symbols) show excellent agreements as demonstrated in Fig. 5a.

Table II presents the result of extraction for all the devices considered in this study. As expected, since the FEOL is same

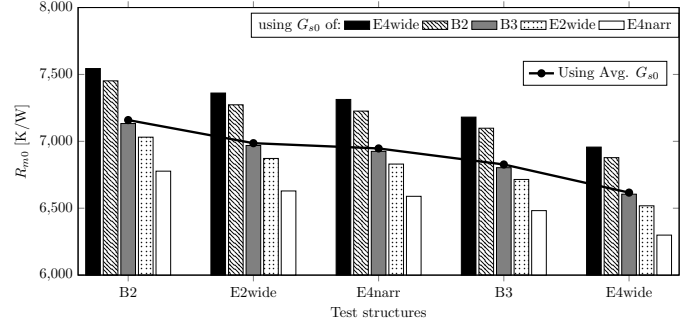


Fig. 6. R_{m0} for the test structures calculated using different G_{s0} values listed in Table II. The solid line represents R_{m0} obtained for each structure with an average G_{s0} .

for all the devices, α and G_{s0} values are in good agreement across the devices. Even the parameters of temperature dependent R_m are also in the same range. The variation in R_{m0} is expected because of the deliberate BEOL change made in the test structures. Since stacking more dummy levels reduces the BEOL thermal resistance [23], B3 has smaller R_{m0} than B2. Use of wider metal layers also reduces R_{m0} as it increases the volume of metal present in the BEOL structure. Therefore, we expect E4wide to have the least R_{m0} due to four levels of metal dummies above the emitter contact. However, we see that the extracted R_{m0} value of E4wide is not consistent. Such an error is mainly due to the sensitivity of the parameters obtained from a nonlinear extraction method. Eventually, we performed a sensitivity study on the extracted R_{m0} values by fixing the FEOL thermal resistance across the test structures. We calculate different R_{m0} values for a given test structure with different G_{s0} values listed in Table II following the relation, $1/R_{m0} = G_{th}(T_0) - G_{s0}$. The resulting R_{m0} values for all the test structures are represented as a bar chart in Fig. 6. The values of R_{m0} obtained for the test structures with an average G_{s0} are also plotted (solid line). Since these structures have the same FEOL, the solid line is a better representation of the actual R_{m0} variation. Note that these values are in alignment with our expectation, For example, we observe that using identical G_{s0} for all the test structures yields the least R_{m0} for the E4wide structure. From the various combinations considered in Fig. 6, the maximum deviation of R_{m0} from the corresponding average value is found to be less than 5.4%. For such an inverse problem, this range of error is fairly acceptable.

V. CONCLUSIONS

A robust method to extract the parameters related to the FEOL and BEOL components of thermal resistances in SiGe HBTs was presented. The method allows extraction of these components and their temperature dependent parameters. The method, when tested on synthetic or TCAD generated data, gave excellent results. We also applied the method on measured data obtained from devices with the same FEOL but different BEOL stack. The returned values were similar for FEOL and showed an expected trend for BEOL components across the devices confirming the proposed method's accuracy.

REFERENCES

- [1] U. S. Raghunathan, P. S. Chakraborty, T. G. Bantu, B. R. Wier, H. Yasuda, P. Menz, and J. D. Cressler, "Bias- and temperature-dependent accumulated stress modeling of mixed-mode damage in SiGe HBTs," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2084–2091, 2015. doi: 10.1109/TEDE.2015.2433299
- [2] J.-S. Rieh, J. Johnson, S. Furkay, D. Greenberg, G. Freeman, and S. Subbanna, "Structural dependence of the thermal resistance of trench-isolated bipolar transistors," in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2002, pp. 100–103. doi: 10.1109/BIPOL.2002.1042896
- [3] J.-S. Rieh, D. Greenberg, Q. Liu, A. J. Joseph, G. Freeman, and D. C. Ahlgren, "Structure optimization of trench-isolated SiGe HBTs for simultaneous improvements in thermal and electrical performances," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2744–2752, 2005. doi: 10.1109/TEDE.2005.859652
- [4] J.-S. Rieh, D. Greenberg, A. Stricker, and G. Freeman, "Scaling of SiGe heterojunction bipolar transistors," *Proceedings of the IEEE*, vol. 93, no. 9, pp. 1522–1538, 2005. doi: 10.1109/JPROC.2005.852228
- [5] R. D'Esposito, S. Fregonese, T. Zimmer, and A. Chakravorty, "Dedicated test-structures for investigation of the thermal impact of the BEOL in advanced SiGe HBTs in time and frequency domain," in *2016 International Conference on Microelectronic Test Structures (ICMTS)*, 2016, pp. 28–31. doi: 10.1109/ICMTS.2016.7476168
- [6] R. D'Esposito, S. Balanethiram, J.-L. Battaglia, S. Frégonèse, and T. Zimmer, "Thermal penetration depth analysis and impact of the BEOL metals on the thermal impedance of SiGe HBTs," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1457–1460, 2017. doi: 10.1109/LED.2017.2743043
- [7] R. D'Esposito, S. Frégonèse, A. Chakravorty, P. Chevalier, D. Céli, and T. Zimmer, "Innovative SiGe HBT topologies with improved electrothermal behavior," *IEEE Trans. Electron Devices*, vol. 63, no. 7, pp. 2677–2683, 2016.
- [8] R. D'Esposito, M. De Matos, S. Fregonese, S. Balanethiram, A. Chakravorty, K. Aufinger, and T. Zimmer, "Influence of the BEOL metallization design on the overall performances of SiGe HBTs," in *2016 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, 2016, pp. 358–360. doi: 10.1109/ICSICT.2016.7998920
- [9] A. Gupta, K. Nidhin, S. Balanethiram, R. D'Esposito, S. Fregonese, T. Zimmer, and A. Chakravorty, "Extraction of true finger temperature from measured data in multifinger bipolar transistors," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1385–1388, 2021. doi: 10.1109/TEDE.2021.3054602
- [10] Z. Huszka, K. Nidhin, D. Céli, and A. Chakravorty, "Extraction of compact static thermal model parameters for SiGe HBTs," *IEEE Trans. Electron Devices*, vol. 68, no. 2, pp. 491–496, 2021. doi: 10.1109/TEDE.2020.3045688
- [11] J. Li, D. Hitko, M. Sokolich, and P. Asbeck, "Experimental method to thermally deembed pads from r_{TH} measurements," *IEEE Transactions on Electron Devices*, vol. 53, no. 10, pp. 2540–2544, 2006. doi: 10.1109/TEDE.2006.882270
- [12] B. Yeats, "Inclusion of topside metal heat spreading in the determination of HBT temperatures by electrical and geometrical methods [GaAs devices]," in *GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. 21st Annual. Technical Digest 1999 (Cat. No. 99CH36369)*. IEEE, 1999, pp. 59–62.
- [13] S. Balanethiram, R. D'Esposito, A. Chakravorty, S. Fregonese, and T. Zimmer, "Extraction of BEOL contributions for thermal resistance in SiGe HBTs," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1380–1384, 2017. doi: 10.1109/TEDE.2016.2645615
- [14] M. Pfof, V. Kubrak, and P. Brenner, "A practical method to extract the thermal resistance for heterojunction bipolar transistors," in *Proc. 33rd Conference on European Solid-State Device Research (ESSDERC)*, 2003, pp. 335–338. doi: 10.1109/ESSDERC.2003.1256882
- [15] S. Balanethiram, J. Berkner, R. D'Esposito, S. Fregonese, D. Celi, and T. Zimmer, "Extracting the temperature dependence of thermal resistance from temperature-controlled DC measurements in SiGe HBTs," in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2017, pp. 94–97. doi: 10.1109/BCTM.2017.8112919
- [16] J.-S. Rieh, D. Greenberg, B. Jagannathan, G. Freeman, and S. Subbanna, "Measurement and modeling of thermal resistance of high speed SiGe heterojunction bipolar transistors," in *Proc. Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2001, pp. 110–113. doi: 10.1109/SMIC.2001.942350
- [17] A. K. Sahoo, S. Fregonese, M. Weib, C. Maneux, and T. Zimmer, "A scalable model for temperature dependent thermal resistance of SiGe HBTs," in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2013, pp. 29–32. doi: 10.1109/BCTM.2013.6798137
- [18] D. J. Walkey, T. J. Smy, R. G. Dickson, J. S. Brodsky, D. T. Zweidinger, and R. M. Fox, "Equivalent circuit modeling of static substrate thermal coupling using VCVS representation," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 9, pp. 1198–1206, 2002. doi: 10.1109/JSSC.2002.801200
- [19] S. Balanethiram, A. Chakravorty, R. D'Esposito, S. Fregonese, D. Céli, and T. Zimmer, "Accurate modeling of thermal resistance for on-wafer SiGe HBTs using average thermal conductivity," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3955–3960, 2017. doi: 10.1109/TEDE.2017.2724939
- [20] Synopsys TCAD, "Sentaurus: Sentaurus device user guide, release H-2013.03," 2013.
- [21] V. d'Alessandro, A. Magnani, L. Codecasa, N. Rinaldi, and K. Aufinger, "Advanced thermal simulation of SiGe: C HBTs including back-end-of-line," *Microelectronics Reliability*, 2016.
- [22] M. Schröter and A. Chakravorty, *Compact Hierarchical Bipolar Transistor Modeling with HICUM*. World Scientific, 2010. [Online]. Available: <https://doi.org/10.1142/7257>
- [23] R. D'Esposito, "Electro-thermal characterization, TCAD simulations and compact modeling of advanced SiGe HBTs at device and circuit level," *Doctoral dissertation, Univ. of Bordeaux, Talence, France*, 2016.