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BI-DIRECTIONAL FOUR QUADRANT (BDQ4) POWER CONVERTER DEVELOPMENT

FINAL REPORT

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prepared for

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I. INTRODUCTION

I - 1. The Problem

The need for the transformation of polyphase ac power with a given frequency to that of another frequency, including dc, arises in cases such as those involving: the controlled drive of machines, the efficient transfer of electric energy over high voltage dc lines and its temporary storage in secondary batteries, to name a few well known applications. Certain chemical and metallurgical processes require dc or deterministically mixed ac and dc power. Sophisticated equipment as computers or critical signal processors or monitors may require "no-break power". One can add the whole family of supplies of dc power which use the polyphase distribution network as primary source of energy common for communication, x-rays, radar and practically all electronic systems with a power consumption, in excess of several kilowatts.

A subgroup of the above named ac/ac and ac/dc converters requires a reversal of the controlled power flow. A common example is that of a battery charger, used for power "peak sharing" purposes. Low cost excess electric energy is stored in batteries at certain times of the day or night; this energy is then returned to the local or regional three phase network during the hours of peak demand. Valuable and, possibly, scarce fuel can be saved in this manner. The described process

can be implemented by the use of two separate pieces of equipment, (1) a controlled rectifier filter and (2) an inverter. The same process can be, preferrably, performed by one single converter with a reversible flow of controlled power. It will be indicated further on that every process involving "reactive" power components requires a recurrent and rapid succession of reversals of the flow of energy in and out of a power converter.

The interface between a polyphase ac and a dc system is, traditionally, envisioned as the connection of two voltage sources with the corresponding characteristics via an appropriate passive low frequency filter. The interposition of this filter between the two voltage sources is necessitated by the requirement to

a. avoid excessive currents that may arise from even minor and short lived differences between these voltage sources;

b. allow the reconciliation of character of the concerned sources with the jointly transferred energy;

c. prevent the "pollution" of either of the interlinked systems by the character of the opposite partner, namely ac or dc.

It is the primary objective of the here presented work to remove the need for a passive low frequency filter between two non-synchronized systems of the same or of different character. The implacable requirement

for an efficient reconciliation of the different characters of two interlinked systems is satisfied by providing the concerned converter with the capability to function as a non-dissipative active filter, concurrent with its performance of the function of transfer and control of the flow of energy in either direction.

The symbolic presentation of a controlled polyphase ac to dc converter is shown in Fig. I - 1.1. The three phase ac source of supply of energy is presented as a voltage source which "works" into controllable impedances. These controllable impedances are meant to symbolize the "controllability" of power intake by the converter, independent of variations of the impressed voltage and of the character of each of the impedances as "seen" by the feeding phase pairs. The dc output is symbolized as a voltage limited controlled current source.

The chosen presentation implies that the dc output port is short circuit proof and that its voltage will adjust automatically to the load, as seen by the converter. A number of these converters can be, furthermore, parallelled without the need for any specific precautions.

The main objective is to avoid the harsh conditions which are otherwise caused when two different voltage controlled systems are interlinked.

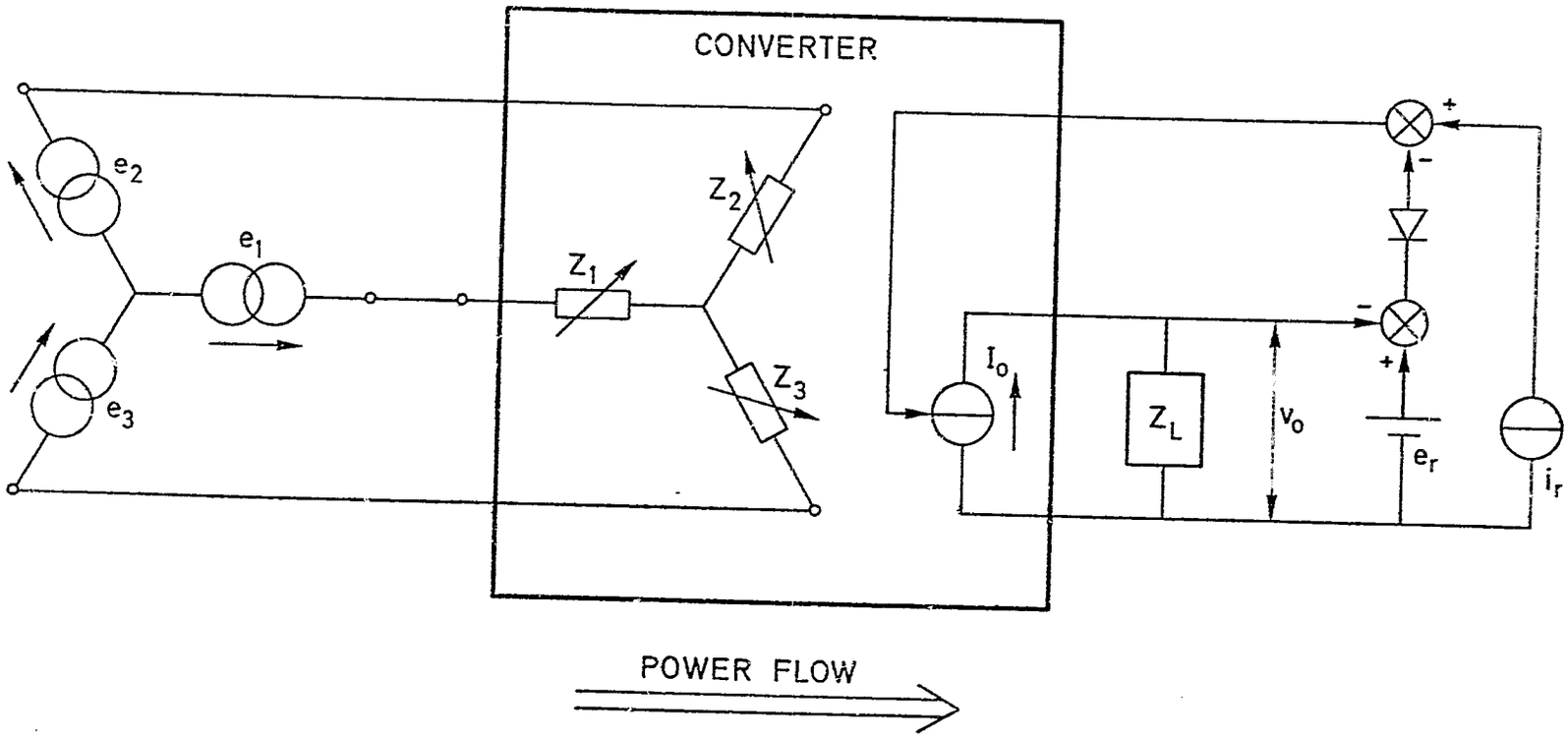


Fig. I - 1.1 Symbolic diagram of a three phase ac to controlled dc converter with the output characteristic of a controlled current source.

The converse of the system shown in Fig. I - 1.1, a dc to ac inverter, is shown in Fig. I - 1.2. Here the power flow emanating from a dc voltage source is controlled by the thereto connected variable impedance. The output ports are symbolized by three voltage limited current sources. The direction of transfer of energy is indicated in both figures.

The intended process is the converse of the one described with reference to Fig. I - 1.1. Again, a number of converters can be parallelled without the need for precautions to prevent excessive currents.

Energy can be transferred free of most customary hazards from one voltage source to another without concern for synchronization, momentary voltage excursions within design limits and the character of the linked systems.

An ac to ac converter could consist of a back to back tandem combination of the systems indicated in Figs. I - 1.1 and I - 1.2. A thorough integration of these two systems then removes the need for an internal dc link. Such a system adjusts its input-output characteristics in such a manner that those ports which function as output ports assume momentarily the character of current sources.

I - 2. The Content of the Study

The technical problem area as a whole is the subject of this study.

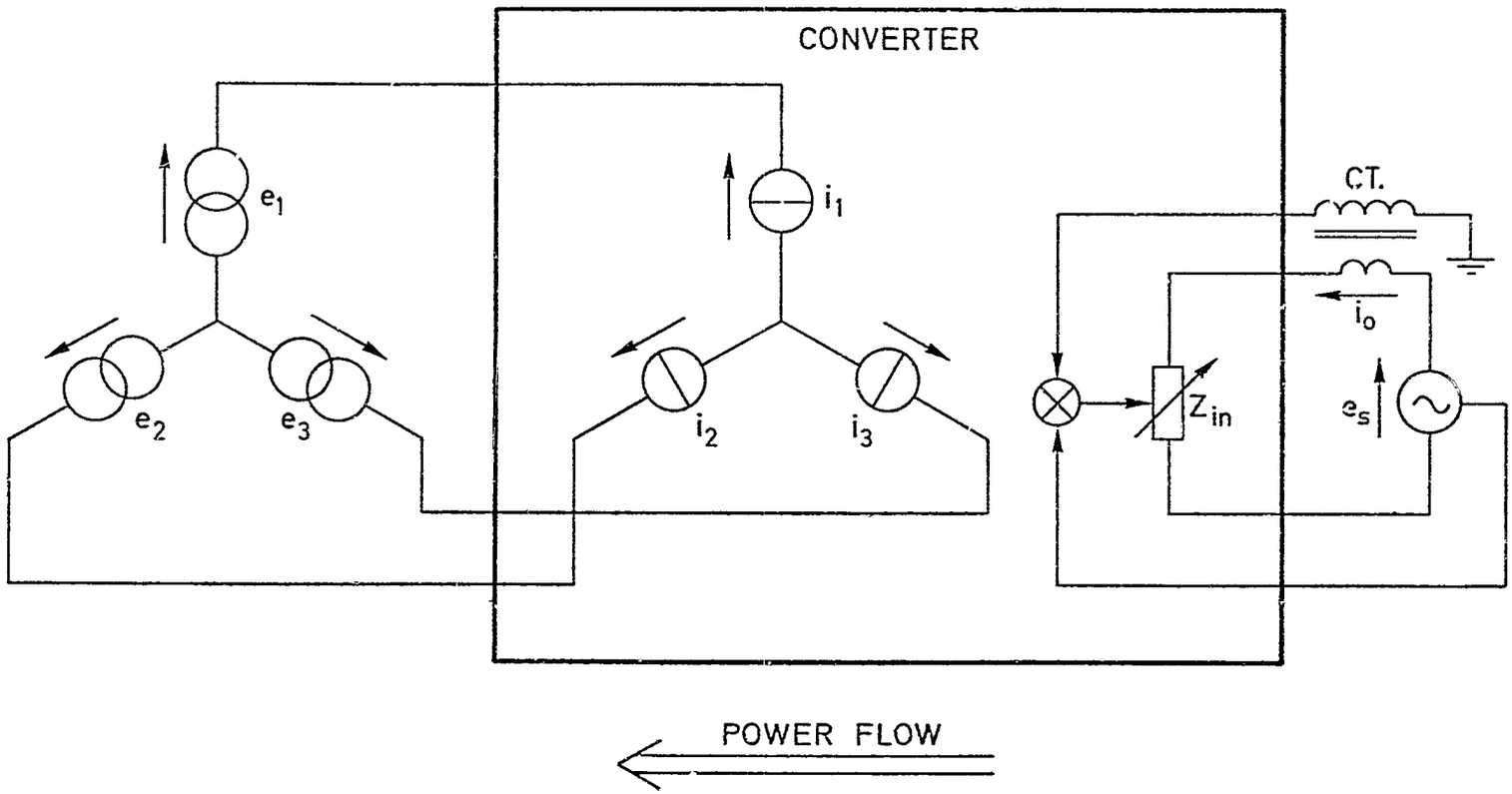


Fig. I - 1.2 Symbolic diagram of a controlled dc to three phase ac inverter with the output characteristics of a current source.

A philosophy for the improvement of technology is outlined in chapter II of this presentation. This is followed by the experimental verification of the critical aspects of the improved technology in chapter III. An assessment of the significant aspects of the newly acquired improvements is presented in chapter IV.

II. CONCEPT FORMULATION

II - 1. Goals of Technology Improvement

Presented is an exploratory first approach to the technical problem of controlled bidirectional four quadrant (BD4Q) power transfer between a polyphase ac and a dc system, using high power freuqency techniques.

Application of higher internal converter frequencies (10 kHz) is meant to improve the reliability of these devices, and to reduce their cost substantially. This improvement of cost is paired with an appreciable reduction of physical weight and size of the equipment.

In essence, it is intended to extend the power capability of space type equipment to the submegawatt range (order of 100 kW) with potential benefits of this technology for terrestrial use, such as for vehicular and stationary applications.

New characteristics of power conversion are sought, including the capability of extraction of ac power from a polyphase line at an arbitrarily determined power factor, independent of line and load conditions. Conversely, the same can be applied for return of electric energy to the polyphase line. This significant and intrinsic property, which has significant economic implications is not found in the state of the art equipment, even if voluminous and expensive filters were to be used.

II - 2. Definition of a Representative System

A system that would embody the technology needed for implementation of the bidirectional four quadrant ac to dc converter, as described in A., part III of the Exhibit "A" of subject contract, is chosen for purpose of this study.

This system should, furthermore, be suited to meet the concerned design requirements of this contract as stated in B. part III of the same Exhibit "A".

A system is studied which:

II - 2.1. derives power from a conventional three phase ac supply line and transfers energy to an electric storage battery;

II - 2.2. can reverse the flow of energy so that electric power is delivered from the storage battery to the three phase supply line;

II - 2.3. embodies the potential to be modified and/or expanded to attain a maximum of the design goals stated in C., part III of the same Exhibit "A".

The above described system is devised to also satisfy the desired characteristics and the functional requirements formulated in part II - 3 of this report.

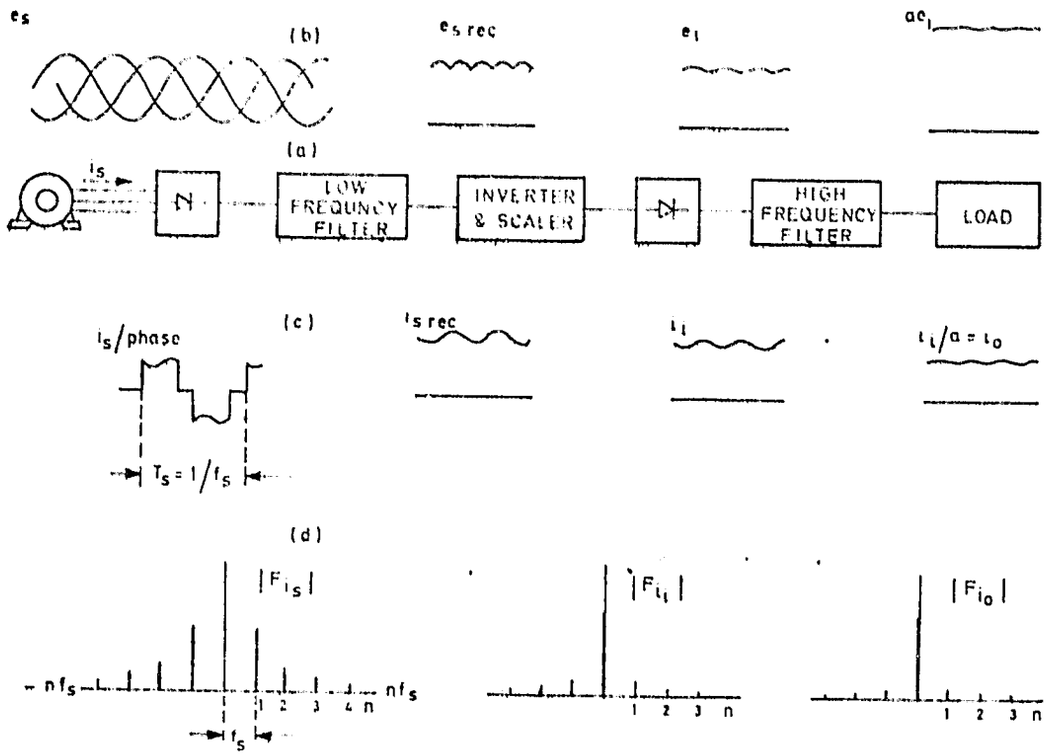


Fig. II - 2.1.

Conventional configuration of a three phase ac to dc converter with unidirectional transfer of electric energy with characteristic wave forms and some of their frequency spectra.

The conventional configuration of a three phase ac to dc converter with unidirectional transfer of electric energy as shown in Fig. II - 2.1. Parts (a) and (b) of this figure are self explanatory. A characteristic current waveform i_s in one of the phases of the ac supply line is shown in part (c) of that figure. The other sections in the same part (c) show the well known waveforms of the current in the various stages of the transformation process. The frequency spectra which pertain to these current waveforms are qualitativly indicated in part (d) of Fig. II - 2.1.

The above described system is limited in its capability to control the power transformation process in order to:

(a) control the rate of charge of the battery according to a preset program or in response to appropriate feedback signals;

(b) shape the frequency spectrum of the currents in the ac feeder lines to desired forms;

(c) control the power factor as viewed from the three phase supply line.

A more sophisticated ac to dc converter system for controlled bidirectional flow of electric energy is shown in Fig. II - 2.2 in the form of a three phase "antiparallel" full wave thyristor bridge. This system and its function is described in the literature |1|.

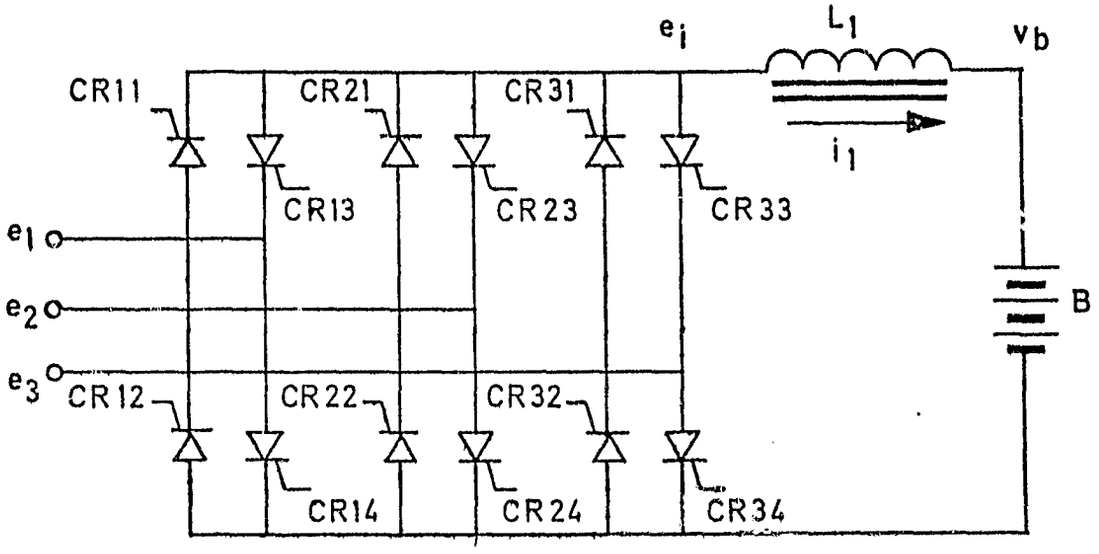


Fig. II - 2.2.

Symbolic schematic of bidirectional three phase ac to dc converter, used as battery charger.

The thyristors are selected to conduct current by the application of trigger signals to their gates. These thyristors are selected in pairs according to (1) the relative polarity of the phase voltages e_1, e_2 and e_3 and (2) the direction of transfer of energy. Thyristors CRi1 and CRi2 (i = 1, 2, 3) can transfer energy from the ac supply line to the battery B. Conversely, will thyristors CRi3 and CRi4 transfer energy from the battery to the ac supply line. Each of these two groups operates in pairs thus connecting the two of the three phases at one time to the battery or vice-versa. If "full" voltage e_i is desired, where $e_{i\,av} = v_b$, then all thyristors of the group CRi1 and CRi2 are fired in such a manner that this group functions as a full wave diode bridge. This is further discussed with reference to Fig. II - 2.3(a). Operation of a diode bridge is

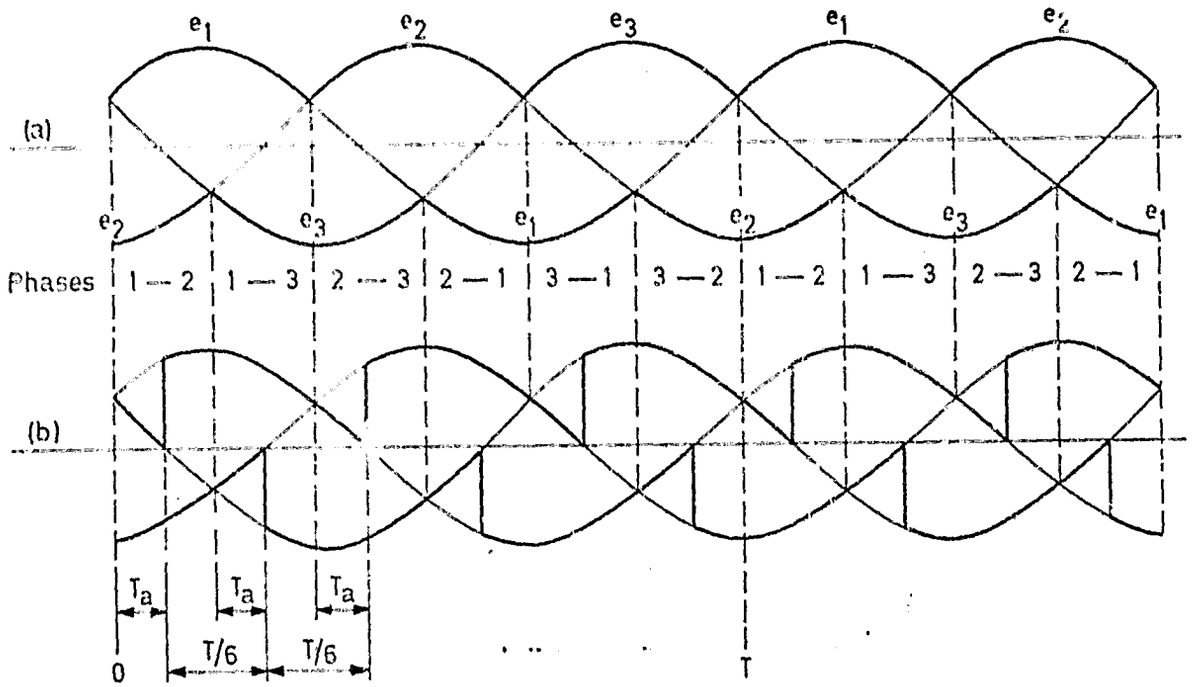


Fig. II - 2.3

Rectified three phase voltage wave form of (a) full wave diode bridge and (b) full wave thyristor bridge, with indication of intervals.

performed if phases with voltage e_1 and e_2 are connected to the battery in the interval marked 1-2; phases with voltage e_1 and e_3 in the interval 1-3, and so on. The respective pairs of thyristors are fired accordingly as discussed with reference to Fig. II - 2.2. The firing signals are provided by a control system which does, at this time, not enter the discussion.

If it is desired to reduce the average value $e_{i\ av}$ of the voltage e_i, then this is accomplished by delay of the firing signals beyond the intervals i-j (i, j = 1, 2, 3; $i \neq j$) as indicated in Fig. II - 2.3(b). For instance thyristor CR32 which should connect phase No. 3 to the charger system is not fired at the end of interval 1-2. Its firing instant is delayed to a point in the interval 1-3.

The average voltage $e_{i\ av(1-2)}$ in this interval

$$e_{i\ av(1-2)T_a} = \frac{6}{T} \int_{T_a}^{T/6+T_a} (e_1 - e_2)dt \qquad (2.1)$$

with

T = the period of one cycle of one phase of the ac wave in the three phase supply line;

T_a = the delay introduced for the firing of thyristors CR11 and CR24 after the start of the interval 1-2 and of CR32 after its termination.

Evidently is $e_{i\ av(1-3)T_a}$ a maximum when $T_a = 0$ and decreases with increasing T_a. It is envisioned that firing of all thyristors in the "line of firing" is delayed by the same delay time T_a so that the length of the individual intervals in which two thyristors conduct remains the same, namely T/6, yet all of these intervals are shifted by a delay T_a to the right compared to the corresponding intervals shown in figure 2.3.

The average voltage $e_{i\ av(1-3)T_a}$ is, eventually, reduced to zero, even though the instantanuous values of $e_i \neq 0$, except at isolated

points. This is described in great detail in the literature [1]. Control of the average output voltage $e_{i\ av}$ is thus attained as a function of the above discussed delay T_a of firing instants.

The price for the described process of control is the tolerance of more or less serious deviations of the waveforms of the currents in the individual phases of the supply line from sinusoidal shapes. These deviations give cause to the generation of higher harmonic components and poor power factors in the ac supply line which in turn cause unproductive heating of the supply line and the thereto connected generators [1]. This is a feature which is still being tolerated by the utility companies because of (1) the relative rarity of connected power electronics equipment of appreciable single or cumulative size and (2) the lack of low cost wider band wattmeters and power factor meters to record the actual effort of the supplier of electric energy in order to provide the average power to the battery in its various stages of charging.

The above referred to adverse effects on the supply line can be mitigated, or avoided by having the thyristor bridge shown in Fig. II - 2.2. preceded by an ac filter which (1) reduces the higher harmonic content in the phase currents and (2) corrects the power factor. As a corollary it is necessary that the inductor L_1 be sufficiently large as to smoothe the current i_1 in order that the battery would not be, unnecessarily heated by its harmonic content. It is thus necessary to mitigate the distortion of the current waveform

introduced on both sides of the thyristor bridge by its inherent process of operation. The above referred to price is thus translated into appreciable bulk and cost of filters.

Another disadvantage of the described process is the limited speed of response of the system to an externally given or internally generated command. This limited speed of response is rooted in (1) the minimum switching intervals T/6 or approximately 2.74 msec in a 60 Hz supply line and (2) even more so, the needed heavy filters, referred to above, with time constants far in excess of T/6. This limitation in the speed of response may not be a matter of concern for a battery charger. It becomes, however, a problem when the direction of transfer of energy is reversed.

In the case of dc to ac inversion it is necessary that the flow of current into the individual phases is guided by the momentarily present conditions of voltage and current in these phases so that (1) the power factor in the line can be matched, or even corrected, (2) a minimum of harmonic distortion enter the line and (3) unexpected time varying conditions can be met, such as transient phenomena. Concurrent meeting of the above enumerated requirements cannot be achieved by use of a preprogrammed system. A system is required that adjusts its transfer characteristic almost from instant to instant as to taylor its output to the momentary line conditions. This cannot be achieved by use of a low frequency system which is burdened, furthermore, with heavy filters. The term "low frequency" is used here in the sense that the shortest time intervals for realignement

of the system are not substantially shorter, but are in fact the same as the time intervals during which the current should be tailored, thus reducing the intended task to an impossibility.

The above described problem area concerning the power factor and the harmonic distortion of current by thyristor bridges has its roots in the abrupt switching action of the electronic devices, compounded by thrifty use of materials in filters. This is explained with reference to Fig. 11 - 7a,b. The nth phase which feeds a three

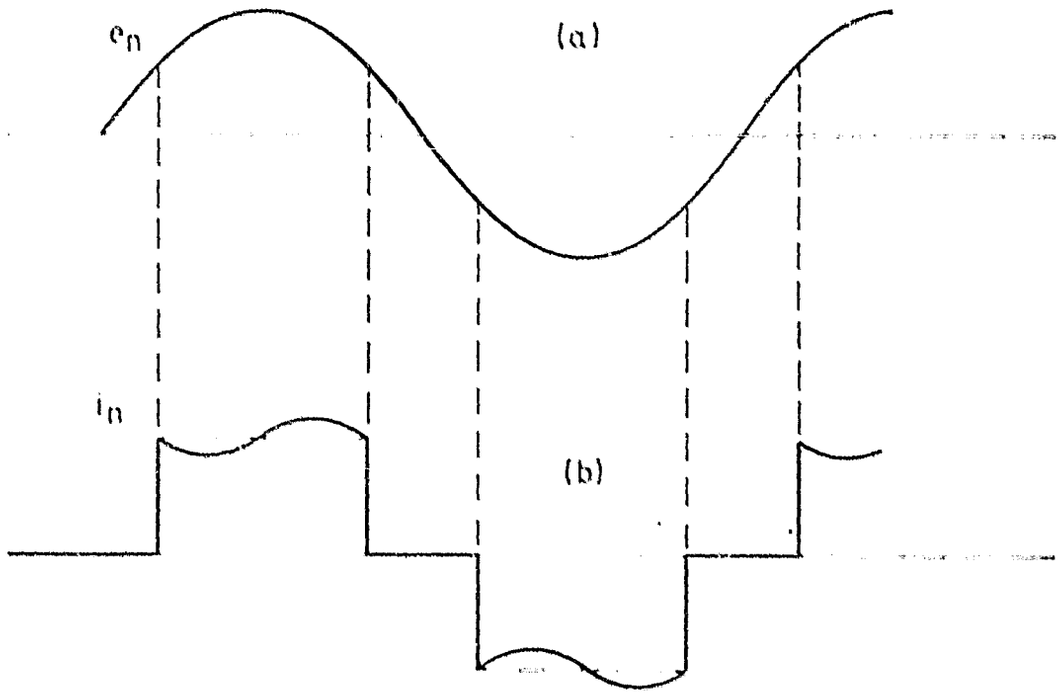


Fig. 11 - 7a,b.

Waveform of (a) voltage e_n (n = 1, 2, 3) and (b) typical current i_n in one of the phases of the three phase supply line for a full wave bridge rectifier-filter.

phase rectifier-filter bridge "cuts in" at an angle $\pi/6$ after $e_n = 0$ and $de_n/dt > 0$, when its voltage exceeds that of the formerly conducting other phase. Current i_n which was zero at that instant rises to a level prescribed by current i_l in the inductor L_l. The shape of the top of the shown current pulse depends on the size of L_l and the degree of loading of the system. The most favorable shape is that of a horizontal top which is indicated by a broken line. This condition occurs when $L_l \to \infty$. Current i_n terminates at the angle $5\pi/6$ when another phase "cuts in" and assumes conduction of the current i_l.

The power factor p.f. in each of the three phases is given by

$$\text{p.f.} = \frac{\frac{1}{T}\int_0^T e_n i_n \, dt}{e_{n\ \text{rms}}\ i_{n\ \text{rms}}} \qquad (2.2)$$

when defined in the time domain |2|. This power factor is approximately .955 when $L_l \to \infty$; it decreases when L_l is reduced to manageable sizes and deteriorates rapidly with decreasing $e_{i\ av}$ as explained before.

This deterioration of the power factor is caused by:

(1) the shift of the intervals of current conduction i-j to the right with respect to the voltage sine wave, as explained before;

(2) the increasing "distortion" of the waveform of i_n, whose individual pulses, eventually, reach into the range of opposite polarity with respect to e_n. The transfer of energy to the filter-load network ceases eventually since the numerator in question (1.2) becomes zero. The power factor is then reduced to zero.

This deterioration is compounded by the effects that are caused by the limited size of inductor L_1.

An analogous argument can be made for the reversal of flow of energy, namely from the battery to the three phase line. Here the process of power transfer is also controlled by the firing angles of the thyristors. Yet, the whole process is at the mercy of ac line conditions, the battery voltage, and the desired magnitude of power transfer. There is no degree of freedom left in the system to taylor the harmonic content of the i_n, which flow now in the reverse direction, and/or to control the contribution of this power transfer to the power factor in the line.

The above described adverse effects on power factor and harmonic content of the current manifest themselves in the form of heat which does not contribute to the transfer and transformation of power.

A suppression of the described effects by use of heavy low frequency filters is possible. The use of filter elements which can store appreciable quantities of electric energy creates the hazard

of unexpectedly high current peaks under dynamic conditions of system operation. These current peaks are difficult to control, to say the least; they can imperil the structural integrity of the thyristors.

The representative system which was defined at the outset of this part of the report should provide substantial improvements and alleviate the problems which exist in the state of the art, as discussed above.

II - 3. Formulation of Needed System Concept

II - 3.1. Desired Characteristics

It is intended to improve the technology of the class of electric converters, which comprises the representative system described in II-2. The power range of interest is in the order of 100 kW. Yet, it is intended to clear the way for an expansion of the power level of these converters toward the megawatt range.

The needed system characteristics should include improvements in order to increase the:

a. power density of converter equipment, expressed in kW/kg;

b. reliability of this equipment by (1) confining the absolute instantanuous and transient stresses on critical components, such as semiconductor switching devices to unconditionally predictible limits, even under the most adverse operating conditions and (2) to minimize the ratio of steady state peak vs. average stresses in the same critical components;

c. efficiency of power conversion by (1) containment of the current form factors $\rho_i = i_{1\ rms}/i_{o\ rms}$ where i_1 is the significant internal converter current and i_o the output current(s) and (2) minimization of power losses in the switching devices by appropriate tayloring of their functions within circuits which are devised to lessen the stress on these devices, also indicated under b.;

d. dynamic characteristics of these converters, with particular emphasis on reaction speed to externally imposed changing conditions or to applied control signals;

e. cost effectivness by (1) sparse use of raw materials such as iron and copper causing (1a) lowering of raw material cost, (1b) cost of handling of materials and equipment during manufacturing, transportation, installation and maintenance work, (2) lower frequency of maintenance due to improved reliability and (3) lowering the losses of energy in the equipment, due to improved efficiency, as stated under c.

II - 3.2. Functional Aspects

A number of functional aspects of converter operation will have to be satisfied on the way in order that the converter acquire the desired characteristics, stated in II - 3.1 above. These functional aspects will be treated in a way that holds the promise for an expansion of the resulting technology to a multitude of electric power transformation processes, This is meant to be, in particular, consistent with the Specifications contained in part III of Exhibit "A" for bidirectional three phase ac to dc conversion.

The functional aspects of the class of converters under considerations which appear to be needed for a materialization of the above listed desirable characteristics require basic functional concepts to;

a. derive power from a source of three phase ac power with a power factor in excess of 0.85 for all conditions of loading;

b. confine the power derived as stated under a. at any instant to the first and the third quadrants of the V_{AC} - I_{AC} plane only;

c. cause a minimum pollution (current distortion) in the ac feeder lines;

d. supply regulated dc voltage or current with deviations of no

more than 1 % from a nominal value to a dc load, such as a battery operating in the first quadrant of the V_{DC} - I_{DC} plane only;

e. derive power from a source of dc energy via the same terminals through which power was supplied as stated under c. with a dc power factor of no less than 0.85 in accordance with equation (2.2) and operating in the second quadrant of the V_{DC} - I_{DC} plane;

f. supply power emanating from the dc source stated under e. into a three phase ac line, causing a minimum network pollution in doing so; perform that supply of electric power, preferrably, in the second and the fourth quadrants of the V_{AC} - I_{AC} plane;

g. provide galvanic isolation between the input and the output terminals of the converters, as viewed from both directions of transfer of energy;

h. endure progressive overloads and external fault conditions including shorted output terminals without damage to the converter;

i. be capable of power flow directional changes within no more than 1.0 milliseconds and to apply measures for the stabilization of external conditions within the same time interval.

Efforts were made to incorporate the above enumerated functional aspects in the converter concept which is described in the following part II - 4.

II - 3.3. Philosophy of Functional Concept

In order that the system characteristics stated in II - 3.1 and the therewith associated functional aspects stated in II - 3.2 be achieved it appears necessary to introduce the following functional properties. Planned is a converter device which:

(a) extracts electric energy in pulsating form at a kHz rate directly from the three phase ac line without interposition of a low frequency - 360 Hz - filter;

(b) functions as a nondissipative active filter in order to:

(b1) perform the spectral transformation indicated in figure II - 2.1(d);

(b2) scale and stabilize the system output (load) voltage v_o;

(c) has a high degree of reliability, demonstrated by its inherent short circuit capability;

(d) has a high energy density (kW/kg), or conversly, has a light weight due to the complete absence of low frequency (up to several hundred Hertz) components, because of its high internal

frequency of operation in excess of 10 kHz;

(e) generates little heat because of its inherent efficiency;

The following advantages are expected:

II - 3.4. Expected Benefits

(a) an adaptation of the waveshaping processes to the requirements of generator and load which is presently not possible in efficient light weight equipment;

(b) ultra light weight of equipment due to:

(b1) elimination of all low frequency components between generator and load, including the elimination of entire (heavy) functional blocks;

(b2) use of high internal frequencies of operation in excess of 10 kHz.

II - 4. Functional Concepts for the Planned System

II - 4.1. General System Concept

A system that appears capable to embody the properties described

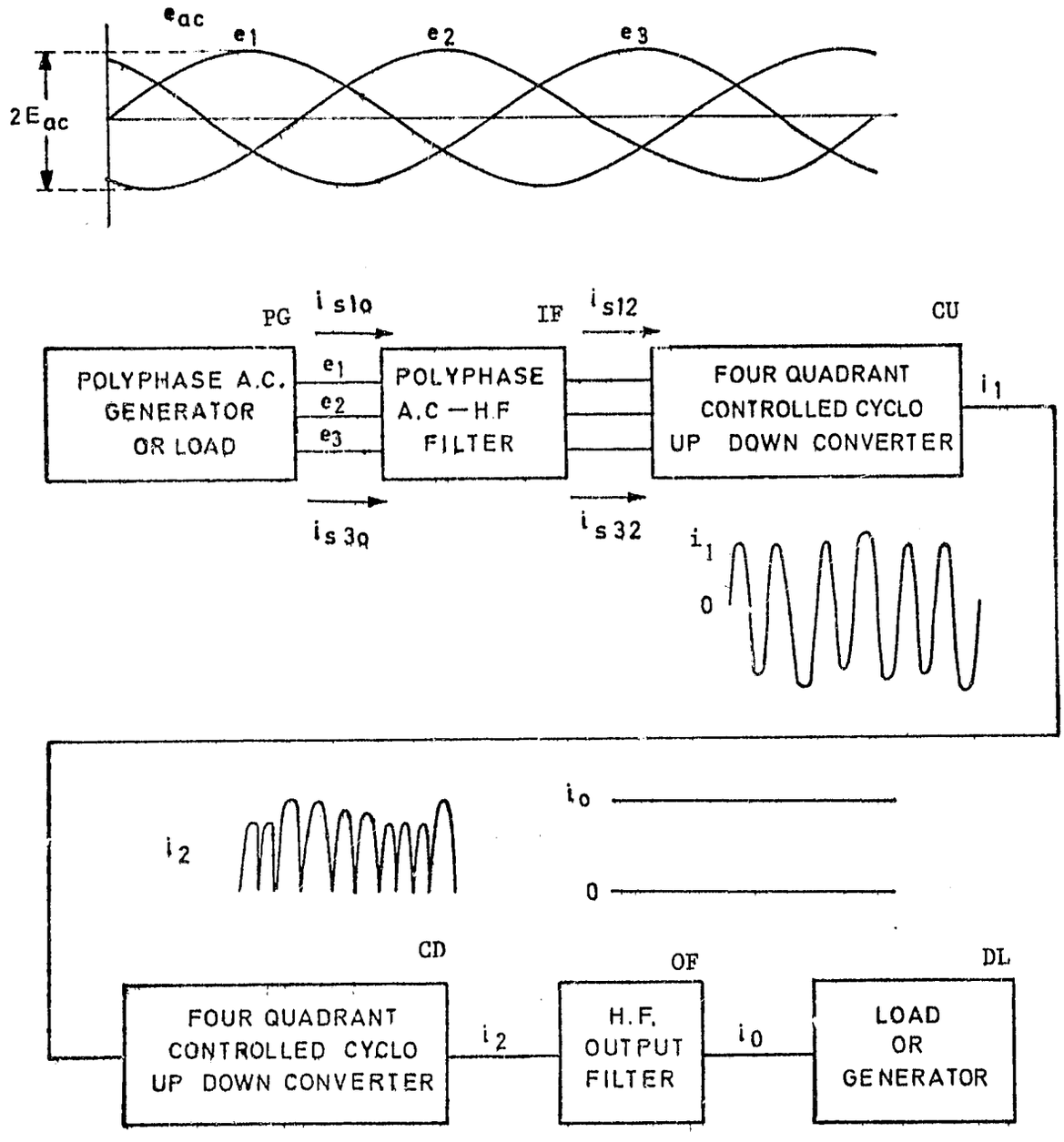


Fig. II - 4.1.

Symbolic block diagram of bidirectional, four quadrant three phase ac to dc converter using a modulated high frequency carrier link.

in the preceding part II - 3 of this report, is now described with reference to Fig. II - 4.1. The three phase supply line (PG) is connected via a high frequency low pass filter (IF) to the input stage of the power converter in the form of a four quadrant controlled "cyclo up" converter.

This cyclo up converter extracts energy from the supply line which is used to generate a high frequency (10 kHz) single phase modulated carrier oscillation with current i_1. The above described transformation process occurs in a nondissipative way with use of a thyristor matrix which will be described further on. The carrier waveform i_1 is both frequency and amplitude modulated to mitigate its own harmonic content with a fundamental 360 Hz frequency, or to accomodate the low frequency spectrum desired in the supply line, or for any other intended purpose, such as power factor correction.

The low frequency content of the above described carrier is then "detected" through rectification by way of a four quadrant controlled cyclo down converter (CD) and by subsequent filtering by a high frequency low pass filter (OF) with a cut off frequency below the lowest frequency of the carrier oscillations.

All operations are being carried out in a nominally nondissipative fashion by use of matrixes of "on-off" thyristor switches supported by filters and other circuits which contain solely reactive elements.

The philosophy for the generation of a modulated high frequency

carrier for purpose of the spectral transformation of the source signal as it appears to the cyclo-converter process is treated in the literature [3, 4, 5, 6].

The two four quadrant controlled cyclo up down converters are equipped for equivalent bidirectional operation. It means that each of these converters can generate a modulated carrier in the above referred to sense, when viewed from one set of its ports and can selectivly demodulate a modulated carrier when viewed from the other set of ports.

Based on this bidirectional characteristic of these cycloconverters it is possible to reverse the above described flow of energy. A source of electric energy (DL) in form of a battery can energize the four quadrant controlled cyclo up converter (CD) via the (high frequency) low pass filter (OF). A modulated carrier with current i_1 is generated, which is demodulated by the four quadrant cyclo down converter. The outcome of this demodulation process is distributed in sequence to selected pairs of the three phase line. The electric dc energy emanating from the battery is thus transferred to the ac line.

During the above described dc to three phase ac inversion process it could be advantageous to modulate the carrier with current i_1 in order to (1) convey current with a desired low frequency harmonic content to the individual phases of the polyphase supply line, and

(2) to determine the power factor for this transfer. This is further discussed with reference to Fig. II - 4.2. Illustrated is

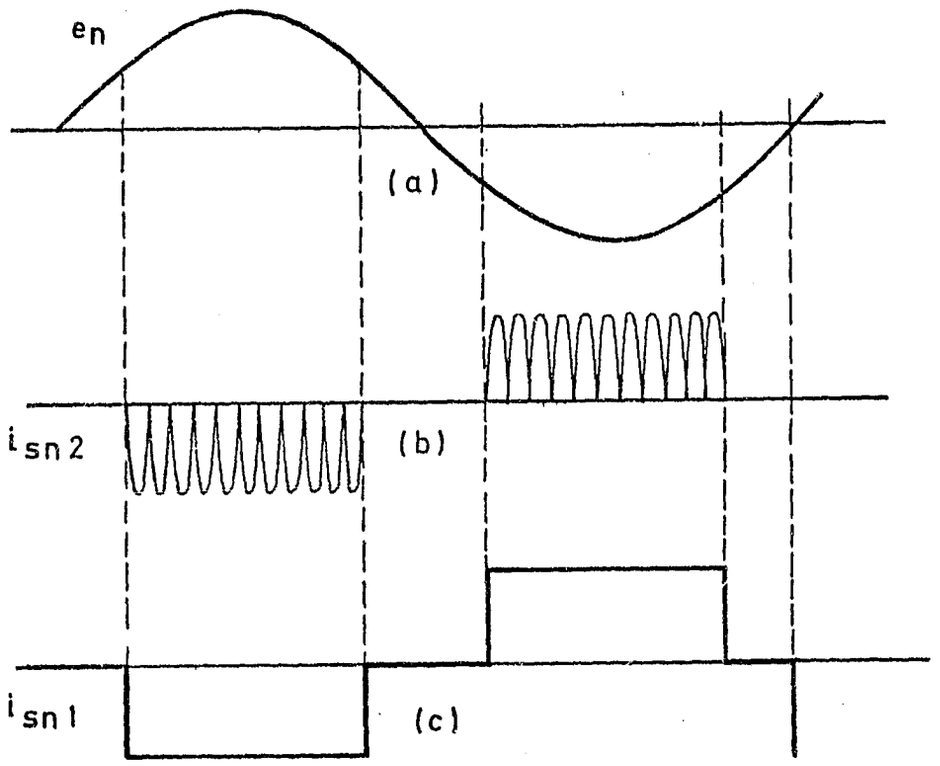


Fig. II - 4.2.

Phase (a) voltage e_n, (b) demodulated carrier current i_{sn2} and (c) filtered current i_{sn1}, during transfer of electric energy to the polyphase line.

the case in which the carrier is not modulated. The "detected" current i_{sn2} consists of a succession of uniform pulses which are distributed to the individual phases in such a way, that their smoothed form i_{sn1} is the replica of the phase currents in a three

phase supply line which feeds a full wave rectifier diode bridge, followed by an infinitely large inductor.

The just described mode of operation could be desirable in many cases. Yet, there are three degrees of freedom inherent in this process.

(a) The time interval T_a introduced with reference to Fig. II-2.4 with a minimum value of $T_a = 0$ can be enlarged or reduced at will. It means that the current blocks shown in Fig. II-4.2(c) can be shifted, arbitrarily, with respect to the voltage sine wave for any polarity. Shifting of these blocks in time does not have an effect on the harmonic content of the current, but provides control on the power factor with which the electric energy is transferred to the polyphase line.

(b) The uniform amplitude of the current blocks i_{snl} can be controlled by adjusting amplitude and frequency of i_l in a way that a specific amount of charge per second is processed by the detector.

(c) The shape of each of the blocks of the current i_{snl} can be taylored by appropriate modulation of the carrier.

The advantage of these properties of the presented system is that the waveform of the current i_{snl} can be taylored at will to control.

(a1) the power factor with which energy is transferred to the polyphase network;

(b1) the magnitude of the current i_{sn1}, and

(c1) the power factor correction in the polyphase line which can be achieved by the combined carrier modulation and current pulse shifting process explained under (a) above.

The preceding argument concerning the transfer of electric energy can be equally applied for the case of "forward" transfer of energy. Control of the average current is attained by adjustment of the average value of each half cycle of the carrier current i_1. The individual phases carry then the current $-i_{sn1}$ shown in Fig. II-4.2 or the flat top pulses (broken top line) in Fig. II-2.4. These phases "see" thus an imaginary inductor behind the full wave rectifier bridge. This effect is accomplished by appropriate control of the carrier with current i_1. The freedom to shift the current pulses with respect to the voltage sine wave and to taylor its tops is retained, if so desired, in order to meet specific supply line conditions, such as to improve the power factor in the line concurrent with the charging process.

The advantages of the here described system over the state of the art in form of the "antiparallel" thyristor bridge are rooted in the facts that: (1) the phase currents can be initiated and terminated

at will at any instant of time and (2) form and harmonic content of these phase currents can be deterministically taylored by an active filtering process. A minimum of passive component effort is required because of the relativly high frequencies, involved in this process.

The approach for the implementation of the above described system concepts is presented in the following.

II - 4.2. The Bidirectional Series Capacitor Inverter Converter

A power circuit which can embody the properties, presented in the preceding section is now discussed with reference to Fig. II-4.3. The thyristor bridge in block CU is fed from a three phase supply line (PG). The just described configuration is identical with the thyristor bridge shown in Fig. II-2.2. This thyristor bridge is connected to the primary winding of a transformer XF, the inductor L_1 and capacitor C_1, all named elements being arranged in series. The secondary winding of the transformer is connected via another series resonant circuit L_2C_2 and another thyristor bridge (CO) to the load Z_L which is parallelled by the filter capacitor C_c (OF). The secondary circuit can be thought of as being reflected via the transformer back into the primary circuit whereby L_1C_1 and L_2C_2 are thought of as being embodied in one LC_1 combination.

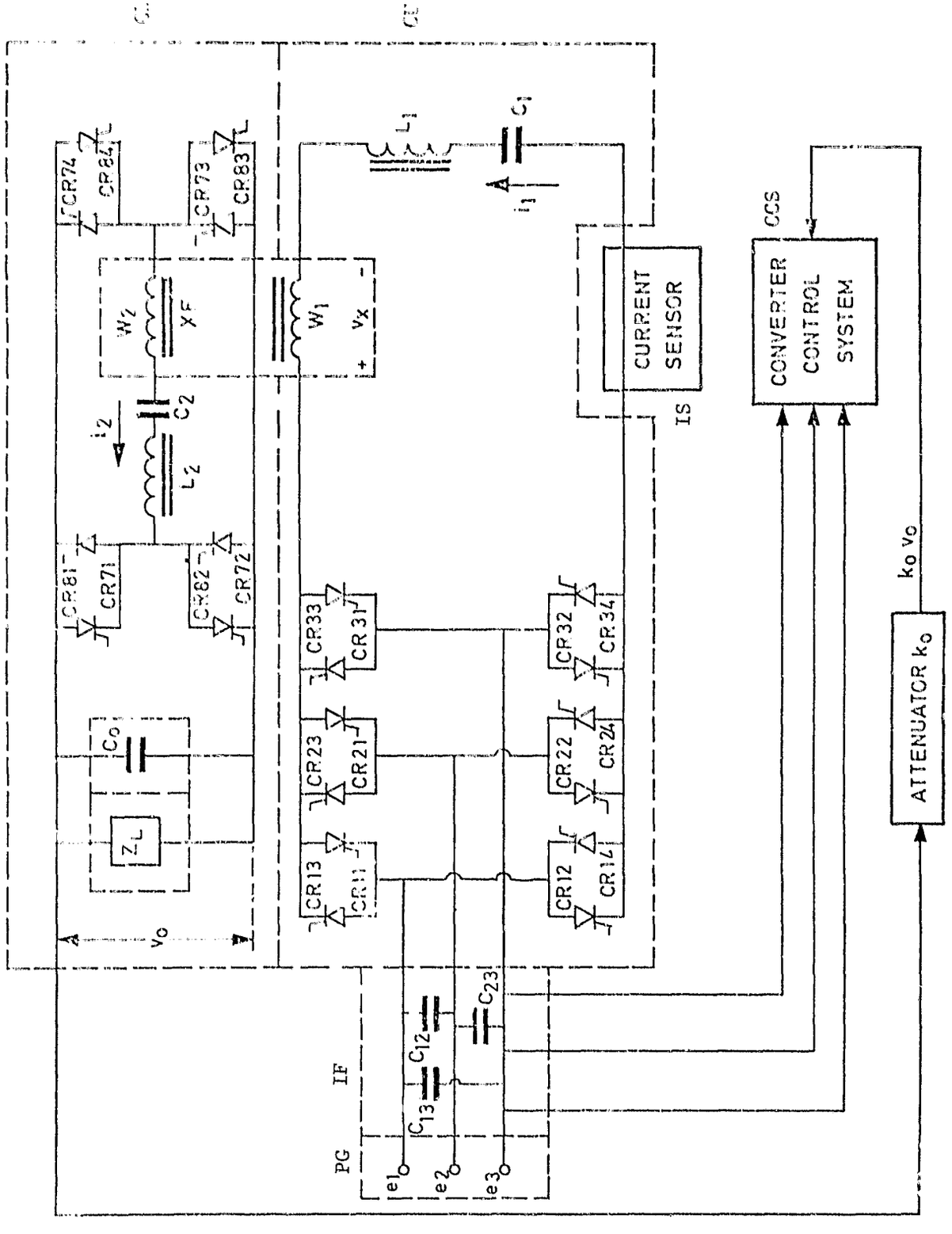


Fig. 11 - 4.3.

Symbolic schematic of bidirectional four quadrant series capacitor inverter-converter.

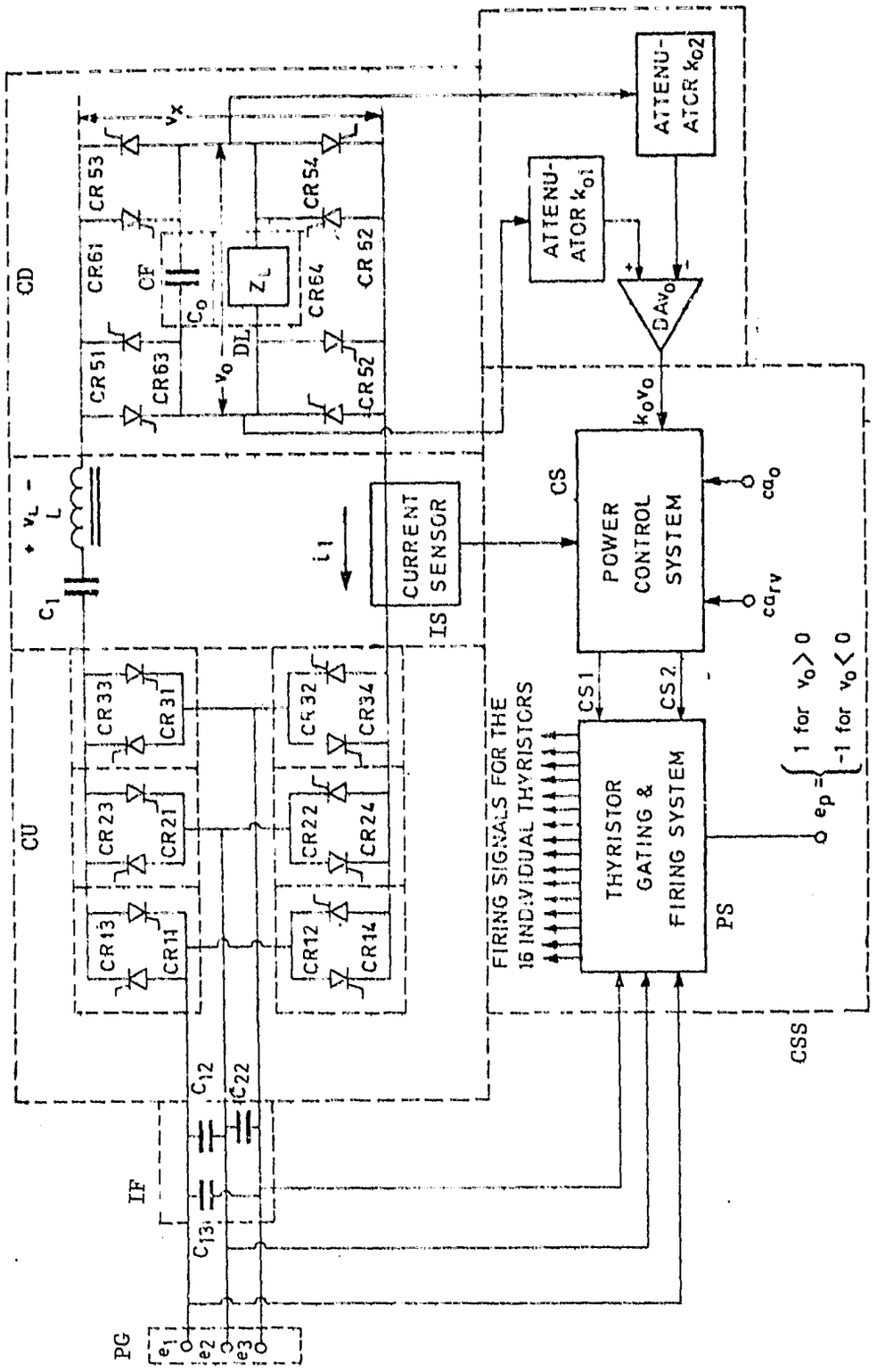


Fig. II - 4.4.

Equivalent circuit of the symbolic schematic of the bidirectional series capacitor inverter-converter shown in Fig. II - 4.3.

The resulting equivalent circuit is shown in Fig. II-4.4. The further discussion is continued with reference to this figure for purpose of simplicity of presentation. Yet; the circuit shown in Fig. II - 4.3 is meant to be used for the intended purpose.

Two phases of the supply line (PG) are, at a given time, connected via two thyristors of bridge CU the series resonant LC_1 link and two thyristors of bridge CD to the load (DL) which is shunted by the filter capacitor C_o(OF). All concerned four thyristors will conduct in the discontinuous current mode for one half period of the resonant frequency

$$f_i = 1/2\pi\sqrt{LC_1} = 1/2T_o \qquad (4.1)$$

where

T_o = the half period of the resonant circuit.

All four thyristors will open at the termination of this half cycle because current i_1 reverses its direction of flow. It is this process of natural commutation which allows termination of current in any of the supply lines at any time. The expression "any time" is, of course, meant in the sense that

$$T_o << T/6 \qquad (4.2)$$

It is assumed that the four thyristors in question were the thyristors CR11, CR51, CR54 and CR24. It means that we operate in the interval 1-2, as discussed with reference to Fig.II - 2.3 so that $e_1 > e_2 < e_3$. Inequality (4.2) implies that the phase voltages e_1 and e_2, actually, stand almost "still" in time. If we ignore at this time the moderate variations of $e_1 - e_2$ within the interval 1-2, as referred to before, then the functional philosophy of a dc converter of the described class applies [6, 7]. The resonant current i_1 reverses direction when thyristors CR13, CR53, CR52 and CR22 are triggered into conduction. Thyristors CR13 and CR22 now assume the function of the "antiparallel" diodes D11 and D12 shown in the half bridge configuration of this class of dc converters. The just referred to circuit is reproduced here for convenience. All voltage and current waveforms in the LC_1 circuit are analogous to those explained for the circuit shown in Fig. II - 4.5.

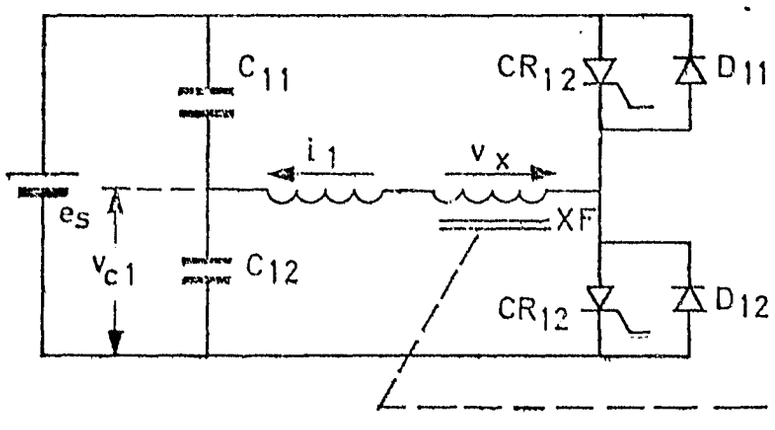


Fig. II - 4.5.

Symbolic schematic of the primary circuit of a series capacitor inverter-converter in half bridge configuration.

The respective waveforms are reproduced for convenience in Fig. II - 4.6. The role of the various capacitors is now explained. Capacitor C_1 in Fig. II-4.4 assumes the function of both capacitors C11 and C12 in Fig. II-4.5. Capacitor C_0 performs the function of the (high frequency) low pass filter (OF), explained with reference to Fig. II - 4.1. Capacitors C12, C13 and C23 perform the function of the (high frequency) low pass filter (IF) explained with reference to the same figure.

One can view the presented system in each time interval i-j, referred to before, as a converter fed from a dc source with a moderate voltage ripple. The effects of this ripple are being removed by a control system which embodies an advanced version of the analog signal to discrete time interval converter (ASDTIC) [3, 4, 5, 6].

The "forward" operation of the system thus consists of a succession of time intervals i-j during which it selects two of the three phases with the most appropriate voltage difference in order to perform the customary operation of a dc converter of this class.

A number of simplifications was introduced in the preceding explanation for purpose of simplicity of presentation. The complexity which is needed for purpose of a three phase ac to dc operation or its inverse will be gradually indicated as the explanation of the system progresses.

The process of transfer of energy from the battery to the three phase line is analogous to the above described "forward" transfer. In this

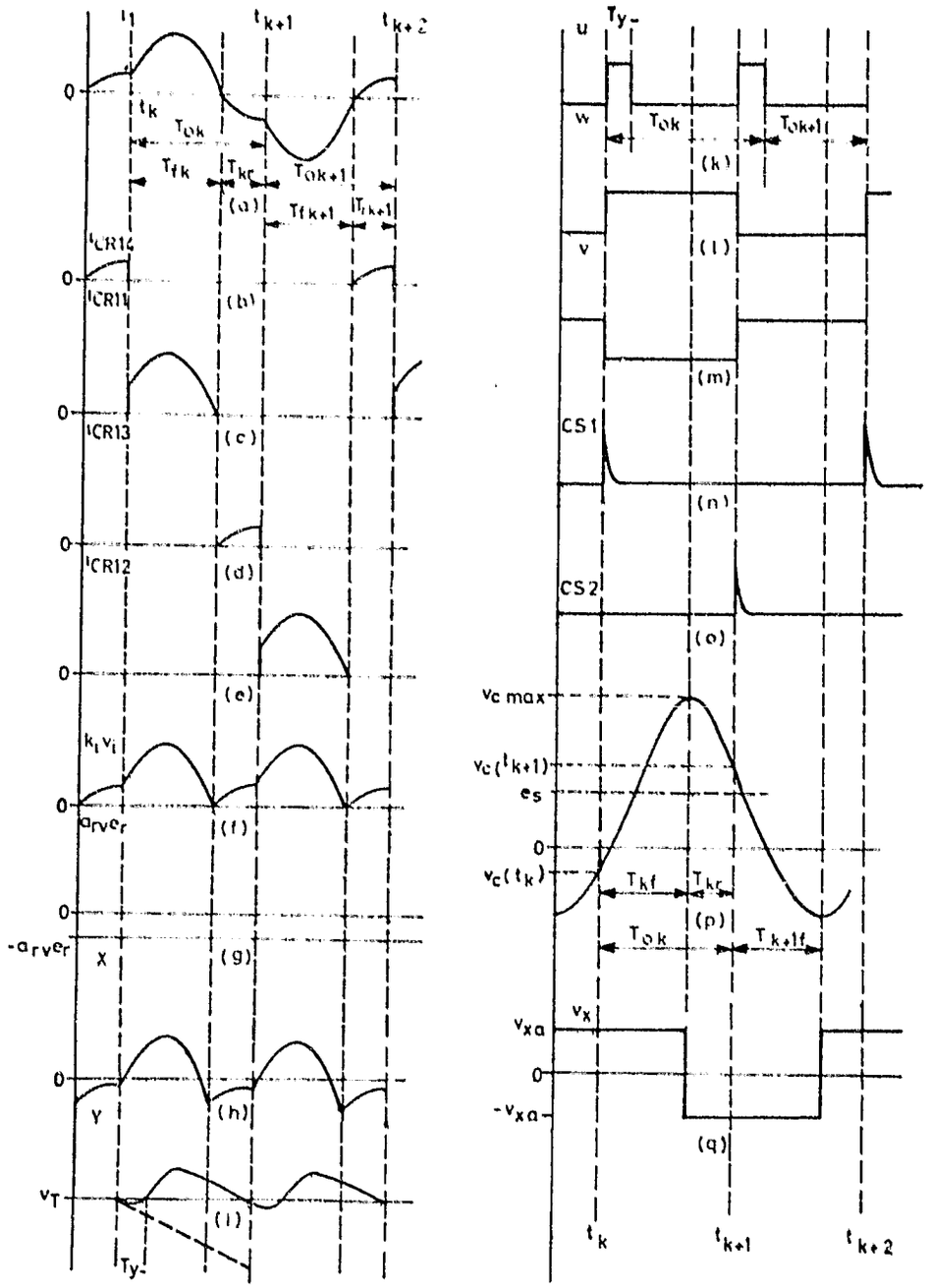


Fig. II - 4.6.

Significant voltage and current waveforms in the series capacitor converter.

case it is assumed that the battery voltage $e_b = v_o$, the voltage over the load Z_L shown in Fig. II-4.4, since the battery replaces this load. The thyristor bridge (CD) associated with Z_L becomes now the input of a full bridge series capacitor inverter-converter, whose functional properties are analogous with those of its half bridge version [6]. There are, again, four thyristors in conduction at any time; two thyristors of the "battery bridge" (CD) and two thyristors of the dc/ac bridge (CU), so that the battery is connected during each of the carrier frequency cycles to two selected phases of the three phase power line. Assume that thyristors CR62, CR63, CR13 and CR22 are in conduction in the time interval 1-2. One high frequency current pulse is then generated which enters the phase pair with voltage e_1 and e_2. This pulse can be one of the pulses shown in Fig. II - 4.2 with a polarity which is the opposite of that of the thereto pertaining phase voltage, because of the direction of power flow. When the resonant current has run its course, then thyristors CR11, CR51, CR54 and CR24 are fired in order to back bias the formerly conducting thyristors for an interval

$$T_{kr} \geq t_{off} \tag{4.3}$$

where

t_{off} = the turn off time of the thyristors.

This is also expressed in radians as

$$\psi_r \leq \psi_{r\ min} \tag{4.4}$$

where

$$\psi_{r\ min} = \omega_o T_{kr\ min}$$

Thyristors CR61, CR64, CR14 and CR21 are then fired after elapse of the interval T_{kr} which is also determined by the control system. The battery feeds again charge in form of one current pulse into the phases with voltage e_1 and e_2.

The described process goes on with the assumption that, again, time stands "still", that is, the voltage difference e_1-e_2 changes only moderately within the time interval 1-2. Clearly, the thyristor bridges CU and CD have changed roles. Bridge CU is now the input bridge and CU the output bridge. Instead of a source voltage ripple we have now a load voltage ripple to contend with. Selection of the phase pair is made according to the relative polarities of e_1, e_2, and e_3 which results in a succession of intervals 1-2, 1-3, etc. in which energy is transferred to the respective phases.

The pulse pattern is governed by the same ASDTIC type control system as discussed before with the three degrees of freedom which were previously enumerated in order to satisfy requirements on the harmonic content of phase currents and the power factor of

energy transfer into the polyphase line.

If one looks back on the sequence in which the thyristors of the first phase CR1i (i = 1, 2, 3, 4) operate, then it becomes obvious that, for instance, thyristors CR11 and CR13 change roles depending upon in which direction energy is being transferred. That is, thyristor CR11 carries the main pulse and thyristor CR13 acts as the back biasing "diode" when energy is being transferred from the polyphase line to the battery. Conversely, thyristor CR13 carries the main pulse and thyristor CR11 acts as the back biasing "diode" when energy is being transferred from the battery to the polyphase line. This is further explained with reference to Table II-4.1. The sequence (S) of thyristor conduction during "forward"

Table II - 4.1.

Sequence (S) of conduction of thyristors CRij in the bridge CU during the time interval 1-2 for "forward" (FWD) and "reverse" (REV) transfer of energy, including requesite back bias (BB) conditions.

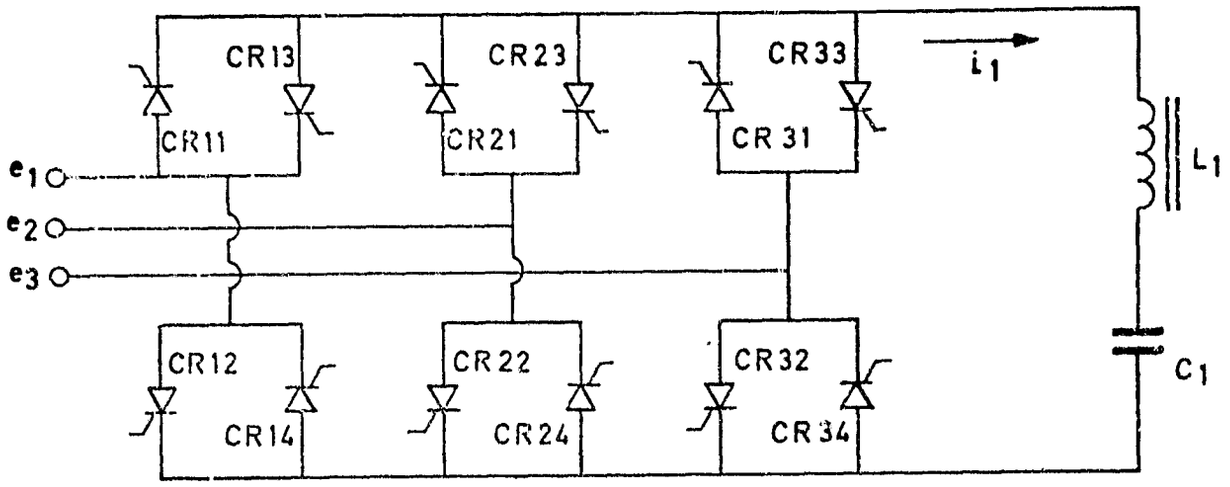
	FWD		CR's		REV	
i_1	S	BB	ij		BB	S
>0	1		11	24		2
<0	2		13	22		1
<0	3		12	23		4
>	4		14	21		3

(FWD) and "reverse" (REV) transmission of energy through the first two "legs" of the bidirectional cycloconverter CU is more detailed indicated. Curved arrows point, furthermore, to the individual pairs of thyristors which are fired once an adequate back bias is ascertained for the thyristor pairs from which these arrows emanate. It appears easy to expand Table II-4.1 to cover all conditions of thyristor conduction in the time intervals i-j to supplement the table shown in Fig. II - 4.7.

The automatic and unfailing mechanization of the therewith associated back bias detection, interpretation and protection against untimely firing of thyristors is one of the important, if not the most important technical feature of this system; it is requesite to its successful materialization.

A summary for the selection of thyristors as function of the phase voltages, the thereto pertaining time interval i-j and of the direction of flow of current i_1 is given in the lower part of Fig. II - 4.7.

The upper part of the same figure shows the thyristor bridge CU connected to a closed resonant LC_1 circuit with current i_1 for purpose of identification of the respective switching elements. The abbreviation FWD is used for "forward" and REV for "reverse" transmission of electric energy.



PHASE VOLTAGES OPERATING PHASES			$e_1 > e_2$ 1 – 2	$e_1 > e_3$ 1 – 3	$e_2 > e_3$ 2 – 3	$e_2 > e_1$ 2 – 1	$e_3 > e_1$ 3 – 1	$e_3 > e_2$ 3 – 2
THYRISTOR PAIRS CR	$i_1 > 0$	FWD	11, 24	11, 34	21, 34	21, 14	31, 14	31, 24
		REV	14, 21	14, 31	24, 31	24, 11	34, 11	34, 21
	$i_1 < 0$	FWD	13, 22	13, 32	23, 32	23, 12	33, 12	33, 22
		REV	12, 23	12, 33	22, 33	22, 13	32 13	32, 23

Fig. II - 4.7.

Antiparallel thyristor bridge and series resonant circuit with identification matrix of thyristor firing selections.

II - 4.3. Assessment of Significant Physical Features.

The two most important features of the presented system are (1) the natural current commutation of the thyristors by virtue of the series resonant LC_1 circuit and (2) the complete absence of power frequency low pass filters. The first feature allows efficient thyristor operation at frequencies near 10 kHz; the second makes it possible to use capacitors, exclusivly, for purpose of filtering current pulse trains at 10 and 20 kHz.

The functional aspects of the "output" capacitor C_o are discussed and explained in the literature [6, 7]. The "input" capacitors C12, C13 and C23 appear here in a new light. Their primary purpose is to close the resonant circuit and to shield the polyphase line from the effects of its high frequency operation. These capacitors carry at the same time a low frequency current which is caused by the voltage difference between each of the two lines of the three phase system. The ratio of admittances for the low frequency signal Y_s and for the pulse repetition rate Y_F.

$$Y_F/Y_s = f_F/f_s \approx 333 \qquad (4.4)$$

for

$$f_F = 20\ 10^3 = 2f_i = 1/T_{ok\ av}$$

$$f_s = 60\ Hz$$

The relativly high pulse frequency of approximately 20 kHz makes its possible to place these capacitors between the low frequency power phases, without causing an appreciable leading current effect in the polyphase supply line.

The thyristor bridge (CD) associated with the battery circuit will be modified for purpose of convenient reversal of flow of energy as indicated in Fig. II-4.8. Transformer XF has a tapped

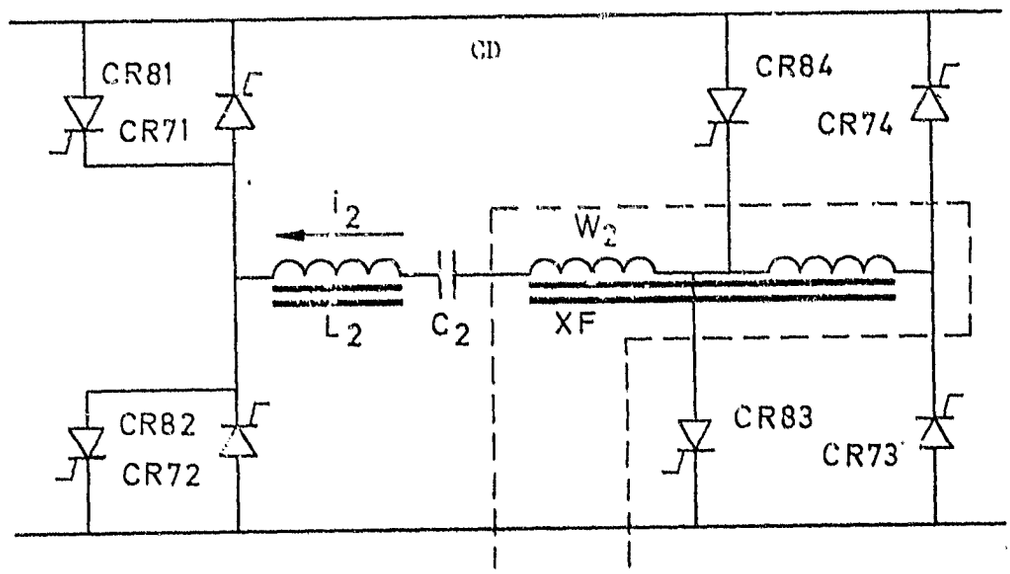


Fig. II - 4.8.

Thyristor bridge associated with dc circuit.

secondary winding in order to implement a different turns ratio of the transformer for forward and for reverse transfer of electric energy through the converter.

II - 4.4. The Control System

The electronic control system (CCS) consists of:

(a) the thyristor gating and firing system, a protection system (PS) which governs the sequence of firing of thyristors and prevention of accidental "illegitimate" firings;

(b) the power control system (CS) which governs the process of high frequency carrier generation and its modulation.

The function of the thyristor gating and firing system was described in II-4.2 above. It is in essence, analogous to the protection system used in simple dc converters in this class [8, 9] used for ion propulsion engines. However, there are aspects of considerable added complexity associated with its functions, especially concerning the connections with the ac polyphase line. To use the terminology associated with the half bridge converter of this class of converters shown in Fig. II - 4.5, this protection system has to distinguish, unerringly, which two of the three phases of the supply line have to be engaged for power flow in one or the other direction; which of these thyristors will remain in a forward biased condition once it ceases to conduct and thus requires thus a grace period (turn off time) in the form of back bias; which of these thyristors will carry the "main" forward resonant current, whatever the forward direction may be in the

sense of energy transfer; and, finally, which of the thyristor assumes the "diode" function in the sense of the half bridge circuit for a given pulse.

The protection system for the dc output or input of the converter is somewhat less complex. Yet, the fact that thyristors for opposite directions of conduction have to work next to each other poses problems that are less severe than those associated with the antiparallel three phase bridge; this type of problems is, of course, completely absent in the case of a simple diode output bridge.

Signals e_1, e_2, and e_3 are fed into a sequence of polarity discriminators which, eventually, generate the signal blocks i-j which identify the relative polarity of phases, as introduced before. The output signals of the discriminatory logic which relates to these intervals i-j is indicated in parts (k) through (p) of Fig. II-4.9. Signals v12, v13, v23 and signals $v1^+$, $v1^-$, etc., indicated in parts (b) through (j) of the same figure, signify steps in the process of successive discrimination of the logic process. These blocks i-j are used to clear access to the gates of the eligible thyristors. The actual command for firing comes from the power control system (CS) in the form of signals Cs1 and Cs2 indicated in Fig. II-4.6. These signals Csi fire the thyristors which were selected by the thyristor gating

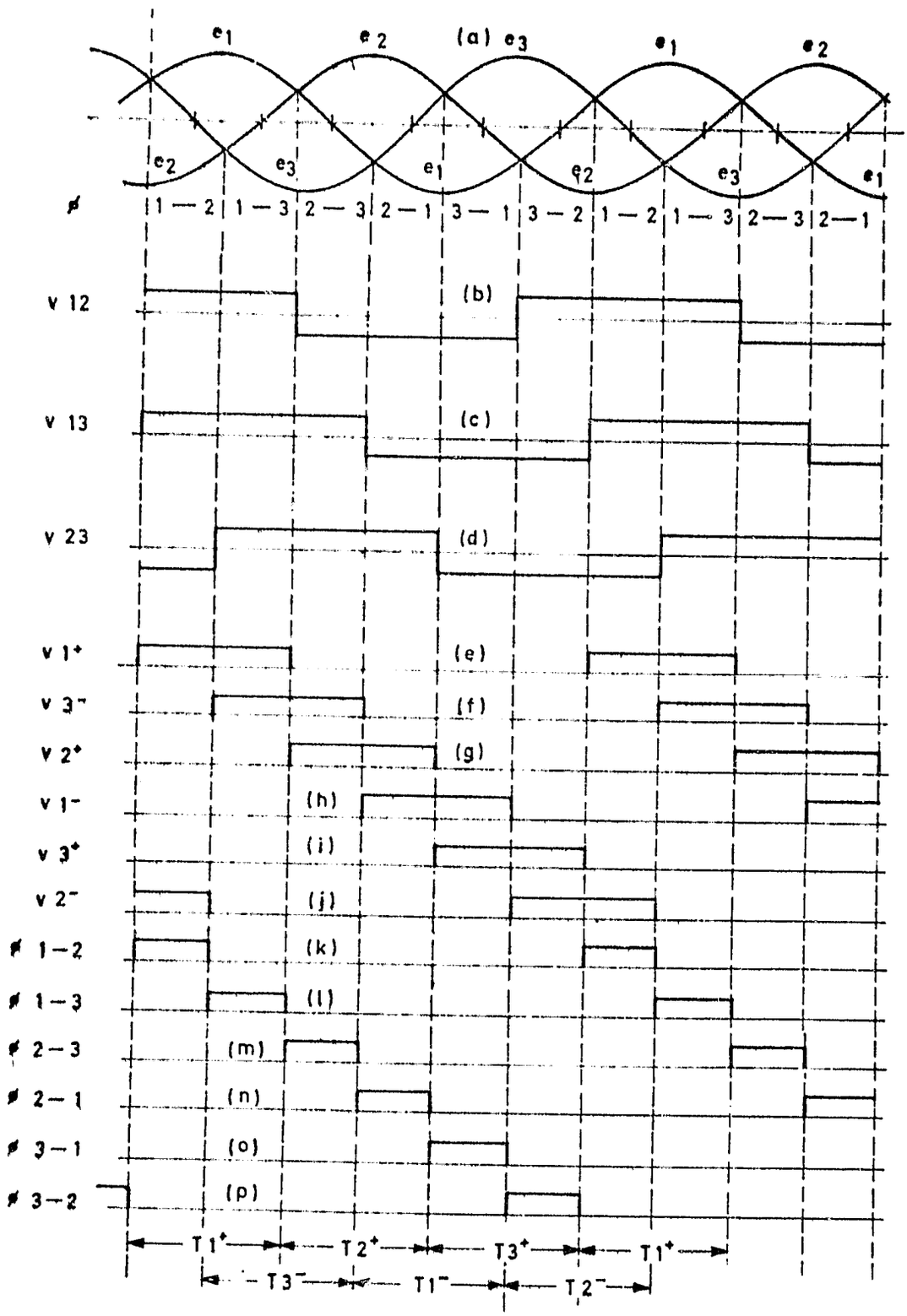


Fig. II - 4.9.

Signals for the control logic of the thyristor gating and firing system.

and firing system. The referred to selection process includes also a command given to the thyristor firing and gating system, which indicates the direction of power transfer.

The resulting firing pulse trains and their relative position in time are summarily indicated in parts (c) through q) of Fig. II - 4.10. These signals are referred to the time intervals $T1^+$, $T2^+$, etc. found at the bottom of Fig. II-4.9. The significance of this figure appears self explanatory. Back bias detectors BBij and firing pulse generators FPGij are associated with each thyristor CRij.

The power control system has, in principle. the structure of the formerly referred to ASDTIC system |3, 4|. It is indicated in its well known form in block diagram form in Fig. II-4.11. Input for signals ca_{ov} and c_{arv} are provided for application of continuous electric control signals to govern independently the power system output of current and voltage.

Access to the control system's current control and of its voltage limiting capability are necessary in order to achieve the pulse modulation processes which are essential for the materialization of the presented system. The control system receives its inputs from the current sensor (IS) the attenuated output voltage and the two before named signals ca_{rs} and ca_{ov}.

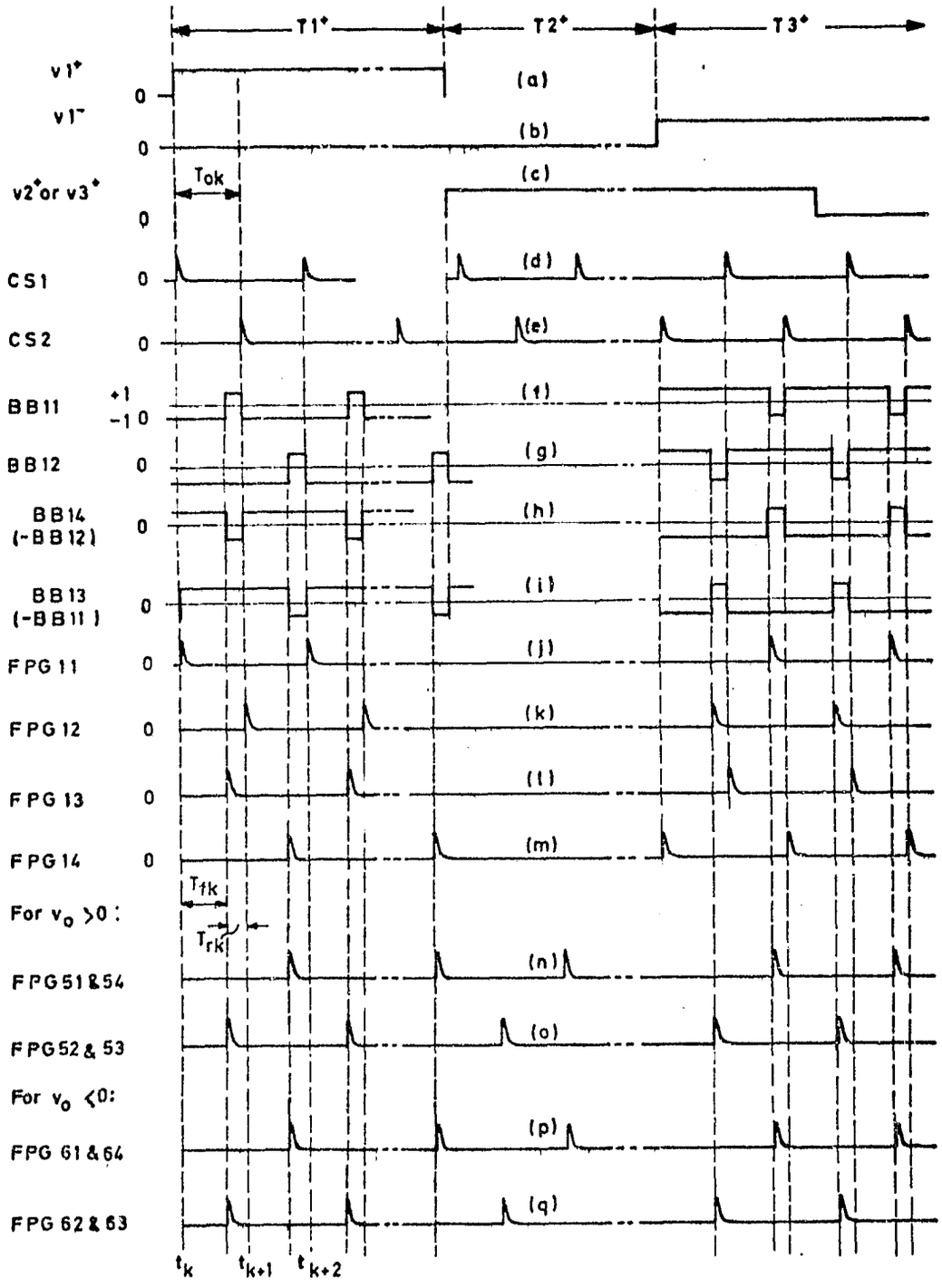


Fig. II - 4.10.

Illustration of representative firing signal sequence emitted by the firing pulse generators, FPGij and the back bias conditions BBij, associated with thyristors CRij.

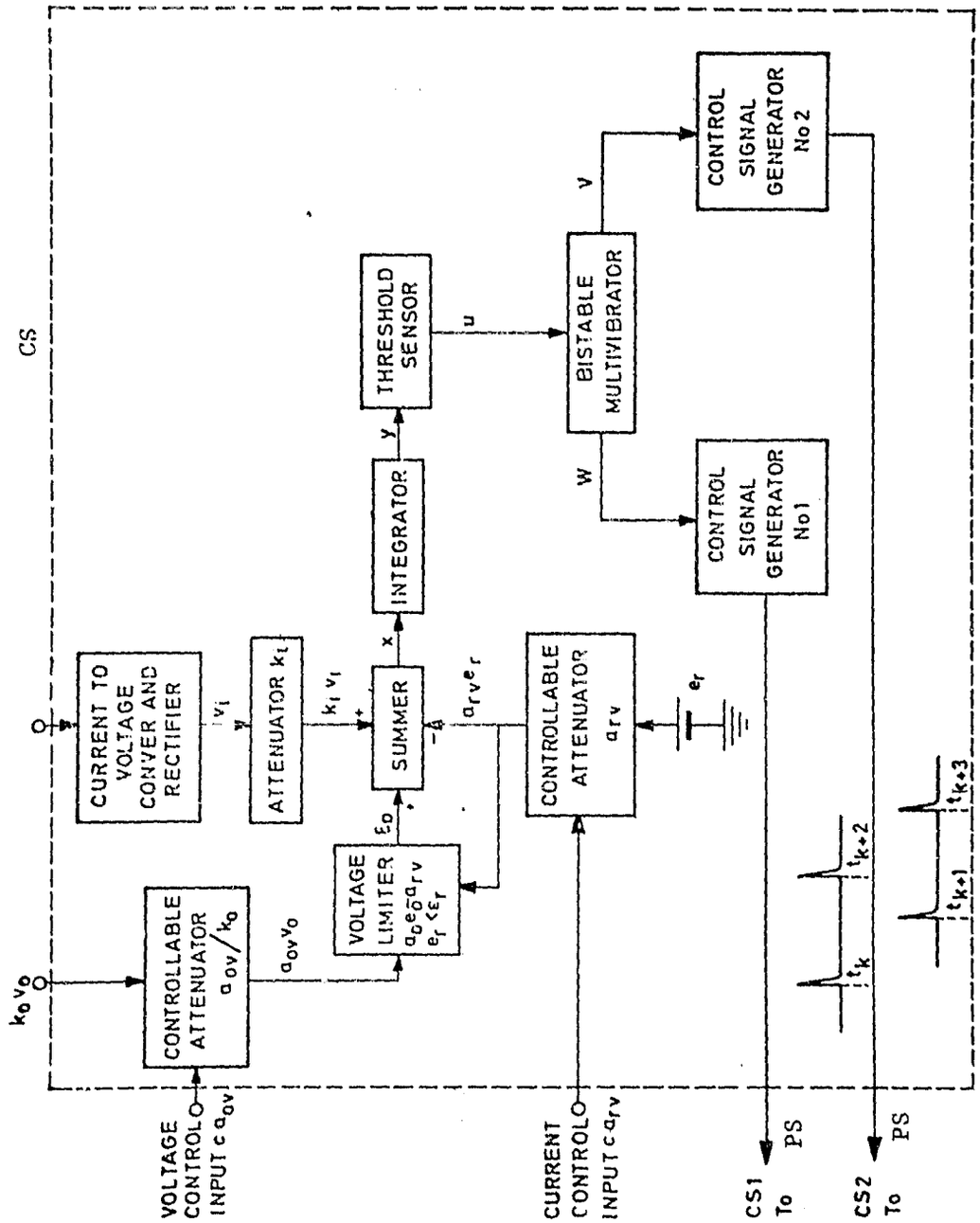


Fig. II - 4.11.

Block diagram of ASDTIC control system CS with inputs for voltage and current control.

II - 4.5. Component Requirements

No other component improvements appear needed than those used for dc converters of this class,

With regard to thyristors, it means that single module converters with power capacitors up to the order of 100 kW could be presently implemented with commercially available components. Expansion to the megawatt range can be implemented with larger thyristors, such as 1 to 3 kV forward blocking capacity, 1 kA current carrying capability, with turn off times between 10 and 15 microseconds. Another approach is that of modularization, whereby converters for the megawatt range could be constructed, once the technology is established.

The technology of capacitors has greatly improved in recent years and appears adequate for equipment in the 100 kW range up to the multimegawatt range.

Wire wound devices such as transformers and inductors use increasingly lower cost ferrite cores instead of the more expensive tape wound cores, if physical weight is not at a very high premium. Yet, tape wound cores with an inserted air gap can be used in certain cases. Construction of larger ferrite cores, needed for inductors beyond the submegawatt (100 kW) range does not seem a major hurdle to overcome. Currently available cores can be paralleled or devices arranged in series in order to construct megawatt size converters.

II - 5. System Analysis and Characterization

II - 5.1. General Aspects

Analysis of the bidirectional three phase ac to dc converter is analogous to the analysis of dc converters of this class.

The operation of the resonant circuit is studied in a succession of time intervals i-j as explained before with reference to Figs. II - 2.3 & II - 4.9. The series resonant LC_1 circuit "sees" on the ac side an input voltage e_i which is identical with the output voltage of a loaded full wave diode rectifier bridge, energized by a threee phase line. The difference between the characteristics of a diode bridge and the here presented system lies in the fact that the appropriately selected thyristors sample this voltage e_i in succession to carry the resonant current i_1 in both directions. The ratio between the cumulative charge per unit of time which passes in either of the two directions depends on the intended direction of power transfer. The resonant circuit, thus remains continuously connected to the three phase system, even though only selected thyristors carry high frequency pulses at one time, that is, as long as the resonant current i_1 is continuous. This current becomes discontinuous for conditions of lighter loading, such as one half of the rated output current or less, depending upon the ratio, T_{kr}/T_{kf} indicated in Fig. II-4.6, and further defined and

explained in the literature [6, 10]. Yet the discontinuity referred to above occurs at a kHz rate, which is (1) usually substantially above 0 Hz rate of ordinary thyristor bridges and (2) concerns, inherently, current pulses with an oscillation frequency of no less than 10 kHz. The low pass filters (IF), (OF) which are part of the conversion process need, therefore, not be designed for the lowest current pulse repetition rate of the LC_1 circuit, but for less than twice the resonant frequency of this LC_1 circuit.

The just described general philosophy of system analysis is now illustrated with a numerical example. A small scale example is chosen for the purpose of simplicity of treatment. Translation of this small scale example to the intended 100 kW range is briefly indicated at the conclusion of this report.

II - 5.2. A Numerical Example.

Assumed is a dc source voltage e_s with a nominal value E_s = 270 VDC. It is assumed that this source voltage is the average $e_{i\ av}$ of a voltage e_i which would appear at the output terminals of a full wave diode bridge which is fed from a 117/208 VAC three phase line with corresponding phase voltages e_1, e_2 and e_3. Assumed is, furthermore, that the average $i_{1\ av}$ of the absolute value of the resonant current $|i_1|$ in a converter of the discussed class is 11 Amperes.

The value of capacitor

$$C_1 = i_{1\ av} T_{ok} / v_{cpp} = 11\ 50\ 10^{-6} / 1100 \approx 0.5\ \mu F \qquad (5.1)$$

where

$T_{ok} = t_{k+1} - t_k = 1/2\ f_i$; see Fig. II - 4.6(p);

v_{cpp} = the peak to peak voltage on capacitor C_1, which is in excess of $4e_{i\ av}$.

The series inductor

$$L = (T_{ok}/\pi)^2 / C_1 \approx 340\ \mu H \qquad (5.2)$$

Consider now the effects that are introduced by the fact that $e_i \neq E_s$:

The steady state peak to peak input voltage variation to a converter of the here described class which is caused by a rectified three phase line amounts to approximately 11 percent of $e_{i\ av}$. This is the largest steady state input voltage variation that the converter will "see" under nominal operating conditions, when this input voltage consists of succeding intervals i-j, as discussed above.

One will allow as a rule a certain steady state tolerance of the ac line voltage of, say, $\pm$ 10 perecent. The smallest instantaneous input voltage

$$e_{i\ min} \simeq e_{i\ av}(1 - 0.1 - 0.06) = 0.84\ e_{i\ av} \tag{5.3}$$

If it is assumed that the system will operate with an efficiency $\eta \simeq .95$, then it can be concluded that [6, 7, 11]

$$v_2 \simeq (0.95)(0.84)(270) \simeq 215\ V \tag{5.4}$$

where

v_2 = the apparent primary transformer voltage amplitude.

L and C_1 are now modified since $i_{1\ av} = VA/v_2 = 3000/215 \simeq 14$ A:

$$C_1 \sim 0.6\ \mu F; \qquad L \simeq 280\ \mu H \tag{5.5}$$

It is here, tacitly, assumed that the system would cease to operate whenever $e_i < e_{i\ min}$. This can be remedied by making a further allowance for transient excursions of the ac line voltage. This allowance can, of course, affect the efficiency of the system, since the span of the current form factor

$$\rho_i = i_{1\ rms}/i_{o\ rms} \tag{5.6}$$

increases, and so will the ohmic losses increase approximately with the square of ρ_i [2, 6, 12]. Similar considerations apply for excursions of the line voltage toward increasing magnitudes;

provisions for lock out and temporary clamping of excessive voltages via filters will be made in that case, at the stage of design for a specific application.

The voltage of the inverter ($e_s = e_i$) has an average

$$e_{s\ av} = E_s(1 \pm 0.1) \tag{5.7}$$

with the characteristic ripple of full wave rectified ac, that is a ripple with a peak to peak value of

$$v_{rpp} = 0.11\ E_s \tag{5.8}$$

Control of the output current i_o to the load, such as a battery is accomplished by an almost common version of ASDTIC [3, 4]. A more complex form is needed if the low frequency (360 Hz) content of e_i should be suppressed. A passive low pass filter would defeat the intended purpose of light weight construction.

The common ASDTIC version, including the one now in use for the ion engine power processor [8] differs little from the basic philosophy of the analog signal to discrete time interval converter. The output of the integrator depends also on extraneously introduced signals which serve the purpose of system stabilization. Yet, these signals shift the limiting values of the integrator output

in such a way that a change in these extranuously introduced signals causes an appreciable delay in system response. The just described delay in response reduces the attenuation of the ripple of the converter's input voltage.

The input voltage ripple of 4 % rms of $e_{i\ oo}$ at 360 Hz should be reduced to [3, 5]

$$v_{o\ rms} = .04\ V_o/a_{d1} \tag{5.9}$$

where

V_o = the nominal output voltage of the converter

a_{d1} = the attenuation of the first harmonic component of the 360 Hz input voltage ripple.

The active attenuation effect

$$a_{d1} = N/\pi \tag{5.10}$$

where

N = the number of samples (half waves of the modulated carrier) that are taken from e_i during one interval i-j.

At an input filter frequency

$$f_F = 20 \text{ kHz} = 2f_i \tag{5.11}$$

is

$$N = 20\ 10^3/360 \approx 55 \tag{5.12}$$

The attenuation a_{d1} is then given by

$$a_{d1} = 55/3.14 \approx 17.5 \tag{5.13}$$

The rms content of the output voltage at 360 Hz is then

$$v_{o1\ rms} = .0023\ V_o \tag{5.14}$$

or approximately one quarter percent of the nominal output voltage, using (5.9) for that purpose.

It is, however, contended at this time that it may not be possible to attain the "ideal" attenuation of the first harmonic component, which is given by equation (5.13). Extended theoretical and experimental studies, which are now in progress on another (internal) program for over two years indicate that, possibly, only one part of the attenuation indicated by (5.13) could be materialized,

At an input jitter frequency

$$f_j = 20 \text{ kHz} - f_i \tag{5.11}$$

is

$$N = 20 \cdot 10^3 / 360 = 55 \tag{5.12}$$

The attenuation a_{d1} is then given by

$$a_{d1} = 55/3.14 = 17.5 \tag{5.13}$$

The rms content of the output voltage at 360 Hz is then

$$V_{o1\ rms} = .0023\ V_o \tag{5.14}$$

or approximately one quarter per-cent of the nominal output voltage, using (5.9) for that purpose.

It is, however, contended at this time that it may not be possible to attain the "ideal" attenuation of the first harmonic component, which is given by equation (5.13). Extended theoretical and experimental studies, which are now in progress on another (internal) program for over two years indicate that, possibly, only one part of the attenuation indicated by (5.13) could be materialized,

because of a multi cycle response, rather than a complete system response within each closed cycle. The resulting attenuation of the input ripple to more, rather than one quarter percent of V_o still appears adequate for the case in question. This compares favorably with low frequency choppers - approximately 400 Hz - which require very substantial filters to remain even then with an appreciably larger low frequency harmonic content.

The current carrying capability of thyristors is estimated in the following. Each of the two "forward" conducting thyristors associated with each phase conducts for 40 % of the time, ∿ 40 μsec., out of 100 μsec when that phase is "on" as explained in part II - 2 through II-4 of this report and described in the referred to literature [6]. Each phase is "on" one third of the time of one period with its "forward" thyristors, such as CR11 and CR14, and one third of the time with its "reverse" thyristors such as CR12 and CR13, even though power is being transferred in the "forward" direction (see also the matrix in Fig. II - 4.7).

The average current $i_{th\ av}$ of each of these thyristors

$$i_{3th\ av} = 2/3\ 0.4\ i_{1\ av} = 28/7.5 = 3.73 \qquad (5.15)$$

The rms content of the same current is approximated by the relation

$$i_{rth\ rms} = \rho_i\ i_{l\ av}\sqrt{2}/7.5 = 1.4\ i_{l\ av}/1.93 \qquad (5.17)$$

The value $\rho_i \approx 1.4$ is a typical value for the discussed current wave form. The analytic derivation of the values of ρ_i is found in the literature [6].

$$i_{3th\ rms} \approx 10\ A \qquad (5.18)$$

The rms value shown in (5.18) appears as an acceptable first order approximation. The same thyristors carry the "diode" current as explained in II-4; it appears that this approximation would then be nearer to the actual rms value of the current passing through the concerned thyristor.

The current form factor $\rho_{i\ th}$ for a thyristor in the antiparallel thyristor bridge can be defined as

$$\rho_{i\ th} = i_{3th\ rms}/i_{3th\ av} \qquad (5.19)$$

In the case under consideration is

$$\rho_{i\ th} \approx 10/3.73 \approx 2.68 \qquad (5.20)$$

Relation (5.20) shows that a thyristor-bridge consisting of thyristors which are rated for, say, 250 A_{rms} could provide a dc current of

near 100 Amperes to a dc load. It means that a 255/440 VAC line could supply 60 kW to a dc load using a single module converter of the discussed class. A 440/760 VAC line could supply over 100 kW dc power under the same conditions. Higher ac line voltages are customary for yet higher power levels in order to limit the involved currents and the therewith associated heating effects.

The proposed use of thyristors with an almost 0.33 duty cycle in which inverter operation is required for each of the thyristors, deviates from the condition for which thyristor ratings were established, namely continuous inverter or chopper operation. It is believed that the stress imposed on the thyristors is lighter than the one applied in current test procedures. More will be learned about this topic through actual experimentation. It is expected that a larger rms current carrying capability will be found because of the above referred to duty cycle.

The input filter IF, indicated in Fig. II - 4.1 serves the purpose (1) to close the ac side of the resonant circuit, consisting of the series combination of the capacitor C_1 and its companion inductor L and (2) to isolate the three phase line from the high power frequency components which are contained in the previously explained rectified resonant current i_1.

This filter IF consists of three capacitors C_{12}, C_{13} and C_{23}, shown in Fig. II - 4.3; the subscripts associate the capacitors

with the individual phases of the ac supply line with voltages e_1, e_2 and e_3.

The composite of these capacitors forms the time invariant input filter capacitor C_i as viewed from each individual phase pair with voltages e_{12}, e_{13} and e_{23}; only one of these pairs is engaged in the conversion process of the cyclo up converter CU at one time. The magnitude of this capacitor

$$C_i = C_{ij}(1 + \tfrac{1}{2}) \tag{5.21}$$

where

$$C_{ij} = C_{12} = C_{13} = C_{23}.$$

In order to arrive at an acceptable approximation for the value of C_i it is now assumed that the reactances $\omega_s L_i$ (i = 1, 2, 3) of each of the individual phases are purely inductive and equal, when looking back toward the source PG. These reactances

$$\omega_s L_i >> 1/2\omega_F C_i \tag{5.22}$$

where

ω_s = the radial frequency of the individual phases of the ac supply line, such as $2\pi 60$.

ω_F = the radial frequency of the simplified, sinusoidal carrier current i_1, such as $2\pi 10^4$.

The factor 2 appears in expression (5.22) because the filter IF "sees" a waveform with double the radial frequency ω_F, since the current waveform as reflected through the thyristorbridge CU appears rectified.

The assumption made in (5.22) allows to view each pair of phases that is connected via the bridge CU to the series resonant circuit LC_1 as a current source with magnitude I_{sk} during the time interval T_{ok} of existence of the kth half cycle of the carrier current i_1. This is illustrated in Fig. II - 5.1.

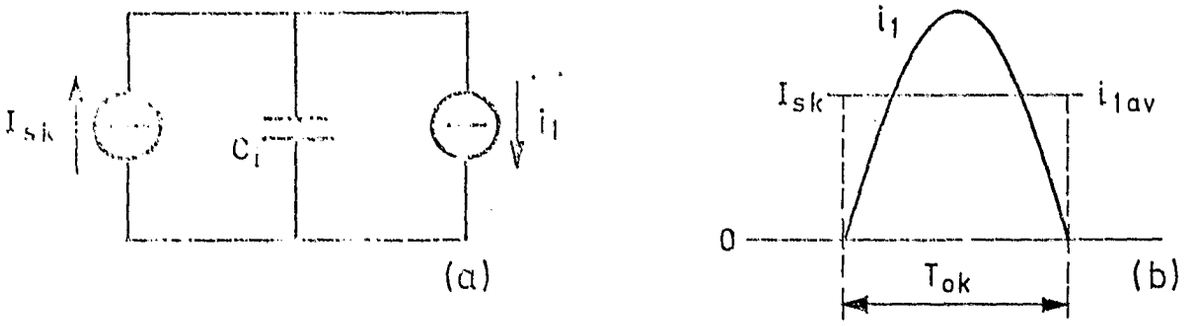


Fig. II - 5.1.

(a) Input filter capacitor C_i connected to the "equivalent" current sources I_{sk} and i_1; (b) current waveforms I_{sk} and i_1 during the kth half wave interval T_{ok} of i_1.

The phase current i_i (index i = 1, 2, 3) has a magnitude I_{sk} which is nearly equal to the average $i_{1\ av}(k)$ of $|i_1|$ during its kth half cycle. Therefore

$$i_{1\ av}(k) \approx I_{sk} \tag{5.23}$$

It is assumed, furthermore that

$$I_{sk} = I_{sk+1} \tag{5.24}$$

because it is desired that

$$i_{1\ av}(k) = i_{1\ av}(k + 1) \tag{5.25}$$

in order to supply a steady dc current to the battery. The assumption of a current source I_{sk} is based on inequality (5.22) which does not allow a significant change of the phase current i_i within an interval T_{ok}. It follows that capacitor C_i must reconcile the difference.

$$i_{c1} = i_1 - I_{sk} \tag{5.26}$$

by carrying an alternating current i_{c1}. This current i_c generates a voltage ripple

$$i_{c1\ rms} = v_{r\ rms}\ 2\omega_F C_i \tag{5.27}$$

where

$$i_{c1\ rms} = \{\frac{1}{\pi} \int_0^{\pi} (i_1 - i_{1\ av})^2 d\beta\}^{\frac{1}{2}} \tag{5.28}$$

and

$$\beta = t/\sqrt{LC_1} \tag{5.29}$$

Another constraint is introduced in the form of

$$r_n = v_{r\ rms}/e_{ij\ rms} \tag{5.30}$$

where

r_n = the voltage ripple between the phase pairs with voltages e_i and e_j, normalized with respect to the rms voltage of one of these phases.

Each of the two concerned phases will then carry a voltage ripple

$$v_{rph\ rms} = r_n\ e_{ij\ rms}/2 \tag{5.31}$$

near the radial frequency $2\omega_F$ since these phases will divide this voltage equally between themselves. The size of C_i can be calculated,

once the magnitude of $v_{rph\ rms}$ is accepted as an externally imposed constraint. The equation

$$C_i = \frac{i_{c1\ rms}}{4\omega_F\ v_{rph\ rms}} \tag{5.32}$$

serves to calculate C_i using (5.28) for the calculation of $i_{c1\ rms}$. The rms content of the current i_{c1} in capacitor C_i which is caused by i_1 was defined in equation (5.28). It is recalled that

$$i_{1\ av} = 2I_1/\pi \tag{5.33}$$

if one uses the simplifying assumption that

$$i_1 = I_1\ \sin t/\sqrt{LC_1} \tag{5.34}$$

Equation (5.34) is only an approximation. It will be used for purpose of the following analysis since this shortcoming is largely remedied at a later time, with introduction of the current form factor [6]

$$\rho_i = i_{1\ rms}/i_{1\ av} \tag{5.35}$$

Introduction of (5.33) and of (5.34) in (5.28) yields

$$i_{c1\ rms} = (I_1/\sqrt{2})(1 - 8/\pi^2)^{\frac{1}{2}} \tag{5.36}$$

or

$$i_{c1\ rms} = 0.342\ i_{1\ av} \tag{5.37}$$

Introduction of (5.35), finally yields

$$i_{c1\ rms\ \rho_i} = 0.4788\ i_{1\ av}; \qquad \rho_i = 1.4 \tag{5.38}$$

The value for $i_{c1\ rms\ \rho_i}$ of (5.38) is now introduced in (5.32) to calculate

$$C_i = \frac{0.48\ i_{1\ av}}{2\omega_F\ r_n\ e_{ij\ rms}} \tag{5.39}$$

For the example under consideration is

$$C_i = \frac{(0.48)(11)}{2\ 20\ \pi\ 10^3\ 2\ 10^{-2}\ 208} \approx 10\ \mu F \tag{5.40}$$

if

$$r_n = 0.02 \quad \text{and} \quad v_{rph}/e_i = \frac{\frac{1}{2}2\ 2.08}{117} = 0.0178 \tag{5.41}$$

If, for instance a ripple of 1 percent at a radial frequency $2\omega_F$ is acceptable in each of the phases, then

$$C_{12} = C_{13} = C_{23} \simeq 10\ \mu F \tag{5.42}$$

according to (5.21) and

$$C_i \simeq 16\ \mu F \tag{5.43}$$

Each of the capacitors $C_{11} = C_{23} = C_{13}$ will have to be capable of carrying an rms current

$$i_{cc1\ rms} \simeq (2/3)(0.48)(11) \simeq 3\ A_{rms} \tag{5.44}$$

at 20 kHz or $\simeq 0.3\ A_{rms}/\mu F$, which is well within the ratings of currently available good quality capacitors which employ metalized film as "plates".

The same capacitors $C_{12} = C_{13} = C_{23}$ will conduct another current at the single phase line frequency, such as 60 Hz. The phase currents $i_{cs\ rms}$ at this frequency is given by

$$i_{cs\ rms} = e_{ij}\ \omega_s\ C_i \tag{5.45}$$

This

$$i_{cs\ rms} \approx 208\ 2\pi 60\ 16\ 10^{-6} = 1.25\ A_{rms} \tag{5.46}$$

The individual capacitor currents

$$i_{ccs\ rms} \approx (2/3)(i_{cs\ rms}) = (2/3)(1.25) \approx 0.82\ A_{rms} \tag{5.47}$$

The radial frequency components ω_s and ω_F are sufficiently far apart to neglect cross modulation terms so that the total rms current $i_{c\ rms\ T}$ per microfarad amounts to

$$i_{c\ rms\ T} \approx \sqrt{3^2 + 0.82^2}/10 = 0.31\ A_{rms}/\mu F \tag{5.48}$$

The output filter OF consists of a simple capacitor which closes the resonant circuit toward the converter's load terminals. Its size is determined by the amount of current ripple that the battery plates can tolerate, without causing appreciable efficiencies. The analysis is similar to the one presented for the input filter IF. Yet, it is expected that the battery can tolerate a larger high frequency (20 kHz) current ripple, because the battery in itself has a significant capacitive effect.

The magnitude for the output filter capacitor C_o can be derived from equation (5.39) as

$$C_o = \frac{0.24\ i_{l\ av}}{\omega_F\ r_{no}\ V_o} \tag{5.49}$$

where

$$r_{no} = v_{o\ rms}/V_o;$$

$v_{o\ rms}$ = the rms content of the output voltage ripple in the presence of a resistive load;

V_o = the nominal dc output voltage.

In the numerical example under consideration is for $r_{no} = 10^{-2}$ and $V_o = 250$ VDC

$$C_o = \frac{0.24\ 11}{2\pi 20\ 10^3\ 10^{-2}\ 250} \approx 10\ \mu F \qquad (5.50)$$

The ripple current $i_{c10\ rms}$ through capacitor C_o is calculated form (5.38)

$$i_{c10\ rms} \approx 0.48\ i_{1\ av} = (0.48)(11) = 5.28\ A \qquad (5.51)$$

The output capacitor will thus carry 0,53 $A_{rms}/\mu F$, still well within the current carrying capability of good quality film capacitors.

II - 6. Engineering Assessment of the Proposed Concept

II - 6.1. Critical Aspects

A concept is presented here which promises the benefits that were described in subsection II - 3.4. It is intended to define the critical technical features of this system which depart significantly from the known state of the art, best known as "bottle necks".

Some of the semiconductor switching components seem to fall in the category of bottle necks. That is, for power capacities in the order of 100 kW and with internal frequencies up to 10 kHz. An expansion of power capacities into the MW range will require larger thyristors with current carrying capacities up to the range of kiloamperes with turn off times near 10 μsec.

Conversely, one could lower the internal frequency to, say, 5 kHz and use thyristors with current carrying capabilities up to 500 Amperes. The price is then heavier weight of equipment and higher cost. Yet, cost and weight would be by far more favorable than with conventional equipment.

Development of capacitors appears well advanced to meet the requirement of the proposed system. Efficient metal foil series

capacitors with rms current carrying capability up to 30 Amperes per microfarad have been successfully demonstrated at frequencies of 10 kHz. Metallized film filter capacitors for current carrying capacities up to 0.5 Amperes/μF have been successfully fabricated with magnitudes in the order of 100 μF at weights of approximately 20 J/kg, such as 600 VDC capacitors.

Construction of magnetic components at power levels of 10 kW and at frequencies of 10 kHz has been successfully demonstrated [6] with use of low cost ferrite core materials, when compared to tape wound iron cores.

The most significant bottle neck is seen in the development of an autonomous and unconditionally reliable electronic protection system for the bidirectional (antiparallel) three phase thyristor bridges CU and CD.

It is recalled that the protection system which is currently being used for thyristor converters which employ series resonant circuits [8, 12] is meant to prevent accidental firing of the "wrong" thyristor out of a total of two thyristors in a half bridge circuit. These two thyristors operate always in the same sense of polarity with respect to the dc source e_s [6].

It was explained before, with reference to Fig. II-4.3 that twenty thyristors will be used alltogether in the proposed system. This is no more than needed in conventional systems. Yet, the much lighter

frequency of change of paths of current flow requires careful control of the fast succeeding sequence of firing of these thyristors. This sequence is subject to coincidence of two signals for each of the thyristors, where one of these is uniquely associated with the same thyristor only!

Each of these two signals CS1 or CS2, explained in section II-4 exerts control on the oscillations of the current carrier i_1. The path for this current carrier is determined by the thyristor selection and firing system (PS). This system allows signals CS1 and CS2, respectively to reach the gates of four of the twenty thyristors at one time, depending on the polarity of the ac phases, the direction of energy transfer, the requested average (dc) load current, and on the desired power factor at the three phase ac ports.

The new features which need to be embodied in this more extensive protection system are the capabilities to

(1) distinguish the relative polarities of phases in the ac supply and to select the two phases with the largest voltage difference at any time;

(2) assign to the eight thyristors of which four are associated with each phase the appropriate rate for forward or reverse

energy transfer, subject to the conditions enumerated under (1) above;

(3) provide the appropriate selection for the sequence of firing for the purpose stated in (2);

(4) provide the required delays in the firing sequence so that the needed turn-off time is guaranteed for all thyristors;

(5) coordinate the firing of thyristors in the bidirectional dc bridge with the above enumerated conditions;

(6) provide the same conditions of sequencing and other protective features for the dc bridge as these stated for the ac bridge in (1) through (4) above.

It is recalled that the development of the "old" protection system for one pair of thyristors required approximately on year's time until unfailing operation could be attained under all regular and irregular conditions of operation. The now required protection system is much more complex in its functional mechanism, since new dimensions have been added to these functions.

The establishment of the described protection system is seen as the most challenging part of the proposed system, though its implementation does not require new electronic components, but

tenacious and meticulous electronic circuit development.

II - 6.2. Integration of Existing Technology

The existing technical elements of the series resonant converters technology will be integrated into the newly developed more broader systems concept. One of the essential technical requisites which are needed for that purpose is the above described protection system. The entire system will be governed by a control system of the ASDTIC type, whose purpose it is to provide this converter with the properties and the characteristics explained in section II-3 of this report [3, 4].

No fundamental theoretical or physical problems are apparent at this time, since the proposed bridge is intended as the high frequency version of a proven concept; the high frequency feature should allow the embodiment of the advanced external characteristics, defined in sections II - 2 through II - 4.

II - 7. Summary of Concept Formulation

A concept for a class of bidirectional four quadrant (BD4Q) converters was presented which promises to, substantially, improve the state of the art concerning: (1) functional reliability,

(2) speed of dynamic response, (3) cost, (4) efficiency and (5) physical size and weight. This system could, furthermore, be used for purpose of power factor correction in polyphase ac lines.

It appeared that appreciable systems analysis and circuit development work was needed in order to achieve the set goals. Yet, no significant component development work appeared required to materialize converters of this class for a power range in the order of 100 kW. Larger thyristors of higher quality will be needed beyond this range, unless weight and size is traded off against cost.

Indication of conceptual feasibility was the purpose of this chapter. A more detailed analysis of the potential benefits of the current program is found in chapter IV.

References - chapter II

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III. CONCEPT VERIFICATION

III - 1. Objectives

It is the objective of this chapter to describe the forms of functional solutions for the technical problems which were identified in subsection II - 6.1.

It is intended to let the series resonant circuit "see" a voltage source which is the equivalent of the output voltage of a three phase full wave rectifier bridge. The three phase cyclo-converter CV is contained in Fig.III - 1.1 which is reproduced here for convenience. The twelve thyristors CR_{ij} ($i = 1,2,3$; $j = 1,2,3,4$) form an array of switches for the purpose of:

a. connecting the series resonant LC_1 circuit to any of the three phases and

b. connecting the load bridge CD to any of the same three phases,

to conduct the resonant current i_1 which changes direction during each half cycle of operation of the resonant circuit. To be more specific, it is reiterated that the resonant current flows in succession during each half cycle through a "forward" conducting thyristor such as CR11 into the resonant circuit where $e_1 > e_2$ and through its antiparallel thyristor such as CR13. The therewith associated waveforms are also reproduced for convenience in Fig.III - 1.2.

The above referred to change of direction of current is necessary in order to limit the capacitor peak to peak voltage

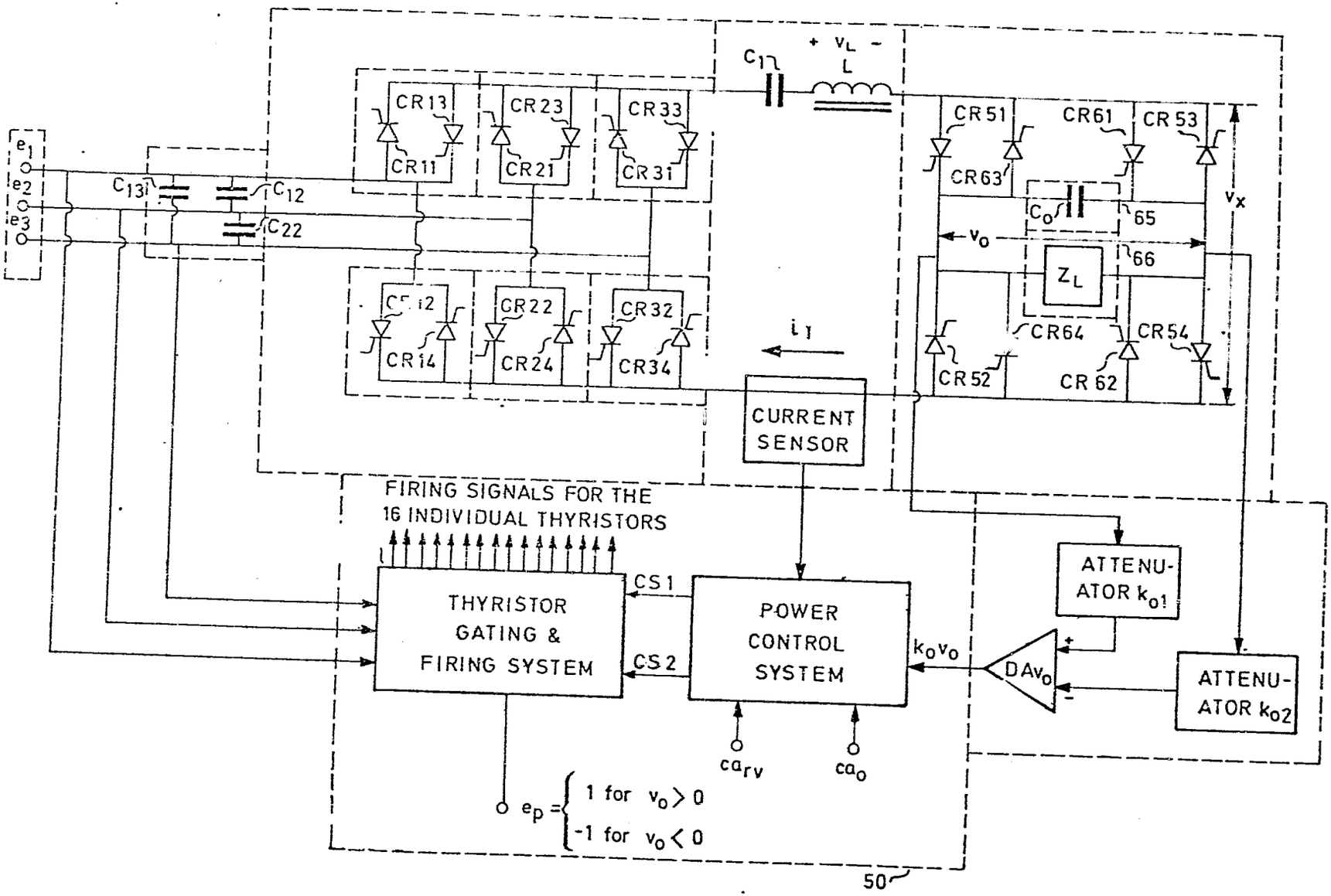


Fig. III - 1.1.

Symbolic schematic of the bidirectional series capacitor inverter-converter for operation of a dc load (source) with balanced voltage vs. the three phase neutral node.

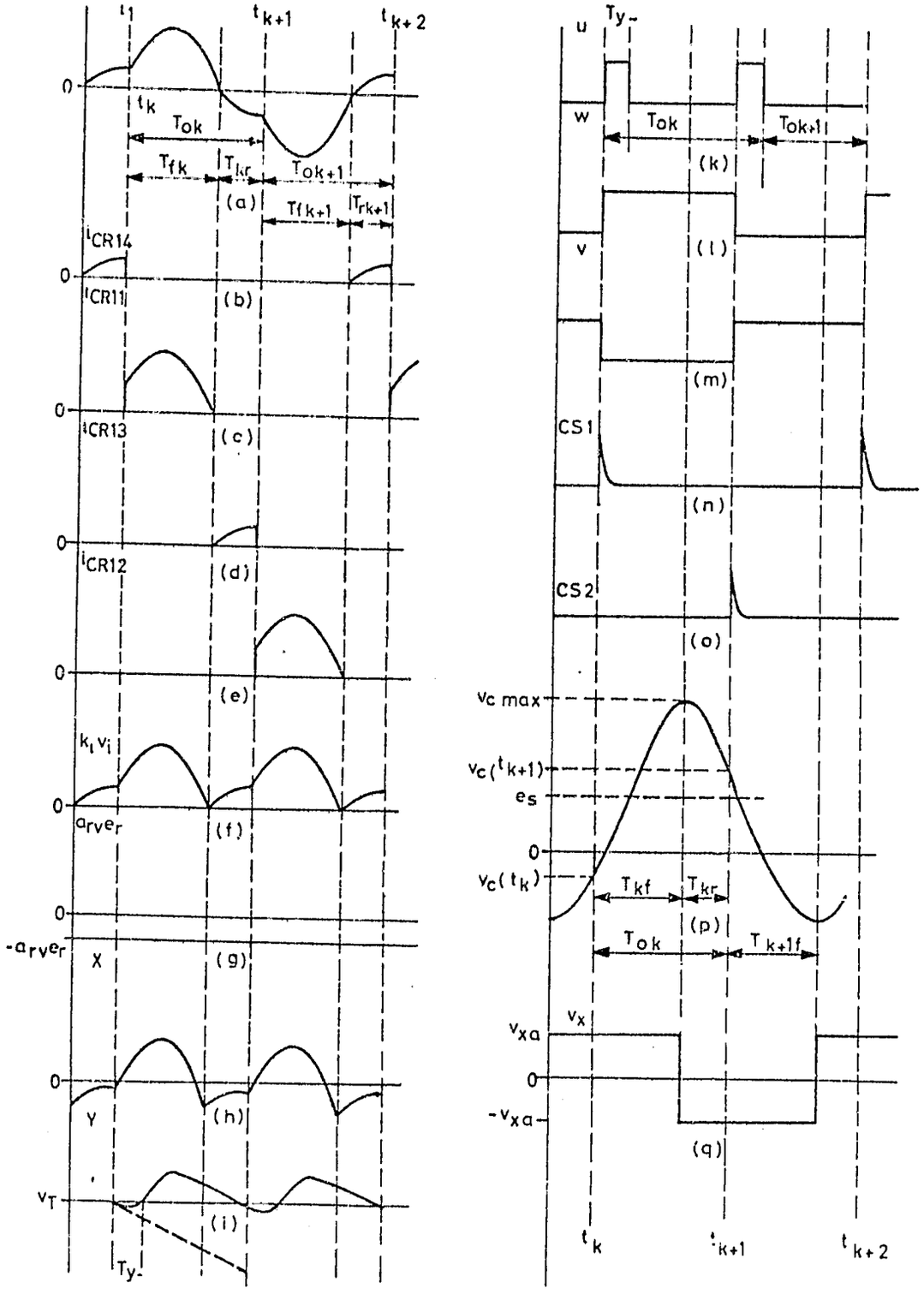


Fig. III - 1.2.

Significant voltage and current waveforms in the series capacitor converter.

$$v_{c1pp} = |i_1|_{av} T_{ok}/C_1 \qquad (1)$$

where

i_1 = the resonant current indicated in Fig. III - 1.2(1);

T_{ok} = one half inverter cycle interval; $T_{ok} = t_{k+1} - t_k$
and $2T_{ok\,av} = 1/f_i$, where f_i = the frequency of inversion.

The average of the absolute value of the resonant current i_1 is determined by the ASDTIC type control mechanism which is documented in the literature [1,2,3,4,5]. This control mechanism secures a constant amount of Ampere-seconds per second for each half cycle of operation of the series resonant circuit with duration T_{ok}. This is expressed in quantitative terms as

$$(1/T_{ok}) \int_{t_k}^{t_{k+1}} |i_1| dt = |i_1|_{av} = k_r i_r \qquad (2)$$

where

i_r = a controllable reference signal;

k_r = a signal level adjusting fixed constant

The reference signal i_r has the property that

$$di_r/dt = 0 \tag{3}$$

for three phase ac to dc conversion, as intended here.

It follows then by use of equations (1), (2) and (3) that

$$v_{c1pp} \simeq k_r i_r T_{ok}/C_1 \tag{4}$$

The only variable in relation (4) is T_{ok} whose variations within the range of continuous current i_1 are limited to

$$T_{ok\ max}/T_{ok\ min} \simeq 2\pi/(1+1/4)\pi \tag{5}$$

if a turn-off time of

$$t_{off} \simeq (1/4)\pi/\omega_o \tag{6}$$

is allowed and

$$\omega_o = 1/\sqrt{LC_1}. \tag{7}$$

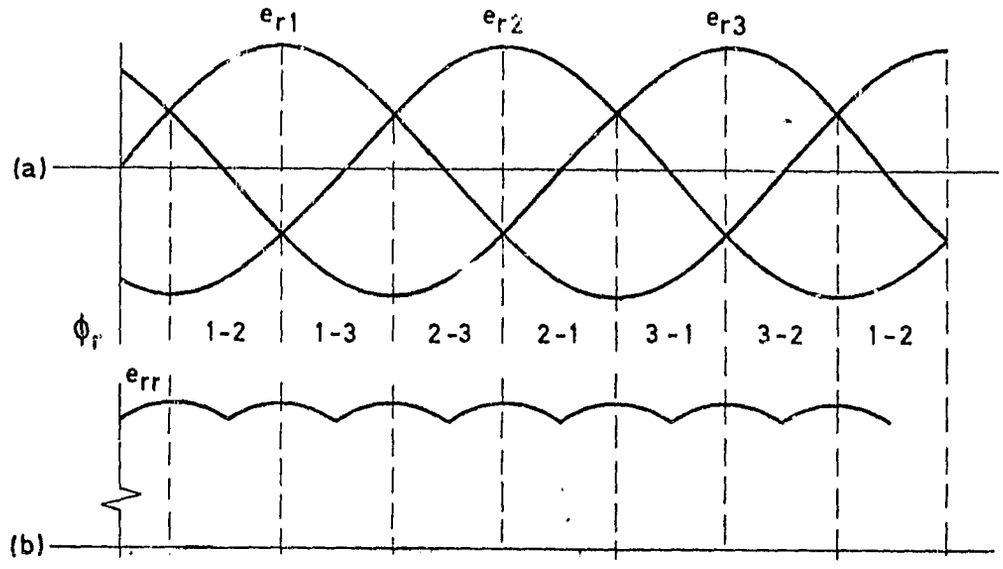


Fig. III - 1.3.

(a) Voltage waveform of a three phase ac system with indication of phases i - j (i,j = 1,2,3) engaged in the rectification process and (b) the resulting scaled rectified voltage e_s.

c-2

It follows from (5) that

$$v_{clpp\ max}/v_{clpp\ min} \approx 2/(5/4) \approx 1,6 \qquad (8)$$

in the range of continuous current, which includes the effects of variations of the input voltages e_s.

The three phase voltages e_1, e_2 and e_3 of a symmatrical polyphase ac system are shown in Fig. III - 1.3(1). The difference between the potentials which is indicated by the boundaries of the upper and on the lower part of this figure constitutes the unipolar voltage e_s which appears at the output terminals of a full wave three phase diode rectifier bridge. A scaled version of this voltage e_s is shown in Fig. III - 1.3(b).

The shown voltage e_s can be thought of as the input voltage of an ordinary dc converter, utilizing the power transfer and control method by way of a series resonant circuit |4,5|. The then following process of power conversion is analogous to the one described in the literature |4,5,6|.

Several aspects of technology deserve attention to implement the just stated functional philosophy:

(a) to select the appropriate thyristors of the cyclo-up converter CU in accordance with the respective phase voltages and to assign to these devices a "thyristor" or a "diode" function, as required;

(b) to modulate the current carrier i_1 in such a manner that the condition stated in equation (2) is satisfied for every half cycle |1,2|;

(c) to select the appropriate rectifier bridge in the cyclo-down converter CD;

(d) to interdict accidental malfunction due to "spurious" firing of thyristors;

(e) to perform the above described process in reverse so that power is derived from a dc source, connected instead of the load Z_L to the corresponding terminals of the bridge DU and said power is transferred to the three phase system by selection of the appropriate thyristor of CU, all shown in Fig. III - 1.1.

The above enumerated concepts distinguish the here presented system from the common dc converter of this type |4,5,6|. The functional philosophies for implementation of these concepts will be treated in this presentation with due identification of the therewith associated problem areas.

III - 2. The Doublesided Cyclo-Converter

The array of switches CR_{ij} (i = 5,6; j = 1,2,3,4) will work as an ordinary rectifier of the alternating current i_1, when CR's 51,52,53 and 54 are permanently energized, or energized at the appropriate instants of time.

Conversely will the same array of above indicated switches generate a current carrier i_1 if Z_L is replaced by a dc source and if these switches are energized in an appropriate sequential order. The specifics of this process will be presented further on.

The two above described processes of demodulation of the current carrier i_1 and of generations of this carrier respectively which can be performed by the same array of switches CD, characterize this array as a cyclo-down and as a cyclo-up converter for each case. This dual capability of carrier demodulation and of generation of a modulated carrier is characterized as that of a doublesided cyclo converter.

The three phase cyclo-converter CU can be thought of as an expansion of the two terminal cyclo-converter CD with appropriate analogy of operation. It is in the same sense a doublesided cyclo-converter.

The functional logic which governs these cyclo-converters is presented in the following.

III - 2.1. The Doublesided Three Phase Cyclo-Converter

The cyclo-converter DU generates the current carrier i_1, as described in the preceding material. For this purpose it derives power from the appropriate phase pairs with voltages e_1, e_2 and e_3. These phase pairs are identified in

Fig.III - 1.3(a); the first number i of the i-j pair identifies the phase with a voltage

$$e_i > e_j \tag{9}$$

For instance: if

$$e_1 > e_3 > e_2 \tag{10}$$

then i = 1 and j = 2 so that power is derived from phases with voltages e_1 and e_2; this pair with the largest potential difference between them is identified as the phase pair 1-2 in Fig.III - 1.3(a), followed by pair 1-3, and so on.

Each of these time intervals ϕ i-j is identified in Figs. III - 2.1(k) through (p). The logic schematic for the electronics which provide the electric signals ϕ i-j is presented in Fig. III-2.2. Reference is made to the two just named figures for purpose of explanation of the phase gating process.

The signals e_1, e_2 and e_3 are processed by individual attenuators k_1, k_2 and k_3, respectively. The resulting signals k_1e_1, k_2e_2 and k_3e_3 are fed into the differential amplifiers DE_{ij} (i=1,2; j=2,3). The output of these differential amplifiers are called v12, v23, and v13 respectively. The corresponding voltage waveforms are shown in Figs. III - 2.1(b) through (d).

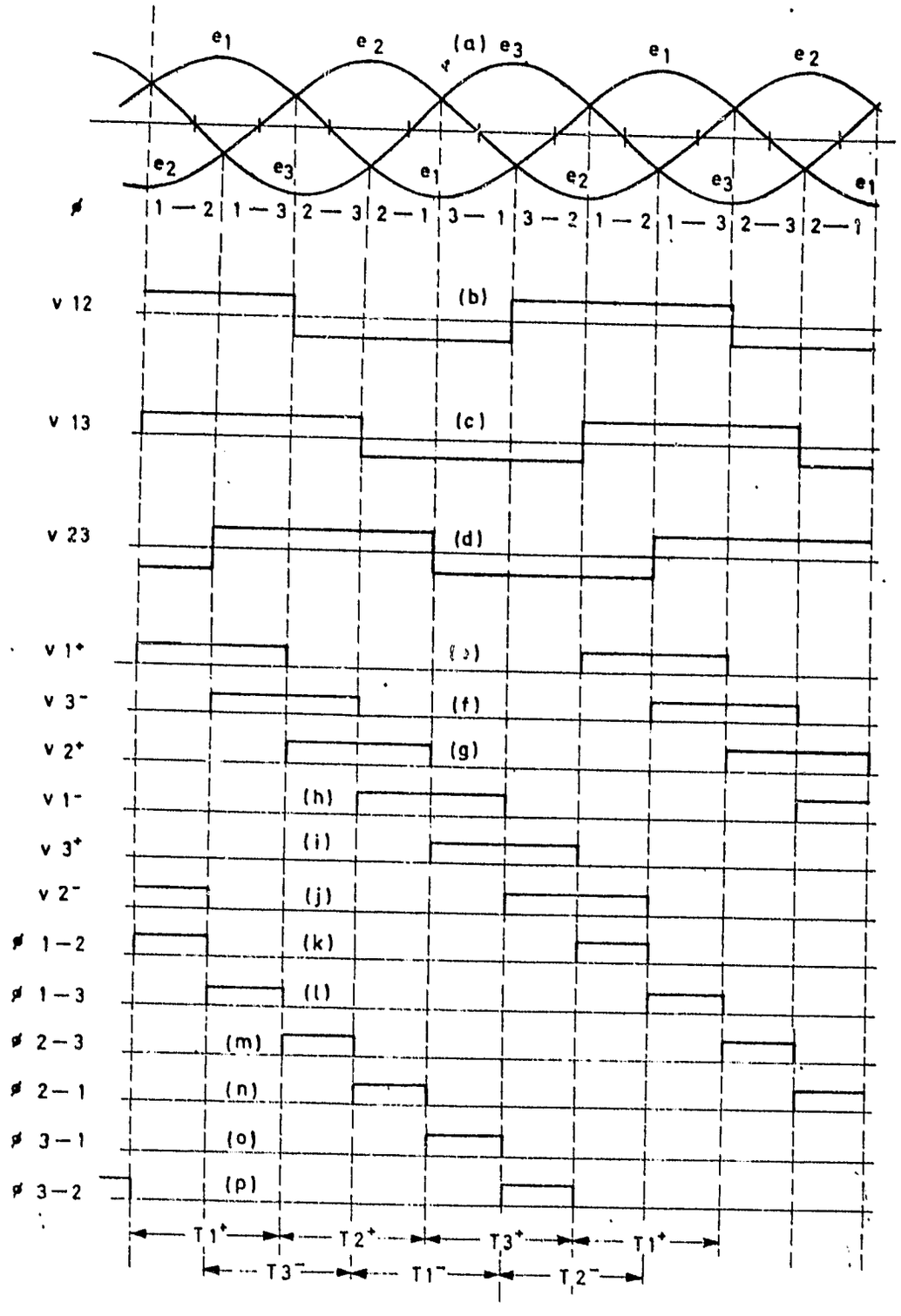


Fig. III - 2.1.

Signals for the control logic of the thyristor gating and firing system.

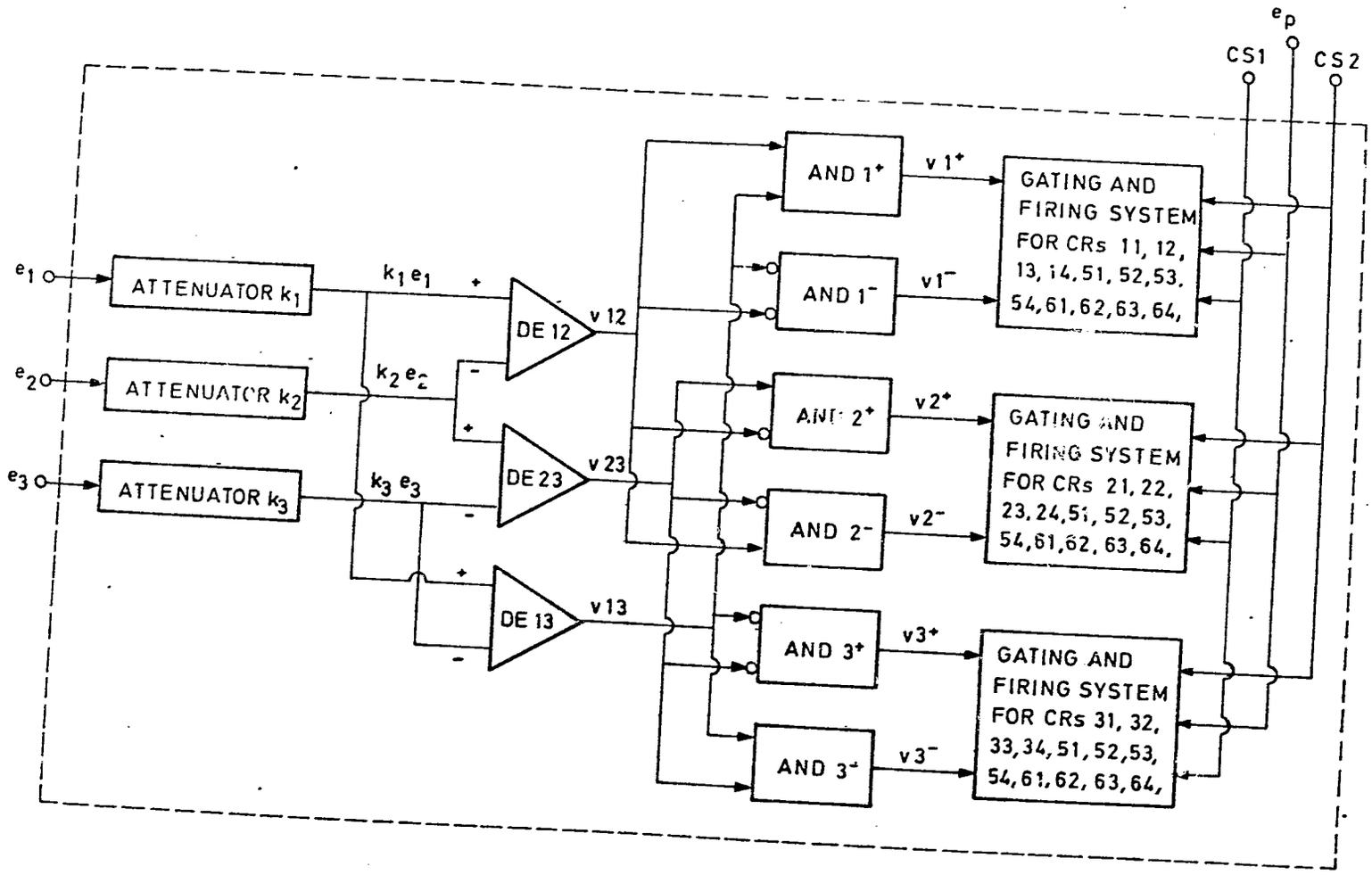


Fig. III - 2.2.

Logic schematic for the electronics to provide the signals indicated in figure III - 2.1. and the thyristor's firing pulses.

The outputs of DE_{ij} are fed into a battery of six AND gates for purpose of their operation as indicated in Fig. III - 2.2.The outputs of these AND gates take the form of signals $v1^{+}$, $v1^{-}$, $v2^{+}$, $v2^{-}$, $v3^{+}$ and v^{3-} as shown in Figs.III-2.1(3) through (j).

The signals vi^{+} and vi^{-} (i=1,2,3) are fed in pairs into the Gating and Firing Systems (GFS) for CR's i1 through i4 (i=1,2,3) and for CR's jk (j=5,6; k=1,2,3,4). These GFS also governed by the signals CS1, CS2 and e_p. Signals CSi (i=1,2) emanate from the Power Control System (PCS) indicated in Fig.III-1.1 as acting on the Thyristor Gating and Firing System (TGFS) which is presented in more detail in Fig. III-2.4; it comprises the above described electronic logic.

At this time it is assumed that the signals CS1 and CS2 arrive in recurrent sequence at times t_k, t_{k+1}, t_{k+2}, etc. to cause firing signals for the appropriately selected CR's if this selection has been completed by the above cited TGFS.

The electronic implementation of the above described logic procces which provide the electric signal ϕ i - j is indicated in simplified form in the schematic shown in Fig. III-2.3. Also shown there is the forming of the inverse of certain signals, such as $\overline{v1^{+}}$, $\overline{v1^{-}}$, $\overline{v^{2+}}$, $\overline{v^{2-}}$, $\overline{v^{3+}}$, $\overline{v^{3-}}$ and $\overline{\phi\ 1-2}$, $\overline{\phi\ 1-3}$, $\overline{\phi\ 2-3}$, $\overline{\phi\ 2-1}$, $\overline{\phi\ 3-1}$ and ϕ 3 - 2. These inverse signals ar being generated for purpose of convenience in the interface with the respective electronic control

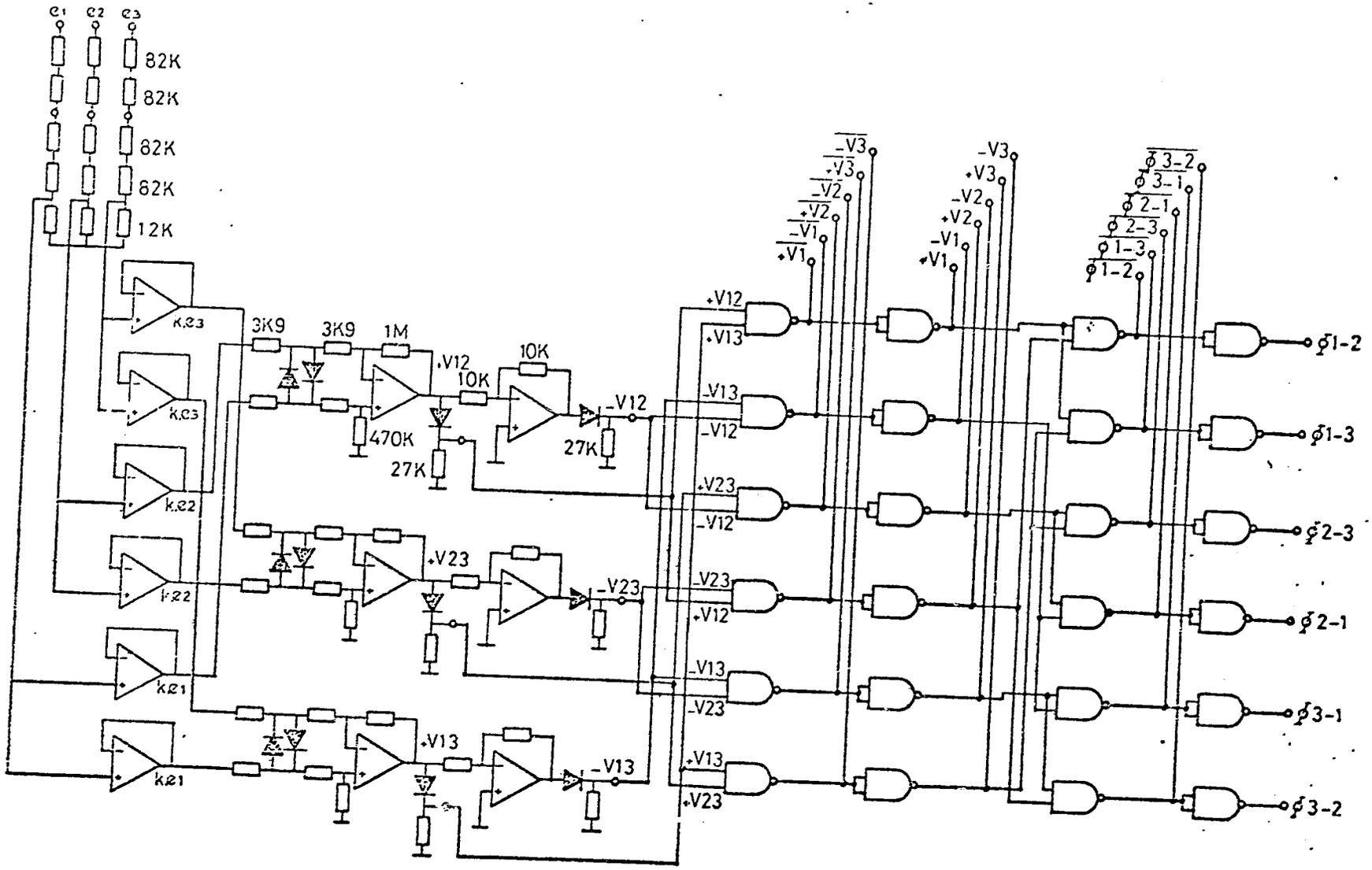


Fig. III - 2.3.

Simplified electronic schematic of the logic for the generation of selection signals for the thyristors of the three phase cyclo-converter.

circuits. The internationally agreed to electrical symbols were used in the preparation of Fig. III - 2.3.

III - 2.1.1. Selection of the Thyristors for Forward Power Transfer

The functions of the above referred to Gating and Firing Systems (GFS) are further described with reference to Fig.III-2.4. This figure indicates the functional logic diagram, for gating and firing of the thyristors which are associated with the first phase, namely thyristors CR1i (i=1,2,3,4) and all thyristors of the DU bridge, identified in Fig. III-1.1. One such GFS is associated with each of the three phases of the power supply systems. The other two logic schematics are obtained by changing all identifying numbers 1j (j=1,2,3,4) to 2j or 3j, respectively. The functional philosophy of the logic schematic depicted in Fig. III-2.4 which is now explained, is thus analogous to that of the other above referred to GFS. The broken line which encloses the logic schematic in Fig. III-2.4 is the boundary of the GFS.

The voltage discriminator DC11 has a negative signal output as long as:

(1) thyristor CR11 has a forward voltage drop from anode to cathode and thus could carry current, such as during its cycle of operation; this thyristor current is identified in Fig. III - 1.2(a) and more specifically in Fig. III - 1.2.(c); the location of CR11 is indicated in Fig. III - 1.1;

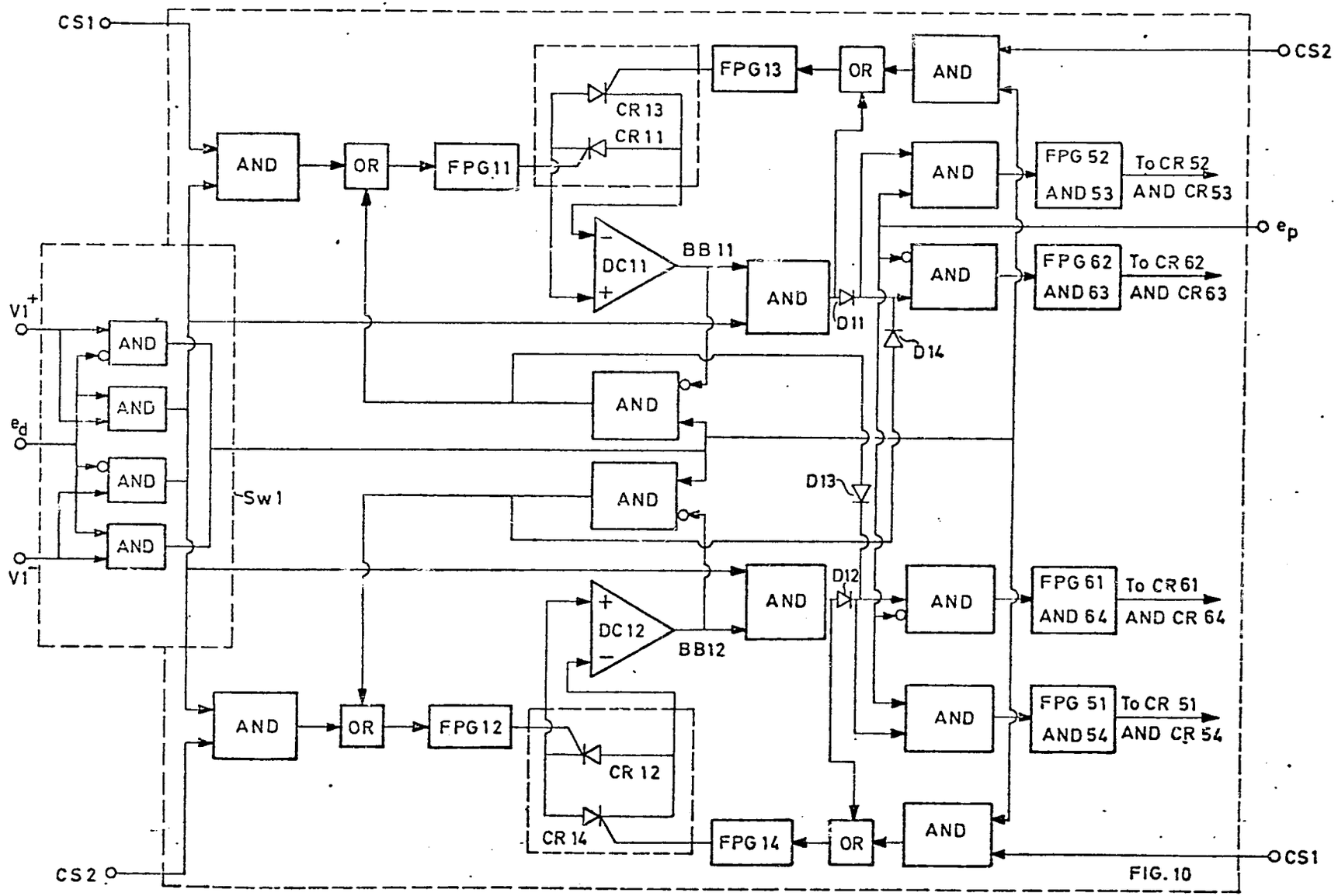


Fig. III - 2.4.

Functional schematic of one of the three Gating and Firing Systems

(2) The signals $v1^+$ and e_d are present or absent.

The same voltage discriminator DC11 has a positive signal output when:

(3) thyristor CR11 is back biased; this occurs whenever the "antiparallel" thyristor CR13 conducts the resonant current i_1 which follows in immediate sequence after termination of the current conduction cycle of CR11; this is shown in Figs. III - 1.2(a), (c) and (d);

(4) The signals $v1^+$ and e_d are present or absent.

Assume now: $e_d > 0$ for "forward" power transfer, $v1^+ > 0$ and $v1^- = 0$.

The AND gate which is energized by the positive outputs of DC11 and of $v1^+$ emits a positive signal which energizes the Firing Pulse Generator FPG13 by way of an OR gate, as shown. This FPG13 triggers thyristor CR13 into conduction in order to carry the current i_{CR13} indicated in Fig. III-1.2(d) and discussed above.

The analog of what was just described occurs with reference to the signals which govern thyristors CR12 and CR14. These four thyristors can be thought of as performing within the time interval governed by signal ϕ 1 - 2 (see Fig. III-2.1.) the "thyristor" and the "diode" functions of a full bridge dc converter [5]. The symbolic schematic of such a converter is shown in Fig. III - 2.5.

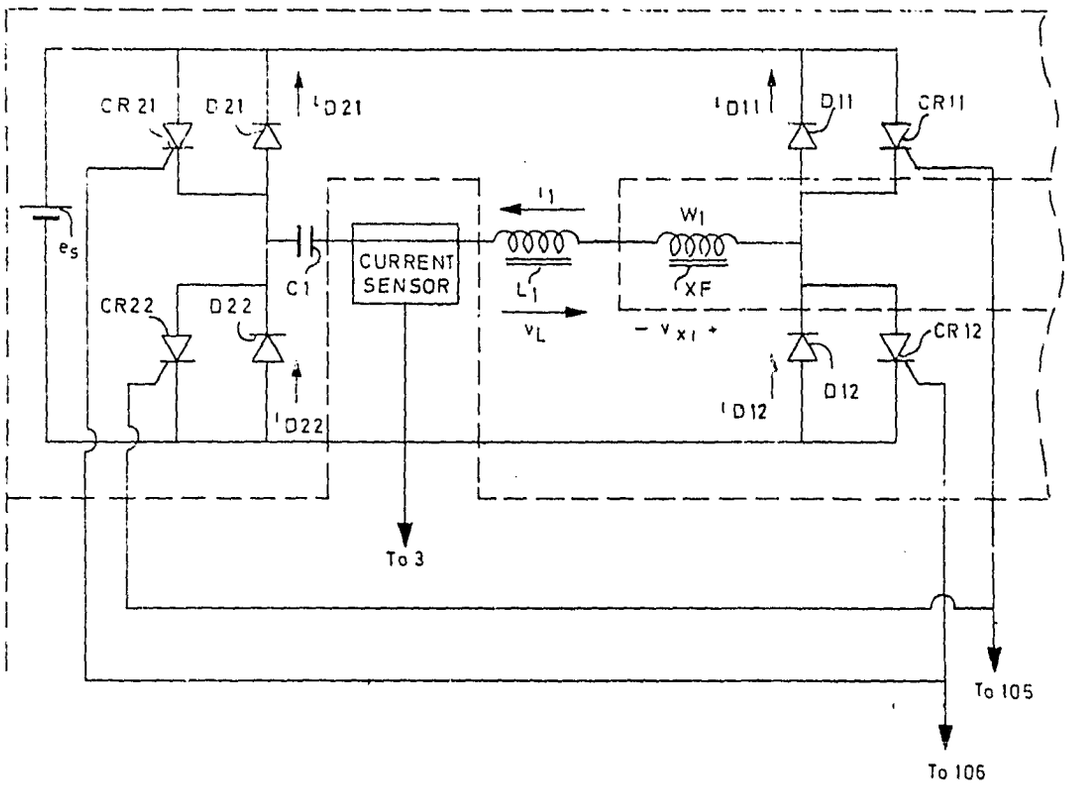


Fig. III - 2.5. Symbolic schematic of full bridge series capacitor inverter-converter.

The analogies of the functions of the thyristors CR1i (i=1,2,3,4), which are associated with phase 1 of the discussed three phase system, and the functions of the thyristors and diodes associated with the positive terminals of the voltage source e_s in Fig.III-2.5 are indicated by setting the corresponding symbols side by side in pairs: CR11 - CR11, CR13 - D11, CR12 - CR21, CR14 - D21.

It means that if a dc source with voltage e_s is connected between the first phase with voltage e_1 and the second phase with voltage e_2, indicated in Fig. III - 1.1, then the cyclo-up converter CU will operate as a full bridge dc

powered converter of the described type. The signal connections of the third phase should be grounded for that purpose as to not cause inappropriate interference with the signal flow process.

Returning to the description of the function of the GSF shown in Fig. III - 2.4: thyristor CR11 is fired by the FPG11 if the control signal CS1, the signal $v1^+$ and the signal e_d coincide. Likewise, is thyristor CR12 fired by the FPG12 if signals CS2, $v1^+$ and e_d coincide.

The firing mechanisms for all four thyristors CR1i (i=1,2,3,4) have been described for $v1^+ > 0$ and $e_d > 0$, corresponding to the condition when $e_1 > e_2$ and $e_1 > e_3$, as indicated in Fig. III-2.1 as the time interval $T1^+$.

Yet, e_1 undergoes the condition when $e_1 < e_2$ and $e_1 < e_3$ in the time interval $T1^-$, indicated in Fig. III-2.1 the signals $v1^- > 0$ and $v1^+ = 0$ in the named interval. If $e_d > 0$, and if control signal CS1 is injected through the connection shown in the lower right corner of Fig. III-2.5, then the operated on AND gate will emit a signal and fire CR14 through its FPG14. This thyristor CR14 has now the function of one of the thyristors in the lower half of the full bridge configuration of this system shown in Fig. III-2.5. Analogously does signal CS2 cause the firing of thyristor CR13, again, comparable to the function of one of the thyristors located in the lower half of the full bridge of Fig. III-2.5. A back bias condition exists in thyristors CR14 and CR13 after completion of their respective conduction cycles. Back bias detectors DC12 and

D11 will be energized accordingly in succession and at the individually appropriate times. Their outputs are now conveyed to the AND gates which are located in the center of Fig. III-2.4. These AND gates emit then signals in the presence of signal $v1^-$ and whenever the just named back bias signals BB12 and BB11 occur. The outputs of these AND gates reach in succession by way of OR gates FPG12 which fires CR12 and FPG11 which fires CR11.

If the terminals of a dc source with voltage e_s are connected to the phase pair with voltages e_1 and e_2 such that $e_1 < e_2$ and if the full bridge configuration of Fig. III-2.5 is observed, then analogies can be drawn by, again, setting side by side the switching elements of the three phase and of the dc system, whereby: CR14 - CR12, CR12 - D12, CR13 - CR22, CR11 - D22. The first named switching elements are those of the three phase system shown in Fig. III-1.1; the second named switching elements are those of the full bridge shown in Fig. III-2.5.

Operation of the thyristors which are associated with phases 2 and 3 is achieved in an analogous manner, as described above. The GFS for phase 2 is controlled by signal $v2^+$ for $e_2 > e_3$ and $e_2 > e_1$ and by signal $v2^-$ for $e_2 < e_1$ and $e_2 < e_3$. Furthermore, is $e_d > 0$ for forward transfer of power. Signals CS1 and CS2 enter this GFS in the same manner as above described for the GFS associated with the first phase. The thyristors of the three phase bridge which are being controlled by this GFS are CR2i (i=1,2,3,4). The analogy for the GFS associated with phase 3 is based on the analogous relabeling of input signals and thyristor numbers.

III - 2.1.2. Reconfiguration of the Three Phase Bridge for Reverse Power Transfer.

One of the intended properties of the described system is its capability for reverse power transfer, in this case, into the three phase network shown in Fig. III-1.1.

The thyristor matrix contained in the doublesided cyclo-converter CU then assumes the task of a gated three phase bridge whereby its thyristors perform exclusively "diode functions" when the appropriate polarity conditions in the three phase system prevail.

The objective is to pump a train of a finite number of unidirectional current pulses against the sine wave voltage e_n of the nth phase of the three phase voltage source so that this train is centered under each half sine wave as shown in Fig. III-2.6. These trains of finite numbers of pulses occur with alternating polarities as indicated in the same Fig. III-2.6. The indicated opposing polarities of current and voltage characterize the power transfer into the three phase system.

The trains of pulses, indicated in Fig. III-2.6(b) are the rectified half waves of the resonant current i_1 which is now being generated by the cyclo-converter bridge CD powered from a dc source. The matrix of thyristors CU demodulates and distributes this carrier to the appropriate phase pairs of the three phase

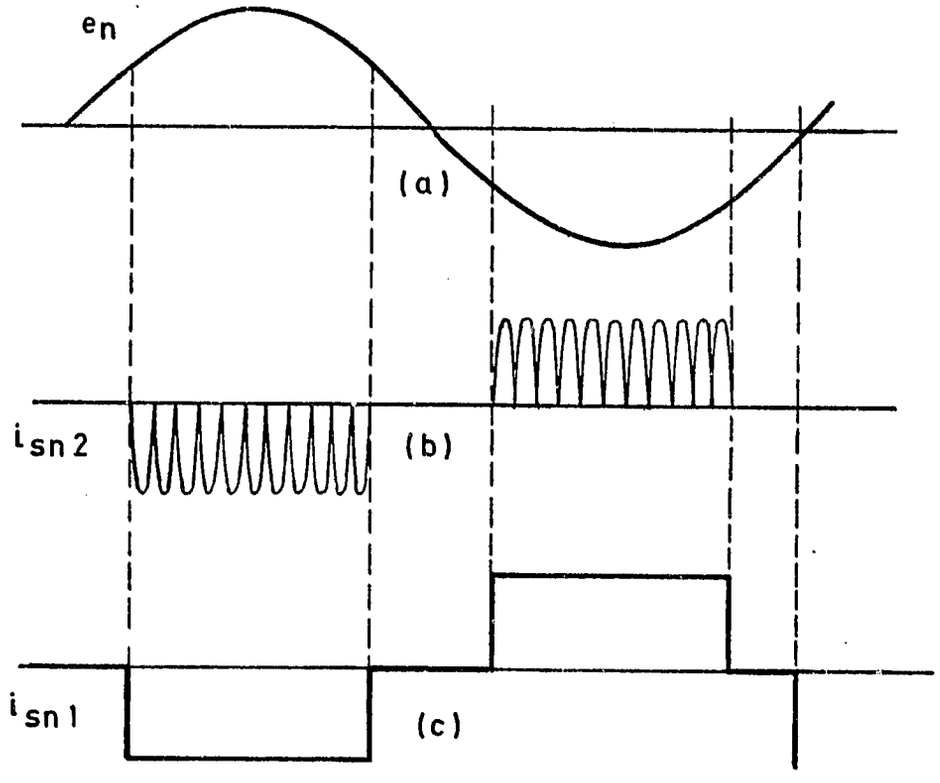


Fig. III - 2.6.

(a) Phase voltage e_n; (b) demodulated carrier current i_{sn2} and (c) filtered current i_{sn1}, during the transfer of electric energy to the three phase line.

system. This process is in essence the "reverse" of a three phase full wave rectification process.

Selection and gating of the appropriate thyristors is guided by the following philosophy:

The thyristors which oppose the prevailing voltage between two phases with the largest potential between them will conduct the resonant current against this potential.

This is illustrated for the time interval ϕ 1 - 2 defined in Fig. III - 2.1. In this interval is $e_1 > e_2$, $e_1 > e_3$ and $e_3 > e_2$; it means that current is pumped from phase 2 to phase 1 in order to comply with the above stated philosophy.

Thyristor pairs CR13 - CR22 and CR14 - CR21 conduct in alternating recurrent succession the halves of the resonant current i_1. Thyristors CR11,12,23 and 24 do not participate in this phase of power transfer.

The thyristor which perform this "reverse" transfer of electric energy are identified below for the individual time intervals ϕ i - j:

TABLE III - I

Pattern of Gating and Firing of Thyristors for Reverse Power Transfer

	Thyristors		
ϕ i - j	phase 1	phase 2	phase 3
1 - 2	13,14	22,21	-- --
1 - 3	13,14	-- --	32,31
2 - 3	-- --	23,24	32,31
2 - 1	12,11	23,24	
3 - 1	12,11		33,34
3 - 2		22,21	33,34

All twelve thyristors of the bridge CU are engaged in this process; however each thyristor pair carries one full half cycle of the resonant current i_1, rather than to share its conduction with its "antiparallel" companion as under conditions of forward power transfer.

The phase gating circuits which were described in the introductory part of subsection III-2.1 continue to perform their function for the conditions of reverse power flow. What is altered in order to achieve the thyristor selection pattern contained in Table III - I is the function of the thyristor Gating and Firing systems, the three GFS.

Signal $e_d < 0$ for the above stated purpose. This reversal of polarity reverses the effect of signals $v1^+$ and $v1^-$ on the selection process of the thyristors. It means that for $v1^+ > 0$ thyristors CR13 and CR14 are energized in succession in the presence of signals CS1 and CS2, respectively, rather than thyristors CR11 and CR12 as decribed before. Conversely will thyristors CR11 and CR12 be energized by the signals CSi (i=1,2) in succession when $v1^- > 0$.

No back bias occurs in this case because the concerned thyristors carry, exclusively, forward currents; they terminate their current conduction when no energy is left in the series inductor L because $i_1 = 0$ and when the voltage on capacitor C_1 opposes the voltage of the current accepting phases of the three phase system. Back bias of the concerned thyristors does, therefore, not occur and the antiparallel thyristors are not fired.

III - 2.1.3. Protective Suppression and Interlock of Signals.

The avoidance of occurrence of a direct path of conductance from line to line of the polyphase system is an imperative requirement to secure the functional integrity of the power system.

This topic is treated in the literature concerning dc converters of the discussed type |6|. It will be shown that the here described three phase power converter is in almost every respect nothing else than an expanded version of

the above referred to dc converters. The needed protective measures are, therefore discussed first with reference to the thyristor bridge DU, indicated in Fig. III - 1.1.

This bridge DU operates during conditions of "reverse" power flow as if it were working in a dc to dc converter. A dc source of electric energy with voltage e_s is connected instead of the load Z_L to this bridge; it processes the power "without knowing" that the thus generated resonant current carrier is distributed in three phases instead of being rectified to cause a dc output.

The functional schematic of the concerned protection system is indicated in Fig. III-2.7. The significant waveforms which are associated with this process are shown in Fig. III-2.8. Both figures are reproduced here from the literature for convenience [6].

A very brief description of the concerned process is entered here for completeness of presentation.

Reference is made to Fig. III-2.5 and more specifically to its series combination of thyristors CR11 and CR12 on the right hand side of this figure. It is intended to show that the electronic protection system which is contained in Fig. III-2.7 prevents simultaneous firing of thyristors CR11 and CR12. This philosophy can be extended to include the complementary series combination of thyristors CR21 and CR22 on the left hand side of the same bridge.

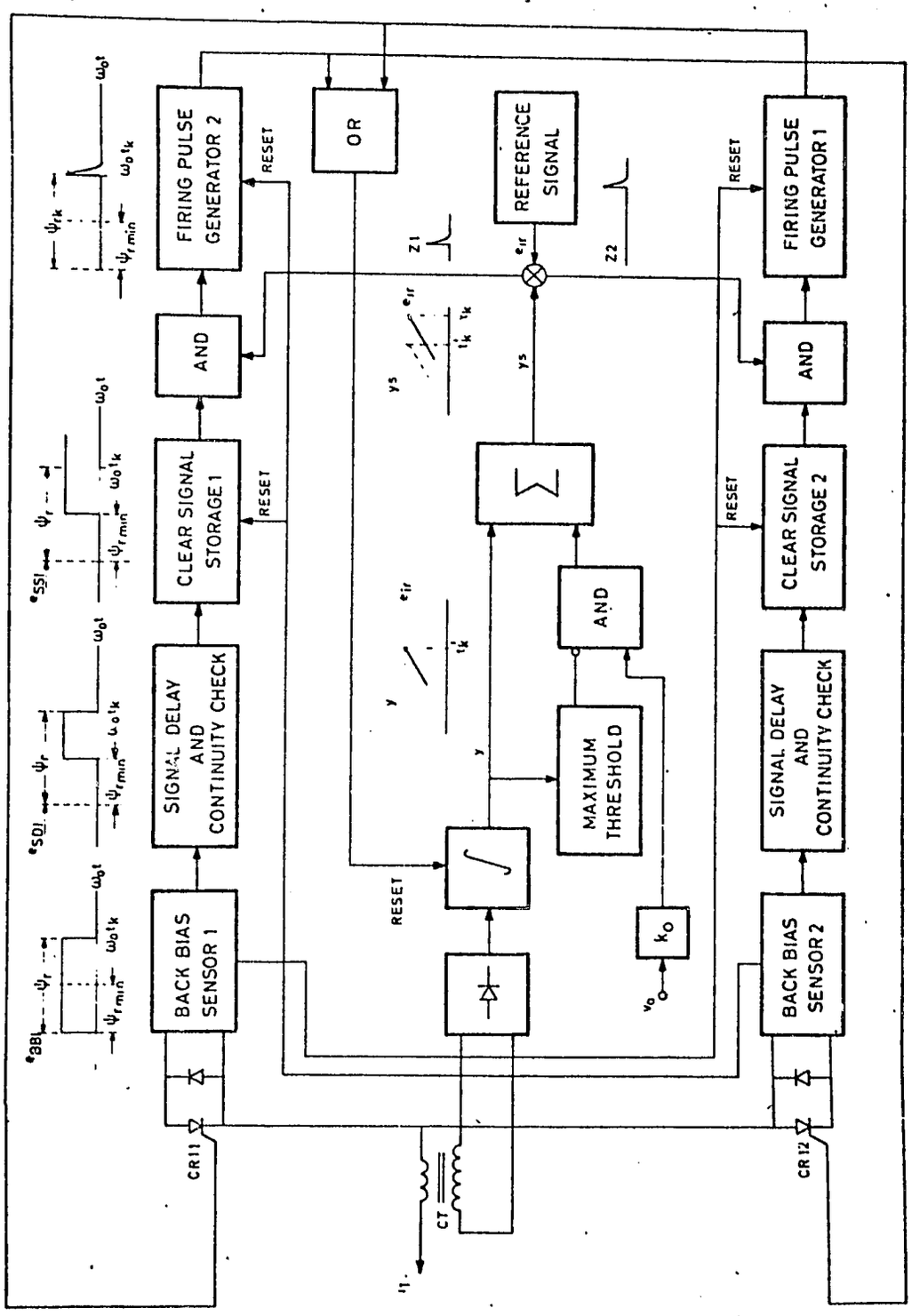


Fig. III - 2.7.

Functional schematic of the control and protection system.

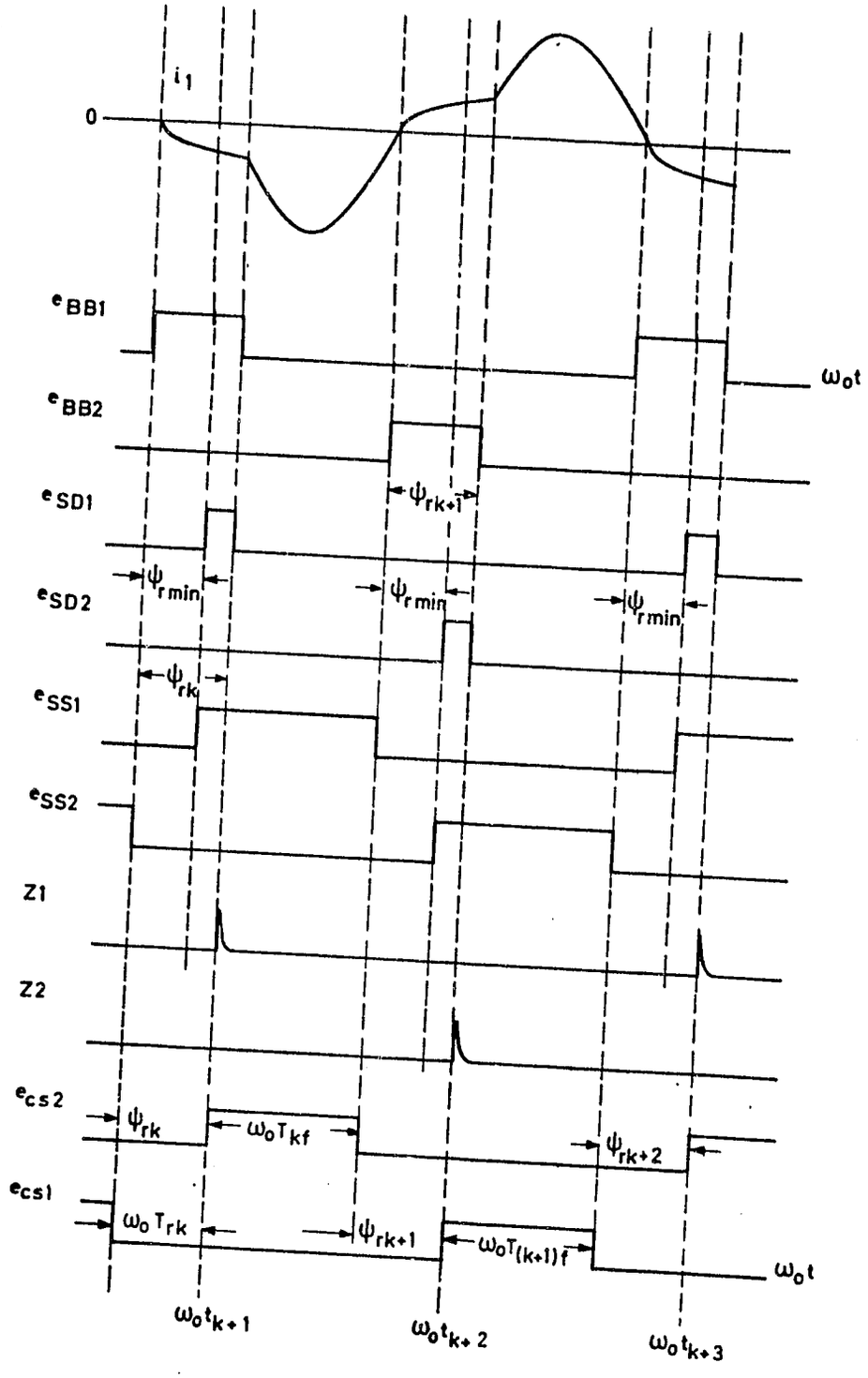


Fig. III - 2.8.

Significant signal waveforms of the protection system.

The electronic protection system prevents firing of thyristor CR1i (i=1,2) as long as the companion thyristor has not terminated its cycle of conduction and has regained its forward blocking capability.

A back bias signal appears on thyristor CR11 after completion of conduction of the resonant current in the normalized time interval $\omega_o T_{kf}$, of which T_{kf} is defined in Fig. III-1.2. The cause for appearance of this signal is the state of conduction of the "antiparallel" diode D11 which now conducts the current i_1 for the normalized time interval $\psi_{rk} \geq \psi_{r\ min}$. The length of this time interval is not yet known at $t = t_k + T_{kf}$. The Back Bias Sensor 1 establishes the fact of the existence of a back bias condition and conveys this information in the form of a 0 - 1 signal e_{BB1} to the Signal Delay and Continuity Check block; this block emits a signal e_{sD1} if, and only if the signal e_{BB1} has persisted without interruption for a normalized interval $\psi_{r\ min} = \omega_o t_{off}$. Signal e_{sD1} energizes the Clear Signal Storage 1, which stored the received information "indefinitely" until such time when a reset signal is applied to it. The above referred to clear signal appears at the time $\psi_{r\ min}$ and energizes one input port of the following AND circuit. Thyristor CR12 is now free to be triggered at the option of the electronic control system.

A signal Z1 which emanates from the electronic control system appears at the second port of the above referred to AND gate when

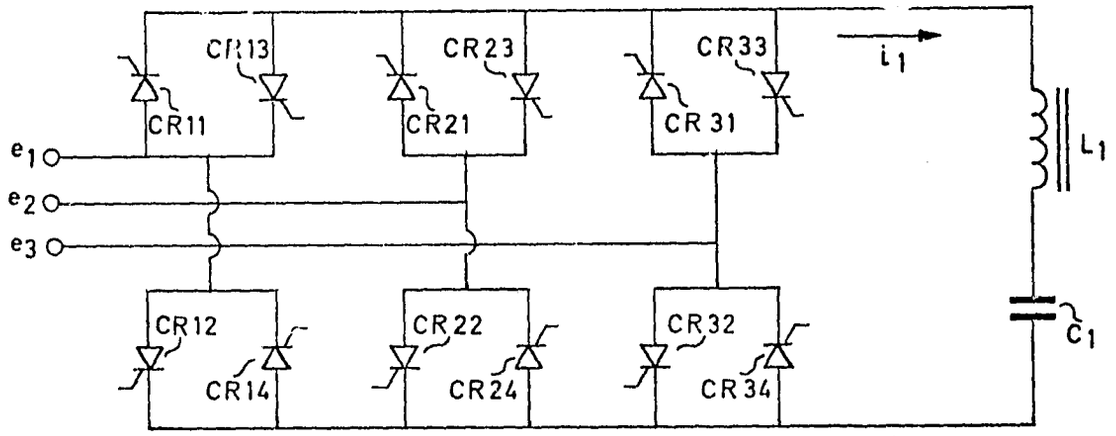
$$\beta = \beta_{k+1} - \psi_{rk} = \omega_o t_{k+1} - \omega_o T_{kr}; \qquad (11)$$

the origin of this signal Z1 will be explained in the description of the control system in section III - 3.

Coincidence of signals e_{sD1} and Z1 at the AND port energizes the Firing Pulse Generator 2 which then fires thyristor CR12; this thyristor conducts the resonant current i_1 until $i_1 = 0$; diode D12 then continues conduction of the resonant current. The ensuing back bias condition of thyristor CR12 is detected by the Back Bias Sensor 2. Signal processing, which is analogous to the explained processing of signal e_{BB1} ensues and thyristor CR11 is, eventually, fired.

It is stressed that the protection system acts completely independent from the control system in its approval for access of the firing signals of the control system to the respective gates.

Thyristor firing signal protection was, so far, discussed for a two terminal dc source of electric energy. If the source voltage e_s were to reverse its polarity and if a resonant current carrier i_1 should be derived from it, then the roles of diodes and thyristors must be interchanged. Let the polarity of



PHASE VOLTAGES OPERATING PHASES			$e_1 > e_2$ 1 – 2	$e_1 > e_3$ 1 – 3	$e_2 > e_3$ 2 – 3	$e_2 > e_1$ 2 – 1	$e_3 > e_1$ 3 – 1	$e_3 > e_2$ 3 – 2
THYRISTOR PAIRS CR	$i_1 > 0$	FWD	11, 24	11, 34	21, 34	21, 14	31, 14	31, 24
		REV	14, 21	14, 31	24, 31	24, 11	34, 11	34, 21
	$i_1 < 0$	FWD	13, 22	13, 32	23, 32	23, 12	33, 12	33, 22
		REV	12, 23	12, 33	22, 33	22, 13	32, 13	32, 23

Fig. III - 2.9.

The thyristors of the three phase bridge and their functions.

e_s be reversed in Fig. III-2.5. Diodes D11 and D12 would short circuit the source; the same applies for diodes D21 and D22. All these diodes must be replaced by thyristors which must be gated accordingly. These "new" thyristors assume the role of thyristors, as discussed above for the dc system and the former thyristors assume the role of "diodes".

The thyristors of the doublesided cyclo-converter associated with the three phase system are shown in Fig. III-2.9. The series resonant circuit consisting of the inductor L_1 and the capacitor C_1 is "short circuited" in the sense that not other thyristor bridge and load is shown; this is avoided for purpose of simplicity of presentation of a system which can be short circuited. The functional aspects of the dc bridge are treated in subsection III-2.2. The indices ij of the thyristors CR_{ij} are shown below the schematic to indicate which thyristors conduct for the given specific conditions of forward (FWD) and reverse (REV) power transfer.

The protection philosophy for this sytem is in essence the same as the one applied for the dc systems. Yet, there are now three instead of two source terminals with the thereto connected thyristors involved.

First, only phases 1 and 2 are considered; assumed is, furthermore that $e_1 > e_2$. The function of the thyristor bridge associated with these two phases is then identical with that of the full bridge configuration of the dc converter shown in Fig. III-2.5. This was explained in subsection III-2.1.

The protection system as explained with reference to Figs. III - 2.7 and 2.8 would suffice for this purpose if this mechanisms were to be expanded to process concurrently the signals which fire the thyristors that conduct the current at the same cycle intervals. This could be true, as long as only two phases are in operation as assumed here. This holds true even if the polarity of phases 1 and 2 are reversed, as explained in III - 2.1.1.

Yet, if $e_3 < e_2$ then phase 1 forms a full bridge with phase 3. It means that all back bias signals emanating from the thyristor of phase 1 have to be interpreted now by the electronics which protects phase 3. The protection requirements require a more complex interpretation to prevent that any thyristor of one phase should not cause a short circuit with any thyristor of another phase.

A visual inspection of Fig. III-2.9 reveals the following requirements to clear any thyristor for firing by

(a) establishing with which thyristors it could form a short circuit between phases, for given phase voltage conditions ϕ i - j, as identified with reference to Fig. III-2.1;

(b) suppression of unnecessary, and thus interfering signals;

(c) positive identification of those signals that are required to clear the respective firing channel.

The results of the above enumerated requirements are summarized in Table III-II. This table shows which thyristor's back bias condition is required to fire any thyristor within the time interval ϕ i - j when certain phase voltage relations prevail. The same table shows which back bias signal is being eliminated by the existence of the ϕ i - j signal. Comparison of the rows ϕ 1 - 2 and ϕ 1 - 3 confirms that the non-active phase is being eliminated when two other phases are engaged in power transfer, that is, phase 3 when ϕ 1 - 2 prevails and phase 2 when ϕ 1 - 3 prevails. The "antiparallel" thyristor of those which are fired are cleared by signal $v1^{+-}$ to perform their "diode" function whenever required. No back bias is needed in this case, since the cathodes of the respective thyristors oppose a positive phase voltage in the concerned time intervals.

The "thyristors" of the dc bridge are also identified by their numbers, CR5k (k=1,2,3,4). However, diodes D5k are being used instead, because the intended voltage over output filter capacitor C_o has only one polarity for either direction of power transfer.

These same "diode" function performing thyristors of columns five and six in Table III - II are also cleared for the process of reverse transfer of power to the three phase system. All thyristor functions, indicated in columns two through four are eliminated under these conditions. The conditions of columns eight and nine remain unchanged. Added are the common thyristor functions of CR6k (k=1,2,3,4) for purpose of conventional dc operation of this type of converter |1,2,6|.

TABLE III - II

Gating Conditions for the three phase cyclo-converter

ϕ i - j	Back Bias on	Controls Thyristor	ϕ i - j Eliminates	vi^{+-} Clears (ac)		vi^{+-}	vi^{+-} Clears (dc)	
1-2	12 *	24	34	21	22	$v2^-$	51 **	53
	11	23	33	13	14	$v1^+$	52	54
1-3	11	33	23	13	14	$v1^+$	52	54
	12	34	24	31	32	$v3^-$	51	53
2-3	22	34	14	31	32	$v3^-$	51	53
	21	33	13	23	24	$v2^+$	52	54
2-1	21	13	33	23	24	$v2^+$	52	54
	22	14	34	11	12	$v1^-$	51	53
3-1	32	14	24	11	12	$v1^-$	51	53
	31	13	23	33	34	$v3^+$	52	54
3-2	31	23	13	33	34	$v3^+$	52	54
	32	24	14	21	22	$v2^-$	51	53

* Indices of thyristors CRij

** Diodes D5k (k=1,2,3,4) are used for purpose of this project.

III - 2.2. The DC Cyclo-Converter

The dc bridge of this converter operates as described in the literature for conditions of "reverse" power flow, meaning out of a dc source connected across the filter capacitor C_o |1,2,6|. Thyristors CR6k (k=1,2,3,4) then perform the thyristor functions within a full bridge configuration. The thyristors CR5i (i=1,2,3,4) act as diodes, if appropriately energized; they perform this diode action for both direction of power transfer since $v_o > 0$ for either direction and thus no precautions are required.

III - 2.2.1. Organization of Power Flow

The Gating and Firing System for the thyristors of the three phase bridge as shown in the functional schematic of Fig. III-2.4 was discussed with reference to that figure. The back bias sensor DC11 triggers thyristor CR13 upon receipt of a back bias signal and in the presence of the gating signal $v1^+$. Yet, it also triggers the thyristor pair CR52 and CR53 or the thyristor pair CR62 and CR63, depending upon the polarity of a control signal $e_p \lesseqgtr 0$ which is externally imposed on the system.

One pair of the same thyristors is also energized if CR11 is being back biased in the presence of the gating signal $v1^-$, as indicated in Fig. III - 2.4; the selection between the pairs CR52 - CR53 or CR62 - CR63 depends, again on the polarity of the external signal $e_p \lesseqgtr 0$.

The firing pattern of the thyristor pairs in the dc bridge CD for purpose of power transfer to a dc load is summarized in Table III-III; this pattern, as presented, is governed by the externally impressed signal $e_p \lesseqgtr 0$. Signal e_p determines the polarity of the output voltage v_o; it does this by selecting which of the two "antiparallel" sets of thyristors of the dc bridge is fired for "forward" transfer of energy.

TABLE III - III

Firing Conditions for the Doublesided DC Cyclo-Converter for Power Transfer to a DC Load.

Gating signals		Fired Thyristor Pairs CR				
$V_o \lesseqgtr 0$	$v1^{+-}$	51 - 54	52 - 53	61 - 64	62 - 63	
$e_p > 0$	$v1^{+} > 0$	12	11	--	--	Caused by Back Bias on Thyristor CR
	$v1^{-} > 0$	13	14	--	--	
$e_p < 0$	$v1^{+} > 0$	--	--	12	11	
	$v1^{-} < 0$	--	--	13	14	

The firing pattern as contained in Table III - III indicates the requirements for "forward" power transfer resulting from an inspection of Fig. III-1.1 which are "implemented" by the logic schematic shown in Fig. III - 2.4.

These requirements can be reinforced with a further study of the significant current waveforms shown in Figs. III- 2.1 and 2.8 in conjunction with the converter schematic of Fig. III-1.1. The respective thyristor pairs of the dc bridge transfer conduction of current to each other whenever the resonant current i_1 changes the direction of flow; this occurs when the voltage v_{c1} on the series capacitor C_1 reaches its crest and thus causes a reversal of this current. This in turn requires firing of the respective pair of thyristors in the three phase bridge which then perform a "diode" function.

The respective thrysistor pair in the dc bridge is then fired, based on the information that the formerly conducting "thyristors" in the three phase bridge are back biased because of the current flow through their antiparallel "diode" function performing thyristors.

III - 2.2.2. Reconfiguration of the DC Bridge for Reverse Power Transfer

Operation of the dc thyristor bridge DU for purpose of generating the modulated resonant current carrier i_1 is amply described in the literature [4,5,6], to which is referred here for purpose of detailed explanation; study of this

process is also facilated by the discussions with reference to Figs.III-1.1., 1.2., 2.5., 2.7. and 2.8. "Reverse" transfer of power, from the dc system to the three phase system is implemented in this case; the three phase thyristor bridge then functions as a gated "diode" bridge, as also identified in the discussion with reference to Table III - II.

The signal e_d controls the configuration of the three phase bridge for "forward" or "reverse" power flow as explained in III - 2.1.2.
This signal acts on the three Gating and Firing Systems which are explained with reference to Fig. III-2.4 so that $e_d > 0$ causes "forward" and $e_d < 0$ "reverse" power transfer. This is implemented by arranging the firing sequence of the thyristors in such a manner that they perform the function of the resonant current carrier generation for "forward" transmission of power as explained in III - 2.1.1. This requires careful gating and positively ascertained turn-off of the forward biased thyristors. No such precautions are needed for "reverse" power transfer in which the energized thyristors are always in a back biased condition, when non-conducting; careful surveillance of their state of conduction or recovery from conductions is, therefore, not required.

The same signal e_d is being used to govern the "forward" or the "reverse" of power by the dc bridge; it then acts on the firing logic in an analogous manner as the one which was explained for the three phase bridge. This process of reconfiguration of the firing logic of the dc bridge is, therefore, not further treated here as being an analog application of a known process |4,5,6|.

III - 3. Control System Characteristics

Objective of control is to:

(a) stabilize the average value V_o of the output voltage v_o of the converter independent of variations of the line voltage variations and of the load, both within design limits;

(b) remove the voltage ripple effect which stems from the rectification of a three phase line so that the normalized ripple

$$v_{rn\ rms} \simeq v_{s1\ rms}/e_{s\ av}\ a_{F1} = v_{r1\ rms}/V_o \qquad (12)$$

where

$v_{s1\ rms}$ = the rms value of the first harmonic coefficient of e_s;

e_s = the apparent voltage waveform "seen" by the totality of thyristors of the three phase bridge during the intervals when they are energized; it is the equivalent of the output voltage of a full wave bridge rectifier;

$v_{r1\ rms} \simeq v_{rpp}/2\sqrt{2}$;

v_{rpp} = peak to peak ripple of the output voltage $v_o \simeq V_o + v_{r1}$;

a_{F1} = the attenuation of the first harmonic conponent of e_s

which is due to a deterministic modulation process of the resonant current carrier i_1.

(c) limit the output current i_o of the converter to a maximum value

$$i_{o\ max} \leq i_{o\ limit} \tag{13}$$

for conditions of overload, which includes short circuited output terminals.

Conditions (a) and (b) are met by a control system which employs the Analog Signal to Discrete Time Interval Converter (ASDTIC) |1,2,3|. Condition (c) is satisfied when the ASDTIC system is incorporated in the improved series capacitor inverter-converter |4,5,6|. Only the basic reference material is quoted here, which does not include the use of ASDTIC for the development of the ion engine power processor and the many recently publicated industrial applications.

Laboratory studies have confirmed that the effect caused by the addition of a sine wave voltage ripple

$$v_{s1} \sin \omega_s t$$

to the dc input voltage E_s, which would affect the system output voltage v_o, can be reduced by a modern version of ASDTIC.

The observed attenuation factor a_{Fl} of the harmonic component with amplitude v_{sl} was

$$a_{Fl} = \frac{v_{sl}/E_s}{v_{rl}/V_o} \simeq (f_F/f_s)/\pi \tag{14}$$

for

$$v_{sl}/E_s = (0)\ 10^{-1} \tag{15}$$

where

$\omega_s = 2\pi f_s$, the radial frequency of the sinusoidal disturbance of the source voltage;

$f_F = 2f_i$, the pulse (filter) frequency of the carrier i_l which is the twofold of the inverter frequency

(0) = "the order of"

Equation (14) is explained in reference 1 and moreso in the therero pertaining reference material. Its mathematical symbolism can be expressed in words:

Each harmonic component which is contained in a source voltage signal is reduced by a factor

$$a_{Fm} \simeq N/\pi n \tag{16}$$

when this source voltage signal is being processed by an ASDTIC controlled system. The factor

N/n = the number of pulses of the power processing system per period of the concerned harmonic component.

In the case of equation (14) is

$$f_F/f_s = N/1 \tag{17}$$

because only the first harmonic is being considered. Consideration of the first harmonic is general practice since it is the most significant contributor to the output voltage ripple.

The first harmonic component of a rectifier voltage which emanates from a three phase source has an rms value of approximately

$$v_{s1\ rms} \simeq 4\ 10^{-2}\ e_{s\ av} = 4\ 10^{-2}\ e_{n\ rms}\ 3\sqrt{6}/\pi \tag{18}$$

where

$$a_{Fm} \simeq N/\pi n \tag{16}$$

when this source voltage signal is being processed by an ASDTIC controlled system. The factor

N/n = the number of pulses of the power processing system per period of the concerned harmonic component.

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The first harmonic component of a rectifier voltage which emanates from a three phase source has an rms value of approximately

$$v_{s1\ rms} \simeq 4\ 10^{-2}\ e_{s\ av} = 4\ 10^{-2}\ e_{n\ rms}\ 3\sqrt{6}/\pi \tag{18}$$

where

The excellent dynamic properties of ASDTIC controlled systems have been described in the literature [3]. The modern version of ASDTIC controlling the series converter has been tested, so far, only in experimental systems. Yet, it appears on the basis of these tests that the reported dynamic properties of ASDTIC controlled systems, can be approached by control of a resonant circuit system.

III - 4. Experimental Verification of Key Circuit Elements

The preceding part of the presentation was based on the expectation that certain key features of the three phase ac/dc converter could be reconciled with the known characteristics of the referred to type of dc converters [4,5,6]. It appeared necessary to perform experiments to verify this expectation and to identify any aspects that would indicate a deviation from this expectation.

An experimental investigation was carried out to verify the feasibility and applicability demonstration and verification for the purpose of correlation with the preceding theoretical predictions.

The critical aspects which distinguish the here presented BDQ4 ac/dc converter from its predecessor, the above referred to dc converter of this type, are identified below. The following functional properties of the breadboard were characterized in order to demonstrate the feasibility and applicability of the key circuit elements and of the converter system as a whole, meaning that it:

1. can extract dc power from a 117/208 VAC three phase supply line without the use of a conventional rectifier filter system with a cut off frequency well below six times the single phase frequency;
2. can transfer electric energy from a dc source to a 117/208 three phase ac line without the use of line frequency output filters;

3. causes a high power factor in excess of 0.85 when the dc load is varied over a 3:1 ratio or when transferring power from a dc source to the ac system;

4. is capable of decreasing the effects of the conventional six pulse ripple of approximately 4 percent rms of an apparantly rectified three phase supply line by virtue of the internal modulation (ASDTIC) process of the converter; a response time in the order of 0.1 msec is needed for this purpose;

5. conforms to the expectation of regulation capability which is comparable to that of dc converters, employing series resonant circuits, with a deviation in the order of $\pm$ 1 percent from a nominal dc output voltage;

6. holds the promise to operate with an efficiency which is comparable to that of dc converters of the same type, thus well in excess of 90 percent.

III - 4.1. The Experimental Material

The breadboard of a converter was constructed, as described with reference to Fig. III-1.1 of this presentation (III) and in section II - 5.

Exception is taken concerning:

(a) Diodes $D5_i$ (i = 1,2,3,4) which were used instead of the thyristors $CR5_i$ shown in Fig. III-1.1, since verification of inversion of the polarity of the output voltage v_o is outside the scope of this work;

(b) The introduction of a signal e_p for purpose of the above referred to inversion of the polarity of v_o, consistent with the explanation given in (a) above.

Design and construction of the power circuit followed closely the presentations of ch. 11. Organization of the control and protection system follows the explanations given in both, the CFR and CVR. Certain detailed aspects will be highlighted in the context of the verification of specific functions.

Power was derived from:

(c) A variable three phase power transformer for utility line frequencies with an 117/208 VAC output voltage for forward power transmission;

(d) Two regulated Sorensen 200 VDC, 15A dc power supplies, in series connection, for reverse power transmission.

A passive load in the form of a bank of resistors was used as a dc load.

The three phase utility distribution network was used as the "load" when fed via the power transformer identified in (c) for demonstration of "reverse" power transmission.

Three wattmeters with an bandwidth of 100 kHz (Marek, Bremen) were used to measure: (1) the ac power in both directions, respectivly;

(2) the rms content of the three individual line currents, and (3) the rms value of the three individual line voltages. A fourth wattmeter of the same type was used to varify the product of the volt-ampere readings at the dc port of the system.

Finally a Tektronix dual beam scope equipped with differential input amplifiers was used to observe the concerned voltage and current waveforms.

III - 4.2. Forward Power Transmission

Throughout the presentations made in the chapters II and III it was assumed that the series resonant circuit consisting of L_1 and C_1 should behave as if it were working within an ordinary dc converter with an input voltage e_s which contains a ripple e_{rr} as identified and explained with reference to Fig. III - 1.3. Selection of the thyristors for this purpose is described in subsection III - 2.1.1.

The transfer of the resonant current carrier i_1 from one pair of phases, such as phases with voltages e_1 to e_2 at the transition of the time intervals $T1^+$ to $T2^+$, identified in figure III - 2.1, proved to be one of the most difficult technological problems of the presented system.

The difficulty arises because of the asynchronism between the above referred to ripple e_{rr} of e_s and of the non-linear oscillation

of the resonant current carrier i_1. It means that the moment of transition of deriving power from phase 2, following the same function of phase 1, can happen at any angle of the 10 kHz oscillation of i_1. The resonant carrier i_1 must then be free to be solely governed by its control system. The function of the here used ASDTIC type control system was explained with reference to Fig. II - 4.11. It is necessary that the described control function should not be affected by the above referred to phase transition process in order that the source voltage ripple suppression, described in subsection II - 5.1, is achieved.

The above referred to difficulty did arise when the above referred to moment of transition occurred within the time interval T_{kr} of "diode" current conduction of an "antiparallel" thyristor CR13 or CR14 associated with the first phase. The opposite "thyristor" of the same phase, CR12 or CR11 were then cleared to fire the next half cycle of the resonant current carrier i_1, consistent with the protection philosophy explained with reference to Fig. III - 2.7. However, that firing signal for thyristors CR11 or CR12 never came because the control logic of Figs. III - 2.1 and III - 2.3 had by then transferred the "thyristor" functions to thyristors CR21 and CR22 of the second phase. Firing signals were sent to these thyristors, but blocked by the respective protection systems, described with reference to Fig. III - 2.4.

To summarize: When the transition from the time interval $T1^+$ to $T2^+$ fell within the interval T_{kr}, the "diode" current, then the thyris-

tors which were cleared for firing, could not receive a firing signal since the thyristors of another phase were meant to carry the current. Yet these thyristors of the other phase could not be fired because the protection system did not recognize the clearing signals that were meant for the previously functioning set of thyristors.

The above described process was compounded by the 20 kHz "noise" on the input filter capacitors C_{12}, C_{13} and C_{23}, which is caused by the converter operation and is superimposed on the sine waves of the e_i (i = 1,2,3). This noise pentrates into the control logic of the thyristor gating and firing system of figures III - 2.1 and 2.3 and causes vacillations in the direction of the firing signals, thus interfering and destroying the clearing process for the firing of these thyristors.

The above described problem led to sporadic interruptions of the converter operation with a frequency of approximately one in four transitions or 1½ times the single line frequency. These frequent interruptions of converter operations were entirely unacceptable, even though the system would automatically resume operation within one or two milliseconds.

An electronic interlock system was devised to prevent a change in the state of the output of the control logic of the thyristor gating and firing system of figures III - 2.1. and III - 2.3 during any of the time

intervals T_{kr}. It follows that as soon as a thyristor firing clearing process has begun, the transition of ac phases has to wait until the thyristor, whose firing is being cleared, has fired. The change of phases occurs thereafter, before the next thyristor firing clearing process is initiated.

One specific example of the difficulties of control electronics development was described above. The control system as a whole had to be tightened up considerably as compared to the simple dc to dc converter, requiring many more precautionary interlock measures for the firing of 16 thyristors to perform their time varying functions in association with a three phase ac system.

The power output circuit is identical with that of an ordinary dc converter of this type with inclusion of a diode rectifier bridge |4,5,6|.

III - 4.3. Reverse Power Transmission

Feeding of the power, emanating from a dc source of energy into the three phase network is achieved by application of the functional philosophy as described in the preceding subsection III - 2.1.2; the "mechanization" of this philosophy is summarized in Table III - I of the same subsection. The there identified thyristors are energized in the indicated polarity conditions of the three phase ac system; they act,

accordingly, as gated "diodes" which operate against an opposed positive polarity.

The protection electronics was implemented so that each of the above referred to thyristors of the three phase bridge would be fired, simultaneously with the thyristors $CR6_i$ (i = 1,2,3,4) of the "dc bridge" of the figure III - 1.1. This "dc bridge" is being operated in accordance with the functional philosophy of common dc converters of this type |4,5,6|.

The thyristors of the three phase bridge are divided into two groups: one which can conduct current in the same direction as thyristors CR61 and CR64, namely thyristors CR11, CR21, CR31, CR14, CR24 and CR34, and another group which can conduct the current in the same direction as thyristors CR62 and CR63, consisting of thyristors CR12, CR22, CR32, CR13, CR23 and CR33 of the three phase bridge.

The "dc bridge" is then operated in the conventional manner and transfers energy via the LC circuit and the thereto selected thyristors of the three phase bridge in the above described manner from the source of dc energy to the three phase system. The dc source of energy is now connected in the place of the former load Z_L, as indicated in Fig. III - 1.1.

The foremost difficulty which arose in this context, was the starting process of the thyristor firing sequence.

Firing of the thyristors in the three phase bridge, which perform now gated "diode" functions only, does not require a preceding back bias condition of another thyristor of the same bridge for purpose of clearance of the concerned firing signal. The protection mechanism, as explained with reference to figure III - 2.1 had to be expanded for the purpose of reverse power transfer. The thyristors identified in Table III - I are cleared for firing solely on the basis of the therein indicated polarity of the respective lines of the three phase system. The firing signals must be generated by a starter system at a time when the system is at stand-still and it is desired to initiate operation.

III - 4.4. Test Results

The converter was first applied for forward ac to dc transmission and control of power. The output voltage

$$v_o \simeq 215 \text{ VDC} \tag{22}$$

was chosen, consistent with (5.4) of ch. II. A maximum output current

$$i_{o\,max} \simeq 16 \text{ A} \tag{23}$$

was obtained accordingly in order to achieve the required operation in excess of three KVA.

The single phase input voltages were varied in the range

$$105 < e_i < 129 \quad \text{VAC rms} \tag{24}$$

The nominal value of the resistor load bank was established as

$$R_{L\ nom} \approx 13{,}4 \text{ ohm} \tag{25}$$

The load R_L, expressed in the normalized form

$$R_{Ln} = R_L / R_{L\ nom} \tag{26}$$

was varied over the range of

$$0 < R_{Ln} < 5 \tag{27}$$

The data which were observed at the significant points of the range indicated by (24) and (27) are tabulated in tables III- IV and V. The other data indicate a monotonic behavior between the listed points. The variable three phase transformers were adjusted as to yield almost completely balanced voltages. The concerned power and VA readings were sufficiently near as to be listed as one representative set of data per phase.

The data for forward power transmission are listed in Table III - I, those for reverse power transmission appear in Table III -V; only summary data were acquired for the purpose of reverse power transmission. The characteristics of critical significance appeared to be associated with the forward transmission of power, being the more complex of the two modes of operation. It is for this reason that the data for the indicated mode are, substantially, more elaborate, than the one for reverse power transfer.

The curve trace of the resonant current carrier for the case of forward power transmission is shown for different time scales in Fig. III-4.1(a) through (e). Shown is the output signal of a 1000:1 current transformer, terminated by a 68 ohm resistor. The resulting transformation ratio is 14.7 A/div for 100 mV/div sensitivity of the input amplifier of the oscilloscope, using a conventional 10:1 attenuation probe. The above described source of the resonant current signal is part of the control electronics, used in the described system. The photographs of the curve traces shown in Fig.III-4.1 were taken for the condition of progressive overload, for V_o = 110 VDC and for e_i = 117 VAC.

The curve trace in Fig. III- 4.1(a) shows the characteristic waveform of the current i_1 for the above described conditions. The control angle ψ_r which controls the average $|i_1|_{av}$ of the absolute value of i_1, is discernibly larger than $\psi_{r\ min} \simeq \pi/4$ in order to accommodate the above described overloading condition of the system |4,5|. The current i_1 shows a peak value $I_a \simeq 33$ Amperes for the purpose of providing an $|i_1|_{av}$ = 16.1 A_{av}, as listed in Table III- IV. The resonant circuit with a natural frequency f_o = 12 kHz is excited with a lower frequency $f_i \simeq$ kHz so that above indicated firing angle ψ_r can form. The needed higher apparent impedance of the now appreciable mismatch between the exciting frequency f_i and that of the resonant circuit is thus created.

Fig. III - 4.1(b) shows the trace of the same current i_1, under the same conditions of operation, but at the substantially larger time scale of 200 μsec./div. A careful examination of this trace, indicates a slight variation in amplitude of i_1.

TABLE III - IV

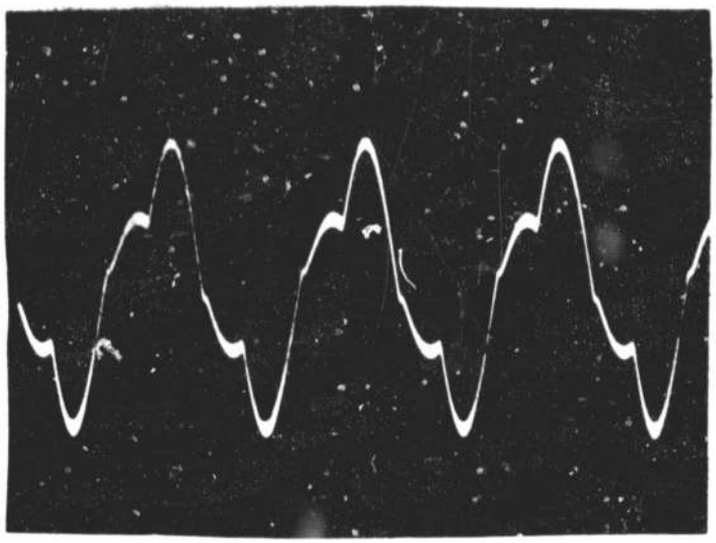
Characterization of Forward Power Transmission

e_i V_{rms}	i_{si} A_{rms}	P_i/ph Watt	VA/ph	P_i Watt	VA	p.f.	V_o VDC	I_o ADV	P_o Watt	100η %	v_r V_{rms}	100 v_r/V_o
105	0.775	74.3	81.4	223	244	.914	0	16.1	0	0	0	0
105	6.93	665.	727.3	1997	2182	.915	110	16.1	1771	88.68	.374	.34
105	12.66	1220	1330	3660	3990	.917	215	16	3440	94.14	.344	.16
105	6.42	617.3	647	1852	2022	.916	215.4	8.06	1736	93.73	.301	.14
105	2.60	248.4	273	745.3	819	.910	215.6	3.21	692.1	92.86	.259	.12
117	0.65	69.7	76	209	228	.917	0	16.1	0	0	0	0
117	6.14	659	718	1978	2155	.918	110	16.1	1771	89.53	.396	0.36
117	11.3	1217	1322	3650	3966	.920	215.3	16.0	3445	94.38	.366	0.17
117	5.85	628	684.4	1884	2053	.918	215.5	8.22	1771	94.0	.323	0.15
117	2.31	246	270	739	811	.911	215.7	3.19	688	93.13	.280	0.13
129	0.576	68.3	74.3	205	223	.919	0	16.1	0	0	0	0
129	5.54	658	714.6	1974	2144	.921	110	16.1	1771	89.71	.429	0.39
129	10.21	1216	1317	3648	3951	.923	215.5	16.0	3448	94.50	.388	0.18
129	5.23	621	657	1863	2025	.920	215.6	8.13	1753	94.09	.345	0.16
129	2.09	247	270	741	811	.913	215.7	3.21	692	93.26	.302	0.14

TABLE III - V

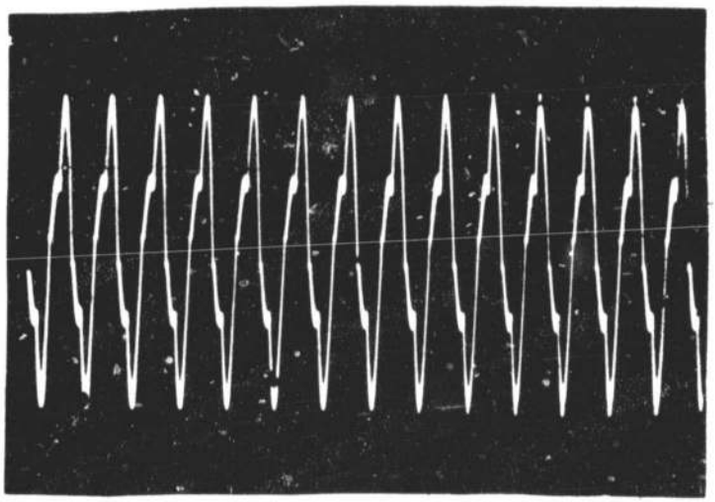
Characterization of Reverse Power Transmission

E_i VDC	I_i ADC	P_i Watt	P_o/ph Watt	VA/ph	p.f.	P_o Watt	VA	η	e_i V_{rms}	i_{si} A_{rms}
300	10.1	3030	943	1032	.913	2828	3097	93.32	117	8.82
300	5.2	1600	494	544	.908	1482	1632	92.62	117	4.65
300	1.02	306	93.7	103.3	.906	281	310	91.88	117	2.65



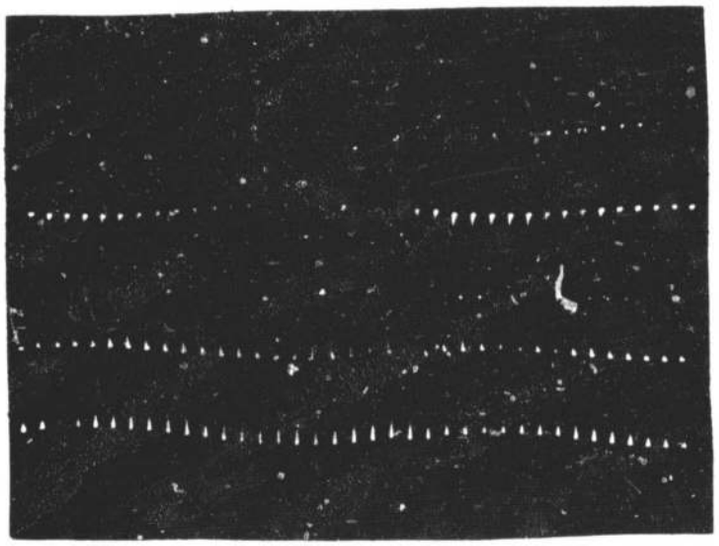
Vertical: i_1 = 14.7 A/div.
Horizontal: t = 50 μsec./div.

(a)



Vertical: i_1 = 14.7 A/div.
Horizontal: t = 200 μsec./div.

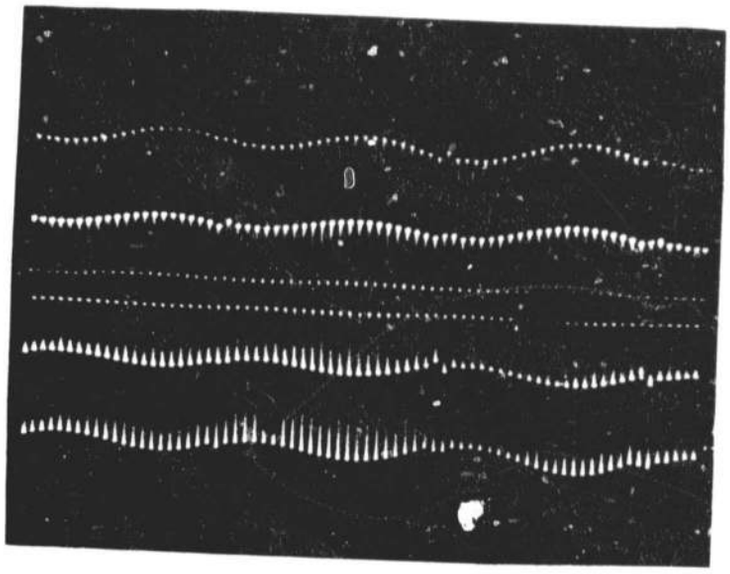
(b)



Vertical: i_1 = 14.7 A/div.
Horizontal: t = 0.5 msec./div.

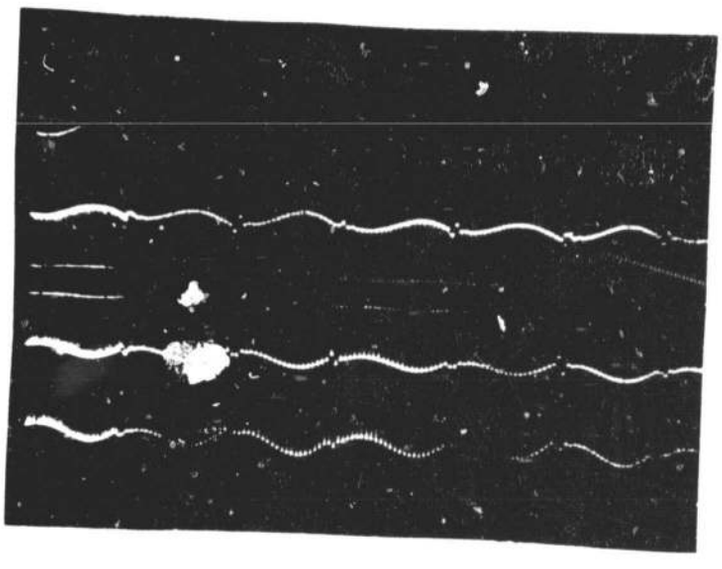
(c)

Fig.III- 4.1. Traces of the resonant current carrier i_1 at different time scales



Vertical: i_1 = 14,7 A/div.
Horizontal: t = 1 msec.:div.

(d)



Vertical: i_1 = 14,7 A/div.
Horizontal: t = 2 msec./div.

(e)

Fig. III - 4.1. (continued)
Traces of the resonant current carrier i_1 at different time scales.

The just referred to variation of the amplitude reveals itself as part of a modulation process, when examining, next the Fig. III - 4.1(c). This figure depicts, again, the same resonant current i_1, for all the same conditions, as do all the five Figs. III - 4.1(a) through (e). The working of a full wave "rectified" three phase system becomes now discernible, when viewing i_1 at a time scale of 0,5 msec./div.. The "seam" between two of the six sections within one period $T_s = 1/f_s$ of one phase of the ac source is discernible, about 3 cycles to the right of the center of the trace: One amplitude $I_a(k)$ is somewhat larger than fitting the general trend of the modulation pattern at that instant of time. This "irregularity" is caused by the phase to phase transfer mechanism which was described in section II - 6 and subsection III - 4.2.
The there described "hesitation" of the modulation process is caused by the phase to phase transfer for providing the resonant carrier's energy. This "hesitation" causes a deviation of i_1 from its smooth modulation pattern because the ampere-seconds area of the concerned half cycle of i_1 remains unconditionally true to the requirements of (2) of ch. III. Implementation of the generation of the carrier i_1 in spite of the asynchronism of e_s and i_1 and its reconciliation with the needed modulation requirements, as formulated by (2) above, proved as the most trying and difficult aspect of the technology of this work.

Inspection of the two following curve traces in Figs. III - 4.1(d) and (e), finally, unfolds the process of direct extraction of a powerful modulated current carrier i_1 from an ordinary low frequency three phase power system, without the interposition of a conventional passive rectifier-low pass filter system. The six "rectifier" intervals within one period T_s of the

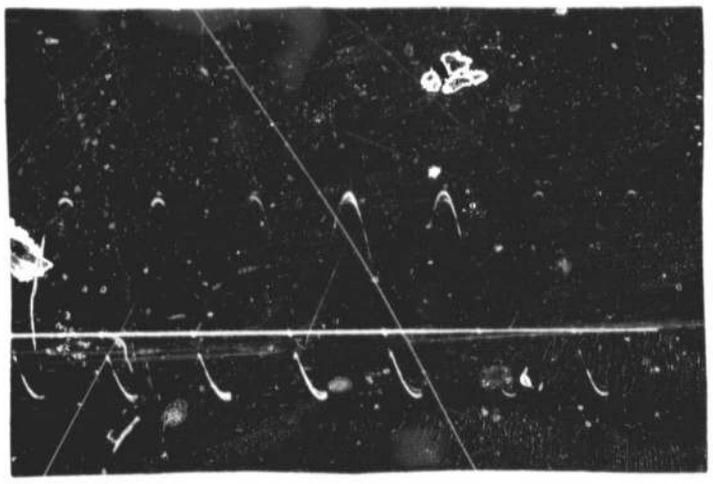
single phase sine wave are clearly discernible. Yet, these "seams" are dissimilar, because of the dissimilarity of the conditions of asynchronisme between e_s and i_l at each of these "seam" instants.

Also, the fact that the carrier i_l follows moderately the contour of e_s, obscures the fact that the ampere-second areas of its half cycles continue to obey the rule imposed by (2) of ch.II. The angle ψ_r is governed by the same rule and imposes it on each half cycle of i_l, even though this process is associated by variations of the $I_a(k)$, necessitated by the variations of e_s |4,5|. The source ripple attenuating effect is thus obtained, as described earlier in this section.

The beneficial effect of the described process of the power factor, p.f., in the three phase system is now discussed with reference to the curve traces shown in the photographs of Fig. III-4.2(a) through (c).

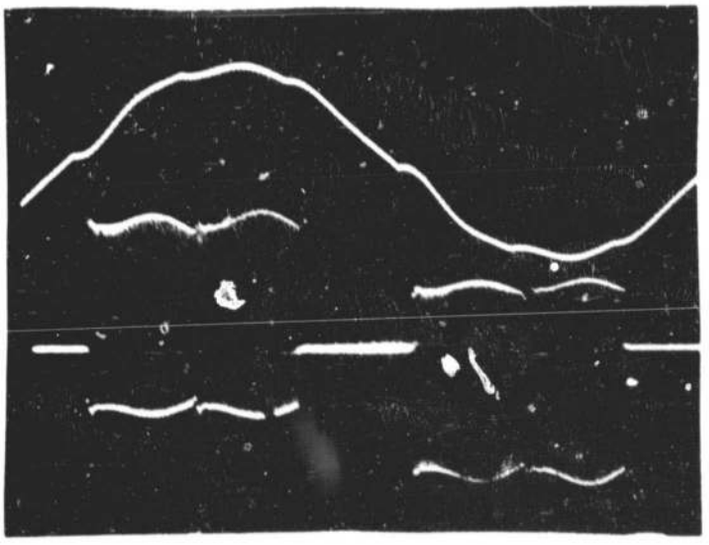
The oscilloscope trace of the portion of the current i_{lph} in one of the three phases of the sc supply inside the h.f. filter is shown in Fig. III-4.2.(a). The line $i_l = 0$ appears also on the same photograph, being traced by a zero volt signal on the dual input scope in order to facilitate the interpretation of the current trace.

This current i_{lph} elucidates one of the key charateristics of the workings of the converter. The integral of the negative part of i_{lph} for each of the half cycles of i_l is very small for maximum forward power transmission. The same negatively valued integral becomes almost as large as its positive counterpart when the output terminals of the converter



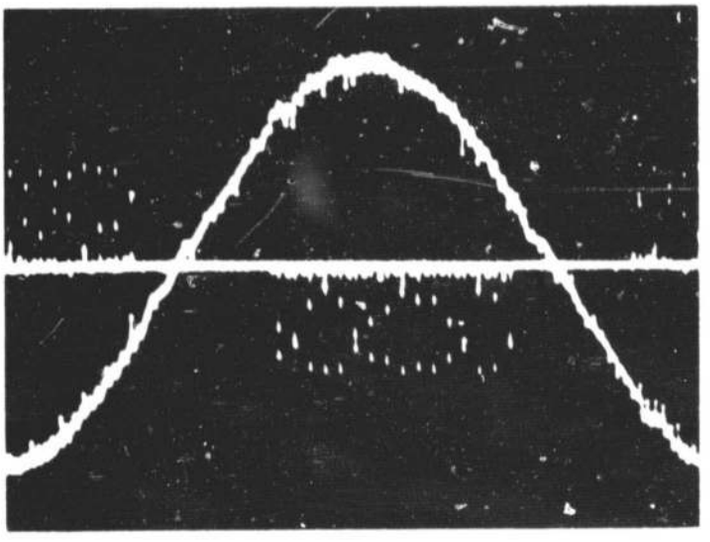
Vertical: i_{lph} = 14.7 A/div.
Horizontal: t = 50 μsec./div.

(a)



Vertical: e_i = 50 V/div.
$i_{l\,ph}$ = 14.7 A/div.
Horizontal: t = 2 msec./div.

(b)



Vertical: e_i = 50 V/div.
i_{lph} = 14.7 /div.
Horizontal: t = 2 msec./div.

(c)

Fig.III-4.2. Voltage e_i and current i_{lph} in one of the three phases of the ac supply inside the input filter.

are short circuited. The converter accepts then only the power, needed to cover its own losses. It is noted in passing that the absolute value $i_{l\ ph}$ of the phase current passes through the load. The above explained mechanism makes it possible to maintain an unconditionally limited current $i_{o\ max}$ through the load at any output voltage v_o and yet to derive only as much power from the source, as needed.

Fig. III - 4.2(b) shows the voltage sine wave of one phase with the thereto belonging phase current $i_{l\ ph}$ for forward power transmission. The shown current pattern is idential with the one in Fig. III - 4.2(a), except for the now compressed time scale. The contour of the modulated current $i_{l\ ph}$ is reminiscent of the modulated current carrier i_l of Fig. III-4.1(e). Forward transmission of power is indicated by the coincidence of the polaritics of e_i with the net transfer of charge by way of $i_{l\ ph}$.
The distortion of the voltage waveform of e_i is caused by the "soft" impedance of the variac type three phase auto-transformers, operated by one single rotary shaft. This peculiar property of the used ac transformer appears also as the cause of a slight leading tendency of the current intervals i_{lph}; this tendency is ascribed to the interaction of the transformers' "softness" and the filter capacitors which isolate the low frequency system of the ac supply from the high frequency operation of the converter. The slightly delayed response of these filter capacitors to the sudden demand and cessation of demand of high frequency current components accounts for the measured favorable power factor in excess of 0.9.

This favorable power factor remains unchanged by variations of the level of processed power. This property follows from the fact that neither the shape of the current i_{lph} nor its position with respect to e_i is modified when the value of $|i_l|_{av}$ is varied.

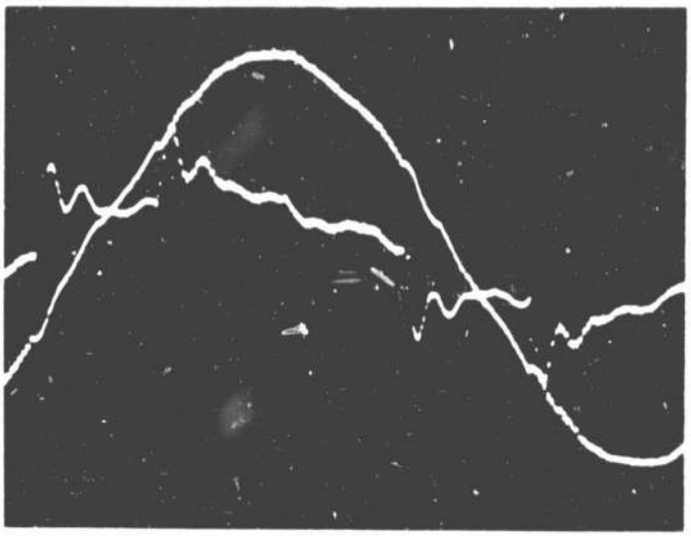
The control system requires 2 one half cycles or 100 μsec. of i_l to settle to a new steady state following introduction of an external disturbance.

Reversal of the power flow is indicated by the trains of current pulses which are derived from the resonant current i_l and constitute rectified pulse sequences with cyclically alternating polarity. A photograph of the trace of these pulse sequences is shown in Fig. III-4.2(c). The polarity of current opposes clearly that of the thereto pertaining sine wave voltage. The number of pulses per half cycle of the 60 Hz sine wave has been reduced so that the character of single pulses could be clearly seen. A further important feature of the current trace in Fig. III-4.2(c) is the fact that the pulses show only one single polarity within the time frame of one single half sine wave of the source voltage.

The reason for this cyclical "unipolarity" of the current pulses is the fact that the three phase thyristor bridge behaves now as a "gated diode bridge"; this was previously explained in III - 2.2.2.

The "fuzzy" appearance of the trace of the voltage sine wave in the same photograph is explained with the reversal of flow of energy into a source which has been "characterized" as being "soft" in the preceding description of forward power transfer.

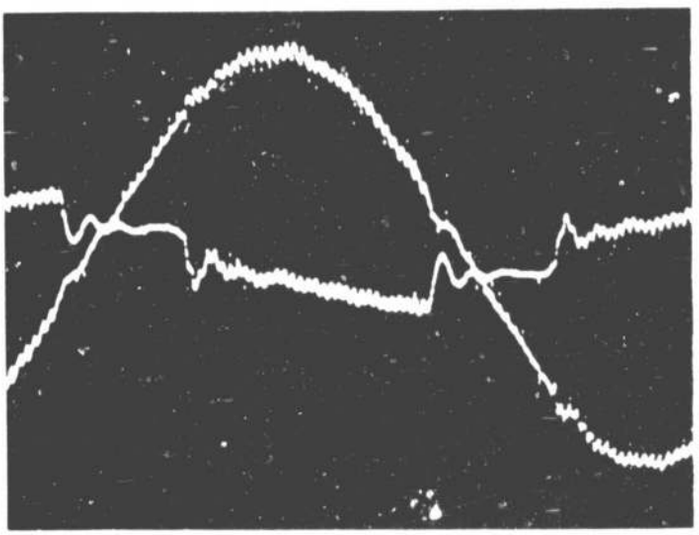
A filtered version of Figs.III-4.2(a) & (b) is shown in Figs. III-4.3(a) and (b). The previously shown individual pulses have given way



vertical i_{ph} = 10 A/div

horizontal t = 2 msec/div

(a)



vertical i_{ph} = 10 A/div

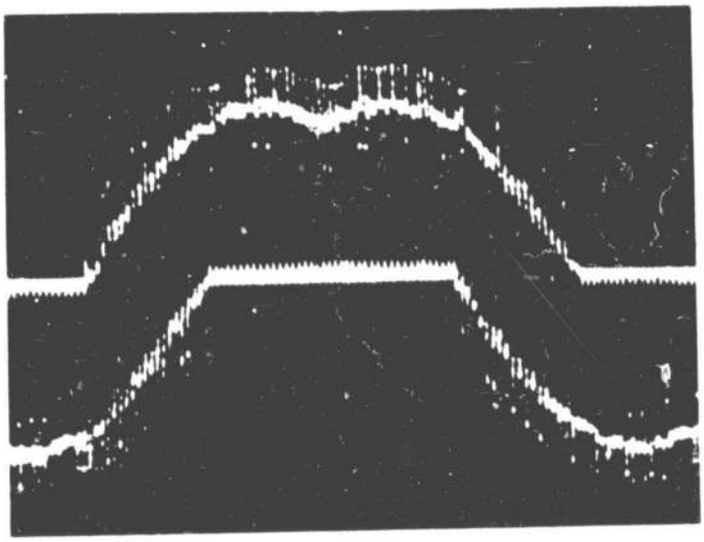
horizontal t = 2 msec/div

(b)

Fig. III - 4.3. Phase voltage e_i and current i_{si} for (a) forward and (b) reverse transfer of power through a doublesided cyclo-converter.

to continuous waveforms, even though they are considerably distorted by the parasitic properties of a "soft" supply line. The continuity of these current waveforms is caused by the inclusion of the effects of the line to line filter capacitors in the waveforms. The supposedly "rectangular" current waveforms are clearly discernible after discounting of the "damped oscillatory" reaction of the "soft" power network to the on-off switching of the phase current i_{si}. The volt-ampere pattern for "forward" transfer of power emerges from the tracs of Fig.III-4.3(a); the same pattern but for the "reverse" transfer of power is recognizable in Fig. III - 4.3.(b).

A trace of the anode to cathode voltage across one of the six antiparallel thyristor pairs of the three phases bridge is shown in Fig. III - 4.4. The cyclically alternating change of roles from "thyristor" to "diode" and vice versa of one of these antiparallel pairs of thyristor emerges, impressively, from that photograph. This trace gives an indication



vertical 100 V/div

horizontal 2 msec/div

Fig. III - 4.4. Voltage across one pair of antiparallel thyristors of the three phase bridge.

of the burden which is carried by the electronic protection and control system to implement the concept of the doublesided cyclo-converter, as formulated in chapter II and in the concerned literature [7].
It can be added here, that the advanced version of the electronics to protect and control this system, follows in general the line of its now classical dc converter forerunner and has adopted its virtues of unconditional protection of the system against externally induced disturbances.

III - 4.5. Discussion of the Results

The obtained results are in accordance with the predictions made in both chapter II and III. The internal system behavior is that of an ordinary dc converter which is fed from a voltage source e_s, consisting of a dc component $e_{s\ av}$ and the thereto pertaining ripple, as defined below (12) in section 3 of chapter III.

The test results concerning the dc characteristics of the presented system which are summarized in Table III - IV confirm the above made statement. Short circuit capability of the dc output terminals, dc regulation, efficiency and the suppression of the ripple of the "input voltage" e_s, are consistent with the characteristics of this type of dc converters, as described in the literature |4,5,6|. The somewhat lower efficiency near 94 percent at rated operating conditions is attributed (1) to the relatively low input voltage of 117/208 VAC and (2) to the fact that no attempt for optimization of components was made, beyond reasonable care for acceptable performance. The cause for this relaxation was the concentration on the primary objective of this work: to demonstrate the feasi-

bility of the direct ac/dc conversion concept with reversible power flow and the analogy of its internal charateristics with those of the common dc converter of this type.

The ripple suppression of

$$a_{FI} \approx 4/0.18 \approx 22 \tag{28}$$

exceeds the value 17.7, calculated in (20) of the preceding section. This improvement is attributed to the effects of the mixed AM-FM process, which occurs for purpose of modulation of the resonant current carrier i_1. The prediction of equation (20) was based on the effects of the FM process only. It is believed that more favorable attenuations can be achieved with the used control system, given sufficient effort of development. Yet, the achieved ripple of 0.18 percent is well within the customary practice in the intended area of applications.

The maximum output voltage variations ΔV_o, outside the area of overload is limited to

$$100\ \Delta V_o/V_o \approx 200(215.7 - 215)/(215.7 + 215) \approx 0.325\% \tag{29}$$

This can be also expressed as a maximum deviation

$$\left| \pm\ 100\ \tfrac{1}{2}\ (V_{o\ max} - V_{o\ min})/V_{o\ nom} \right| = 0.163\ \% \tag{30}$$

well within the intended goal of 1%.

The response time to step changes of 100 μsec is well within the goal of a 1 msec. response.

The input characteristics, as viewed from the three phase supply line are consistent with the predictions of chapters II and III. A power factor in excess of 0.9 was observed for all conditions of operation, including progressive overloading in each of the individual phases. The variations of these power factors was less than 1% for all conditions of testing, tabulated in Table III-IV. These test data confirm the engineering judgement which is derived from the inspection of the oscilloscope trace photographs, depicted in Fig. III - 4.2: the power factor can be taylored at will between $-0.9 < p.f. < 0.9$ because the position of the current "rectangle" under the sine wave voltage can be initiated and terminated at any time, as programmed, via an electronic control system. Insertion of appropriately timed and sized square wave voltages into the reference terminals of the second vertical row of differential amplifiers of the electronic logic shown in Fig. III - 2.3, can shift the points of "phase transition" as discussed above. The result is then a shift of the "rectangular" current pulses of Figs. III-4.2(b) and III-4.2.(c) to the right and to the left with respect to the voltage sine wave, depending upon the polarity relative to the respective single phase ac voltage and the amplitude of the above referred to square wave signals.

Only limited test were carried out to demonstrate the reverse transfer of power from a dc source into the three phase ac system. Efficiency and power factor confirm the original expectation that

(1) dc power can be transferred in this way to a three phase ac system and (2) that this transfer can be implemented efficiently and at a favorable power factor. The used mechanism of selection of phase pairs, discussed above with reference to the discussion of forward power transmission applies as well for the purpose of reverse power transmission. It means that the current i_{lph} can be injected at any angle of e_i, the reverse power transfer can thus be implemented for any desired power factor in the ac system. The materialization of this mechanism did not appear as a technologically critical process, even though it would require appreciable electronic work.

III - 5. Summary of Concept Verification

The critical aspects of the presented concept as listed in section III - IV have been experimentally verified. Data taken with operation of a 3 KVA breadboard confirm the expectation that the presented system embodies the characteristics of a dc converter of the concerned type, connected via a "high frequency antiparallel thyristor bridge" to a common three phase ac supply system [4,5,6].

Reverse transfer of electric energy was demonstrated with the same breadboard. The "antiparallel thyristor bridge" was then operated as a gated and in reverse operating three phase "rectifier" system.

No problem area of significance was encountered in the behavior of the power system. The main work effort was dedicated to the control electronics; appreciable simplifications could be attained following the application of suitable development efforts.

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2. ---------- "Analog signal to discrete time interval converter (ASDTIC)," U.S. Patent 3, 659, 184, April 1971.

3. Yu, J., Biess, John, J., Schoenfeld, Arthur, D., and Lalli, Vincent, R. "Circuits to three dc to dc power converters," Proc. IEEE Power Electronics Specialists Conference, 1973.

4. Schwarz, Fransisc, C., "An improved method of resonant current pulse modulation for power converters," IEEE Trans. on Ind. Electronics and Control Instrum., Vol. IECI - 23, No. 2, May 1976

5. ---------- "Electronic control system for efficient transfer of power through resonant circuits," U.S. Patent No. 3, 953, 779, April 27, 1976.

6. ---------- "A 10 kW feasibility model for a megawatt dc converter," AFAPL, Wright, Field, OH, 1977.

IV. PRELIMINARY DESIGN AND PERFORMANCE PREDICTION

IV - 1. Introduction

A system was studied, that can realize a direct connection of a polyphase source with a dc system. This system can transfer electric energy in a controlled form in either direction. The significance of the presented system lies in the fact that it avoids the use of passive low pass filters for the purpose of performing its task. The elimination of the low pass filters has at least two significant effects:

(1) the speed of response of the system is greatly increased, since this speed is commonly restricted to approximately one tenth of the lowest ripple frequency content that should be suppressed by that filter;

(2) the physical weight and size of the equipment are substantially reduced, since the low pass filter constitutes the most significant contribution to the weight of well engineered equipment.

The second statement, above, has also significant implications concerning the cost of equipment in terms of materials and their handling during manufacture, transportation, installation and servicing.

The above indicated effects characterize unique and useful properties which identify the advantages of the presented system; these properties constitute improvements of orders of magnitude over the present "state of the art". Reversibility of controlled ac/dc or ac/ac power flow by application of one single electronic process and without the application of low frequency magnetics, as indicated here, is not even contemplated in the present "state of art".

It is believed that in the light of the results of this program and the therefrom derived expectations of further development of the here evolved principles it could become necessary to reconsider

(a) the use of low frequency - three phase, 60 or 400 Hz sine wave - power distribution systems on space and air craft;

(b) the synchronization of ac power on multigenerator aircraft other than by the currently used processes;

(c) the use of three phase ac power for direct conversion for controlled (servo) motor drives;

(d) common controlled areas of application of ac utility type power, such as controlled ac and dc motor drives, energy storage for peak shaving purposes, induction heating, controlled electrolytic processes, HVDC transmission, and power supplies for electronic systems.

The following engineering assessment is preceded by the design of a representative system for the purpose of illustration and verification of quantitative estimates. This example is in close accordance, but not identical with the 3 kVA breadboard which was studied for purpose of concept verification.

The quantitative insight which is gained in the section IV - 2 Engineering Design of a representative BD4Q System is then used in section IV - 3 to arrive at an engineering assessment and an evaluation of the new system. The unique and useful characteristics of the newly developed system are singled out, as the significant results of this program.

IV - 2. Engineering Design of a Representative BD4Q System.

The type of BD4Q converter which was studied throughout this program will be used for purpose of the following engineering assessment and evaluation. This representative study follows the design of the used 3kVA breadboard in general terms and is presented as a self contained study for purpose of illustration of certain critical engineering aspects. The salient features of the concerned engineering consideration can be translated to other power levels by extension of the design philosophy for dc converters of the discussed type |1,2,3|.

IV - 2.1. System Design

At the outset of this discussion, it is pointed to the fact that the primary resonant circuit "sees" through the matrix of thyristors which connect it to the three phase line, a rectified voltage

$$e_s^* = E_s \sum_{k=o}^{\infty} \sin\{\beta + (\pi/6)(1-4k)\} - \sin\{\beta - (\pi/6)(3+4k)\} \qquad (2.1)$$

which contains a constant

$$e_{s\ av}^* = \frac{3}{\pi} \int_0^{\pi/3} (e_1 - e_2)\, d\beta \qquad (2.2)$$

on which a ripple voltage

$$e_{s\ r}^* = e_s^* - e_{s\ av}^* \qquad (2.3)$$

is superimposed.

Reference is made to Figs.IV-2.1 and 2.2 which are being reproduced here for the purpose of convenience. Fig. IV - 2.1 shows a symbolic schematic of the bidirectional four quadrant series capacitor inverter-converter. Thyristors CRij (i = 1,2,3; j = 1,2,3,4) constitute the above referred to thyristor matrix. Fig. IV-2.2 shows the significant voltage e_s^*, v_o, current i_{sr}, i_{si}, waveforms and the thereto pertaining input power P_s. The frequency f_s of one single phase of the ac source is normalized to

$$f_s = 1/2\pi \tag{2.4}$$

for simplicity of presentation. The validity of equation (2.1) is further clarified by the definition

$$\sin\{\beta + (\pi/6)(1 - 4k)\} = \begin{cases} \{\gtrless 1\} & \text{for } \pi/6 \leq \beta + (\pi/6)(1 - 4k) \leq \pi/2 \\ 0 & \text{everywhere else} \end{cases} \tag{2.5}$$

and with the understanding of a corallary restriction on the second sine function in the same equation. Fig. IV - 2.2 shows six pulses (k = 0,1,.....5) of e_s^* which would result over a length of time of 2π from a full wave rectified three phase ac system, even though no formal input rectifier bridge is involved.

The ripple of e_s^* is, usually, expressed in normalized form as [4]

$$e_s^*/e_{s\ av}^* = 1 - \Sigma \frac{2\sqrt{1 + (np\ \tan\alpha)^2}}{(np)^2 - 1} \cos\ (np\beta - \psi_{np}) \tag{2.6}$$

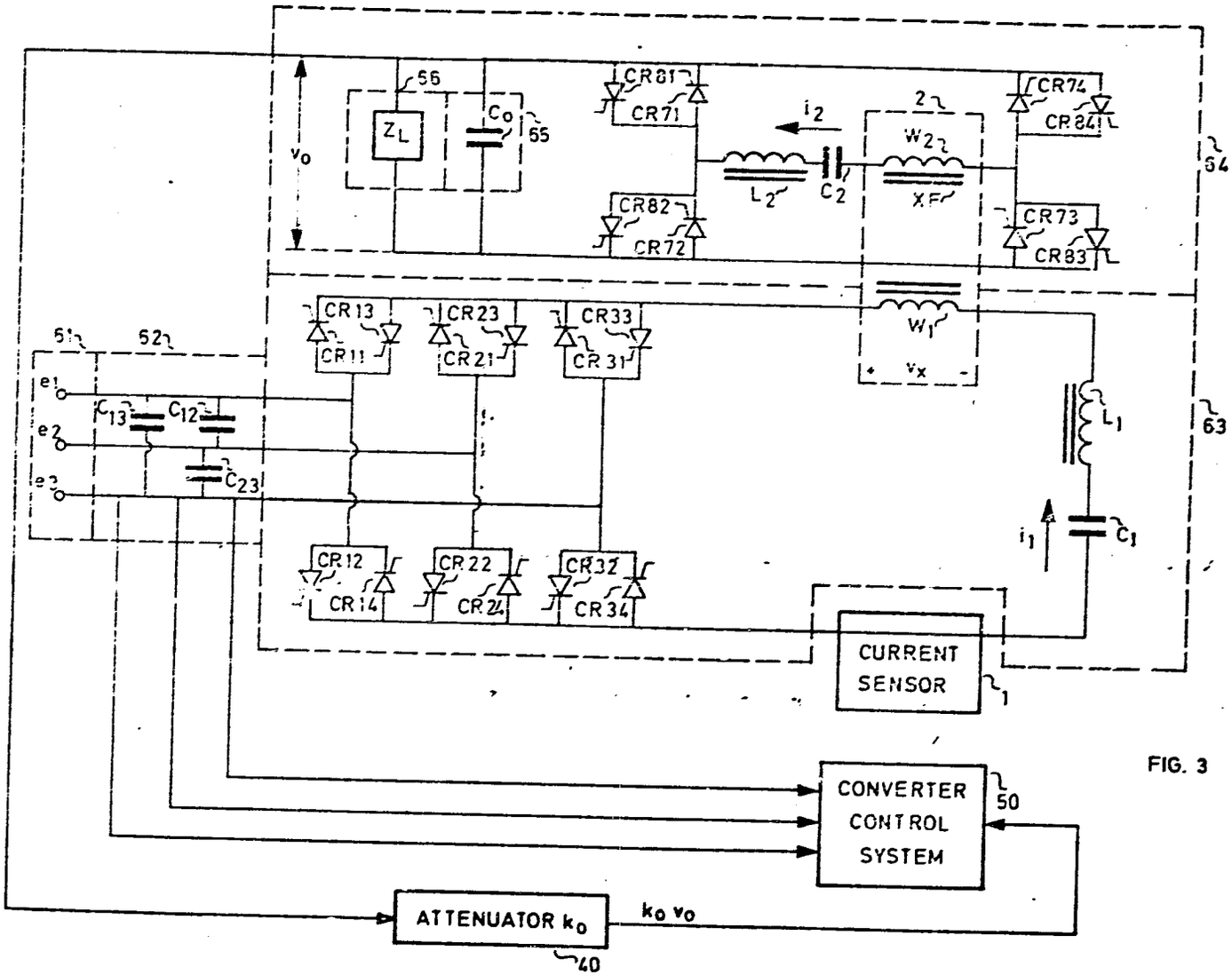


FIG. 3

Fig. IV - 2.1.

Symbolic schematic of the bidirectional series capacitor inverter-converter for operation of a dc load (source).

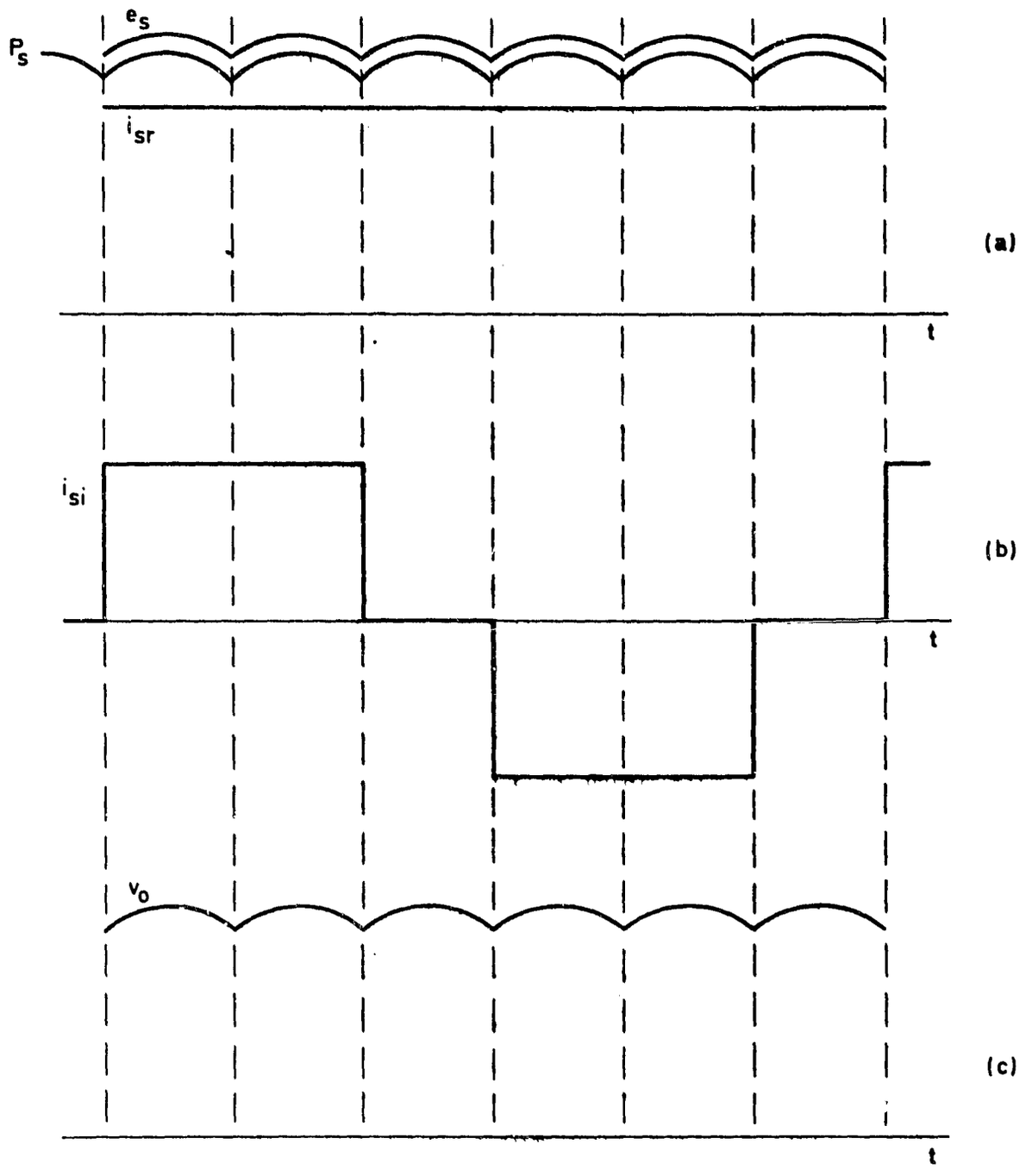


Fig. IV - 2.2.

(a) The output voltage e_s^* of a three phase full wave bridge rectifier, the filter current i_{sr} and the filter input power P_s; (b) the phase current i_{si} and (c) the filter output voltage v_o.

where

p = the number of effective phases per period of one single phase of the supply line; $p = 6$ in this case of a three phase full wave bridge controlled rectifier process which is being studied here;

ψ_k = arc tan A_k/B_k, where A_k are the coefficients of the harmonic component of the Fourier series associated with its sine and cosine terms respectively;

α = 0 in this case, being the customary phase control angle, which is not applicable for the here presented technology.

The rms value of the first harmonic component, amounts to the well known 4.04%. The composite effect of the first three harmonic components is restricted to 4.16%. The 4% value is, therefore, widely used for engineering approximations. The normalized maximum peak to peak variation of e^*_s

$$(e^*_{s\,max} - e^*_{s\,min})e^*_{s\,av} \approx 0.11 \qquad (2.7)$$

The relative ripple $v_{o\,rms}/V_o$ of the dc output voltage of the system, was assumed as

$$v_{o\,rms}/V_o \approx 1\%\ rms$$

for the purpose of this study, where

$v_{o\ rms}$ = the actual rms value of the output voltage ripple;

V_o = the average dc output voltage

The input voltage variations were assumed, not to exceed 10%, such that

$$e_s^* \simeq e_{s\ nom}^* (1 \pm 0.1) \tag{2.8}$$

Equations (2.1) and (2.2) were used to calculate the respective values of $e_{s\ av}^*$, $e_{s\ max}^*$ and $e_{s\ min}^*$ for a nominal three phase supply line of 117/208 VAC. The results are summarized in

TABLE IV - 2,1.

Applicable Apparent Input Voltages e_s^*

	e_s^*	$e_{s\ av}^*$	$e_{s\ max}^*$	$e_{s\ min}^*$	
1.0	$e_{s\ nom}^*$	274	287	248	V
1.1	$e_{s\ nom}^*$	301	315	271	V
0.9	$e_{s\ nom}^*$	246	258	223	V

The converter must be capable to operate at the lowest average input voltage $e_{s\ av}^* \simeq 246$, even though the temporary value of e_s^* may reach, periodically, a short lived low point of 223 Volt. The energy, which is stored in the LC circuit prior to this instant of time allows

operation of the converter system near the average level $e_{s\,av}^{*}$ of e_{s}^{*}.

The projection of an efficiency $\eta \simeq q \simeq 0.95$, indicates a primary transformer voltage amplitude $|1|$

$$v_{xa1} \simeq q\, e_{s\,av}^{*} \tag{2.9}$$

or

$$v_{xa1} = (0.95)(246) \simeq 238\ V \tag{2.10}$$

A lower square wave voltage amplitude

$$v_{xa} = 220\ \ V \tag{2.11}$$

is chosen, consistent with cautious engineering practice.

The ensuing absolute value of the average primary current

$$|i_1|_{av} = P_o/v_{xa} = 3000/220 = 13.64\ A_{av} \tag{2.12}$$

The rms content of this current is given by

$$i_{1\ rms} \simeq \rho_i\ i_{2\ av} \simeq (1.35)(13.64) = 18.4\ A_{rms} \tag{2.13}$$

IV - 2.2. Thyristor Ratings

Each of the twelve thyristors of the input matrix must accommodate a rms current of the magnitude

$$i_{th\ rms} \simeq i_{1\ rms}/\sqrt{6} \simeq 7.51\ A_{rms} \tag{2.14}$$

when evaluated over one cycle of one of the single phases of the three phase supply line. Yet, each of the thyristors has to accommodate peak currents I_1 up to, approximately, twice the average value of i_1. Thus

$$I_1 \simeq 2|i_1|_{av} \simeq (2)(13.64) \simeq 27.4\ A_{peak} \tag{2.15}$$

Use of a thyristor with a capability to process an average current

$$i_{th\ av} = (1/6)2I_1/\pi \simeq 2.91\ A_{av} \tag{2.16}$$

is indicated. This is a thyristor which would process an ac current of sinusoidal form with an average of its absolute value of (2)(2.91) $\simeq$ 5.82 A_{av}, an rms value of $i_{ac\ rms} = 7,51\ A_{rms}$ and with peaks of 27.4 A_{peak}, when working "back to back" with an equal thyristor as companion.

The rms rating for this thyristor can be estimated by

$$i_{th\ rms\ rated} = 2i_{ac\ rms} \simeq 16\ A_{rms} \tag{2.17}$$

The philosophy of the preceding reasoning was to select a thyristor which could accommodate each second half wave of an alternating current of sinusoidal form, with a peak value I_1 that was equal to the peaks I_1 which occur in the resonant current i_1. This assumption is considered to be very conservative and can be adhered to until more experience is gained with the here described type of converters.

It can be concluded that a very conservative rms rating of the used thyristors is unmerically nearly equal to the $|i_1|_{av}$ value, so that

$$|i_{th\ rms\ rated}| \simeq |i_1|_{av} \simeq 16 \tag{2.18}$$

Thyristors of the General Electric C139 series with a forward voltage blocking capability of 800 VDC were used for the construction of the thyristor bridges. These thyristors are rated for an average current of 25 A_{av} and an rms current of 35 A_{rms}; they exceed thus by far the above indicated conservatively established requirements.

A maximum voltage handling capability of the thyristors

$$v_{AC\ max} \simeq 1.25\ e^*_{s\ max} = (1.25)(315) \simeq 400\ Volt \tag{2.19}$$

is required. The factor 1.25 refers to a 25% "overvoltage" over the apparent source voltage e_s. This "overvoltage" is needed to accommodate voltage overshoots which appear on the switching thyristors and are needed to remove residual charges of energy from the distributed elements of the series inductor $L_1|1|$.

It is customary and good engineering practice to add a safety margin to the value in (2.19). This safety margin is determined in accordance with the specific conditions of operation of the converter for a given application.

The above explained consideration will be used further on for the purpose of engineering assessment of the here discussed system.

IV - 2.3. Capacitors

Capacitors are being used in the presented system for two significant functions: The controlled transfer of energy from the source to the load and the filtering of the relatively high frequency currents.

IV - 2.3.1. The Series Capacitor C_1.

The series capacitor C_1 undergoes during conditions of steady state operation a peak to peak voltage swing $v_{c1pp} \simeq 4.4\ e^*_s$.
If this capacitor C_1 is to conduct the current i_1 under the worst conditions of the lowest input voltage, then

$$C_1 \simeq |i_1|_{av}\ T_{ok}/4.4e^*_{s\ av\ min} \simeq (13,64)(50\ 10^{-6})/(4.4)(246) \simeq 0.63\ \mu F \quad (2.20)$$

This series capacitor C_1 has to accommodate a rms current of

$$i_{c1\ rms}/\mu F = 18.4/0.63 \simeq 30\ A_{rms}/\mu F \quad (2.21)$$

The needed peak voltage v_{c1p} capability of the capacitor C_1 is limited to

$$v_{c1p} \simeq 2.2\ e^*_{s\ av\ max} = (2.2)(315) \simeq 600\ VDC \quad (2.22)$$

Both preceding required ratings are consistent with the, generally, encountered requirements of capacitors for the intended use.

IV - 2.3.2. The Filter Capacitors

The ports of the network are "sealed off" to the outside by high frequency filter capacitors. The expression "sealed off" is meant to indi-

cate that these ports provide free passage of low frequency power through either of these ports in either direction. Yet the internal resonant circuits are at the same time short circuited for the purpose of preserving the needed high Q conditions. This double function is achieved by shunting the respective ports by simple filter capacitors. These capacitors appear almost as open circuits at the low power frequencies, and near short circuits at the, relatively high, internal pulse rates.

The largest deviation of voltage on these capacitors from their average steady state value is estimated by a discussion with reference to Fig. IV-2.3. For the sake of argument it is assumed here, that the source current i_{sr} emanates from a ripple free dc current source I_{sk}; the index k indicates the time invarying value of I_s during the kth cycle of converter operation.

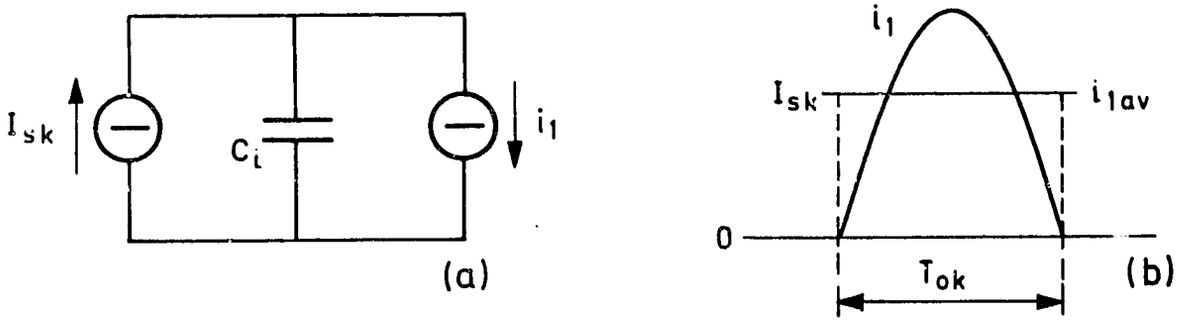


Fig. IV - 2.3.

Equivalent filter capacitor circuit.

The current i_1 in Fig. IV-2.3(b) shows the positive part of the resonant current i_1, which is here assumed to be an ideal half sine wave.

The question arises, what the size of the fictitious input filter capacitor C_i ought to be, so that a certain variation Δv_{ci} of the capacitor voltage v_{ci} would not be exceeded. The capacitor C_i accepts charge when

$$\beta_1/\omega_o < t < \beta_2/\omega_o \tag{2.23}$$

where

$$T_{ok} = \pi\sqrt{L_1 C_1} = \pi/\omega_o$$

$$T_{f1} = (\beta_2 - \beta_2)/\omega_o$$

If the charge ΔQ_n by which one half of the sine wave $i_1 = I_1 \sin \beta$ exceeds the average value

$$i_{1\ av} = I_{sk} = 2I_1/\pi \tag{2.24}$$

exceeds the average charge which is carried by the current I_{sk} during the time interval T_{ok}

$$Q_{n\ av} = I_{sk}\ T_{ok}, \tag{2.25}$$

then the ratio

$$\frac{\Delta Q_n}{Q_{n\ av}} = \frac{\int_{\beta_1}^{\beta_2} (I_1 \sin \beta - 2I_1/\pi)d\beta}{(2I_1/\pi)(\pi/2 - \beta_1)} \tag{2.26}$$

where β_1 and β_2, as defined in (2.23), are the instants of time of intersection of i_1 with $|i_1|_{av} = I_{sk}$.

Calculation of (2.26) yields

$$\frac{\Delta Q_n}{Q_{n\ av}} = \frac{\sqrt{1 - (2/\pi)^2}}{1 - (2/\pi)\text{arc sin } 2/\pi} - 1 \simeq 0.375 \tag{2.27}$$

The "surcharge" ΔQ_f which accumulates during the time interval T_{f_1} on the capacitor C_i is calculated with use of the equation

$$\Delta Q_f = (\Delta Q_n/T_{ok})T_{f_1} = Q_{n\ av}(\Delta Q_n/Q_{n\ av})T_{f_1}/T_{ok} \tag{2.28}$$

The time interval

$$T_{f_1} \simeq (T_{ok})(2)(\pi/2 - \beta_1)/\pi \simeq 28.75 \ \mu\text{sec.} \tag{2.29}$$

The surcharge

$$\Delta Q_f = 0.375\ I_{sk}\ T_{f_1} \simeq 10.78\ I_{sk}\ \mu\text{Coul.} \tag{2.30}$$

Equation (2.12) showed that the average of $|i_1| \simeq 13.64$ A. The surcharge

$$\Delta Q_f \simeq (10.78)(13.64)\mu C \simeq 147\ \mu C \tag{2.31}$$

This "surcharge" ΔQ_f causes the peak to peak ripple v_{cipp} on put filter capacitor. Thus

$$C_i\ v_{cipp} = \Delta Q_f \tag{2.32}$$

.

The rms value of this ripple is related to its peak to peak value by

$$v_{ci\ rms} \simeq (1/2\sqrt{2})\ v_{ci\ pp} \tag{2.33}$$

Normalization of $v_{ci\ rms}$ vs. its "dc source" value $e^*_{s\ av}$ and an arbitrary assumption that

$$v_{ci\ rms}/e^*_{s\ av} \simeq 0.01 \tag{2.34}$$

yields for $e^*_{s\ av\ nom} \simeq 270$ VDC:

$$v_{ci\ pp} \simeq (2.7)(2\sqrt{2}) \simeq 7.64\ V \tag{2.35}$$

It follows that minimum value of the capacitor

$$C_i \simeq \Delta Q_f/v_{ci\ pp} \simeq 147\ 10^{-6}/7.64 \simeq 19.25\ \mu F \tag{2.36}$$

The input filter capacitor C_i is, actually, composed by three capacitors, C_{12}, C_{13} and C_{23} which connect the three phases of the supply line. Each of these three capacitors C_{ij} is related to the input capacitors

$$C_i = (3/2)\ C_{ij} \tag{2.37}$$

A minimum size

$$C_{ij} \simeq (2/3)\ 19.25\ 10^{-6} \simeq 12.8\ \mu F \tag{2.38}$$

is therefore required in order to satisfy the, arbitrarily, established requirement of (2.34). The experimental study model was equipped with input filter capacitors of 25 μF.

The output filter capacitor C_o can be implemented by the same value of C_i, as given by (2.36), if the power transformer XF has a 1:1 turns ratio. If

$$N_2/N_1 = a \tag{2.39}$$

then

$$C_o = C_i/a^2 \tag{2.40}$$

It is recalled at this time that the roles of the input and the output ports of the here described bilateral system are entirely interchangeable. The same criteria of design can, therefore, be applied to any of the ports for either direction of power flow, with due consideration being given to the impedance transformation, as stated by (2.39) and/or (2.40).

The current carrying capability of the filter capacitors should be approximately

$$i_{c\ rms} \approx 0.375\ i_{dc} \tag{2.41}$$

where

i_{dc} = the average dc current which enters or leaves the port at which the filter is placed.

This rms current carrying capacity can be related to the microfarad size of the filter capacitor. The input filter capacitor carries an rms current

$$i_{ci\ rms} \approx (0.375)(13.64) \approx 5.12\ A_{rms} \tag{2.42}$$

Each of the three input filter capacitors C_{ij}, as referred to above, has thus to accommodate a current of

$$i_{cij\ rms}/\mu F \simeq (2/3)(5.12)/12,8 \simeq 0.27\ A_{rms}/\mu F \qquad (2.43)$$

per μF of its nominal capacity. The output capacitor C_o requires the same current carrying capability per μF, unless a change of impedance level takes place, where $a \neq 1$ in (2.40).

The tolerance of rms currents in the respective capacitors could take precedence over the filtering requirements and should be checked, in each case, as an alternative constraint of component specification.

Another significant component specification is that of the recurrent maximum voltage. The voltage limit for the series capacitor is given by (2.22). The maximum steady state voltages for the filter capacitors are also contained in (2.22) and in the output voltage requirements for a specific case.

No significant margins appear needed for the maximum recurrent series capacitor voltage and its nominal rms current, since the control system prevents substantial deviations from the intended maximum stresses. Voltage overshoots of the output voltage occurs, because of the inherent "first order" filter character of the converter; the output filter capacitor C_o can, therefore, be dimensioned accordingly. An analogous argument can be made for the input filter capacitor C_i. Yet, the specific supply line conditions could impose more stringent requirements than the converter system itself.

Series capacitors of the above described type are being us in series inverters of the discussed kind. The weight of these capacitors is approximately 200 g/μF|3|. A capacitor of 0.68 μF could weigh 140 grams.

The weight of this type of filter capacitors amounts to, approximately 10 g/μF. The 13 μF capacitors in question would weigh, approximately 130 g each.

IV - 2.4. Magnetic Components

The magnetic components constitute one of the critical groups, which deserves special attention. The characteristics of these components have a significant bearing on the ratio of maximum vs. average stresses in all components of the converter, its total heat dissipation and its total weight. The components are, furthermore, as a rule custom designed and fabricated by the converter's manufacturer.

IV - 2.4.1. The Series Inductors

Smaller converters of the discussed type, say up to 10 kW, can be constructed with the use of distributed series inductors. The rationals needed for this choice will emerge from the here following discussion and description of the device.

A turn-off time of 12 μsec is provided for the SCR's of the series resonant circuit. The time interval $\Delta\beta_k/\omega_o$ = 50 μsec for full power conditions. The thyristor current interval lasts under these conditions approximately

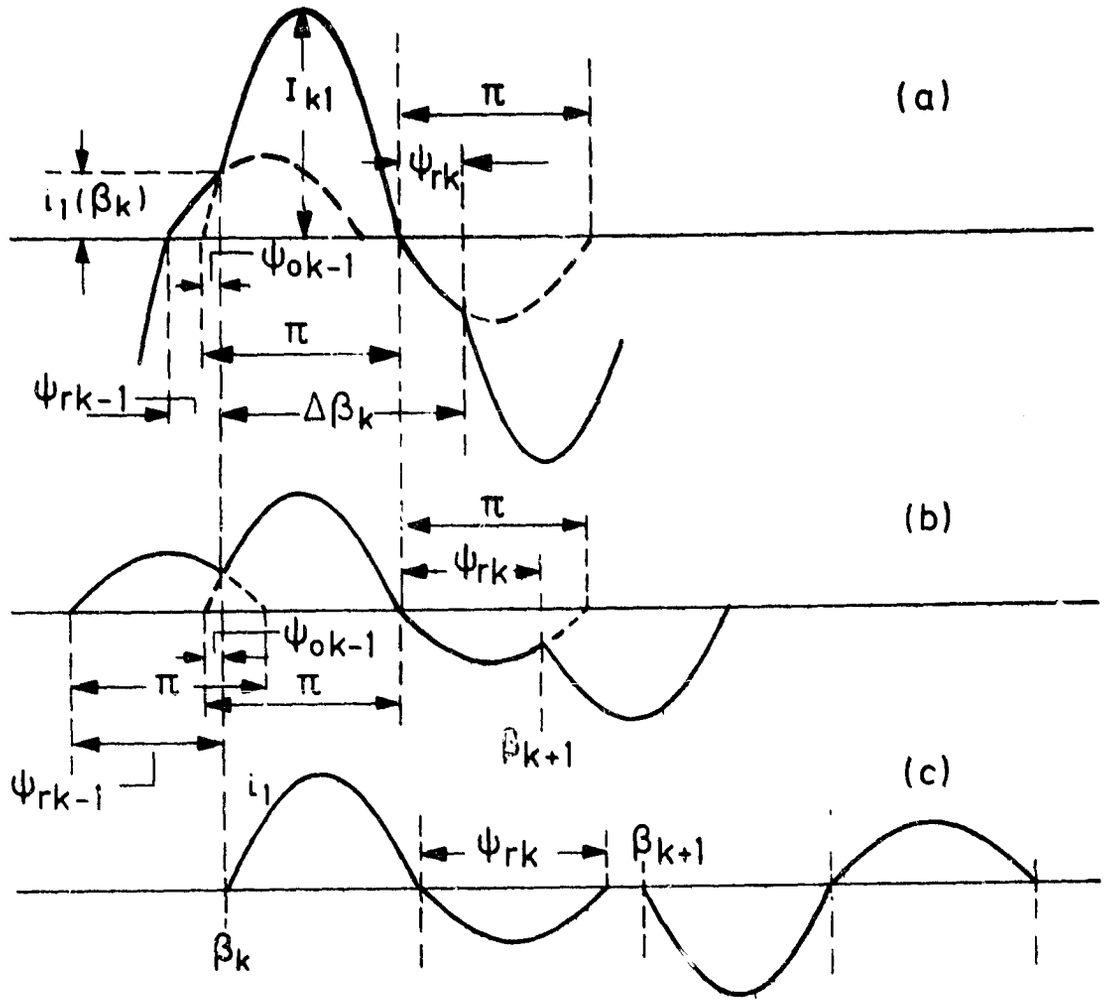


Fig. IV - 2.4.

The resonant current i_1: (a) for $\psi_{rk} \to \psi_{rk\ min}$; (b) $\psi_{rk} \to \pi$; (c) $\psi_{rk} = \pi$ and $\Delta\beta_k > 2\pi$.

$$(\pi - \psi_o)/\omega_o \simeq 38\ \mu\text{sec}. \tag{2.44}$$

The, relatively small, time for the angle $\psi_o/\omega_o \simeq 2$ μsec. This is illustrated in Fig. IV-2.4. The resonant time interval

$$T_o \simeq \pi \sqrt{L_l C_l} \simeq 40\ 10^{-6} \tag{2.45}$$

and

$$L_l \simeq (T_o/\pi)^2/C_l \simeq (162/0.63)10^{-6} \simeq 257\ \mu\text{H} \tag{2.46}$$

It must be said, at this time, that it could be easier to acquire a capacitor of 0.68 μF than of 0.63 μF, even though any of them may have to be custom made. The here presented analysis is continued with the assumption that $C_l = 0.68$ μF. Thus

$$L_l \simeq (162/0.68)10^{-6} \simeq 238\ \mu\text{H} \tag{2.47}$$

This value is divided into four equal parts, so that

$$L_{li} \simeq 238\ \mu\text{H} \simeq 60\ \mu\text{H} \qquad (i = 1,2, \ldots..10) \tag{2.48}$$

Each of these four series inductor parts L_{li} is associated with one antiparallel thyristor pair, ten in all, as indicated in Fig. IV-2.1. Four of these L_{li} will then close the resonant circuits of the thyristors, which act as such in the sense of this presentation, at any time.

IV - 2.4.2. The dv/dt Limiting Networks

Pairs of these L_{li} in series are then at any time "positioned" between the thyristors of two phases in which one is being turned off, while the resonant current is being diverted to the other. The total inductance between two current commutating thyristors is then 2 x 60, or 120 μH.

A snubber capacitor

$$C_d = 10 \text{ nF} \tag{2.49}$$

was chosen for the purpose of limiting the dv/dt of the anode to cathode voltage of the opening thyristor. The maximum dv/dt of the undamped oscillation

$$\omega_{od}\, e^*_{s\,max} = 315/\sqrt{120}\; 10^{-6}\; 10^{-8} \simeq 287 \text{ V/}\mu\text{sec} \tag{2.50}$$

The "rise time" as given by (2.50) is greatly diminished by letting the Q of the dv/dt limiting resonant R_d L_d C_d circuit approach unity for the purpose of its critical damping. Inductor

$$L_d = 2\, L_{li} \tag{2.51}$$

and

$$R_d < 2\sqrt{L/C} \tag{2.52}$$

The initial rise time

$$dv/dt(0) < 200 \text{ V/}\mu\text{sec} \tag{2.53}$$

The limitation which is imposed by (2.53) satisfies the characteristics of most thyristors of the older type for the here considered power range, such as the former G.E. C35 series and is amply met by newer thyristors. The initial rise time, given by (2.53) decreases during the interval of anode to cathode voltage rise, as the effect of circuit damping accumulates.

The dissipation P_d in each of the damping resistors R_d is less than the state of change of energy of the damping capacitor, because of the resonant

character of the circuit. Thus

$$P_{di} < \varepsilon_{cd\ max}\ 2f_i \tag{2.54}$$

where

$\varepsilon_{dc} \simeq \frac{1}{2}\ e^{*2}_{s\ max}\ C_d$, the energy stored in the damping capacitor, when at its peak voltage;

f_i = 10 kHz, the maximum inverter frequency.

For $e^*_{s\ av} \simeq 274$ V, is

$$2\ \varepsilon_{dc\ max}\ f_i \simeq 274^2\ 10^{-8}\ 10^4 \simeq 7{,}5 \text{ Watt} \tag{2.55}$$

The resonant current i_l is being processed by four pairs of antiparallel thyristors, at any time, while the other six pairs of thyristors stand by to be called upon for action. The total power dissipation P_d in the dv/dt networks of the described type is approximated by the inequality

$$P_d \simeq 4P_{di} < 8\ \varepsilon_{dc\ max}\ f_i \simeq 30 \text{ Watt} \tag{2.56}$$

The inequality sign in (2.54) and (2.56) implies that only part of the energy which is acquired by capacitor C_d is dissipated in the damping resistor R_d. This is caused by the resonant character of the concerned circuit. It will be pointed out in the discussion of the characteristics of the newly acquired technology that more powerful tools could limit the dv/dt phenomenon in a non-dissipative manner, especially, when design and construction of heavier equipment is being considered.

All of the power P_{dj} by (2.55) is being dissipated in each of the resistors R_d, which must be dimensioned accordingly.

IV - 2.4.3. Design of the Series Inductor Elements

An iron core, made of .001" thick tape wound Supermalloy is used for the illustration of an inductor design. This C-core is characterized by the type number C100, weighs 104 gram and is provided with an adjustable air gap; it is being manufactured by the Arnold Engineering Co.

The saturation flux density of this material is given with, approximately, 0.7 Tesla. It is intended to magnetize this material to 0.55 Tesla at the peak $A_{peak} \simeq 27.4$ of the resonant current i_1. The core loss for these conditions is given as 10 W/lbs.

The physical characteristics are listed by the manufacturer as:

	D	E	F	G	Weight(brut)	net
inches	.500	.325	.500	1.250	.255 lbs	.2295 lbs
cm	1.27	1.27	1.27	3.175		104 g

The meaning of the symbols of the above listed dimensions can be derived from inspection of Fig. IV-2.5. A "stacking factor" of 0.9 is used to calculate the net iron cross section $A_{c\ net}$ and the net weight.

The net iron cross section

$$A_{c\ net} \simeq (1.27)(1.27)(0.9) \simeq 1.08\ cm^2 \qquad (2.57)$$

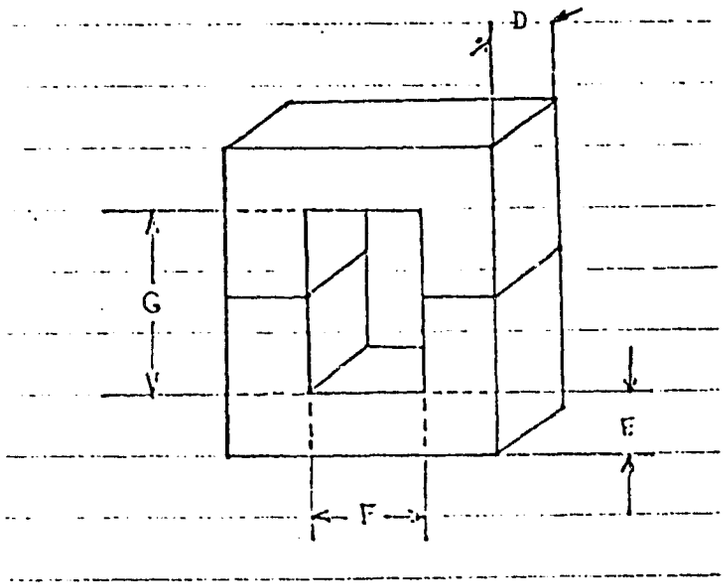


Fig. IV - 2.5.

Symbols for the dimensions of a C - core.

The specific core loss

$$P_c/\text{lbs} \simeq 10 \text{ Watt/lbs} \tag{2.58}$$

for a maximum flux density $B_m = 0.55$ Tesla and an operating frequency of 10 kHz. The net window area

$$\Delta_{\text{window net}} \simeq (0.32)(1.27)(3.175) \simeq 64.5 \text{ mm}^2 \tag{2.59}$$

where

0.32 = the "stacking factor" for Litz wire in a C-core.

The number of turns N of the inductor is given by

$$N = L_{li}\, I_{l\ peak}/A_{cl\ net}\, B_m \simeq 60\ 10^{-6}\ 27.4/1.08\ 10^{-4}\ 0.55 \simeq 28 \qquad (2.60)$$

The average length of each turn is approximated by

$$\ell_{av} \simeq 2(D + E) + F \simeq (2)(2.54) + 1.27 \simeq 5.35\ \text{cm} = 0.0535\ \text{m} \qquad (2.61)$$

The resistance of the winding is approximated by

$$R_T \simeq \frac{(1.2)(1.2)}{\sigma_w}\ \frac{N\ \ell_{av}}{A_{wire}} \simeq \frac{1.44}{56}\ \frac{28\ 0.0535}{64.5/28} \simeq 17\text{m ohm} \qquad (2.62)$$

where

1.2 = factors which account for (1) the rise in the temperature of the magnet wire and (2) for parasitic effects in the same Litz wire;

σ_w = the conductivity of drawn copper at 25°C;

A_{wire} = the cross sectional area of the wire.

The power loss P_w in the wire is given by

$$P_w = \tfrac{1}{2}\ i_{l\ rms}^{2}\ R_T \simeq \tfrac{1}{2}\ 27.4^2\ 17\ 10^{-3} \simeq 6.38\ \text{Watt} \qquad (2.63)$$

The weight W_{wire} of the copper wire is given by

$$W_{wire} \simeq (28)(0.0535)(2.3)(9) \simeq 31\ \text{gram} \qquad (2.64)$$

The core loss P_c is given by

$$P_c = (0.23)(10) \simeq 2.3\ \text{Watt} \qquad (2.65)$$

The total loss P_{LT} of the inductor element L_{1i} then becomes

$$P_{LT} = P_c + P_{wire} = 2.3 + 6.38 \simeq 8.7 \text{ Watt} \tag{2.66}$$

The total physical weight of the inductor

$$W_{L1i} \simeq W_c + W_{wire} \simeq 104 + 31 = 135 \text{ gram} \tag{2.67}$$

The efficiency η_{11} of the series inductor group L_{1i} is approximated by

$$100\ \eta_{L1} = (3000 - 4 \times 8.7)/30 \simeq 98.84\% \tag{2.68}$$

The energy density of the individual inductors

$$\varepsilon_L/\text{kg} = \tfrac{1}{2}\ 60\ 10^{-6}\ 27.4^2/0.135 = 167 \text{ mJ/kg} \tag{2.69}$$

The ten inductors have a cumulative weight

$$W_{L1} \simeq (10)(0.135) = 1.35 \text{ kg} \tag{2.70}$$

IV - 2.4.4. The Power Transformer

A power transformer XF as shown in Fig. IV-2.1 is needed to (1) provide the ohmic isolation between the converter's input and output circuits and (2) perform a needed impedance transformation, if so required. An illustrative example for a 3 kW transformer is worked out for the purpose of analysis.

Intended is the use of an Arnold Engineering core C119 of the above identified type. The physical characteristics of this core are given

below:

	D	E	F	G	Weight(brut)	net
inches	1.0	.563	1.125	2.875	1.1611 lbs	1.45 lbs
cm	2.54	1.43	2.86	7.30	731 g	658 g

Iron cross section

$$A_c = (2.54)(1.43)(0.9) \simeq 3.27 \text{ cm}^2 \text{ net} \tag{2.71}$$

The core loss per lbs of iron

$$P_c/\text{lbs} = 6 \text{ W/lbs for } B_{max} = 0.325 \text{ Tesla at 10 kHz} \tag{2.72}$$

The one half period $T_{ok\ av}$ of an oscillation at 10 kHz is given

$$T_{ok\ av} = 1/20\ 10^3 \simeq 50 \text{ µsec} \tag{2.73}$$

The natural period $2T_o$ of the resonant circuit is, approximately 80 µsec, as given by (2.45).

The worst case of volt-seconds which are impressed on the primary transformer winding W_1 occurs when the resonant current is decreasing and becomes discontinuous. The maximum amount of volt-seconds is then given by

$$(\text{v-sec})_{max} = 2v_{xa}\ T_o \tag{2.74}$$

At that time a maximum flux density of $B_{max} = 0.65$ Tesla is being used. The number of primary turns then becomes

$$N_1 = \frac{2v_{xa}\ T_o}{2B_m\ A_c} = \frac{220\ 40\ 10^{-6}10^4}{0.65\ \ 3.27} \simeq 42 \text{ Turns} \tag{2.75}$$

The average length ℓ_{av} of one turn is approximated by

$$\ell_{av} = 2(D + E) + F = 2(3.97) + 286 \simeq 10.8 \text{ cm} \tag{2.76}$$

The total length of the primary winding

$$\ell = N_1\ \ell_{av} \simeq (42)(0.108) \simeq 4.54 \text{ m} \tag{2.77}$$

The core window A_{window} is given by

$$A_{window} = FG = (2.86)(7.3) \simeq 20.9 \text{ cm}^2 \tag{2.78}$$

The net area $A_{wire\ net\ 1}$ that is available for the primary winding is one half of the above given gross area, modified by a stacking factor of 0.32 for the intended use of Litz wire

$$A_{wire\ net\ 1} = \tfrac{1}{2}\ 20.9\ 0.32 \simeq 334 \text{ mm}^2 \tag{2.79}$$

The wire cross section A_{wire} is calculated from the ratio

$$A_{wire} = A_{wire\ net\ 1}/N_1 = 334/42 \simeq 8 \text{ mm}^2 \tag{2.80}$$

The resistance of the primary winding is now calculated from

$$R_T \simeq \frac{k_w}{\sigma_w}\ \frac{\ell}{A_{wire}} = \frac{1.4}{56}\ \frac{4.54}{8} \simeq 14\ 10^{-3} \text{ ohm} \tag{2.81}$$

where the meaning of the symbols is identical with those, used for the design of the series inductor elements.

The power loss P_{wire} in the two windings of the transformer is given by

$$P_{wire} = (2)(14\ 10^{-3})(340) \simeq 9.52 \text{ Watt} \tag{2.82}$$

for conditions of full power transfer. The core loss for the same conditions of operation

$$P_c = (6)(1.45) = 8.7 \text{ Watt} \tag{2.83}$$

The total power loss of the transformer is given by

$$P_{XF} = 9.5 + 8.7 \simeq 18.2 \text{ Watt} \tag{2.84}$$

when processing full power.

The cooling surface S of the transformer can be approximated by

$$S = 2\{2(E + F)(F + D + G) + G(F + D) + (F + 2D)(D + E)\} \tag{2.85}$$

and is approximated by

$$S = 368 \text{ cm}^2 \tag{2.86}$$

The temperature rise on the surface of the transformer is then calculated as

$$\Delta T = P_{XF}/2\ 10^{-3}\ S = 18.2/2\ 10^{-3}\ 368 \simeq 25\ ^{o}C \tag{2.87}$$

An average heat transfer of 2 mW/cm^2 from the surface of the transformer to still air was assumed for the purpose of analysis as an empirical number, known from experience.

The total weight W_{wire} of the transformer windings is approximated by

$$W_{wire} = (2)(4.54)(8)(9) = 654 \text{ g} \tag{2.88}$$

The total net weight W_{xf} of the transformer is estimated as

$$W_{core} = 658 \text{ g}$$

$$W_{wire} = \underline{654 \text{ g}}$$

$$W_{xf} \quad 1312 \text{ g} \tag{2.89}$$

or 438 g/kW at an efficiency

$$100\,\eta_{xf} \simeq (3000 - 18.2)/30 \simeq 99.4\% \tag{2.90}$$

An appropriate trade-off of efficiency vs weight indicates a weight of 250 g/kW for a transformer efficiency which approaches 99 percent [6].

IV - 2.5. Weight and Heat Dissipation of Power Components.

An inspection of Fig. IV-2.1 leads to the conclusion that the series resonant LC circuit is flanked by two input-output thyristor bridges of "equal standing". Each of these two bridges has, intrinsically, the same functional capabilities, even though one connects to a three phase network and the other to a two wire dc system. This comparison is reinforced if the three phase thyristor bridge is reduced to a two phase bridge by the removal of four of its thyristors, say CR3j (j = 1,2,3,4). The power system then becomes entirely symmetrical with respect to its series resonant circuit.

The above made reflections underline the bilateral character of the discussed system, which is its significant intended property. The question arises to what extent, if any, the power system has to be enlarged beyond its

C - 3

basic dc configuration, in order to acquire the added functions of (1) bilateral operation capability and (2) interface with a polyphase system instead of connecting a dc load to a dc source.

A comparison of the thyristor matrix which connects the system to the two wire dc load or source reveals that:

(1) a simple rectifier bridge consisting of four diodes is needed for load operation;

(2) an antiparallel thyristor-rectifier bridge consisting of four diodes and four thyristors is needed for acceptance of power from a dc source through the same port;

(3) an antiparallel thyristor bridge consisting of eight thyristors is needed for:

(3a) acceptance of power from an alternating bipolar source;

(3b) feeding of a load with dc of either polarity or with an ac of any character.

It can be said that any power transfer to or from a two wire system can be implemented, once the four element rectifier bridge is enlarged by its antiparallel companion. If diodes and thyristors are equated as "power switching elements" then it means that the addition of four such elements adds the property of "bilaterality" to the power system. This philosophy can be extended from two to three wires/phases: Each addition of four more power switching elements can connect one more phase to the system for bilateral power transfer.

The addition of each phase to the system beyond the minimum two wire configuration requires four switching elements, whether meant for single or bidirectional power transfer. The option for use of two switching elements per phase for single directional power transfer is restricted to two wire systems of the type, cited in (1) above.

The foregoing explanations are briefly summarized in Table IV - 2.1. It is, of course, tacitly, assumed that the systems with more than two wire connections operate with the use of alternating currents.

TABLE IV - 2.2.

Number of Required Switching Elements Per Phase.

	No. of Wires		
Power Transfer	2	3	4
Unidirectional	4	12	16
Bidirectional	8	12	16

The expansion of the power circuit is, therefore, restricted to the number of four switching elements for each added phase, whether this system is being used for unidirectional or bidirectional power transfer.

The above explained addition of phases and the therewith associated switching elements, also requires the addition of dv/dt limiting circuits. These circuits take the form of R_dC_d damping circuits and the therewith associated

inductive coils. These coils can be part of the resonant inductor L_{1i}, as described in subsection IV - 2.4 above, or consist of saturable inductors, described in the literature [1,5]. These saturable coils and the therewith associated networks for the feedback of excess energy have a weight of, approximately, one third of the above referred to resonant inductor parts which they replace.

No more than four of the switch pairs and the therewith associated dv/dt networks are in operation at any time, even though ten of these are installed in the above presented example. It means that the component weight increases accordingly, but not the heat dissipation of the power system. The total weight of the two wire bridge of the above presented example is summarized in Table IV - 2.3 and compared to the weight of a three wire bridge. The values of power dissipation are added in each case for purpose of completeness. The indicated weight of components does not comprise the mechanical structures of the converters, which include the cool plates for the semiconductor switching elements. The component weight of the ac/dc converter W_{ac} is, approximately

$$100(W_{ac}/W_{dc} - 1) \simeq 100(5380/3900) - 100 \simeq 38\ \% \qquad (2.91)$$

higher than that of the of the dc converter W_{dc}. This higher weight is caused by the addition of eight switching elements, six elements of the series inductor L_1 with the thereto pertaining R_dC_d damping networks and a doubling of the input filter capacitor C_i.

TABLE IV - 2.3.

Comparative Component Weight and Power Loss in a DC and AC/DC Converter of 3 kW.

Converter Type	DC		AC/DC	
No. of Switches	8 + 4		12 + 8	
	Weight Gram	Power Loss Watt	Weight Gram	Power Loss Watt
Switching Components:				
Thyristors and Diodes (30 g)	360	60	600	60
Capacitors:				
Series, C_1	140	2	140	2
Input Filter C_i	200	1	390	1
Output Filter C_o	200	1	200	1
Magnetic Components:				
Series Inductor L_1 (L_{1i};135g)	540	35	1350	35
Power Transfomer	1300	18	1300	18
R_dC_d dv/dt Networks (40 g)	160	30	400	30
Wiring, Connectors and Misc. Electric Mat'ls	1000	25	1000	25
Totals	3900	172	5380	172

The efficiency of the two systems

$$\eta \simeq 3000/3172 \simeq 0.946 \qquad (2.92)$$

is the same, because of the "time sharing" use of the added components.

IV - 2.6. The Control Electronics

The electronic protection system follows, in principle, the philosophy which is being applied for dc converters of this type: To identify, positively, the accomplished turn-off of the companion thyristor(s) which could cause a short circuit path for the source current |1,5| . The complexity which is added over that needed for a dc converter of the same type is described in the two preceding reports, prepared in the same program. The experimental implementation of the gating procedure, needed for the above referred to purpose, proved to be the most difficult part of the program as a whole. Yet, it posed no other problems than those associated with thorough design and engineering.

The firing signals to each of the 16 thyristors are gated by a "memory" mechanism as described in the preceding Concept Verification Report (CVR) with reference to its Figs. III-2.4 & 2.7. Both figures are reproduced here for convenience as Figs. IV-2.6 and 2.7, respectively. Fig. IV - 2.7 presents a logic schematic of the electronic network and control needed for a dc converter with power transfer in one direction. Fig. IV - 2.4 shows a

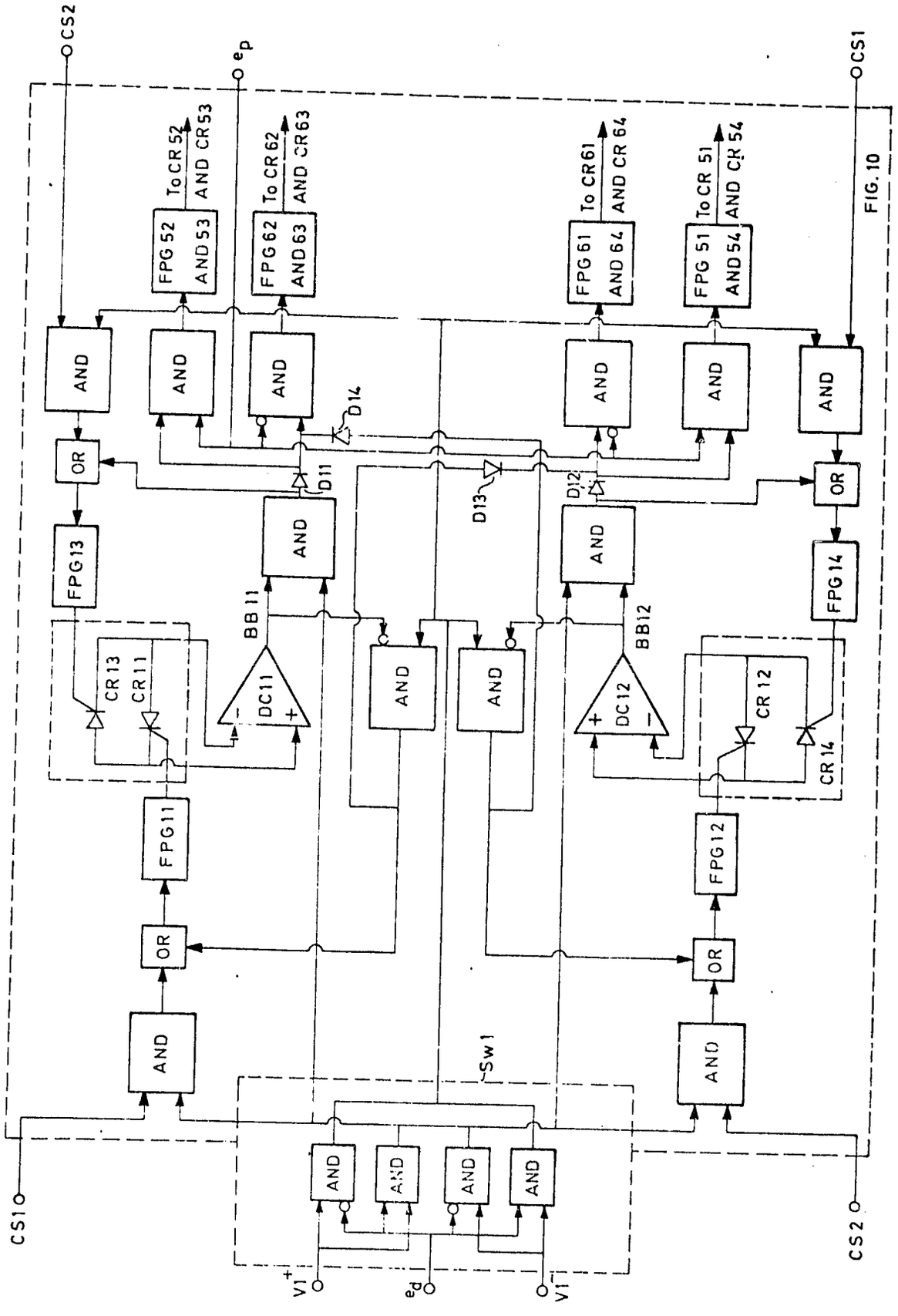


Fig. IV - 2.6.

Functional schematic of one of the three Gating and Firing Systems

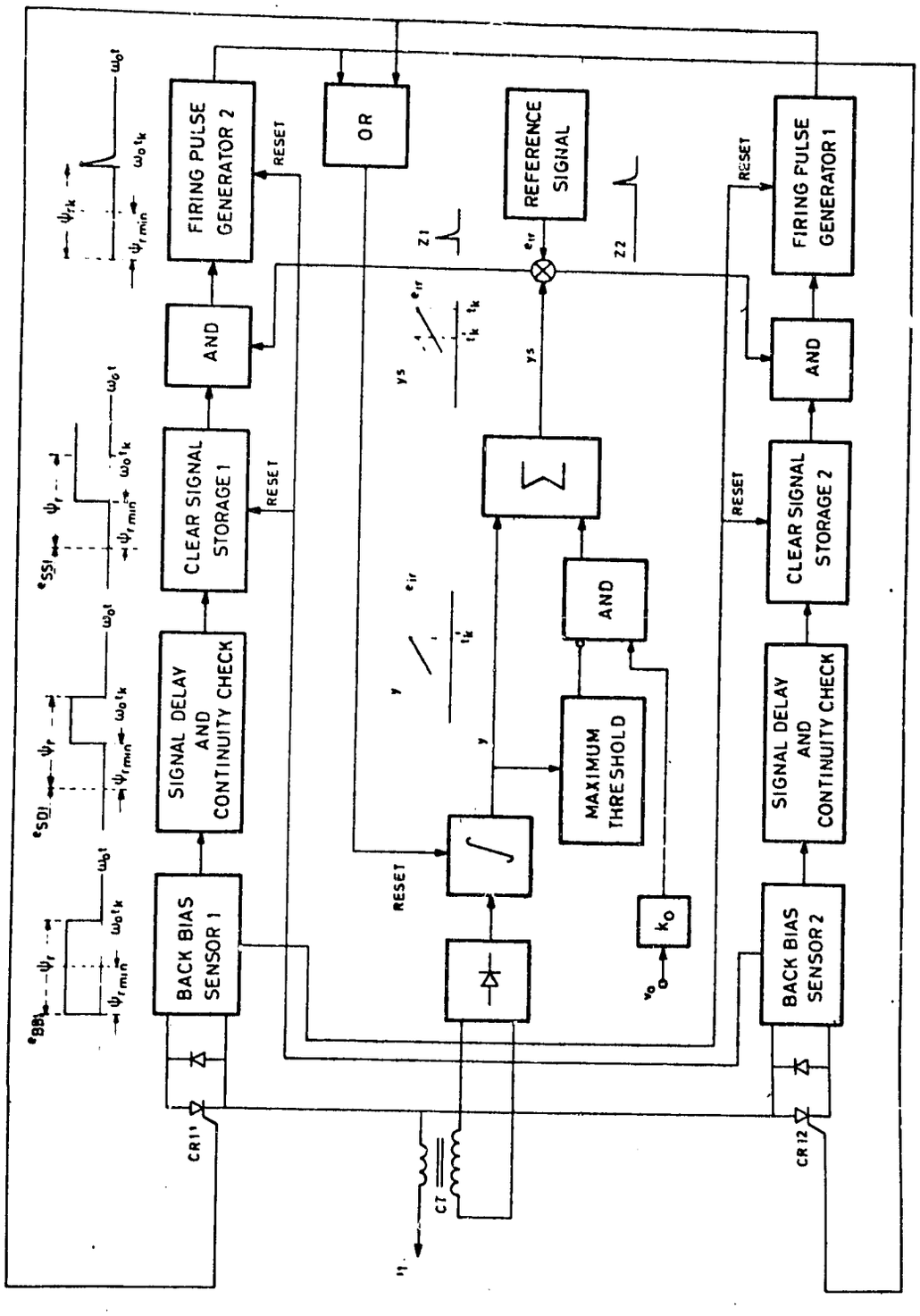


Fig. IV - 2.7.

Functional schematic of the control and protection system.

more detailed logic diagram, enlarged for purpose of bidirectional power transfer.

Each of the thyristors had to be provided by one of the two gating channels shown in Fig. IV-2.7. This "thyristor" signal gating channel was devised to also change to a "diode" gating channel, whenever the respective thyristor was required to perform the analog of a diode function in a dc converter. It means that the diode function performing thyristor would work with its cathode against a positive potential in one of the phases of the three phase ac system.

Twelve of the 16 memory gating systems, as referred to above, are governed jointly by a phase gating circuit of the three phase system. The other four thyristors are governed by a selection switch which determines the state of forward or reverse transmission of power as defined and described in the preceding report which were prepared in this program.

The power control system is devised as a common ASDTIC system, which is amply described in the literature [6,7]. This system supports the performance of the converter as an active filter system for the purpose of removing the 360 Hz ripple without the need for a bulky low pass filter.

IV - 3. Engineering Assessment and Evaluation

The significance of the here presented new technology is assessed with tne use of the following criteria:

(1) What are the unique and useful external characteristics of this new technology;

(2) What are the internal technological advantages which would affect the significant aspects of equipment, such as: reliability, physical weight and cost.

The following discussion draws on the material presented in the preceding part of this report, in the Concept Formulation Report and in the Concept Verification Report (CVR), prepared as part of the same program.

IV - 3.1. Unique and Useful External Characteristics

Reference is made to Fig. II-2.1 in the CFR and the thereto pertaining discussion of the three phase ac/dc conversion and control process. This illustration is reproduced here for convenience as Fig. IV-3.1. Three of the significant technical problem areas which are associated with the here discussed technology are being singled out in the following:

(a) The combined effects of the power factor and the harmonic content of the ac current in the individual phases:

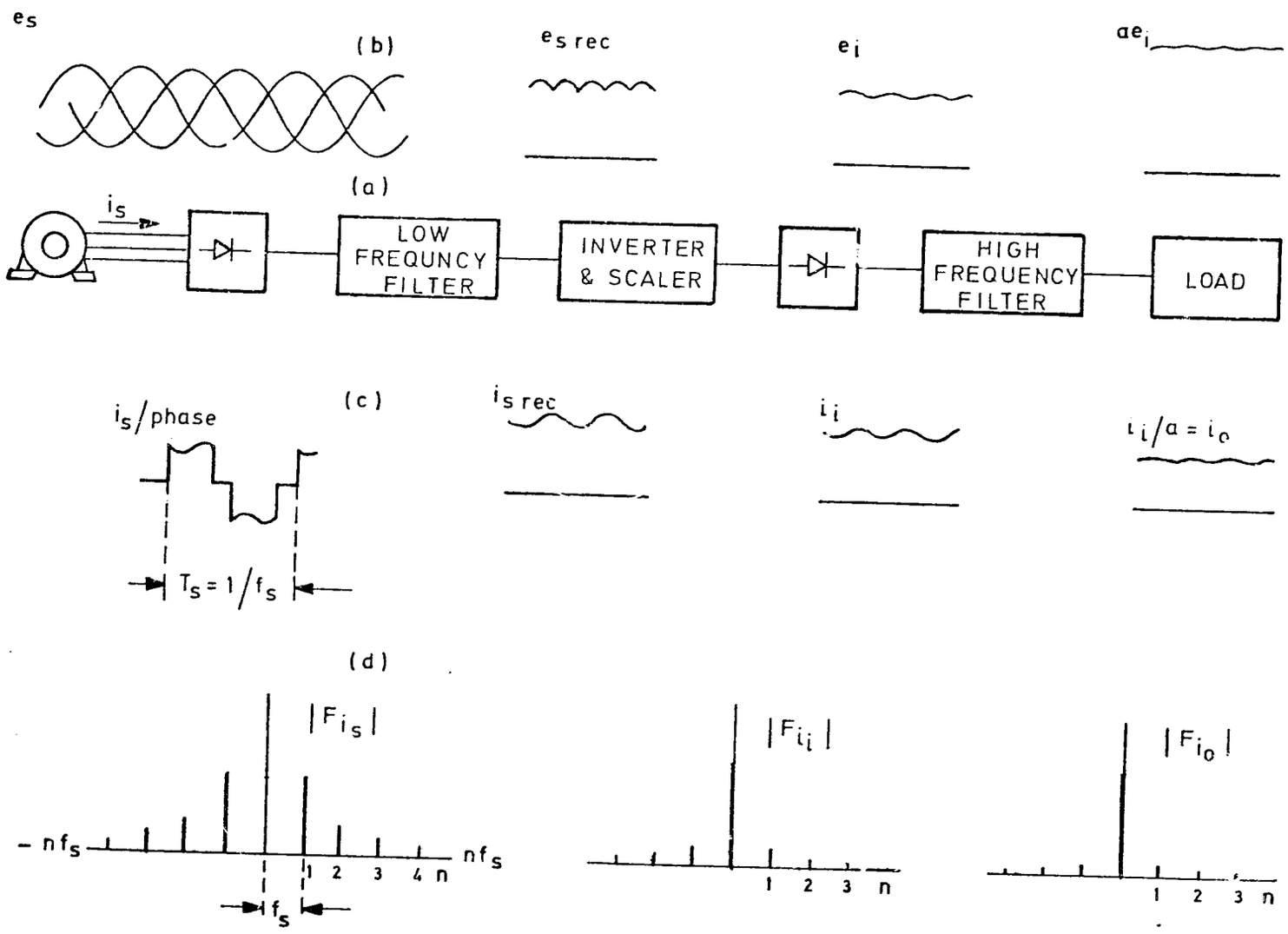


Fig. IV - 3.1.

(a) Symbolic system block diagram, (b) significant system voltage waveforms, (c) significant system current waveforms, (d) current waveform frequency spectra.

(b) The needed size and effects or the passive filters, required for ac ripple suppression;

(c) The capability for speed of response to externally imposed dynamic conditions.

A summary characterization of the system behavior in the above enumerated areas is now presented in the same order.

IV - 3.1.1. Power Factor and Harmonic Content in the AC Supply System.

The power factor, as viewed from the ac supply system, remains near its theoretical maximum of 0.955 for the combined conditions of supply voltage variations and lo ng; this incl·des load variations from zero to partial to full load, all stages of progressive overloading and conditions of short circuited output terminals. Conversely, the power factor remains near the same theoretical maximum, when the direction of power flow is reversed. The respective, experimentally obtained data are comprised in Table III - IV and III - V.

The deviation of the experimentally obtained data from the theoretical maximum is attributed, primarily, to two reasons: (1) the need to shape the phase currents for the purpose of removing the 360 Hz ac line ripple, as discussed with reference to Figs. IV-2.2 and 3.3 further on in the section IV - 3, and (2) the inaccuracies of readings which is

caused by a "soft" three phase Variac source and the interference of the 20 kHz ripple voltages with the acquisition of low frequency data. The first named effect should be restricted to one or two percent of the power factor reading. The contribution of the second named effect to a reduction of the power factor appears comparable, since the actually measured power factor was well above 0.9, as contained in the above referred to Table III - IV.

The harmonic content of the phase currents approaches the same content caused by a full wave diode bridge. followed by an infinitely large inductor. In reality, there is no low frequency inductor at all in the network of the ac/dc converter: suppression of the low frequency ripple is achieved, exclusively, by way of an active filtering process. The shape of the waveforms of the phase currents is not altered by the degree of loading or by variations of the input voltage. The harmonic content of the phase currents remains, therefore, unchanged at its minimum for ac/dc power conversion, independent of externally imposed conditions.

The highest possible power factor appears to be advantageous for ac/dc power conversion, or its converse. There are certain applications in which other power factors appear desirable or necessary. This includes the connection to reactive ac networks and, possibly, the correction of the power factor in an ac supply line, caused by other system components. The power factor in the individual phases is altered by advancing or retarding the classical rectangular current block from its centered position under the crest of the ac voltage, as shown in Fig. IV - 2.2.

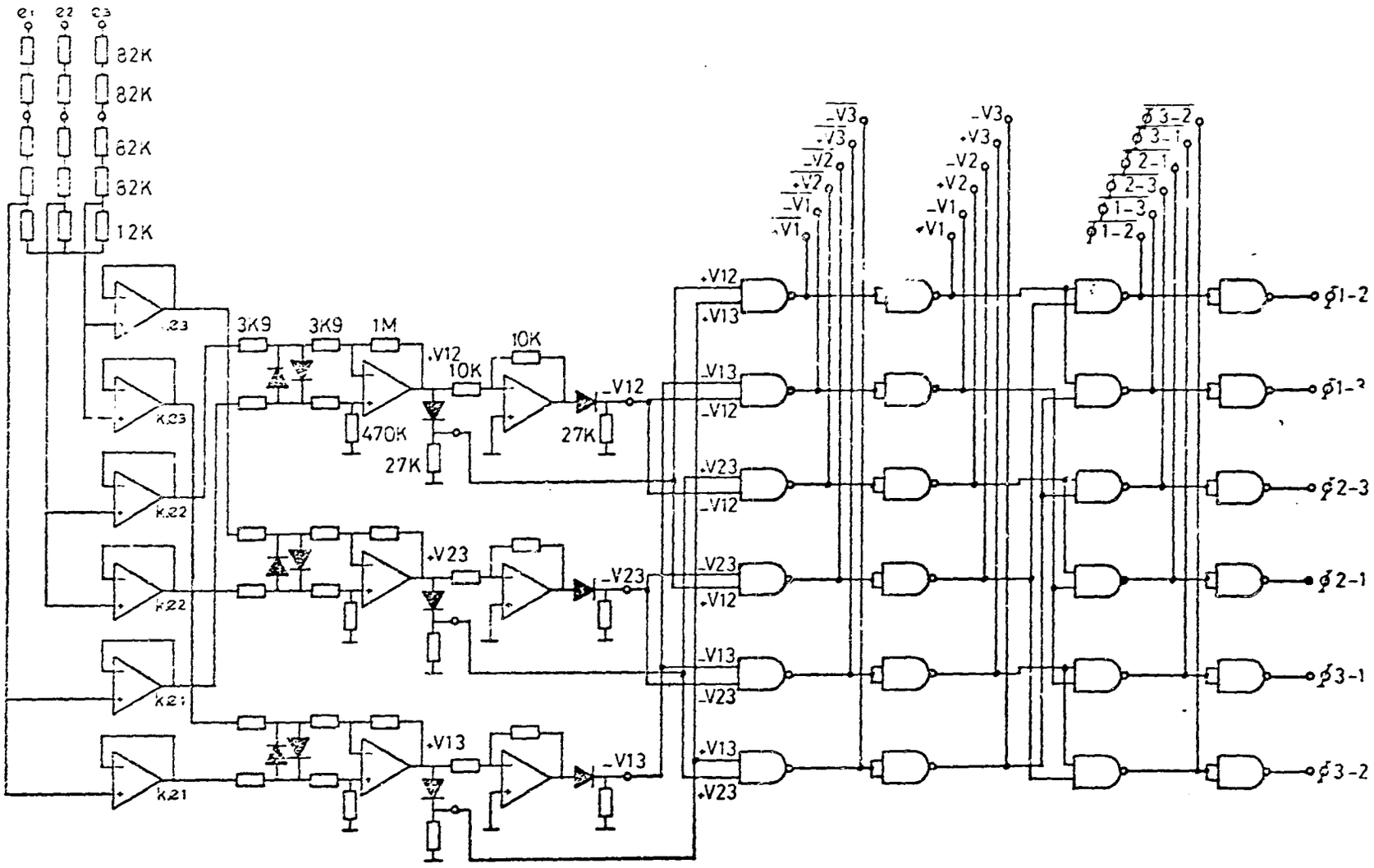


Fig. IV - 3.2.

Simplified electronic schematic of the logic for the generation of selection signals for the thyristors of the three phase cyclo-converter.

The above referred to shift in time of the alternating current in each phase of the supply line is achieved by advancing or retarding the function of the phase voltage discriminators of the phase gating system, which was presented and discussed with reference to Fig. III - 2.3 and is reproduced here for convenience as Fig. IV - 3.2.

One possible form of implementation of shifting of the phase currents i_{si} (i = 1,2,3) with respect to their phase voltages e_i is now discussed with reference to Fig. IV - 3.3.

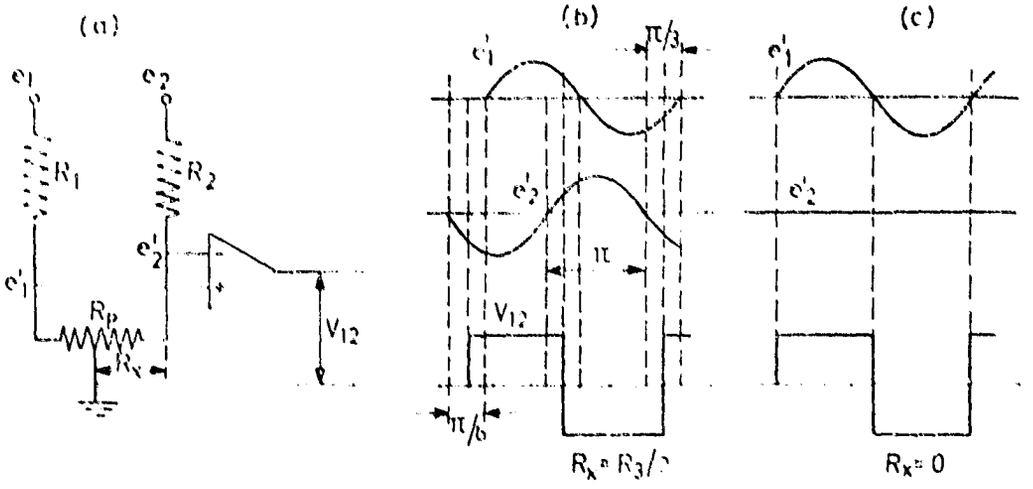


Fig. IV - 3.3.

(a) Symbolic schematic of a controllable phase voltage discriminator; its significant voltage waveforms (b) for zero phase shift and (c) for 30 degrees ($\pi/6$ radians) lagging of the phase current i_{si}.

The voltage discriminator shown in this figure performs now the function of the highest in the second vertical row of voltage discriminators, as viewed from the left of Fig.IV-3.2. The first vertical row of buffers shown in Fig.IV-3.2 has been deleted for convenience of presentation. Each of the individual phase voltages e_1 and e_2 is connected to the equal resistors $R_1 = R_2$, respectively.

The input terminals of the voltage discriminator with the output voltage v_{12} are connected to the second terminals of the named resistors R_1 and R_2, respectively. A "potentiometer" with a total resistance R_p connects the two above referred to input terminals of the voltage discriminator. If the "wiper" of the potentiometer which is connected to the ac ground divides the resistance R_p in two equal halves, then the voltages e_1' and e_2' are attenuated replicas of e_1 and e_2, respectively. If the symbolic schematic as shown in Fig.IV-3.3 is considered as the above indicated part of Fig.IV-3.2 and if the resulting control signal of Fig. III - 2.1 is brought into the appropriate context, then the signal v_{12} in Fig.IV - 3.3 (b) is consistent with the signal v_{12} in part (b) of the named Fig. III - 2.1.

If, however, the "wiper" is moved all the way to the right, so that $R_x = 0$, then the signal v_{12} is delayed by $\pi/6$ radians with respect to its former, above described, position. This is illustrated in Fig. IV - 3.3(c). If the "wiper" is moved all the way to the left so that $R_x = R_p$, then the signal v_{12} will "lead" its position shown in Fig.IV - 3.3(b) by $\pi/6$ radians and thus also the one shown in part (b) of Fig. III - 2.1.

The signal v_{12} can thus be moved to any intervening position, where its leading edge coincides with the zero crossing of e_2 when $de_2/dt < 0$, to a point where its trailing edge would coincide with the zero crossing of e_1 when $de_1/dt < 0$. Yet, the signal v_{12} maintains a width π, when normalized in radians. The above described "movement" of position is caused by positioning the "wiper" at the appropriate spot on the "potentiometer".

The signals v_{13} and v_{23} which are indicated in parts (c) and (d) respectively of Fig. III - 2.1 can be "moved" by a process which is analogous to the one which was described above. If the three potentiometers with individual resistances $R_{p1} = R_{p2} = R_{p3}$ were moved by a common shaft so that $R_{x1} = R_{x1} = R_{x1}$ and $R_1 = R_2 = R_3$, then all of the signals v_{12}, and v_{23} could be shifted synchronously by up to 30 degrees or $\pi/6$ radians ahead or back in time when compared to their position shown in Fig. III - 2.1.

The symbolisms of "potentiometers" and "wipers" were used here for purpose of simplification of explanation. An electronic equivalent of the symbolic schematic of Fig. IV-3.3(a) would be used in an actual implementation of such a system.

A shift in time of the signals vi^+ and vi^- (i = 1,2,3), illustrated in parts (e) through (j) of Fig. III - 2.1, with respect to the power voltage signals e_i of part (a) of the same figure, causes a time shift of the phase currents i_{si} with respect to their phase voltages. The voltage of one phase, the unfiltered succession of phase current pulses and their filtered version are symbolically indicated in Fig. III - 2.6.

The case of "reverse" power flow for zero phase shift is illustrated th re. In the following discussion it is assumed for the purpose of convenience of presentation, that the phase currents i_{si} have an ideal rectangular form of $2\pi/3$ length, are separated by a zero current time interval of $\pi/3$ from their likewise rectangular negative counterpart of $2\pi/3$ length, and so on. This is consistent with the presentation of related topics in the literature and can be expanded to other than rectangular waveforms.

The effects and the functional principles of the system for phase shifts of the rectangular currents beyond $\varphi = \pi/6$ or 30 degrees is now discussed with reference to Fig.IV-3.4. A number of characteristic cases of "phase shift" of the current i_{si} with respect to the thereto pertaining phase voltage e_i is depicted in stylized form in the named illustration. The momentary power P^*_{si} and their average $P^*_{si\ av}$ in the individual phases are added for the purpose of elucidation of the presentation; this information is augmented by an indication of the direction of power flow in the form $\text{sign}(P^*_{si})$.

The various aspects of phase shift are discussed for the case of "forward" power transfer from the source of ac power to a dc load. The case of "reverse" power transmission is then derived therefrom as the functional converse which involves analogous principles.

Parts (a) through (d) illustrate the conditions which occur in the individual phases for the case of forward power transfer at the maximum power factor.

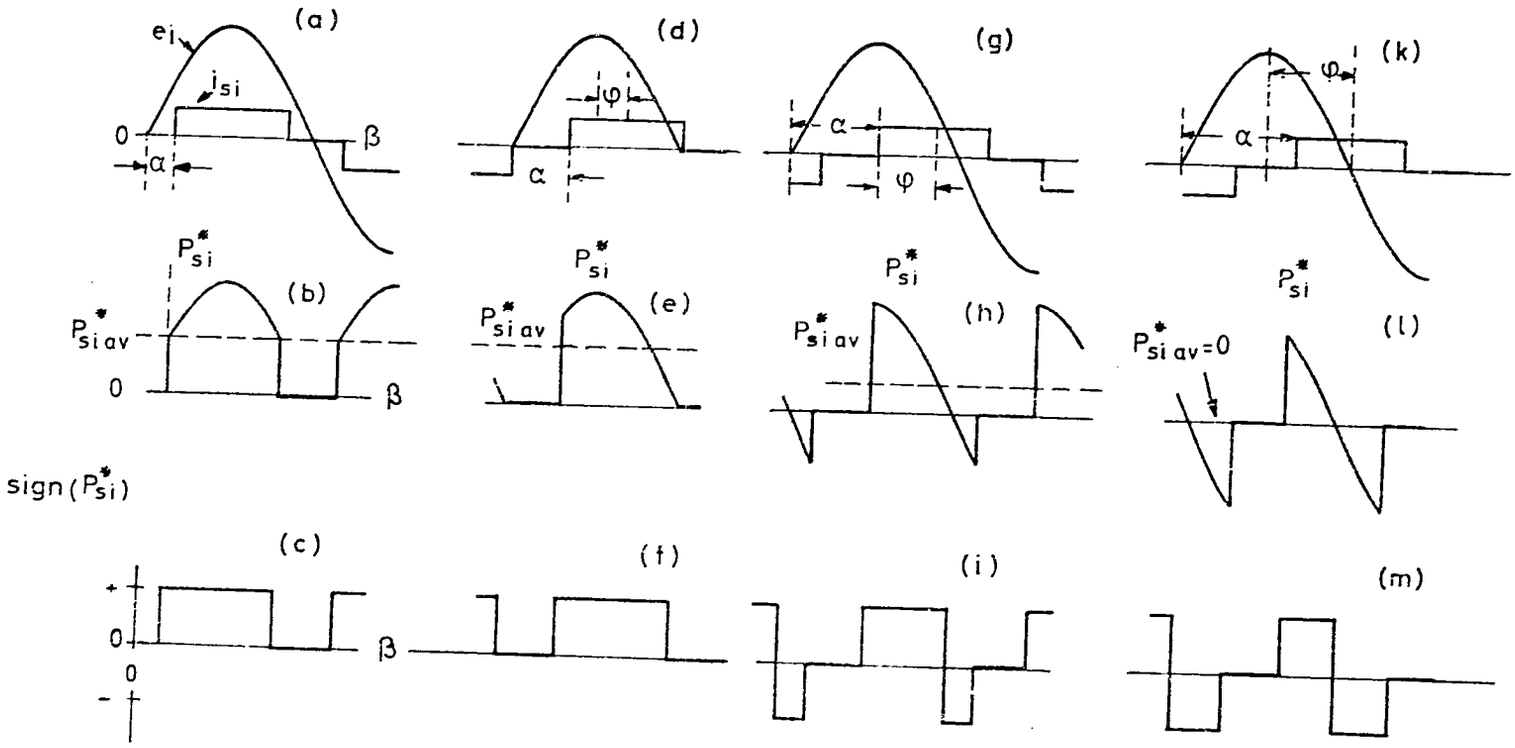


Fig. IV - 3.4. Stylized waveforms of the voltages e_i (i = 1,2,3), the currents i_{si}, the momentary power P^*_{si} and the average power $P^*_{si\,av}$ in the individual phases of the ac supply for phase shift angles $0 < \varphi < \pi/2$ of the current blocks i_{si}, with indication of the thereto pertaining direction of momentary power flow sign(P^*_{si}).

The rectangular block of current i_{si} with a normalized length of $2\pi/3$ finds itself at a time angle $\alpha = \pi/6$ after $e_i = 0$ and $de_i/dt > 0$. The same time angle $\pi/6$ separates this current block from the point $e_i = 0$ and $de_i/dt < 0$. The phase angle φ of this "centered" block of current is measured between the vertical center line of e_i for $e_i > 0$ and the center line of the rectangular current block; this angle $\varphi = 0$ in part (a) of Fig. IV - 3.4.

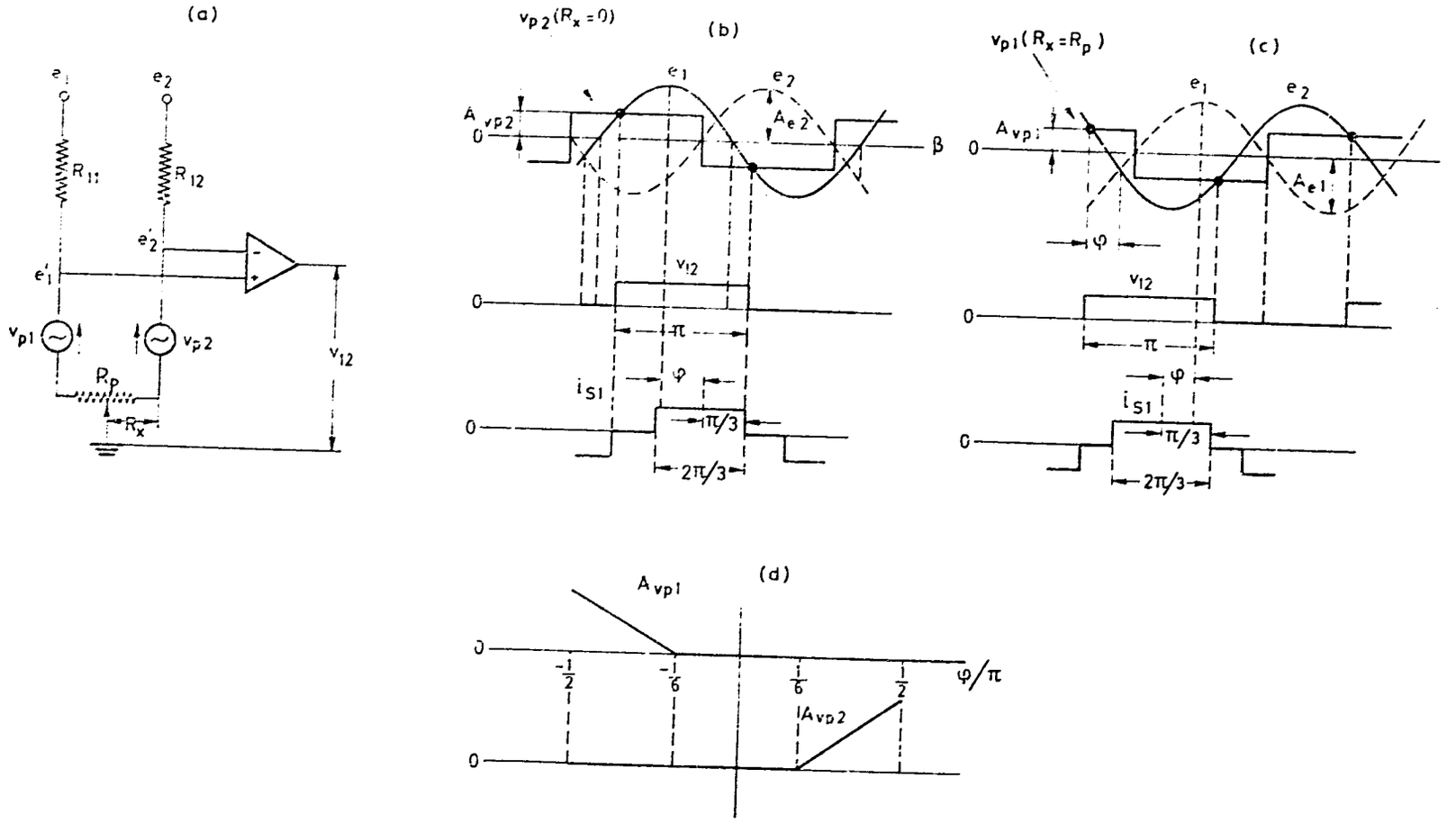
The momentary product

$$P^*_{si} = e_i i_{si} \tag{3.1}$$

is shown in part (b) of the same figure. The average power transfer per cycle

$$P^*_{si\ av} = (1/\pi) \int_0^{\pi} e_i i_{si}\, d\beta \tag{3.2}$$

is indicated by way of a horizontal broken line in figures (b), (e), (h) and (l) of Fig. IV - 3.4. The wave shapes of the momentary power P^*_{si}, as shown in the same figures, are not meant to yield information on the instantanous magnitudes of P^*_{si}, but to indicate the character of the concerned waveshapes. The momentary direction of power transfer is indicated through the sign of P^*_{si} for each of the given cases. No information on the magnitude of P^*_{si} is meant to be conveyed by the parts (c), (f), (i) and (m) of the same figure. The forward direction of the flow of energy from the source of ac power to the dc load is illustrated in Fig. IV-3.4(c). The phase voltage and its current, as illustrated in Fig. IV-3.4(d), indicate a lagging current phase angle of $\pi/6$. This is the borderline case for which the direction of power transfer remains unidirectional at all times, as seen from Fig. IV - 3.4(f).



Pig. IV - 3.5.

(a) Symbolic schematic of the discriminator for voltage e_1 and e_2 with one mechanism for shifting the current phase angle $\varphi \gtrless 0$; (b) and (c) the thereto pertaining waveforms and (d) control signal voltages.

Enlargement of the phase angle beyond $\varphi = \pi/6$ of a current "block" with duration $2\pi/3$ requires a reversal of flow of the momentary power P^*_{si}, as illustrated in parts (g), (f) and (i) of Fig.IV-3.4. The converter transfers energy from the ac supply to the dc load as long as $P^*_{si} > 0$. This means as long as e_i and i_{si} have the same polarity. If $i_{si} > 0$ for $\pi < \beta < 7\pi/6$, while $e_i < 0$ in the same time interval, then $P^*_{si} < 0$ and energy is being returned to the ac supply.

The process of shifting the phase current by $\pi/6$ radians by way of application of means of control in the electronic logic was described above with reference to Fig.IV-3.3. One way to enlarge the phase angle $\varphi > \pi/6$ is described with reference to Fig. IV - 3.5.

Part (a) of Fig.IV-3.3 is modified by the addition of a voltage source v_{p1} in the attenuator of e_1 and another voltage source v_{p2} in the attenuator of e_2, as shown in this illustration. The voltages of the v_{pi} (i = 1,2) are square waves with amplitudes A_{vpi} whose magnitude will be discussed with reference to part (d) of Fig.IV-3.5. This amplitude is a function of the phase angle φ. The magnitude of the A_{vpi} and the position in time of the v_{pi} with respect to the phase voltages e_1 and e_2 is explained in Fig.IV - 3.5. The amplitude

$$A_{vpi} = 0 \qquad \text{for } -\pi/6 < \varphi < \pi/6 \tag{3.3}$$

as explained before with reference to Fig.IV-3.3. It is recalled here that an electronic analog of the symbolic "wiper" can be "moved" by a control signal which is proportional to the phase angle φ.

This signal is now referred to as c_φ; it can be a manual input via the single shaft which controls three potentiometers, or it can be a signal that is derived from the conditions in the power circuit. The response to the signal c_φ corresponding to $\pm\pi/6$ is the "movement" of the "wiper" with $A_{vpi} = 0$ as stated in (3.3). The square wave voltage

$$v_{p2} = k_s(\varphi - \pi/6)A_{e2}\,(-1)^k \qquad \text{for } \varphi > \pi/6; \tag{3.4}$$

where

k_s = a constant of proportionality;

k = the order number 1,2, ... of each succeeding half sine wave of e_2, starting with a positive half wave.

The square wave voltage v_{p2}, as defined by (3,4) has the opposite polarity of e_2 at any time. Its amplitude A_{vp2} is proportional to the factor $(\varphi - \pi/6)$ and to the amplitude A_{e2} of e_2. This square wave appears as e_2' in Fig. IV - 3.5 (a) because $R_x = 0$ when $\varphi \geq \pi/6$.

The effect of the signal c_φ is further elucidated by the part (d) of Fig.IV-3.5. The voltage v_{p2} is zero in the interval $-\pi/2 < \varphi < \pi/6$; its amplitude A_{vp2} then increases for $\varphi > \pi/6$ in accordance with (3.4). Fig. IV - 3.5(b) shows how the voltage v_{12} is delayed beyond $\varphi = \pi/6$ by increasing the amplitude A_{vp2} since the intersection of e_1' with v_{p2} is further delayed with respect to e_1. The linear increase of A_{vp2} with φ/π in Fig.IV - 3.5(d) is a simplified presentation of a curve which in actuality contains a sinusoidal element for the purpose of linear proportionality between the signal c_φ and the resulting phase angle φ.

The phase angle φ can be shifted in the described way by $\pi/2$ and beyond. The power factor p.f. = 0 for $\varphi = \pi/2$.

A leading phase angle φ byond $-\pi/6$ is attained by letting $R_x = R_p$ and then increasing A_{vp1}, as indicated in Fig.IV - 3.5(d). The arguments for that purpose are analogous to the ones made for the case of $\varphi > \pi/6$. The voltage

$$v_{p1} = k_s(\varphi - \pi/6)A_{e1}(-1)^k \qquad \text{for } \varphi < -\pi/6 \tag{3.5}$$

with the analogous interpretation of symbols as defined below equation (3.4). The phase angle φ can be shifted back in time to $-\pi/2$ and beyond, as illustrated in Fig.IV - 3.5(c). The power factor p.f. = 0 and leading when $\varphi = -\pi/2$.

It was indicated in Fig.IV-3.4 that the direction of transfer of energy reverses when the absolute value of the phase angle $|\varphi| > \pi/6$. The electronic control system is so organized that if the signal c_φ requests that $|\varphi| > \pi/6$ and the voltage sources v_{pi} have to get into action, then the electronic control mechanism for the transfer of energy provides the possibility for reversal of the process, so that power can be returned from the converter to the three phase ac system. The principles for reverse transfer of power were presented in subsection III - 2.1.2. The same principles are applied in the case when $|\varphi| > \pi/6$. The transition from the forward to the reverse state or vice versa takes place near the time when $|\varphi| = \pi/6$ or when $e_i \simeq 0$. If signal v_{12} causes the start of the current i_{s1} at a time when $e_1 < 0$, then the direction of power transfer is "reversed" until $e_1 \simeq 0$ and $de_1/dt > 0$. The transmission of power then changes to "forward". The converse happens in the case of a required lagging phase angle $\varphi > \pi/6$.

The arguments which were made above apply, of course, to all signals v_{12}, v_{13} and v_{23} and the therefrom derived logic signals for the operation of the system. Also, do the analogous arguments apply for any phase angle $-\pi/2 < \varphi < \pi/2$ when transferring power from a dc system to a three phase ac system. The definitions of "forward" and "reverse" are then interpreted accordingly.

It is recalled here that the power factor p.f. is defined in the time domain [11] as

$$\text{p.f.} = \frac{(1/\pi) \int_0^{\pi} e_i i_{si} d\beta}{e_{i\ \text{rms}}\ i_{si\ \text{rms}}} \tag{3.6}$$

This general expression for a power factor reduces to p.f. = cos φ if e_i and i_{si} are defined as sinusoidal waveforms. This power factor is independent of the amplitudes of e_i and i_{si}. For purpose of simplicity of presentation it is, therefore, assumed that

$$e_i = \sqrt{2} \sin \beta \tag{3.7}$$

and

$$i_{si} = \begin{cases} (-1)^k & \text{for } \pi(k + 1/6) < \beta < \pi\ (k + 5/6) \quad k = 0,1,2 \ldots \\ 0 & \text{everywhere else} \end{cases} \tag{3.8}$$

The angle α is defined as the time interval between the point when $e_i = 0$, $de_i/dt > 0$ and the leading edge of i_{si}, as illustrated in Fig. IV-3.4. In the defined symbols is

$$\alpha = \varphi + \pi/6 \tag{3.9}$$

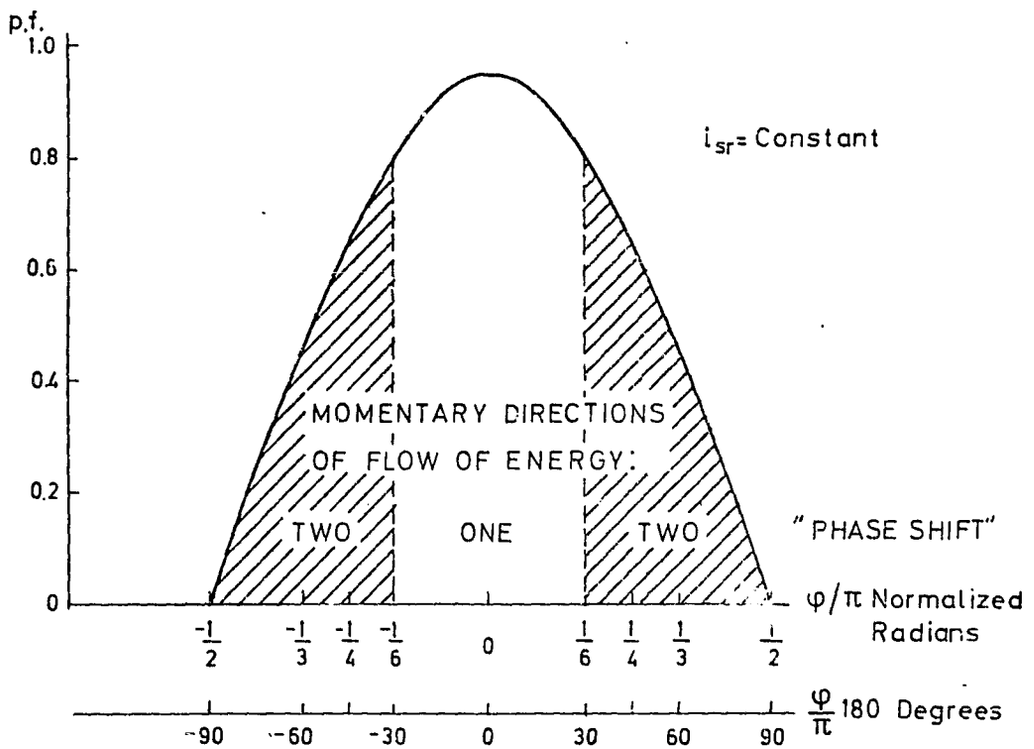


Fig. IV - 3.6.

The power factor p.f. as function of the phase angle φ of a rectangular form alternating current i_{si}.

The expressions (3.7) and (3.9) are used in (3.6) in order to calculate the power factor

$$p.f. = (3/2\pi)\{\sqrt{3}\cos\alpha + \sin\alpha\} \qquad (3.10)$$

The results of a numerical evaluation of (3.10) for i_{si} of the form defined in (3.8) are presented in Fig. IV - 3.6. The number of directions of the flow of energy at the interface with the three phase system during one low frequency current half cycle is indicated in the figure as function of the normalized phase angle φ/π. The range of the power factor p.f. extends from zero leading over its maximum 0.955 to zero lagging.

The above described variation of the power factor allows operation in all four quadrants of the ac system. The above enumerated system characteristics are unique for any realizible ac/dc converter, which otherwise would require a finite size input filter and thus cause lower power factors and higher harmonic contents of the currents in the phases of the three phase supply system [8].

The here presented system embodies the significant external characteristics of this type of dc/dc converters. It will operate from a three phase ac supply into a converter of the described type when its dc output terminals are short circuited. The resonant circuit "looks back" into an apparent dc supply source with voltage e_s^* as illustrated in Fig. IV - 3.7. The system then behaves as a dc converter with short circuited output terminals. The system admits in this case only the power losses of the converter, as amply described in the literature [1,2,3,5].

If the output terminals are left open, then the output voltage limiting function of the control system will reduce the intake of power to a trickle to cover the sparse power losses in the converter under these conditions [1,2,5].

Analogous situations arise under conditions of "reverse" power transfer when the three phase network is short or open circuited. The energized series resonant circuit "sees" one pair of short circuited output terminals at one time, provided that the three phase character of its "output terminals" is governed by an internal three phase reference source, which in turn energizes the phase gating circuit, as was described with reference to Fig.IV-3.2 above. The above referred to terminal pair, which is energized at that time, behaves identical with the output terminal pair of a dc converter under these conditions. This characteristic is transferred to the output terminal pair which follows in time, and so on. The converter thus behaves as a true current source, also when working into a short circuited three phase system.

An open circuit in the ac system is also viewed as an open circuit in the output terminal pair of a dc converter for the duration of operation ($2\pi/3$) of one phase pair. The converter behaves as a voltage limited current source, according to the directives received by its three phase reference source. This behavior is then cyclically transferred to the successively following phase pairs. The converter behaves in this sense analogous to the dc/dc converter counterpart, as well documented in the above cited literature.

The waveform of the individual phase currents i_{si} can be taylored

(a) for the purpose of a suitable compromise between the (1) resulting effectiveness in energizing the load, (2) harmonic content of these currents in the supply lines and (3) simplicity of functional requirements in the converter;

(b) independent of the degree of loading, progressive overloading, even to the point of short circuited output terminals of the converter;

(c) independent of the phase angle φ as required by the prevailing conditions in the ac system, in addition to desired or programmed phase angle conditions.

The significance of the preceding statement is the newly created freedom to treat each of the named effects, independently, rather to have these connected by an inescapable causally necessitated interdependence.
The latter is the case in all conventional low frequency ac/dc thryristor bridge control mechanisms. The effects of loading, which include its degree and characteristics dictate, furthermore, the mode of operation of the thyristor bridge and are then inseparably intertwined.

It speaks for itself that the freedom to cope with each of the above named effects separately and independent of the other named aspects, provides valuable options to ameliorate or eliminate undesirable consequences thereof.

To illustrate the above made statements it is reiterated here that variations

of the level of power transfer for otherwise given conditions in either direction do not necessitate an alteration of the phase angle φ; neither does a variation of the converter's output voltage. As a matter of fact, only specific three phase load or supply line requirements should ever necessitate a phase angle $\varphi \neq 0$. In other words: shifting of the current phase angle φ is no more needed as means of power control. Application of a phase angle $\varphi \neq 0$ is at this time relegated to the purposes of reactive ac loads, such as induction motors and of intended power factor correction in polyphase ac lines in need thereof.

One advantage of the use of the discussed converter should, therefore, be seen in the light of the reduced significance of the phase angle φ. The option to shift the current phase angle φ beyond moderate limits such as $-\pi/6 < \varphi < \pi/6$ could suffice in many cases, even though the principles for larger phase shifts have been explained above.

The harmonic content of the phase currents can be independent of the phase shift φ. If one views the "rectangular" waveform of the currents i_{si} as indicated in the Figs.IV-3.3 and 3.5, then it becomes evident that their harmonic content is independent of the phase angle φ.

Conversely, it is possible to taylor the phase currents in any desired fashion that is compatible with the load or line requirements in the ac system. This is a unique and utterly useful feature of the new, here presented system.

The current i_{si} can be initiated, taylored to desirable waveshapes and terminated at any time. The potential for the generation of continuous sine wave currents is noted only in passing here.

IV - 3.1.2. The Active Filtering Effect

The current i_{si} in the i-th phase of a three phase ac supply is indicated in Fig.IV-2.2(b). This current is caused by a full wave bridge rectifier system, followed by an "infinitely large" low pass filter, as illustrated in Fig.IV-3.1. The apparent dc voltage e_s^*, which appears at the input terminals of that filter is shown in Fig.IV-2.2(a). It consists of the dc voltage component $e_{s\,av}^*$, augmented by the characteristice ac ripple. The rectified current i_{sr} of Fig.IV-2.2(a) is then a constant, as not to cause a ripple in the output voltage v_o. The size of an "infinitely large" input filter inductor L_i causes the flow of a continuous, ripple free current through this inductor. The output voltage v_o is then ripple free. The sum of the real and reactive power P_s which enters the low pass filter is shown in Fig. IV - 3.3(a).

Another philosophy of power processing is indicated in the waveforms shown in Fig.IV-3.3. The ripple waveform of the rectified current i_{sr} of Fig. IV - 3.3(a) is a mirror image of the ripple contained in e_s^*. The power P_s of the same figure, entering the converter is now a constant, and so is the output voltage v_o, shown in Fig.IV-3.3(c). The phase currents i_{si} are derived from the rectified current i_{sr} and thus embody its ripple content.

Analysis of the power factor for these conditions shows that:

$$p.f. = \frac{\frac{1}{T}\int_{o}^{T} e_s^* i_{si} dt}{e_{s\ rms}^* \ i_{si\ rms}} \simeq 0.937 \qquad (3.1)$$

This is, approximately 2% below the maximum power factor of 0.955, calculated for the ideal current waveform shown in Fig. IV - 3.3(b). Similar considerations apply for the harmonic content of the two above discussed current waveforms.

The peculiar current waveform i_{si} of Fig.IV-3.3(b) is caused by application of the formerly referred to ASDTIC control principle |6,7|. The ensuing process of pulse modulation of the resonant current carrier i_1 with a maximum frequency of 10 kHz, results in a train of (20 kHz) rectified pulses whose ampere-second content per unit of time is a predetermined constant for each closed pulse interval. Pumping of a time invarying current

$$i_o = |i_2|_{av} = |i_1|_{av}/a = k_r i_r/a = \text{constant} \qquad (3.2)$$

into a time invarying constant load, causes a "ripple free" output voltage v_o within the boundaries of tolerance, explained in subsection IV-2.3 of this report. The residual maximum excursions v_{cpp} of the 20 kHz ripple of the output voltage v_o is determined by the size of the filter capacitor C_o, which at that frequency remains restricted to a moderate physical size.

The time varying amplitude of the oscillation of the voltage and current in the resonant circuit, which is caused by the ripple of the apparent input voltage e_s^*, indicates a pattern of recurrently repeating changes in the state of maximum energy storage in the components of the series resonant circuit. This continuously changing state of energy is part of the mechanism with which the converter's incoming power

$$P_s = e_s^* i_{sr} \tag{3.3}$$

is kept constant, even though e_s^* varies periodically in magnitude.

The result of the above described process is a unique nondissipative active filtering process, which is part of the transformed ac/dc power conversion. This process removes the need for heaviest system components, the low pass input filter, which have been heretofore considered to be an indispensible functional necessity for efficient ac/dc power conversion [8,9].

IV - 3.1.3. Speed of Response

The lower bound for the response time of any signal transforming equipment is limited by the largest time constant of the filters which are being used in the process of signal transformation. This includes the processing of power "signals" in the form of the therewith associated voltage and current waveforms.

It follows that the speed of response of a power converter using one or more passive low pass filters for the purpose of ripple suppression is, as a rule, approximately, one order of magnitude slower than the slowest suppressed ripple signal.

The above made statement does not apply to an active filter. If the active filtering mechanism is used to remove low frequency components by way of processing continuous signals then the upper cut off frequency of response is limited by the cut off frequency of the active components. The use of a pulse modulation process as part of the internal signal processing mechanism of an active filter requires the removal of the high frequency content which is caused by the mechanics of the pulse modulation process, not including the elements of the modulating signal.

The response time of the active filter is then limited by the low pass filters which remove the above referred to high frequency content. The result of the application of a modulated high frequency pulse train is then the frequency transformation of the used low pass filters from the low frequency content - 360 Hz - of the processed signal to the cut off frequency needed for the high frequency of the modulated carrier at 20 kHz. If the low pass filters have a cut off frquency that is one order of magnitude lower than that of the processed signal, then this cut off frequency of the included low pass filter is raised from 36 to 2000 Hz. The response time of the system is, accordingly, raised to approximately one quarter of the period of the cut off frequency, and is well below 1 msec. The fast

response of an ac/dc converter, as presented here, is unique. No other ac/dc converter can approach the above stated speed of response.

Each of the individual above discussed converter characteristics is unique and useful. Their concurrent embodiment in one single converter increases its usefulness and reinforces its uniqueness. All above made arguments apply, equally, for either direction of power transfer, whether from ac to dc, or vice versa, because of the initially introduced "equal standing" of the two thyristor bridges.

It emphasized that the above stated limitation of speed does not apply to the reversal of flow of energy, required for the purpose of implementation of a current phase angle $|\varphi| > \pi/6$, as explained in subsection reason for this exception is the fact that the flow of the phase currents i_{si} retains the same direction, even though the polarity of the respective e_i reverses. Continuation of the i_{si} in the same direction entails the fact that the direction of flow of the "rectified" current i_{sr}, as explained in the preceding discussions , remains unchanged "forward" or "reverse". The fact of continuity of the current i_{sr} entails that the state of energy of the energy storing elements in the inverter mechanism remains unaffected at the time of reversal of flow of energy. The electronic control and protection system has to accomodate the readjustment of its control signals which govern the converter's operation. This readjustment of the governing electronic system must occur within less than one half of one cycle of the modulated high frequency carrier i_l.

This is analogous to the functioning of the currently used mechanism for the transfer of one phase pair to the next one.

IV - 3.2. Aspects of Technology

The here presented system embodies the well known advantages of the dc converter employing series resonant circuits, as well documented in the literature |1,2,3|. These include:

- high reliability of operation under adverse conditions |3|, as proven in the ion propulsion engine program;

- light weight of equipment that is expected to be approximately 40 % heavier than the known dc converters of this type, and therefore substantially lighter than conventional equipment;

- low cost of equipment, based on the limited use of copper and iron, thus substantially reducing the cost of raw materials, the manpower to handle these materials and components during the processes of manufacturing, transportation, installation and servicing.

The here presented ac/dc converter has shown to have functional properties which are analogous with those of its dc/dc converter counterpart, from which the basic internal mechanism is derived.

The novel aspects are, primarily: its selective connection to suitable phase pairs of a polyphase ac system; the bidirectional power transfer and its capability to reverse the direction of power flow at the termination of each of its internal high frequency half cycles.

Accordingly, the desirable improvements of component technology are identical with those for the related dc/dc converter of the same type [1,2,5]. The power capacity of single modules of these dc converters appears presently [5] limited to 150 to 200 kW for full bridge configurations. Improvements of this power capacity could be attained with larger, fast switching thyristors which appear to be feasible, given the therefore needed interest and funding. These thyristors could be fabricated with the use of 5" diameter silicon wafers and the application of interdigitated gates for purpose of speed of turn-on and turn-off. It is believed that such a thyristor of this general type, such as the Westinghouse T 72 H or the Siemens BSt 49 could process 10 kA_{rms} from a 2 kV DC source. The result could be the construction of dc/dc single module converters with power capacities in the order of tens of MW.

One of the pecularities of the polyphase ac/dc converter, as presented here, is the "time sharing" utilization of its ac/dc interface thyristors, such that the rms content of the thyristor currents $i_{th\ rms}$ is given by

$$i_{th\ rms} = \rho_i |i_1|_{av}/\sqrt{2p} \tag{3.14}$$

where

ρ_i = the current form factor ≈1.3 [1];

$|i_1|_{av}$ = the average of the absolute value of the resonant current [1];

p = the number of phases of the polyphase system.

The term $|i_1|_{av}$ can be equated, roughly, to the average current which would be derived from the ac or dc source of electric power supply. The average e_s^* of the effective "dc" voltage of a rectified ac supply line is given by equations (2.1) and (2.2). The equivalent of this relation is given roughly by

$$e^*_{s\ av} \simeq (3/\pi) e_{i\ rms} \sqrt{\varepsilon} \tag{3.15}$$

If $e^*_{s\ av}$ = 2 kV for the above proposed thyristor, then it could derive power from a three phase supply line with an individual neutral to line rms voltage

$$e_{i\ rms} \simeq \frac{2\pi\ 10^3}{3\sqrt{6}} \simeq 860\ V_{rms} \tag{3.16}$$

This corresponds to a line to line voltage of approximately 1.5 kV_{rms} or any multiple thereof. The absolute value of the momentary current in each phase would amount to

$$|i_{si}|_{av} \simeq |i_1|_{av} = \frac{\sqrt{6}\ i_{th\ rms}}{\rho_i} \simeq 18.8\ kA \tag{3.17}$$

The total power processed by one module is then

$$P_{ac} \simeq (0.955)(1.5)(18.8)\ \text{MW} \simeq 27\ \text{MW} \tag{3.18}$$

The equivalent for the now available Siemens BSt 49 thyristor is similarly estimated to be

$$P_{ac\ BSt} \simeq (0.6/10)(520/860)\ 27\ \text{MW} \simeq 1\ \text{MW} \tag{3.19}$$

where

0.6/10 = the average current ratio 600/10000 for the two here considered thyristors, after derating;

520 $\simeq e^{*}_{s\ av}$ derived from a conventional 220/380 ac supply line.

The BSt 49 is produced as a four terminal device which permits a forced clearing of its junction. This should reduce the turn off time t_q to 6 µsec at 125°C junction temperature.

Recent experimental studies have shown that the junction of the Siemens BSt 49 clears indeed within, approximately, 6 µsec, when the charge which remains in the junction at 125 °C is rigorously extracted after completion of its half cycle of conduction .

But more important it has been shown that the dv/dt of the reapplied anode to cathode voltage can rise up to an excess of 2 kV/µsec when the gate junction is being cleared in the above described manner. The two above stated facts indicate that the internal converter frequency can be raised to 20 kHz for larger modules with submegawatt capacities without a penalty in terms of considerable power losses in the dv/dt control networks.

The effect of a raise of the internal frequency by a factor two to 20 kHz needs to be studied. The series inductors are, certainly, reduced to one half of their electric value when compared to 10 kHz. But the specific magnetic core losses in the same materials will rise and a search for new configurations and/or combination of materials need to be undertaken to reap the fruits of improvement of the semiconductor switching components.

It is recalled here that a continuing "miniaturization" of power equipment requires prolonged and sustained efforts in order to yield useful results. A reduction in size and weight may have to be matched by an improvement of the electric efficiency of the system, unless more powerful methods of heat transfer are applied.

The success of the converter with series resonant circuit can be, largely, credited to the concurrent improvement of the efficiency of converters with this technique. The reduced size and volume was matched by substantially reduced losses which rendered the application of this technique practical.

Nevertheless one should expect at th. end of the road to 20 and possibly 50 kHz thyristor converters power component densities in the order of 2 to 3 kW/kg with undiminished efficiency. Component improvements in the area of magnetics appear mandatory for this purpose. The further improvement of efficient network and system concepts appears highly desirable.

A potentially significant area of improvement is that of the series inductors. The current physical net weight of a larger inductor with one percent loss of the processed power is, at least, 0.5 kg per Joule of stored energy. The series inductor is, presently, the heaviest, and possibly the most expensive component of the class of the here discussed type of converters.

A thorough investigation into the area of momentary storage of magnetic energy, the used concepts, geometrical configuration of magnetic fields and used materials should be undertaken with the objective to substantially reduce the weight and cost of these inductors, without reduction of their efficiency.

Improved "high voltage" fast switching power diodes with current carrying capacities in the order of 100 to thousands of Amperes with recovery times in the order of 100 to 300 nsec would improve, substantially, the chances to reduce the yet substantial dv/dt snubber networks.

Substantial work is needed to (1) "streamline" the control electronics in the light of the recently gained experience, (2) develop the above described phase shifting mechanism, (3) devise the necessary interaction between an internal controllable polyphase reference source, the power control and protection mechanism. This work may require years of dedicated efforts. The time element for that purpose appears comparable to the efforts needed for component development.

IV - 3.2.1. The Present State of Development

It has been shown that the two connections of a converter of the here discussed type [1,2,3] to a dc source of energy can be replaced by connections to the individual phases of an ac source. It has been shown that these connections provide in the form of a thyristor matrix, the equivalent of a dc source with voltage e_s^* (see Fig.IV-3.1) when viewed from the "source end" terminals of the series resonant circuit.

The problem that had to be solved to achieve the above stated purpose can be formulated briefly:

(a) To devise a bipolar mode of operation for a thyristor input bridge to the converter;

(b) To devise an automatic transfer mechanism between three pairs of these input bridges for the uninterrupted power flow to or from the series resonant circuit. These three pairs are formed by the permutations of three phases of an ac system. Each of these three pairs is formed, furthermore, with two polarities. It is, therefore, necessary to interlink, successively, six conditions of connection of the ac system to the converter's input terminals;

(c) To equip each of the two bridges which interface capabilities with other system components, for bilateral power flow;

(d) To devise the control and protection electronics which would implement the above stated requirements.

Other than stated above, the system behaves identically equal as its predecessor, the dc converter of this type [1,2,5].

It has been demonstrated experimentally that the above stated functions, which constitute the essence of the new technology, could be achieved. A 3 kVA laboratory experiment was used to establish the basic properties which appear to hold the promise for the feasibility of construction of equipment of similar or substantially larger power capacities into the MW region.

In its present state of development the system is capable to transfer unregulated polyphase ac power to a closely controlled dc load. It is, furthermore, capable to transfer unregulated dc power in a regulated fashion to an ac powered network. This transfer occurs in both cases near the theoretically possible maximum power factor, independent of source voltage variations and/or loading; this includes the conditions of progressive overloading and short circuited output terminals.

It has been shown above, that it is possible to use the tools of the newly acquired power system to perform the transfer of dc energy to the three phase system with any desirable or necessary power factor between zero leading over its possible maximum to the zero lagging value. It has been shown, furthermore, that the power factor is in the here presented case not a necessary tool of control, and therefore subject to optimization for all conditions of operation of the converter.

IV - 3.2.2. Projections of Applicability

The expansion of the here presented concept in its present state requires further work, primarily in the control electronics for the purpose of its adaptation to a multitude of specific functions.
Transfer of ac to dc power and its converse was experimentally demonstrated. The capability to transfer dc to dc power is inherent in the same system. Each of the three input terminal pairs has to be capable to accept dc power of either polarity.

As a matter of fact this is one of the first verification proofs that were carried out before attempting to connect the system to the three phase line. The apparent application areas of this technology are in the area of controllable dc power supplies for instrumentation, computers, radar, laser and dc machines, when powered from unregulated ac or dc systems. Another applications area is seen in the connection of either side of HVDC lines to the ac neworks.

Ac to ac conversion could be achieved by connecting two of the here described systems back to back, with their equal impedance level dc outputs connected. A little thought convinces that the resulting dc link is unnecessary and that the series resonant circuits could be directly connected. Or for that purpose one single series resonant circuit could link the two three phase matrics. The obvious applications are: induction motor drives and the asynchronous coupling of polyphase ac systems.

Power scaling of single modules up to the megawatt level appears possible with the presently available components, as was discussed in the preceding section. Development of larger fast switching thyristors with up to 5" diameter and interdigitated gates appears possible; its implementation could be a question of availability of funds. Single modules with power capacities near 25 MW could then be constructed. The technology on how to stack these modules in parallel or "on top" of each other, using one single electronic control system, has been demonstrated [10].

Single phase ac systems that would work into controlled dc or polyphase loads are conveivable. Yet the problem of avoiding the "ill" effects of the double line frequency power oscillation requires the development of new concepts in the area of active filters.

Modularization of these systems is neccessitated whenever the needed power capacity exceeds the power handling capability of the switching devices. The use of these devices in distinct modules secures stress and power sharing between the electronic switching devices without imposing any tangible penalties. The number of Joules that need to be stored recurrently by the elements of the series resonant circuits is unequivocally given, once (1) the processed power and (2) the maximum operating frequency have been determined. Components which can store these Joules have to be incorporated into the system whether in one or in several modules.

One significant fact which is related to modularization is the micro-miniaturization of the needed special analog logic. This logic should reach a certain degree of maturity after, say, completion of the third generation of its development. Application of thin film techniques for this purpose should greatly reduce the cost of construction and the reliability of converters of this type. This would include dc converters of the type used for ion propulsion engines.

A study of the literature could augment the here presented material |12|.

IV - 4. Conclusions.

The significance of the advancement of the technology of conversion of controlled polyphase power to dc and its reversal is not limited to the said type of conversion. The option to generate and modulate trains of current pulses efficiently and with an unfailing predetermination of their low frequency content opens entirely new avenues in power technology.
The control philosophies which govern the concerned power pulse modulation processes are briefly reviewed for the purpose of elucidation of the above made statement.

The ideology of functional mechanisms as applied in power technology and their analysis was so far limited to a factual description of the physical processes that would lie within the boundaries of immediate comprehension of the workers in this field. The piecewise linear processes, such as the voltage waveforms which result from phase angle control of sine waves are often, erroneously, referred to as "nonlinear". The most prevalent tool of primary analysis of those processes is the Fourier serie. This tool yields correct results in any case, yet it obscures the essence of the causal relationship between the effect of the time delay of a control signal on the harmonic content of the generated waveform.

Certainly, one can organize the results of a numerical analysis in a graphic form and thus attempt to capture the effects of the above referred to causal relationship. However, the usefulness of the described analysis is, inherently, limited to certain steady state conditions. An inclusion of the effects of reactive elements such as those found in filters, may prove cumbersome when performing an analysis, to say the least.

But, even an analysis of certain steady state conditions could be fraught by shortcomings of the applied method when reducing the physical reality to a mathematical model. The moments of "triggering", as intended by the control system and as actually implemented by the power system, may differ in time; effects which distort the "perfect" shape of the sine waves of the source voltages may not be included in the analysis, not to speak of the unfailing deviations of these sine waves from their ideal form for many other reasons. The effect of deviations of the physical reality from the assumed ideal conditions increases with increasing pulse frequencies. The reasons are rooted in the fact of the increase of the deformation of the intended power pulse signals when the duration of the turn-on and turn-off processes become comparable to the duration of the thus generated pulses as a whole.

Application of the here presented co trol philosophy of the ASDTIC type, removes the above stated difficulties. This control system operates on the principle of fitting each actually generated power pulse area precisely into a time interval which guarantees the intended low frequency content of the concerned train of pulses as a whole. The just described property guarantees further, that this process will be preserved when the dynamic conditions of transient phenomena prevail.

A general modulation theory is applied which need not cling to a meticulous descripti of the detailed conditions during the generation of each individual pulse. As a matter of fact there is no need to know these conditions as long as certain limitations of the engineering design are not exceeded.

The application of this powerful concept is requisite to the selection of power pulse repetition rates in the order of tens of kHz and their secure

control for the unfailing achievement of an intended modulation process. Satisfaction of the physical requirement that these pulses be generated with a sufficiently high efficiency is second to the necessity of proper implementation of the concerned pulse modulation process, even though efficiency is a mandatory requirement in itself.

The above described requisite requirements for the realization of an effective power transformation and control process are restated for the purpose of clarity in the order of their significance as being: (1) an unfailing method for the generation and modulation of a pulse train or "carrier", complemented by (2) a method to switch its appreciable currents, up to the range of kiloamperes, efficiently at frequencies in the tens of kHz.

The option to apply these advancements of power technology in order to devise improved systems creates an analogy to the application of the principles of carrier modulation and demodulation in the area of communication technology. The use of a nonlinear process of generation and modulation of a carrier is an intrinsic byproduct of power handling and conversion. Yet, this nonlinearity is irrelevant once the intended low frequency signal is "detected" in its intended form.

One of the unique inherent advantages of the here described system is the speed of its reaction capability which exceeds the same property of the state of the art by orders of magnitude. This speed is rooted in (1) the high internal frequency of operation of tens of kHz and (2) the short time of response, no longer than one cycle or 10^{-4} seconds at an internal frequency of 10 kHz. These systems are, therefore, capable to follow commands

with bandwidths up to one kHz. An extension of this limit is now in development, since newer thyristor switching devices and the thereto applied methods of control allow switching speeds of inverters up to 50 kHz [9],[14].

The above named possible bandwidth of the discussed type of converters appears to justify the expectation to devise controlled frequency changers, to convert "wild" aircraft ac power with frequencies between 400 and 800 Hz to regulated and controlled 400 Hz. The entire area of single and polyphase inverters appears to be in need of acceptable technology. The present use of dc motors for the application of controlled electro-mechanical power appears solely rooted in the absence of reliable and economically justifiable inverters to power and control single or polyphase motors.

Another area of application is that of an efficient electric link between a vehicle traction machine and an ac driven flywheel, or the reverse thereof. It is known that approximately 25% of fuel could be saved in motor vehicles if a suitable manner to recover the energy of the deaccelerating (braking) vehicle could be devised. The flywheel itself appears excellently suited for that purpose; it can receive appreciable amounts of energy at very high rates and can likewise return energy within short time intervals. Rotational speeds in the order of tens of thousands of r.p.m. are needed for the necessary high energy density of these flywheels. These high r.p.m. speeds require a direct coupling to an ac machine, since (1) dc machines cannot operate at these rotational speeds and (2) the use of gears appears probihitive because of (2a) the continuous loss of energy in gear friction, (2b) the relatively high rate of wear at, say, 30 - 50 thousand r.p.m., and (2c) the need for the suppression of otherwise objectionable audible noise.

The useful application of a flywheel for the above stated purpose depends on an efficient "round trip" of the energy from the axle of the vehicle's wheels to the flywheel and back. If we assume the linkage of two electric ac machines, then this energy is four times "processed" before it returns to the axle for acceleration of the vehicle. An average efficiency of those machines of 90% would result in the return of $(100)(0.9)^4 \approx 65\%$ of the "recovered" energy. An average efficiency of, say, another 90% of the electric linkage between the machines could result in an over all efficiency near $(100)(0.9)^6 \approx 50\%$. This would save one half of the energy, "lost" or converted into heat through recurrent braking in city traffic. Braking is one of the most significant contributors to energy consumption of motor vehicles in city traffic. It is estimated to consume between 50 and 65% of the fuel in city traffic.

The outcome of efforts on flywheels, as successful as it is, appears to hinge on the establishment of the technology for the variable frequency drive of an ac machine to drive the flywheel or add energy to the traction process. This applies to road and rail vehicles which are powered by combustion engines, electric motors or with a hybrid traction system.

Another area of application for a frequency changer is that of controlled field power drives for large generators. A drive of the rotor which is capable to provide zero or any infinitesimally adjustable electric frequency for the field coils of a generator can (1) "catch" unforeseen rapid transients and preserve the integrity of the generation process which may otherwise collapse and (2) synchronize slight variations of the frequency "instantaneously" until the mechanical system has had enough time to react.

One area of current interest is seen in the synchronization of windmill driven polyphase generators in the above described manner. Such a converter will require only 1/12 of the maximum processed power.

It is reiterated that the current technology can provide these features with only marginal quality and an economically unjustifiable effort, because of its shortcomings which are intrinsically rooted in the (1) simplistic concepts of control which are (2) compounded by the low internal frequencies of 0.2 to 0.5 kHz of operation.

Little was said, so far, about cost. The thrifty use of "iron and copper" in high frequency apparatus points in itself the way to low cost equipment. Recent calculations of the cost of production of the here presented type of converters have shown, that it breaks even with the older and more recent "state of the art" technology. Its competitiveness should come in clear evidence within very few years and pave the way to its commercial application. That is for applications which fit the state of technology that will be reached by then.

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