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Bias-Stress Effect in Pentacene Organic Thin-Film Transistors

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***Abstract*—The effects of bias stress in integrated pentacene organic transistors are studied and modeled for different stress conditions. It is found that the effects of bias stress can be expressed in terms of the shift in applied gate voltage ΔV for a given current. An empirical equation describing ΔV in terms of different gate and drain bias stress measurements and stress times is presented and verified. In the measured devices, ΔV saturates at 14 V, independent of the gate bias-stress condition. A model based on carrier trapping rate equation that accounts for this ΔV saturation is developed. The model suggests that the ΔV saturation is due to the small density of traps compared to the channel carrier density.**

***Index Terms*—Field-effect transistor (FETs), organic compounds, reliability, stability, stress, thin-film transistors (TFTs).**

I. Introduction

ORGANIC transistors offer opportunities in flexible electronics that integrate various sensors and actuators with electronic functions [1]. Transistors using pentacene, one of the most widely studied organic semiconductors, exhibit mobilities on par with hydrogenated amorphous silicon (a-Si:H). Such electrical performance is sufficient for many applications such as backplanes of organic light-emitting diode displays [2], imagers [3], and conformal large-area arrays of pressure and temperature sensors [4].

Although sufficient mobility has been achieved with organic transistors for various applications, it has been reported that the current–voltage (I–V) characteristics change with the application of prolonged voltages [5]–[11]. Such change is termed the bias-stress effect. The bias-stress effect is important for practical circuit applications and needs to be understood and reduced. Thus far, published works on the bias-stress effect in organic transistors have been predominantly conducted on SiO_2 gate dielectrics with unpatterned gates. Transistors with patterned gates are necessary for integrated circuits. In addition, there is limited study of different gate and drain bias-stress conditions. To evaluate the bias-stress effect of transistors, it is necessary to investigate how the gate and drain bias stresses affect the I–V characteristics.

The bias-stress effect has also been reported in a-Si:H thin-film transistors (TFTs) and has been studied for decades [12]–[17]. In a-Si:H TFTs, the bias-stress effect is commonly described in terms of a threshold voltage shift. The threshold voltage shift is attributed to the trapping of channel carriers in electronic states, which are created by bias stress [12]. Carriers trapped in these states remain trapped until the defect states are thermally annealed out of the device [13]. In contrast, organic TFTs (OTFTs) normally do not require thermal anneal to reverse the bias-stress-induced changes [6].

In this paper, we study the bias-stress effect in pentacene OTFTs, taking advantage of the framework set by the a-Si:H TFT literature. The studied transistors have patterned gates and use parylene as the gate dielectric. The devices have subpicoampere gate leakage current. Similar to a-Si:H TFTs, the bias-stress effect in OTFTs can be described in terms of the shift in applied gate voltage for a given current ΔV. We derive an empirical equation that models ΔV for various stress conditions in source–gate bias (V_{SG}) and source–drain bias (V_{SD}). Measurements show that ΔV saturates at a certain voltage independent of the stress V_{SG}, contrary to what has been reported for a-Si:H TFTs [13], [16]. A model based on a carrier trapping rate equation suggests that this ΔV saturation phenomenon is due to the small density of trap sites compared to the channel carriers.

II. Experimental

Pentacene OTFTs were fabricated on a 4-in glass wafer (Schott D-263 borosilicate float glass) in a class-100 clean room. The wafer was first cleaned in a solution of sulfuric acid and hydrogen peroxide. A gate layer of 10-nm-thick chromium (for adhesion) and 60-nm-thick gold was e-beam evaporated and patterned by photolithography and wet chemical etching. A 175-nm-thick layer of parylene-N deposited by hot-filament chemical vapor deposition was used as the gate dielectric. Via holes were patterned in parylene by photolithography and reactive ion etching (RIE) in oxygen. A layer of 40-nm-thick gold, which serves as the source/drain layer, was then deposited by e-beam evaporation. Photolithography and wet chemical etching were used to pattern the layer. An 18-nm-thick pentacene film (Luminescence Technology) was blanket deposited by thermal evaporation at a rate of 0.9 nm/min. The pentacene was then encapsulated in a 200-nm-thick film of parylene-N,

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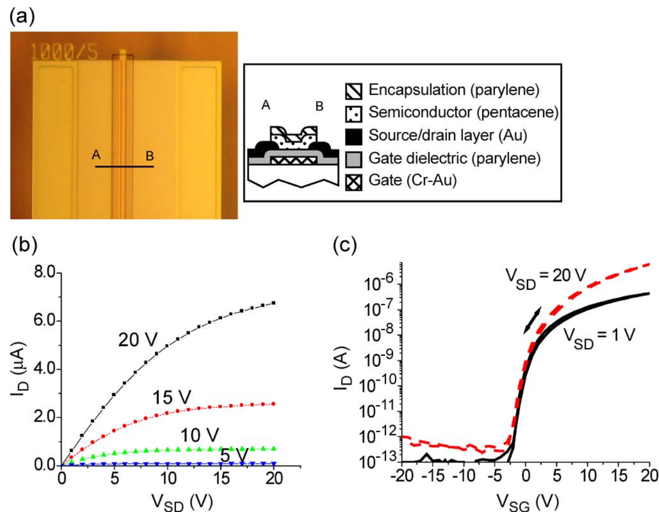


Fig. 1. (a) Photo and the cross-sectional schematic of the device. (b) Output characteristics and (c) transfer characteristics of a 1000/5-μm device.

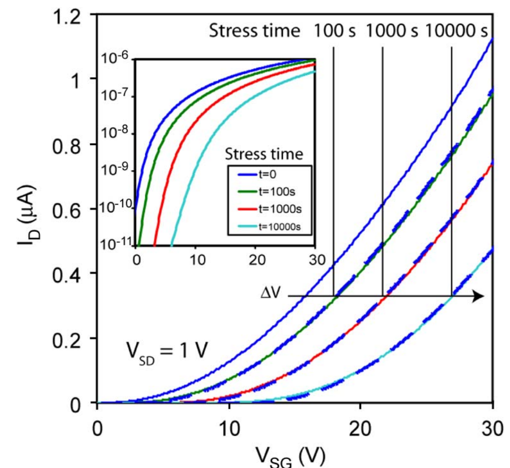


Fig. 2. Transfer characteristics after bias stress at $V_{\mathrm{SG}} = 30$ V and $V_{\mathrm{SD}} = 1$ V at varying stress times t. The dashed lines show the shifted transfer characteristics of the unstressed device ($t = 0$ s). The inset shows the semilogarithmic plot of the same data.

allowing the pentacene/parylene stack to be photolithographically processed without exposing the pentacene to solvents. A subsequent RIE process defined islands of parylene and pentacene, isolating the active area of each OTFT. More details on processing can be found in [18]. Fig. 1(a) shows a photo of the completed transistor and a schematic of the cross section. Fig. 1(b) and (c) shows the measured output and transfer characteristics of a 1000/5-μm device, respectively. The mobility of the completed OTFTs was 0.03 $\mathrm{cm}^2/\mathrm{Vs}$. The devices were stored in nitrogen ambient, and no change in the I–V characteristics was measured over a month of storage.

III. Measurement and Results

To avoid extrinsic degradation mechanisms in OTFTs [11], measurements were done in nitrogen ambient in the dark using an Agilent 4156C semiconductor parameter analyzer on a Signatone S-250 wafer prober with a temperature-controlled chuck. All the measurements were done on fresh 1000/5-μm-size devices at 20 °C. To first analyze the effects of bias stress on the overall transfer characteristics, I_D–V_{SG} was measured at $V_{\mathrm{SD}} = 1$ V for $-2 < V_{\mathrm{SG}} < 30$ V with a step size of 0.1 V on a fresh device. Bias stress was applied for a set time, and the I–V transfer characteristics were measured again. More bias stress was applied, and subsequent transfer characteristics were taken until the desired data were gathered. The sequence of measurements was automated to minimize the error that could be induced by instrument-setting time between the measurements. Fig. 2 shows the resulting measurement for a stress V_{SG} of 30 V and V_{SD} of 1 V for increasing stress time. We observe that the applied stress shifts the transfer characteristics in the positive V_{SG} direction and that the shape of the transfer characteristics does not appreciably change with stress time. Thus, we can describe the after-stress transfer characteristics by shifting the original transfer characteristics of the device by a voltage, which we define as ΔV. ΔV conveniently describes the bias-stress effect in these devices: the drain current after bias stress can be expressed as $I_D = f(V_{\mathrm{SG}} - \Delta V, V_{\mathrm{SD}})$, where $I_D = f(V_{\mathrm{SG}}, V_{\mathrm{SD}})$ is the measured I–V characteristics from a fresh device. Fig. 2 shows the applicability of this idea by shifting the original transfer characteristics and overlaying them (dashed lines) with the transfer characteristics taken after the various stress times (solid lines). The use of ΔV to describe the bias-stress effect is common for a-Si:H TFTs [14] and has been demonstrated on other OTFTs [9], [10]. In the following, we measure ΔV as a function of various bias conditions and time to better understand the source of the bias-stress effect and quantify its effect on the transfer characteristics.

Measuring ΔV by intermittently taking the I–V sweeps during stress measurements is unfavorable because the intermittent I–V sweeps introduce additional stress on the device. The nominally unchanging transfer characteristics shape allows us to measure the current while the device is under constant stress in the linear region and extract ΔV information by using the prestress transfer characteristics. Such measurements of ΔV are preferable because there is less measurement error introduced by stressing caused by the I–V sweeps. Although some error introduced by the initial I–V sweep is unavoidable, this error is relatively small as the device is held at stress conditions for less than a second. The measurements were taken for various stress V_{SG} conditions. The results are shown in Fig. 3. The measured ΔV can adequately be fitted to a stretched-exponential equation, i.e.,

$$\Delta V(t) = \Delta V_{\mathrm{FINAL}} \left\{1 - \exp\left(-(t/\tau)^{\beta}\right)\right\} \tag{1}$$

where t is the stress time, $\Delta V_{\mathrm{FINAL}}$ is the voltage at which ΔV converges, and τ and β are fit parameters. The fit parameters are given in Table I.

The stress V_{SG} was kept at a maximum of 40 V as the effects of gate dielectric breakdown were observed at higher voltages. The measured τ and β are similar to measurements in other pentacene transistors in [10] ($\beta \sim 0.4, \tau \sim 10^4$ s) and [11] ($\beta \sim 0.28, \tau \sim 10^4$ s) and comparable to other organic semiconductors and a-Si:H TFTs [9], [16]. With the exception of stress V_{SG} of 40 V near the breakdown voltage of the gate

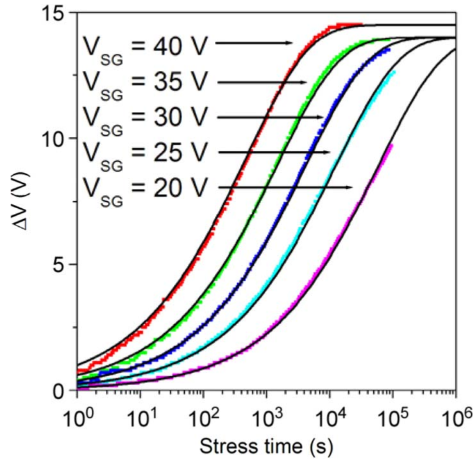


Fig. 3. Time dependence of the induced ΔV for various gate bias-stress conditions. Each stress condition has 50 data points per decade. The solid black lines, representing the stretched-exponential fit made to the data, are plotted on top of the data.

TABLE I
FIT PARAMETERS TO DIFFERENT V_{SG} STRESS CONDITIONS IN THE STRETCHED-EXPONENTIAL MODEL

Stress V_{SG} (V)	ΔV_{FINAL} (V)	τ (s)	β
20	14	55000	0.43
25	14	12000	0.43
30	14	3900	0.44
35	14	1400	0.44
40	14.5	440	0.46

dielectric, it is notable that the ΔV_{FINAL} is not dependent of the stress gate bias. This is attributed to the fact that the channel carriers are not the limiting factor in saturating ΔV for the measured devices. Further explanation on this point is made in Section IV. It is also notable that τ decreases as V_{SG} increases. To express τ as a function of the gate bias, τ versus V_{SG} is plotted on a log–log scale in the inset of Fig. 4. By using $\tau = aV_{\text{SG}}^{-\alpha}$, where $a = 5.3 \times 10^{13}$ sV^{α} and $\alpha = 6.9$, an adequate fit can be made. With this knowledge, (1) is expressed as an explicit function of V_{SG}, i.e.,

$$\Delta V(t) = \Delta V_{\text{FINAL}} \left\{ 1 - \exp\left(-\left(t/aV_{\text{SG}}^{-\alpha} \right)^{\beta} \right) \right\} \qquad (2)$$

where a, α, and β are independent of V_{SG}. Equation (2) is used to produce the solid line in Fig. 4, which plots ΔV after 100 s of stress at different stress V_{SG} measurements. To verify this equation, measured ΔV data for different stress V_{SG} measurements on multiple devices are also plotted in Fig. 4. A good fit to the measured data is produced.

The dependence of ΔV on the drain bias is measured next. We observe that, as the drain bias during stress increases, the resulting ΔV decreases, as shown in Fig. 5(a). It is notable that, while the current increases from zero at $V_{\text{SD}} = 0$ V to tens of microamperes at $V_{\text{SD}} = 30$ V, the ΔV from bias stress decreases, indicating that neither the current nor hot carriers are the direct cause of ΔV.

The V_{SD} dependence can be explained by the conjecture that the ΔV is caused by the channel carriers. The charge in the channel with a varying drain bias can be approximated by the following equation [17]:

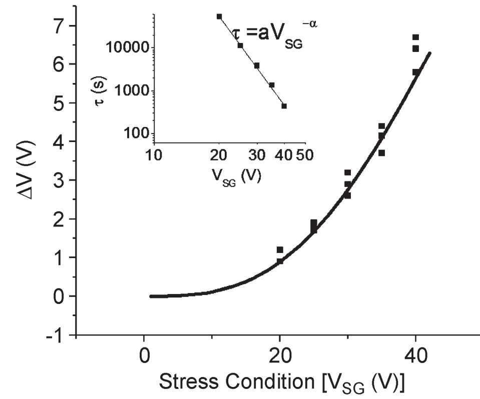
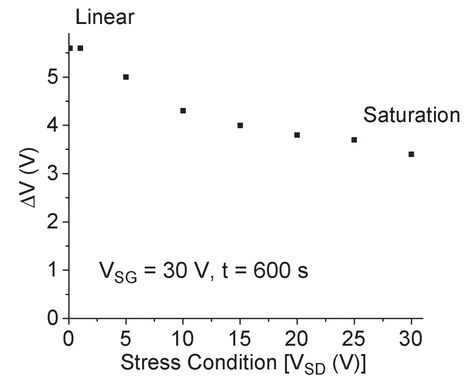


Fig. 4. ΔV versus stress V_{SG} at $t = 100$ s. The V_{SD} during stress was held at 1 V. Each stress condition was repeated three times, each time on a fresh device. The solid line is ΔV predicted by (2). (Inset) Log–log plot of τ versus V_{SG}.

(a)



(b)

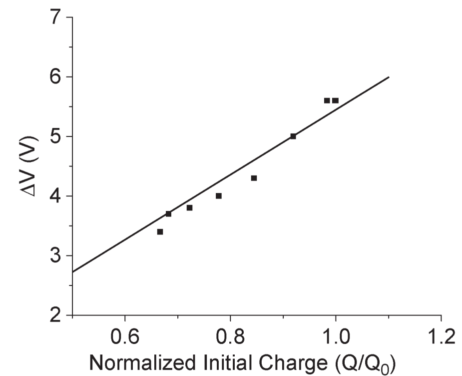


Fig. 5. (a) ΔV versus stress V_{SD} at $t = 600$ s. The V_{SG} during stress was held at 30 V. The induced ΔV decreases with increasing V_{SD}. (b) Data replotted in normalized charge. Q/Q_0 was calculated with (3). The solid line represents a linear fit.

$$Q = \frac{2C_i WL}{3} \frac{(V_{\text{SG}} - V_{T0})^3 - (V_{\text{DG}} - V_{T0})^3}{(V_{\text{SG}} - V_{T0})^2 - (V_{\text{DG}} - V_{T0})^2} \qquad (3)$$

where C_i is the normalized capacitance of the dielectric, W and L are the width and length of the active layer, respectively, and V_{T0} is the initial threshold voltage. As V_{SD} increases, the accumulation charge density at the drain decreases, resulting in less charge in the channel.

Karim *et al.* [17] have first proposed for a-Si:H TFTs that the ΔV for different drain biases can be modeled by multiplying the right-hand side of (2) by (Q/Q_0), where Q_0 is the charge in the channel with $V_{\mathrm{SD}} = 0$ V, which is $WLC_i(V_{\mathrm{SG}} - V_{T0})$. The method was extended to OTFTs on SiO_2 by Zan and Kao [10]. We verify that the correction factor works well for the measured devices as well. Fig. 5(b) shows that the measured ΔV at different V_{SD} measurements linearly scales with Q/Q_0. Q was calculated using $V_{T0} = 0$ V. We acknowledge that it is difficult to accurately measure a true V_{T0} because the devices are operating in accumulation mode, and there is a large number of traps located in the semiconductor or at the interface. The value of V_{T0} can be extracted from a semilog transfer characteristics plot in Fig. 1(c) by fitting a line to the slope in the subthreshold region. The uncertainty in V_{T0} is small compared to the stress V_{SG}, which is 30 V.

By combining the results from different stress V_{SG} and V_{SD} measurements, we can express ΔV in terms of the stress V_{SG} and V_{SD}, i.e.,

$$\Delta V(t) = (Q/Q_0)\Delta V_{\mathrm{FINAL}} \left\{1 - \exp\left(-\left(t/aV_{\mathrm{SG}}^{-\alpha}\right)^{\beta}\right)\right\} \tag{4}$$

where a, α, β, and $\Delta V_{\mathrm{FINAL}}$ are independent of V_{SG} and V_{SD}, and Q and Q_0 are calculated from (3).

IV. Discussion

In the previous section, we explored the empirical modeling of ΔV with the stretched-exponential model under various bias-stress conditions. In this section, we derive the stretched-exponential equation from a simple trapping rate equation that offers physical insight into the cause of ΔV and the interpretation of the fit parameters.

We assume that the ΔV is caused by carriers being trapped in trap sites. To model this process, we define p to be the initial channel carrier density, $p_T(t)$ to be the density of trapped carriers, and N_T to be the density of trap sites in the channel. p is used because pentacene is a hole transport semiconductor. p and N_T are fixed with respect to time, and p_T is a function of time. More specifically, $p = C_i(V_{\mathrm{SG}} - V_{T0})/q$, where V_{T0} is 0 V, as defined in the previous section, and $p_T(0) = 0$. ΔV can be expressed in terms of the trapped carriers. If all the traps are assumed to be at the semiconductor/dielectric interface

$$\Delta V = qp_T/C_i. \tag{5}$$

In order for carriers to be trapped, there needs to be both a free carrier and an empty trap. The rate equation that accounts for the trapping process can be written as follows:

$$dp_T/dt = k(p - p_T)(N_T - p_T) \tag{6}$$

where k is the rate constant. The term in the first bracket is the density of free carriers remaining in the device, and the term in the second bracket is the density of empty traps. It has been shown that, for an exponential distribution of barrier energy for traps, the rate constant k can be a function of time, where $k = \beta k' t^{(\beta-1)}$, $\beta < 1$ [15]. The rate of trapping decreases with time, which can be physically related to the fact that, as traps with shorter time constants are filled, the time constants associated with the remaining empty traps are longer, resulting in a lower rate constant.

The differential equation (6) solved with the application of the boundary condition $p_T(0) = 0$ yields

$$p_T(t) = \frac{pN_T\left(1 - \exp\left((p - N_T)k't^{\beta}\right)\right)}{N_T - p\exp\left((p - N_T)k't^{\beta}\right)}. \tag{7}$$

For $N_T < p$, (7) can be simplified, and when inserted into (5), it results in the following equation for ΔV:

$$\Delta V(t) = \frac{qN_T}{C_i}\left(1 - \exp\left(-(p - N_T)k't^{\beta}\right)\right) \tag{8}$$

which is in the form of a stretched exponential. By comparing (8) with (1), we can infer that $\Delta V_{\mathrm{FINAL}} = qN_T/C_i$, which is independent of V_{SG}. In addition τ in (1) can be related to the rate of trapping by $1/\tau^{\beta} = (p - N_T)k'$.

Similarly, for $N_T > p$, (7) can be simplified to result in

$$\Delta V(t) = \frac{qp}{C_i}\left(1 - \exp\left(-(N_T - p)k't^{\beta}\right)\right) \tag{9}$$

which is also in the stretched-exponential form, but $\Delta V_{\mathrm{FINAL}} = qp/C_i$ and now depends on the channel carrier density p. $p = C_i(V_{\mathrm{SG}} - V_{T0})/q$, and thus, $\Delta V_{\mathrm{FINAL}} = V_{\mathrm{SG}} - V_{T0}$.

For the measured OTFTs at stress V_{SG} ranging from 20 to 35 V, we assume that $N_T < p$ because $\Delta V_{\mathrm{FINAL}}$ is independent of V_{SG}. The assumption of $N_T < p$ is also self-consistent with the observation that $\Delta V_{\mathrm{FINAL}} < V_{\mathrm{SG}} - V_{T0}$. In the measured OTFTs, the ΔV saturates at 14 V, independent of V_{SG} because the trap sites are exhausted before the channel carriers. In contrast, for stress $V_{\mathrm{SG}} < 14$ V, it has been verified that $\Delta V_{\mathrm{FINAL}} = V_{\mathrm{SG}} - V_{T0}$, as predicted by the model for the case $N_T > p$. The $\Delta V_{\mathrm{FINAL}}$ also saturates at $V_{\mathrm{SG}} - V_{T0}$ for a-Si:H TFTs [13], [14], as a-Si:H TFTs are always stressed in the region $N_T > p$. This is expected in a-Si:H TFTs as the trap sites are created as the weak bonds within the a-Si:H are broken [12].

The measured OTFTs have $C_i = 15$ nF/cm^2, and for the measured $\Delta V_{\mathrm{FINAL}}$ of 14 V, N_T is calculated to be 1.3×10^{12} cm^{-2}. This range of N_T is reasonable considering that the density of interface states in metal–oxide–semiconductor field-effect transistors is in the range of $10^9 - 10^{12}$ cm^{-2} [19]. The calculated N_T is also reasonable considering that the density of pentacene molecules at the interface is on the order of 10^{14} cm^{-2} and is greater than the density of defects. It is difficult to compare N_T with the results from other TFTs as this is the first report of $\Delta V_{\mathrm{FINAL}}$ that is independent of V_{SG}. Even so, if a comparison is to be made, the lower bounds for N_T in other works can be calculated by using the maximum ΔV measured and using $p_T = \Delta V \times C_i/q$. Since there are enough traps to accommodate this p_T, the calculated p_T serves as a lower bound for N_T. Compared to this N_T, the N_T extracted from the OTFTs used in this paper is still lower, as shown in Table II. This low N_T may be attributed to the parylene dielectric and encapsulation, which provide low interface states with pentacene and protection from reactive O_2 and H_2O during processing steps, respectively.

TABLE II
N_T CALCULATED FROM THIS PAPER AND THE LITERATURE

Semiconductor	Max ΔV (V)	C_i (F/cm^2)	N_T (cm^{-2})	Ref.
Pentacene on Parylene	14	1.5×10^{-8}	1.3×10^{12}	This work
PTAA on SiO_2	19	1.9×10^{-8}	2.3×10^{12}	[9]
T6 on SiO_2	16	1.9×10^{-8}	1.8×10^{12}	[21]
Pentacene on AlO_x/SAM	0.8	7×10^{-7}	3.5×10^{12}	[22]
a-Si on SiN	40	1×10^{-8}	2.5×10^{12}	[23]

From the measurements, it is unclear whether the traps are located in the semiconductor, the semiconductor/dielectric interface, or the dielectric. However, the long time for the bias-stress effect to settle indicates a slow trapping rate. Such a slow trapping rate suggests that there is a barrier for the carriers to be trapped. One possible mechanism is the trapping of carriers in traps located in the gate dielectric near the semiconductor/dielectric interface. The carriers are trapped via hopping into these states. Such a mechanism was proposed by Libsch and Kanicki for a-Si:H TFTs [13].

Another possible mechanism is the detrapping of electrons trapped in the semiconductor [11]. This mechanism explains the observed bias-stress effect by detrapping electrons that are initially trapped in the semiconductor gap states. The application of a negative bias on the gate electrode (positive $V_{\rm SG}$) repels electrons trapped in the channel and detraps them. The drain current decreases as the number of extra holes that balanced the trapped electrons decreases. Although such mechanism explains the long time constant for the bias-stress effect to settle, we would expect a fast recovery of the original I–V characteristics when the stress is removed. However, it has been observed by Mathijssen *et al.* that time constants related to recovery are comparable to the bias-stress effect [9].

In polymer TFTs, bipolaron formation has been proposed for the cause of the slow channel carrier trapping [20]. The ΔV dependence on $V_{\rm SG}$ is cubic for short stress times as $\alpha \times \beta$ in (2) is approximately 3. Although this observation excludes the bipolaron formation as the possible mechanism, a similar mechanism that involves three carriers for a formation of lower energy state may explain the slow trapping behavior. The exact mechanism causing the bias-stress effect remains elusive, and more research in the trapping mechanism in organic semiconductors will greatly enhance the understanding of the bias-stress effect.

V. CONCLUSION

The bias-stress effect on pentacene OTFTs with patterned gates and parylene gate dielectric has been studied. The measured devices did not exhibit any measurable degradation due to storage. The bias-stress effect has been quantified in terms of ΔV, which is the shift in gate bias voltage for a given current after bias stress. ΔV has been measured for various stress conditions and times, and it has been found that the stretched-exponential equation can accurately model the measured ΔV. An equation that models ΔV for different stress $V_{\rm SG}$ and $V_{\rm SD}$ measurements has been presented and verified. It has been found that the current is not the cause of the bias-stress effect. The rate equation that describes the rate of channel carrier trapping provides physical relevance to the fitting parameters used in the empirical stretched-exponential equation. In particular, the rate equation suggests that $\Delta V_{\rm FINAL}$, which is the value that ΔV converges to, is independent of the stress gate bias due to a relatively small density of trap sites compared to the density of channel carriers. Possible mechanisms for the bias-stress effect are discussed. Further improvement in the bias-stress effect is anticipated in these devices, considering that they have not been optimized to enhance stability.

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REFERENCES

[1] Y. Kato, T. Sekitani, M. Takamiya, M. Doi, K. Asaka, T. Sakurai, and T. Someya, "Sheet-type Braille displays by integrating organic field-effect transistors and polymeric actuators," *IEEE Trans. Electron Devices*, vol. 54, no. 2, pp. 202–209, Feb. 2007.

[2] L. Zhou, A. Wang, S.-C. Wu, J. Sun, S. Park, and T. N. Jackson, "All-organic active-matrix flexible display," *Appl. Phys. Lett.*, vol. 88, no. 8, p. 083 502, Feb. 2006.

[3] I. Nausieda, K. Ryu, I. Kymissis, A. I. Akinwande, V. Bulovic, and C. G. Sodini, "An organic active-matrix imager," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 527–532, Feb. 2008.

[4] T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi, and T. Sakurai, "Conformable, flexible, large-area networks of pressure and thermal sensors with organic transistor active matrixes," *Proc. Nat. Acad. Sci.*, vol. 102, no. 8, pp. 12 321–12 325, Aug. 2005.

[5] S. J. Zilker, C. Detcheverry, E. Cantatore, and D. M. de Leeuw, "Bias stress in organic thin-film transistors and logic gates," *Appl. Phys. Lett.*, vol. 79, no. 8, pp. 1124–1126, Aug. 2001.

[6] D. Knipp, R. A. Street, A. Volkel, and J. Ho, "Pentacene thin film transistors on inorganic dielectrics: Morphology structural properties, and electronic transport," *J. Appl. Phys.*, vol. 93, no. 1, pp. 347–355, Jan. 2003.

[7] T. Miyadera, S. D. Wang, T. Minari, K. Tsukagoshi, and Y. Aoyagi, "Charge trapping induced current instability in pentacene thin film transistors: Trapping barrier and effect of surface treatment," *Appl. Phys. Lett.*, vol. 93, no. 3, p. 033 304, Jul. 2008.

[8] K. Suemori, S. Uemura, M. Yoshida, S. Hoshino, N. Takada, T. Kodzasa, and T. Kamata, "Influence of fine roughness of insulator surface on threshold voltage stability of organic field-effect transistors," *Appl. Phys. Lett.*, vol. 93, no. 3, p. 033 308, Jul. 2008.

[9] S. Mathijssen, M. Colle, H. Gomes, E. Smits, B. de Boer, I. McCulloch, P. Bobbert, and D. M. de Leeuw, "Dynamics of threshold voltages shifts in organic and amorphous silicon field-effect transistors," *Adv. Mater.*, vol. 19, no. 19, pp. 2785–2789, Oct. 2007.

[10] H.-W. Zan and S.-C. Kao, "The effects of drain-bias on the threshold voltage instability in organic TFTs," *IEEE Electron Device Lett.*, vol. 29, no. 2, pp. 155–157, Feb. 2008.

[11] G. Gu, M. G. Kane, and S.-C. Mau, "Reversible memory effects and acceptor states in pentacene-based organic thin-film transistors," *J. Appl. Phys.*, vol. 101, no. 1, p. 014 504, Jan. 2007.

[12] M. J. Powell, S. C. Deane, and R. B. Wehrspohn, "Microscopic mechanisms for creation and removal of metastable dangling bonds in hydrogenated amorphous silicon," *Phys. Rev. B, Condens. Matter*, vol. 66, no. 15, p. 155 212, Oct. 2002.

[13] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," *Appl. Phys. Lett.*, vol. 62, no. 11, pp. 1286–1288, Mar. 1993.

[14] M. J. Powell, C. van Berkel, and J. R. Hughes, "Time and temperature dependence of instability mechanisms in amorphous silicon thin-film transistors," *Appl. Phys. Lett.*, vol. 54, no. 14, pp. 1323–1325, Apr. 1989.

[15] A. Kuo, T. K. Won, and J. Kanicki, "Advanced amorphous silicon thin-film transistors for AM-OLEDs: Electrical performance and stability," *IEEE Trans. Electron Devices*, vol. 55, no. 7, pp. 1621–1629, Jul. 2008.

[16] W. B. Jackson, J. M. Marshall, and M. D. Moyer, "Role of hydrogen in the formation of metastable defects in hydrogenated amorphous silicon," *Phys. Rev. B, Condens. Matter*, vol. 39, no. 2, pp. 1164–1179, Jan. 1989.

[17] K. S. Karim, A. Nathan, M. Hack, and W. I. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 188–190, Apr. 2004.
[18] I. Kymissis, A. I. Akinwande, and V. Bulovic, "A lithographic process for organic field-effect transistors," *J. Display Technol.*, vol. 1, no. 2, pp. 289–294, Dec. 2005.
[19] J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology Fundamentals, Practice and Modeling*. Upper Saddle River, NJ: Prentice-Hall, 2000, p. 353.
[20] A. Salleo and R. A. Street, "Kinetics of bias stress and bipolaron formation in polythiophene," *Phys. Rev. B, Condens. Matter*, vol. 70, no. 23, p. 235 324, Dec. 2004.
[21] F. Di Girolamo, C. Aruta, M. Barra, P. D'Angelo, and A. Cassinese, "Organic film thickness influence on the bias stress instability in sexithiophene field effect transistors," *Appl. Phys. A: Mater. Sci. Process.*, vol. 96, no. 2, pp. 481–487, Aug. 2009.
[22] U. Zschieschang, R. Weitz, K. Kern, and H. Klauk, "Bias stress effect in low-voltage organic thin-film transistors," *Appl. Phys. A: Mater. Sci. Process.*, vol. 95, no. 1, pp. 139–145, Apr. 2009.
[23] B. Hekmatshoar, K. Cherenack, S. Wagner, and J. Sturm, "Amorphous silicon thin-film transistors with DC saturation current half-life of more than 100 years," in *IEDM Tech. Dig.*, 2008, pp. 1–4.

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