Bias Temperature Instability analysis of FinFET based SRAM cells

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***Abstract*— Bias Temperature Instability (BTI) is posing a major reliability challenge for today's and future semiconductor devices as it degrades their performance. This paper provides a comprehensive BTI impact analysis, in terms of time-dependent degradation, of FinFET based SRAM cell. The evaluation metrics are read Static Noise Margin (SNM), hold SNM and Write Trip Point (WTP); while the aspects investigated include BTI impact dependence on the supply voltage, cell strength, and design styles (6 versus 8 Transistors cell). A comparison between FinFET and planar CMOS based SRAM cells degradation is also covered. The simulation performed on FinFET based cells for 10^8 seconds of operation under nominal V_{dd} show that Read SNM degradation is 16.72%, which is 1.17× faster than hold SNM, while WTP improves by 6.82%. In addition, a supply voltage increment of 25% reduces the Read SNM degradation by 40%, while strengthening the cell pull-down transistors by 1.5× reduces the degradation by only 22%. Moreover, the results reveal that 8T cell degrades 1.31× faster than 6T cell, and that FinFET cells are more vulnerable (∼ 2×) to BTI degradation than planar CMOS cells.**

Keywords*—: BTI, NBTI, PBTI, SRAM cell, Stability metrics

I. INTRODUCTION

The unabated CMOS technology miniaturization has surfaced several concerns. For instance elevation in the oxide field and current densities are threatening reliable transistor operation. Additionally, the introduction of novel materials like high-k dielectrics and device structures like multi gate FET (e.g. FinFET) to keep pace with Moore's law [1] have unknown reliability consequences [2–4]. Finally, diverse operational conditions and applications cause the parameter variations to endanger the circuit reliability [5]. These concerns make it difficult to maintain the strict reliability requirements of the modern systems.

Today Static Random Access Memory (SRAM) occupy over 50% of the total chip area. SRAM cells are the backbone of embedded CMOS memory and its size is shrinking by 50% in each newer technology generation [6]. Hence SRAM cells use the smallest manufacturable feature sizes in a given technology and the number of possible oxide layer defects that significantly impact the cell operations can be literally counted [7]. On the other hand, market is demanding higher reliability levels expressed as single digit FIT rates (1 FIT= 1 failure per 10^9 hours of operations) [2]. These conflicting requirements are balanced by careful sizing of the cell transistors at the design time. The finely tuned designs provide stable SRAM operations, but also make it vulnerable to the failures caused by temporal degradation mechanisms like Bias Temperature Instability (BTI) of the transistors. BTI [NBTI for p-channel FET and PBTI for n-channel FET] weaken the transistors by shifting the threshold voltage (V_{th}), thus resulting in temporal degradation in stability of the SRAM cell. Shift in V_{th} strongly depends on cell's age, supply voltage, strength and technology.

Both traditional planar CMOS and emerging FinFET based SRAMs are now in the mainstream for product designs. Much has been published about BTI analysis of the planar CMOS based SRAM cells. For instance, Kumar et al. in [8] analyzed NBTI impact on Static Noise Margin (SNM) and read stability of the SRAM cell. Kang et al. in [9] investigated the BTI impact on SRAM cell's SNM, read and write stability, and leakage current. Krishnappa et al. in [10] analyzed the BTI impact on write margin, access time and leakage power of several SRAM designs. However, all of these work did not cover aspects such as BTI impact dependency on supply voltage scaling, cell strength, cell design, etc. On the other hand, few authors have focused on the BTI analysis of FinFET based devices [3,4,11]. For instance, Hu et al. in [11] analyzed the combined impact of BTI and variations on the FinFET based SRAM cells. However, to the best of the author's knowledge, a comprehensive BTI impact analysis of FinFET based SRAM cells and its comparison with the planar CMOS based SRAM cells has not been explored yet.

The focus of this paper is the BTI impact analysis of FinFET based SRAM cells by exploring its dependency on cell's supply voltage, device strength and design styles. The paper also provides a comparison of the BTI impact on the planar CMOS and FinFET based SRAM cells.

The rest of the paper is organized as follows: Section II briefly describes a bias temperature instability model. Section III explains the simulation framework, analysis metrics and performed experiments. Section IV presents the analysis results and discussions. Finally, Section V concludes the paper.

II. BACKGROUND

BTI mechanisms in the MOS/FinFET transistors generate charges inside the oxide layer and/or at the silicon-oxide interface. The generated charges mainly elevate the threshold voltage of the transistors that directly affects circuit parameters such as delay, operational margins, leakage current, etc. [12–14].

In this work, BTI impact on the SRAM cell is investigated

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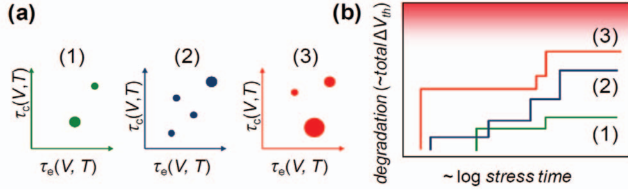

Fig. 1. (a) Timing constants of defects in three FET instances (1, 2 and 3) (b) schematics showing the progress of degradation in the three devices [12].

by the view advocated by Atomistic trap-based model [12]. A general assumption in this model is that each device has a given number of defects (e.g. unwanted charges in the oxide layer) with their unique capture and emission time constants, τ_c and τ_e, as shown in Fig. 1(a). Depending on the device age, temperature, applied voltage and technology, each defect can be charged (captured) or discharged (emitted). When charged, each defect has a unique effect on the device parameters especially on the threshold voltage as shown in Fig. 1(b). Capture/Emission Time (CET) based view of the defects has the advantage of higher accuracy compared to the R-D model [19].

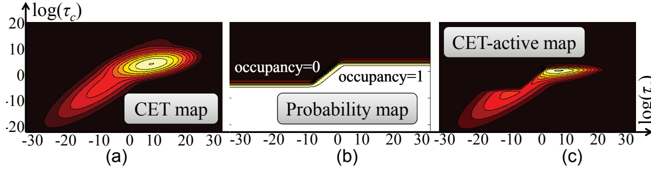

Fig. 2. (a) Integration of CET map (b) the probability map of AC workload (c) the CET-active map [7].

To obtain timing constants of the defects in the devices, a limited CET map for a limited time window can be constructed from the experimental data [7,18,19]. For example, the map used in this paper shown in Fig. 2(a), is built by measure-stress-measure (MSM) experiments on high-k process, and scaled for 10nm FinFET process node by using the voltage-time constant dependence [19]. FinFET thickness $\mathrm{T_{FIN}}$, length $\mathrm{L_{FIN}}$, and height $\mathrm{H_{FIN}}$ are 10, 20, and 30nm, respectively. The effective gate width ($\mathrm{W_{eff}}$) of a FinFET is taken as $\mathrm{W_{eff}}$= $\mathrm{2H_{FIN}}$+$\mathrm{T_{FIN}}$ [20]. The occupancy probability of the defects depend on the workload as shown in Fig. 2(b). The impact of this occupancy can be described from the average number of *active defects/traps* $\mathrm{N_T}$ as shown in Fig. 2(c).

Our analysis focuses on the long term BTI impact of the SRAM cells. However, the measured capture and emission times (i.e. τ_c and τ_e) in a CET map of the transistors are limited to the measurement window. Therefore, an analytical 2-component bivariate log-normal mixture distribution is used to build the complete CET-map covering the short/long operating lifetimes [7]. The occupancy probability, P_{occ}, for a given workload is given by [7]:

$$P_{occ,H}(\tau_c,\tau_e,t_{stress},DF,f)=\frac{1-e^{-\frac{DF}{f\tau_c}}}{1-e^{-\frac{1}{f}\left(\frac{DF}{\tau_c}+\frac{1-DF}{\tau_e}\right)}}\left(1-e^{-t_{stress}\left(\frac{DF}{\tau_c}+\frac{1-DF}{\tau_e}\right)}\right). \quad (1)$$

where $\mathrm{t_{stress}}$, DF, and f are the stress time, duty factor, and frequency, respectively. The piecewise evaluation of P_{occ} during the waveform provides BTI aging under arbitrary workload profiles. Only a fraction of the defect population in the CET map will be active depending on P_{occ} [7].

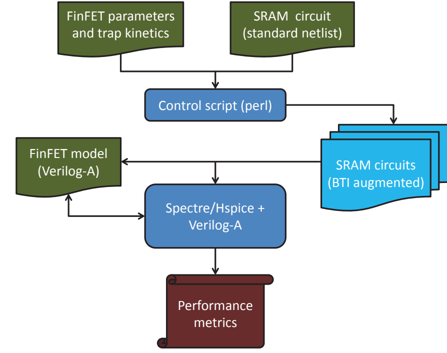

Fig. 3. Analysis framework for the SRAM cell.

The stochastic nature of BTI aging results $\mathrm{V_{th}}$ distributions of the devices in a circuit [18]. Therefore, the aged circuit behavior under the BTI degradation can be generated by Monte Carlo simulations, where instances of a given circuit are populated by trap sampling from the CET-map, i.e. each trap with its corresponding τ_c, τ_e, and $\Delta\mathrm{V_{th}}$ [18].

III. Analysis Approach

This section presents the SRAM cell analysis framework, used metrics, and the performed experiments.

A. Analysis framework

The simulation framework is shown in Fig. 3. Based on the FinFET dimensions and the traps kinetics, the Control script (perl) generates several instances of BTI augmented SRAM cell circuits. Every generated instance has a distinct number of traps (with their unique timing constants) in each FinFET [12], and are incorporated in a Verilog-A module of the FinFET transistor. The module responds to the every individual trap, and alters the transistor's concerned parameters such as $\mathrm{V_{th}}$. After inserting BTI in every FinFET of the SRAM cell, a Monte Carlo (MC) is performed at different time steps (100 runs at each time step) where circuit simulator (HSPICE/Spectre) is used to investigate the BTI impact on the SNM stability metrics (Read, Hold and Write) of the cell. Finally, the results obtained from the simulations are statistically analyzed using Matlab. The simulation framework is generic; different SRAM designs synthesized from various technology nodes are analyzed for various supply voltages.

B. Analysis metrics

Our analyses are based on the two SRAM designs, i.e. 6T-SRAM shown in Fig.4(a), and the write assist 8T design (not shown) [24]. AXL, PUL, and PDL are the access, pull-up, and pull-down transistors on the left inverter of the cell, respectively (while, AXR, PUR, and PDR are that of the right inverter). Two Drive Strengths (DS) for both 6T and 8T designs with β= (no. of Fins in PDL)/(no of Fins in PUL) of DS1=3 and DS2=2 are analyzed. The supply voltage ($\mathrm{V_{dd}}$) is set to three different values of 0.8V (nominal), 0.9V and 1.0V.

Our approach for analyzing BTI impact on the SRAM performance focuses on Static Noise Margin (SNM). SNM can be defined as the maximum value of $\mathrm{V_n}$'s (shown in

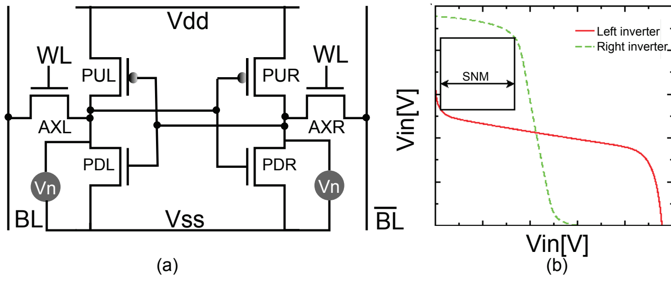

Fig. 4. (a) 6T-SRAM cell with the supply voltages for the analysis (b) schematics to determine SNM of the cell.

Fig. 4(a)) that can be tolerated by the cell before changing state. Schematically, SNM can be obtained by drawing the characteristic curves of the inverters of the cell, and searching for the largest possible square between them as shown in Fig. 4(b). This work is based on the analytical and simulation method of finding cell stability presented in [15]. *The method uses V_n as voltage controlled voltage source and sweeps it from -Vdd to +Vdd. The point of cell state flip gives a measure of the cell's SNM.*

SRAM stability i.e. SNM for different functions can be obtained by node voltage sweep at different locations as suggested in [15]. These metrics are determined as follows:

1) **Read SNM:** is determined by enabling the wordlines to connect the nodes to the pre-charged bitlines, and the V_n is swept from $-V_{dd}$ to V_{dd}. The V_n that flips the cell gives the Read SNM (SNMR).
2) **Hold SNM:** is determined by disabling the wordlines to isolate the nodes from the bitlines, and the V_n is swept from $-V_{dd}$ to V_{dd}. The V_n that flips the cell gives the Hold SNM (SNMH).
3) **Write Trip Point (WTP):** is determined by enabling the wordlines, and sweeping one of the bitline potential from $-V_{dd}$ to V_{dd}. The bitline potential difference at node flipping point gives the write trip point.

C. Performed experiments

Five sets of experiments are performed to investigate the BTI impact on the cell. Each experiment consists of three subset, i.e. NBTI only, PBTI only, and BTI (both NBTI and PBTI). However, only results of limited cases are presented due to the space constraint. The experiments performed are:

1) **Temporal impact:** In this experiment, the temporal BTI impact on 6T SRAM cell's SNMR, SNMH, and WTP are investigated.
2) **Supply voltage dependence:** In this experiment, the impact of supply voltage variation on the BTI induced degradation is investigated.
3) **Design dependence:** In this experiment, a comparison of the BTI impact on 6T and 8T SRAM cells is presented.
4) **Cell strength dependence:** In this experiment, the BTI impact on SRAM cells for different transistor strengths is explored.
5) **Technology dependence:** In this experiment, the BTI impact on SRAM cells synthesized with MOSFET and FinFET transistors is analyzed.

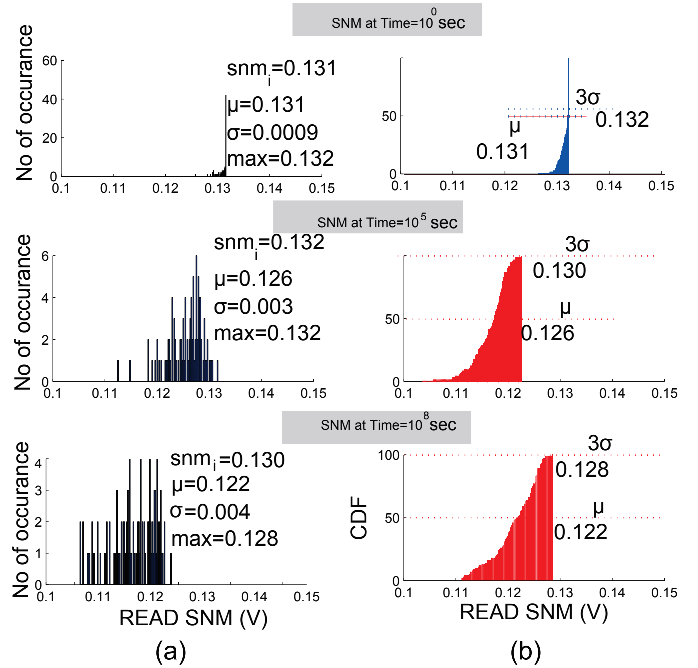

Fig. 5. (a) SNMR distribution of the cell under BTI stress at different age times (b) Cumulative distribution function (CDF) of the SNMR with μ and 3σ points.

IV. Experimental results and discussions

In this section, we present the results and discussions for the SRAM cell experiments described in the previous section.

A. Temporal impact

BTI induced V_{th} shift disturbs the characteristic curves shown in Fig. 4(b), and impacts SNMR, SNMH or WTP. For instance during a read operation, if the shift in V_{th} of AXR is larger than V_{th} shift in PDR, then the external source V_n can change cell state (from 0 to 1 or vice-versa) easily [9]. We have analyzed variation in the metrics due to NBTI alone, PBTI alone and their combination. Fig. 5 shows the SNMR variation due to their combination as the SNMR histogram (Fig. 5(a)), and the cumulative distribution function (Fig. 5(b)). In the cumulative distribution function (CDF), CDF(50%) and CDF(99.7%) correspond to μ and 3σ corner case degradations, respectively. Analysis of the figure reveals that: (a) There is a trend of SNMR shift towards lower values. For instance the 3σ values of the cell SNMR are gradually decreasing from 0.132V to 0.128V (-4%), making it hard for the cells to ensure higher stability, and (b) the distribution spread (difference between μ and 3σ) elevates (from 0.99% at 10^0 seconds to 7.4% at 10^8 seconds) with aging, thus increasing the failure probability during the read operations.

BTI induced variations in other SRAM cell metrics (SNMH and WTP) are also explored by analyzing their cumulative distributions (sorted in an ascending order) at different time steps as shown in Fig. 6. An abstract analysis of the figure shows that SNMR and SNMH decrease with temporal BTI induced V_{th} shift of the FinFETs, while WTP increases with BTI. Furthermore, there is a saturation trend in the distributions at longer ages of the devices. The results are consistent with the FinFET transistor level analysis presented in [4].

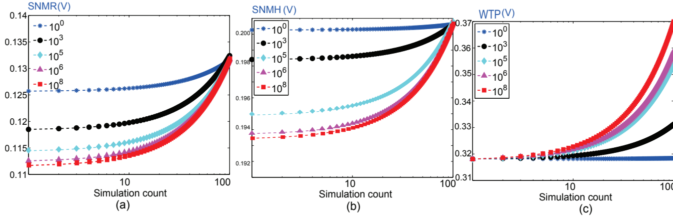

Fig. 6. (a) SNMR, (b) SNMH and (c) WTP distributions (sorted in ascending order) at different time steps.

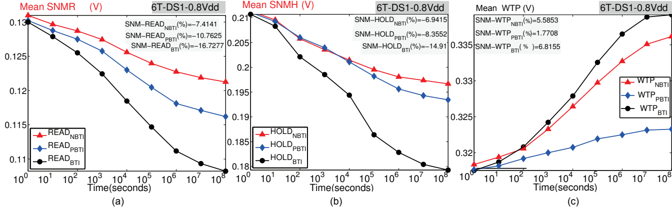

Fig. 7. Temporal degradation of (a) SNMR, (b) SNMH and (c) WTP.

Furthermore, the BTI induced temporal degradation of the 6T SRAM cell is extended by analyzing NBTI, PBTI and their combined impact on all the three metrics with the results shown in Fig. 7. Fig. 7(a) shows that the PBTI impact on the SNMR (10.76%) is more significant than the NBTI impact (7.41%). The higher PBTI impact can be attributed to the bitline discharge through the access and the pull-down transistors during the read operation. Additionally, the BTI impact (16.72%) is less than the linear sum of NBTI and PBTI impacts. It shows that there is some compensation between the impacts. Furthermore, Fig. 7(b) shows that when the cell is not connected to bitlines i.e. during the hold state, the SNMH is equally affected by the NBTI and PBTI in the PFET and NFET causing 6.94% and 8.35% degradation.

Finally, Fig. 7(c) shows that the PBTI impact (1.77%) on the WTP is very low as compared to the NBTI impact (5.58%). This may be attributed to the stronger pull-down transistors in the cell that are less affected by the BTI induced voltage shift.

B. Supply voltage dependence

Supply voltage has a direct impact on the SRAM performance and BTI induced degradation. It has been argued that 10% elevation in the supply voltage can tolerate 10% BTI induced degradation [21]. From cell's perspective, the cells are usually operated at higher supply voltages than the nominal. Hence the current analysis focuses on 6T SRAM cell operation under the nominal (0.8V), and higher 0.9V and 1.0V voltages.

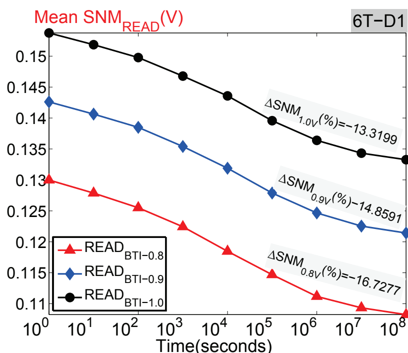

Fig. 8. Temporal variation in SNMR of 6T SRAM cell at different supply voltages.

TABLE I. SNMR DEGRADATION DUE TO NBTI, PBTI AND BTI AT VARIOUS SUPPLY VOLTAGES.

V_{DD} (V)		SNM Read (V) Initial	SNM Read (V) Degraded	Degradation (mV)	Degradation (%)
0.8	NBTI	0.131	0.121	-9.70	-7.41
0.8	PBTI	0.130	0.116	-14.0	-10.7
0.8	BTI	0.130	0.108	-21.7	-16.7
0.9	NBTI	0.143	0.135	-8.60	-5.98
0.9	PBTI	0.143	0.126	-14.5	-10.1
0.9	BTI	0.143	0.121	-21.2	-14.8
1.0	NBTI	0.155	0.147	-7.60	-4.91
1.0	PBTI	0.154	0.140	-13.8	-8.97
1.0	BTI	0.154	0.133	-20.5	-13.3

From Fig. 8, it is apparent that scaling up the supply voltage results in an increased SNMR at 10^0 seconds. For instance, 12% increment (0.9V w.r.t. 0.8V nominal) causes SNMR 9.1% increment (from 0.131V to 0.143V). The increment in the SNMR can be attributed to the availability of higher potential at the cell's nodes that resist attempt of the Vn's to change the cell state during the read operation. Regarding variation in BTI impact with the voltage scaling, the figure shows that the BTI impact decreases with the voltage scaling. For instance, the degradation in SNMR is 16.72% at nominal 0.8V. However, it reduces to only 13.31% when voltage is scaled up to 1.0V.

The analysis are extended to NBTI and PBTI only cases with the results shown in Table I.There is a gradual increment in the initial values of the SNMR (3rd column). The reduction in SNMR w.r.t. the voltage upscaling is more significant in case of NBTI (9.7mV(0.8V)⇒8.6mV(0.9V)⇒7.6mV(1.0V)) than in the PBTI only case (14.0mV(0.8V)⇒14.5mV(0.9V)⇒13.8mV(1.0V)). The difference in the impact can be attributed to the closeness of PFETs to the supply voltage and their smaller sizes w.r.t. NFETs in the cell.

C. Cell's strength dependence

Generally, SRAM cells are designed with minimum sized transistors in a given technology for minimum area and higher density. However, to ensure reliable read and write operations, cell's strength (i.e. transistor sizes) are varied. Among the cell's transistors pull-down transistors of the inverters are more significant. For instance during the read operation, when access transistors are turned on, one of the bitlines discharges through the pull-down transistors. On the other hand, the write capability of the cell is improved by weaker pull-up transistors in the inverters [23]. The current analysis uses 6T SRAM cells shown in Fig. 4 with two drive strengths, i.e. DS1 (PUL:AXL:PDL=1:1:3) and DS2 (PUL:AXL:PDL=1:1:2) at the nominal supply voltage (0.8V).

Fig. 9 shows the mean SNMR degradation due to NBTI, PBTI and BTI as a function of the time. Analysis of the figure shows that weakening of the pull-down transistors in DS2 significantly reduces the SNMR at time 10^0 s. For instance in case of DS1, SNMR=0.131V, however, for DS2 is only SNMR=0.108V. Comparison of SNMR degradation for the two cases shows that the degradation due to NBTI is nearly constant. However, weakening of the NFET significantly increases (from 10.76% to 14.33%) the PBTI induced degradations.

The analysis are extended to SNMH and WTP degradation

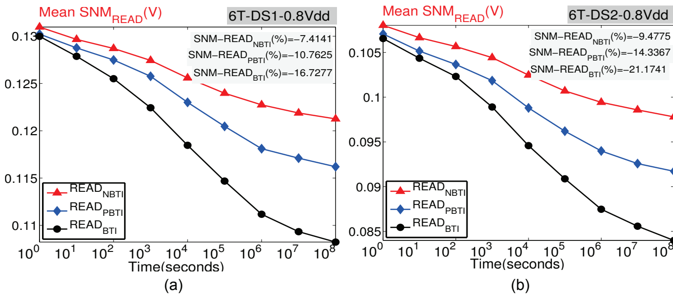

Fig. 9. SNMR reduction due to NBTI, PBTI and BTI in 6T SRAM cell for (a) DS1, and (b) DS2 strengths.

TABLE II. SNMR, SNMH AND WTP DEGRADATIONS IN 6T SRAM CELL FOR THE CELL STRENGTHS OF DS1 AND DS2.

Cell strength		SNMR	SNMH	WTP
DS1	Initial (V)	0.130	0.210	0.317
	Degraded (V)	0.106	0.179	0.339
	Degradation (%)	-16.72	-14.91	6.81
DS2	Initial (V)	0.107	0.392	0.183
	Degraded (V)	0.084	0.361	0.208
	Degradation (%)	-21.17	-12.22	8.35

for BTI only case, and the results are shown in Table II. The table shows that initial values of SNMR and WTP in DS2 are lower than DS1. This can be attributed to weaker pull-down transistors in the inverter. However, the SNMH value for DS2 is higher than DS1. More balanced transistors (pull-up and pull-down) in the case of DS2 also decreases the BTI impact on SNMH.

D. Cell's design dependence

Reliable SRAM cell designs have a major importance for the design community. Researchers have proposed various assist (e.g. read assist, write assist, etc.) methods to improve the write margin, and the read stability of 6T SRAM cell. Improving all the cell stability metrics in a given altered design is difficult. Therefore, a given alteration focuses on a single metric. Chang et al. in [24] have proposed a design with 8T to improve the write margin of the cell. The current analysis focuses on the BTI impact on the 6T (DS1) and 8T (DS1) designs under the nominal voltage. However, they can be extended to other designs easily.

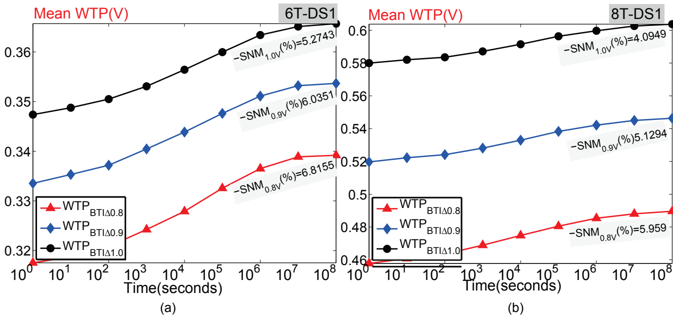

Fig. 10. WTP increment with the stress time in (a) 6T, and (b) 8T SRAM cells.

Fig. 10 shows the temporal degradation in the WTP of both designs as a function of the stress time. Comparison of the two designs shows that 8T design has a high WTP value at 10^0 s. Additionally, the voltage scaling causes more significant improvement on 8T cell than 6T. For instance, 12.5% increment in the supply voltage from the nominal causes 13.05% increment in the WTP 8T, while it is only 6.05% in the 6T cell. Apart from the higher WTP values for the fresh cell, analysis of the degradation slopes reveal that 8T cell are more resilient to the BTI induced performance shift of the transistors.

TABLE III. SNMR, SNMH AND WTP DEGRADATIONS FOR THE 6T AND 8T SRAM CELL DESIGNS.

Cell design		SNMR	SNMH	WTP
6T	Initial (V)	0.130	0.210	0.317
	Degraded (V)	0.106	0.179	0.339
	Degradation (%)	-16.72	-14.91	6.81
8T	Initial (V)	0.067	0.184	0.458
	Degraded (V)	0.052	0.155	0.431
	Degradation (%)	-21.9	-16.1	5.95

The analysis are extended to SNMH and WTP degradation for BTI only case, and the results are shown in Table III. The table shows that initial values of SNMR and SNMH in 8T cell are lower than 6T cell. However, the WTP value for 8T cell is higher than 6T cell due to the enhanced write assist feature of the 8T cell's architecture.

E. Technology dependence

The introduction of FinFET in 22nm and below technologies is a significant deviation from the traditional planar MOSFETs. Therefore, it is necessary to evaluate the reliability of the FinFET based cell in comparison with the MOSFET based cells. At the transistor level, it is claimed that BTI degradation in the FinFET gate dielectric, both NMOS and PMOS BTI degradation mechanisms exist. NMOS PBTI related to the electron trapping in the HK bulk and PMOS NBTI degradation in the IL had been reported [4]. Although, there is no consensus yet, it has been argued that the BTI impact in the FinFET is more significant than in the MOSFETs [4]. On the contrary, C. Auth et al. in [25] have claimed 2× reduction of the PBTI impact in NFET and 2× increment in P-type FinFET w.r.t. to the MOSFETs.

For the current comparative analysis, we have considered the 14nm FinFET [17] and 22nm MOSFET [17] based 6T SRAM cells to evaluate the BTI impact on them under the nominal supply voltage. Fig. 11 shows the SNMR of the two technologies based SRAM cells. Abstract analysis of the figure shows that MOSFET based SRAM cell's SNMR is higher (0.145V) than the FinFET based cell (0.129V). Temporal degradation of the SNMR shows that MOSFET based cells

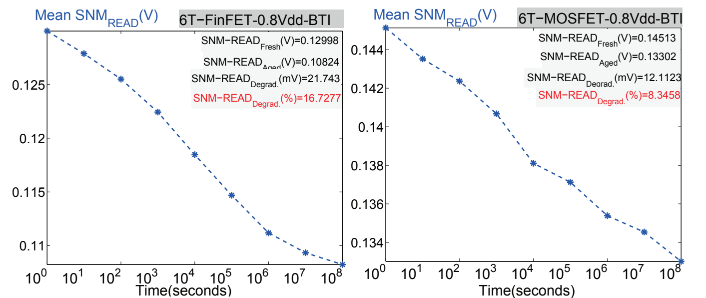

Fig. 11. BTI induced temporal degradation in SNMR for (a) FinFET, and (b) MOSFET based 6T SRAM cells.

TABLE IV. SNMR DEGRADATION DUE TO NBTI, PBTI AND BTI AT VARIOUS SUPPLY VOLTAGES FOR FINFET AND MOSFET TECHNOLOGY NODES.

V_{DD} (V)		FinFET SNM Read (V) Initial	FinFET SNM Read (V) Degraded	FinFET Degradation (mV)	FinFET Degradation (%)	MOSFET SNM Read (V) Initial	MOSFET SNM Read (V) Degraded	MOSFET Degradation (mV)	MOSFET Degradation (%)
0.8	NBTI	0.131	0.121	-9.70	-7.41	0.145	0.132	-12.7	-8.76
0.8	PBTI	0.130	0.116	-14.0	-10.7	0.145	0.148	-2.9	-2.01
0.8	BTI	0.130	0.108	-21.7	-16.7	0.145	0.133	-12.1	-8.34
0.9	NBTI	0.143	0.135	-8.60	-5.98	0.172	0.162	-10.3	-5.99
0.9	PBTI	0.143	0.126	-14.5	-10.1	0.173	0.173	-0.198	-0.112
0.9	BTI	0.143	0.121	-21.2	-14.8	0.174	0.162	-11.3	-6.50
1.0	NBTI	0.155	0.147	-7.60	-4.91	0.209	0.198	-10.8	-5.17
1.0	PBTI	0.154	0.140	-13.8	-8.97	0.208	0.206	-2.30	-1.10
1.0	BTI	0.154	0.133	-20.5	-13.3	0.197	0.195	-11.5	-5.53

are more resilient and degrade only by 8.34% as compared to 16.72% of the FinFET based SRAM cells.

V. CONCLUSION

We proposed a comprehensive analysis to investigate the BTI impact on the SRAM cell metrics. In this paper, we have shown that SNMR degrades at higher rate than WTP and SNMH of the cells. Furthermore, cells with higher pull down transistors operating under higher supply voltages are more resilient to the BTI induced degradation in the FinFETs. Finally, it has been shown that FinFET based SRAM cells are more vulnerable to the BTI degradation than the MOSFET based cells.

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