Bias Temperature Instability and Junction Temperature Measurement Using Electrical Parameters in SiC Power MOSFETs

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***Abstract*—Junction temperature sensing is an integral part of both on-line and off-line condition monitoring where direct access the bare die surface is not available. Given a defined power input, the junction temperature enables the estimation of the junction-to-case thermal resistance, which is a key indicator of packaging failure mechanisms like solder voiding and cracks. The use of temperature sensitive electrical parameters has widely been proposed as a means of junction temperature sensing however, there are certain challenges regarding their use in SiC MOSFETs. Bias Temperature Instability from charge trapping in the gate dielectric causes threshold voltage drift, which in SiC affects some of the key temperature sensitive electrical parameters including ON-state resistance, body diode forward voltage as well as the current commutation rate. This paper reviews the impact of bias temperature instability on the accurate junction temperature measurement using temperature sensitive electrical parameters in SiC MOSFETs.**

***Index Terms*—Bias Temperature Instability, Junction Temperature, SiC MOSFETs**

I. INTRODUCTION

AN industry survey in [1] showed that reliability remains a very critical factor in power electronics. Condition monitoring appears as a suitable method of improving the reliability of power electronics [2], electrical machines [3] and capacitors [4]. In the case of power electronics systems, condition monitoring based on Temperature Sensitive Electrical Parameters (TSEPs) [5, 6] is a suitable method for monitoring reliability since it enables real-time junction temperature sensing during power cycling. This is fundamental for obtaining lifetime estimation [7] since it enables the monitoring of the degradation of the thermal impedance of the device/module due to degradation of the packaging elements, namely solder and wire bonds [8].

TSEPs have been widely used for silicon devices [5], however there are several challenges regarding the use of TSEPs in SiC power devices. SiC power MOSFETs, by virtue of the wider bandgap compared to silicon, are not as temperature sensitive as silicon devices [9-11]. This is sometimes presented as an advantage, especially since the switching and conduction losses do not increase rapidly with temperature. However, this reduced temperature sensitivity of SiC makes the use of TSEPs for junction temperature sensing more difficult, especially considering the practical implementation [12].

One of the main challenges limiting the adoption of SiC MOSFETs as the power semiconductor of choice in power electronic applications is the reliability of the gate oxide [13]. Despite the improvements of the latest SiC power MOSFETs [14], threshold voltage shift caused by Bias Temperature Instability (BTI) and dielectric breakdown remain as reliability concerns for SiC power devices compared with Si power devices [15, 16]. BTI simply refers to the process where threshold voltage (V_{TH}) drift occurs due to gate voltage stress [17].

The application of a positive bias on the MOS gate results in an accumulation of electrons in the semiconductor adjacent to the gate dielectric thereby causing the trapping of negative charges and a concomitant increase in the threshold voltage since a greater positive voltage is required to overcome the negative charges. This is called positive bias temperature instability (PBTI). Likewise, the application of a negative bias on the MOS gate results in an accumulation of holes and a resultant decrease in the threshold voltage resulting from trapped positive charges in the oxide. This is called negative bias temperature instability (NBTI). This phenomenon is well understood on silicon devices and improved oxidation, surface treatment and anneal processes have reduced the occurrence. However, in SiC power MOSFETs, as a result of the presence of carbon atoms during the oxidation of the semiconductor [17-19], the increased oxide, interface and near-interface traps make NBTI and PBTI more active. The threshold voltage shift recovers when the gate bias is removed, and this recovery is accelerated if the gate is biased with the opposed polarity to the stress [19].

A thorough comparison of different power devices under accelerated gate bias stress tests was presented in [20], where it was shown that the voltages required to damage the gate oxide are considerably higher for Si devices. In addition to the breakdown of the oxide, the shift of V_{TH} is a reliability concern which can have implications for the application [16, 17, 21].

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These may be increased power losses due to increased ON-state resistance [17], uneven current sharing during switching transients if the V_{TH} shift is different for devices connected in parallel [22, 23] or increase the susceptibility of the device to parasitic turn-ON [24] due to V_{TH} reduction.

Furthermore, the drift of the threshold voltage caused by BTI in SiC MOSFETs [17, 21, 25] increases the complexity of junction temperature measurement, making it a challenge compared to Si devices and will have a negative impact on the implementation of condition monitoring.

This paper expands the initial investigations on accurate junction temperature measurement in SiC MOSFETs using TSEPs initially presented in [26] and it is organized as follows: Section II presents a review of some of the most important TSEPs in SiC MOSFETs, Section III presents a summary of the investigations on threshold voltage instability and the measurement of threshold voltage in SiC MOSFETs, Section IV analyzes the impact of the threshold voltage shift caused by BTI on the measurement of the junction temperature using TSEPs and Section V concludes the paper.

II. TSEPs In SiC MOSFETs

The temperature sensitivity of some of the most common TSEPs for SiC MOSFETs is presented in this section. The evaluated TSEPs are the threshold voltage V_{TH}, ON-state resistance $R_{DS\text{-}ON}$, gate voltage plateau V_{GP}, the body diode voltage V_{SD} and the switching rate of the drain current dI_{DS}/dt. There are other TSEPs like the internal gate resistance or peak gate current [27, 28] which are not covered in detail in this paper, however the implications on their use for accurate temperature sensing are also applicable. The devices evaluated in this investigation are discrete TO-247 packaged devices. For characterization, the temperature was set using a small heater attached to the device, allowing sufficient time for thermal equilibrium where the junction and case temperatures are the same.

A. Threshold voltage

The threshold voltage V_{TH} is a well-known TSEP for MOS gate devices [29, 30]. It can be defined as the gate voltage required to invert the channel i.e. to raise the MOSFET surface potential to twice the bulk potential [30]. An expression of V_{TH} is given by (1) [30], where ε_{SiC} is the dielectric constant of SiC, k is the Boltzmann's constant, T is temperature, N_A is the doping density, n_i is the intrinsic carrier concentration, C_{ox} is the specific oxide capacitance, q is the fundamental charge and Q_{ox} is the effective charge in the oxide. The trapped charges in the oxide and interface are part of Q_{ox}, hence their role on V_{TH} can be analyzed. From (1), the trapping of positive charges causing a reduction of V_{TH} and the trapping of negative charges causing an increase of V_{TH}.

$$V_{TH} = \frac{\sqrt{4\varepsilon_{SiC}kTN_A ln\left(\frac{N_A}{n_i}\right)}}{C_{ox}} + \frac{2kT}{q} ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{ox}}{C_{ox}} \quad (1)$$

V_{TH} reduces with temperature due to the increasing intrinsic carrier concentration n_i and a detailed expression of the temperature sensitivity of V_{TH} is given in [30]. In the datasheets of power devices there are two methods that are commonly used for determining V_{TH}. One consists in forcing a low current (several mA) through the device, with the gate and drain shorted. [29]. In other cases, a fixed low drain-source voltage (1 V to 10 V) is used and the gate voltage of the device is adjusted until the required current (range of mA) flows through the device [29]. The threshold voltage as a function of temperature of different power devices, including a 650 V field stop trench silicon IGBT, a 650 V trench SiC MOSFET and a 900 V planar SiC MOSFET has been characterized in this paper using the constant current method with a drain current of 10 mA.

The selected devices have a similar current rating at 25°C which is 40 A in the case of the 650 V silicon IGBT, 39 A for the 650 V SiC trench MOSFET and 36 A for the 900 V SiC planar MOSFET. The measured V_{TH} at ambient temperature (21 °C) is shown in Table I, whereas the normalized V_{TH} as a function of temperature is shown in Fig. 1.

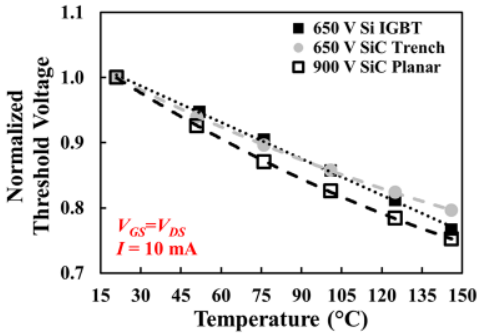


Fig. 1 Normalized threshold voltage as a function of temperature for different device technologies

TABLE I THRESHOLD VOLTAGE AT 21 °C
(Measured at 10 mA, Gate and Drain Shorted)

	650 V Si IGBT	650 V SiC Trench MOSFET	900 V SiC Planar MOSFET
V_{TH} (V)	5.39	4.45	2.31

Analyzing the nominal V_{TH} value, the threshold voltage of the planar SiC MOSFET is considerably lower than the threshold voltage of the IGBT and the trench SiC MOSFET. The V_{TH} is determined by the gate oxide thickness and the p-body doping [30]. V_{TH} is usually lower in SiC MOSFETs [31, 32] due to the lower effective p-body doping resulting from the incomplete ionization of the boron atoms during the post-implantation anneal [33, 34].

From the results in Fig. 1, it is clearly observed that V_{TH} reduces with temperature for all the devices with similar normalized temperature sensitivities. V_{TH} could be considered a good TSEP, if the challenge of threshold voltage instability coupled with the difficulty of accurate on-line measurements was not present in SiC MOSFETs.

B. ON-state resistance

The ON-state resistance $R_{DS\text{-}ON}$ of a MOSFET is the resistance between the drain and source terminals when the device is ON. It is comprised of different parasitic resistances which contribute to the total ON-state resistance, as defined in [30, 35]. In the case of a SiC planar MOSFET, the total $R_{DS\text{-}ON}$

can be expressed using (2) [10, 35]. R_{CH} is the channel resistance, R_{JFET} is the resistance of the JFET region and R_{DRIFT} is the resistance of the drift layer. In a SiC trench MOSFET, there is no JFET resistance, so R_{JFET} is eliminated from (2).

$$R_{DS\text{-}ON} \sim R_{CH} + R_{JFET} + R_{DRIFT} \quad (2)$$

In SiC MOSFETs, as a result of the high critical electric field, a thinner drift layer is required for blocking high voltages, hence the contribution of R_{DRIFT} to the total ON-state resistance is reduced compared with Si MOSFETs. This means that the contribution of R_{CH} to the total $R_{DS\,ON}$ is higher for SiC MOSFETs compared to silicon devices, especially for low voltage devices.

The channel resistance R_{CH} is given by (3) [17], where V_G is the gate driving voltage, μ_n is the electron effective mobility, C_{OX} is the gate oxide capacitance density, L_{CH} is the length of the channel and W is the channel width.

$$R_{CH} = \frac{L_{CH}}{W\mu_n C_{OX}(V_G - V_{TH})} \quad (3)$$

In SiC MOSFETs, the magnitude of the temperature coefficient of the effective mobility is lower than that of Si MOSFETs [36]. Since V_{TH} reduces with temperature in both Si and SiC MOSFETs, R_{CH} decreases with increasing temperature, meaning it has a negative temperature coefficient (NTC) [10]. R_{DRIFT} and R_{JFET} increase with temperature due to increased phonon scattering [10], hence exhibit a positive temperature coefficient (PTC). As a result, the different resistances in (2) have competing temperature coefficients which will determine the global temperature sensitivity of $R_{DS\text{-}ON}$. As the relative contribution of R_{CH} is higher in SiC MOSFETs, the temperature sensitivity of $R_{DS\text{-}ON}$ is not as pronounced as in Si MOSFET, where the PTC of R_{DRIFT} dominates. This is shown in Fig. 2, where the normalized $R_{DS\text{-}ON}$ is plotted as a function of temperature for a series of different 1200 V MOSFETs.

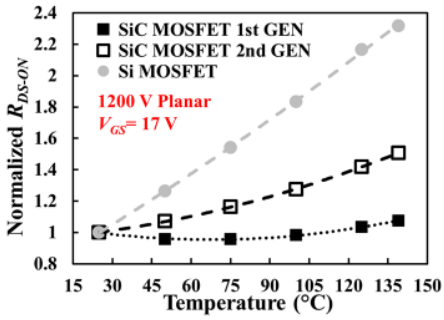


Fig. 2 Normalized ON-State resistance as a function of temperature for different 1200 V Si and SiC MOSFETs

For the silicon MOSFET $R_{DS\text{-}ON}$ increases by over 100% whereas for the SiC devices, $R_{DS\text{-}ON}$ increases by 40% for the 2nd generation device and is nearly temperature invariant for the 1st generation device. Comparing the first and second generation SiC devices, the higher temperature sensitivity of the second generation is due to the improved channel resistance [10]. This results on a well-defined PTC, which is required for paralleling devices safely.

From (3) it is observed that R_{CH} is affected by the gate voltage used to turn-ON the MOSFET as well as temperature (mobility and threshold voltage). Driving the device with lower gate voltage will increase the partial contribution of the R_{CH} to the total $R_{DS\text{-}ON}$, resulting in different temperature coefficients as a function of the gate voltage [37]. The ON-state resistance as function of the gate driver voltage for 1200 V silicon MOSFET is shown in Fig. 3, where a clear PTC is observed for the whole driving V_{GS} voltage range. This is due to $R_{DS\text{-}ON}$ being dominated by R_{DRIFT}, which has a PTC. The $R_{DS\text{-}ON}$ approximately doubles its value with temperature.

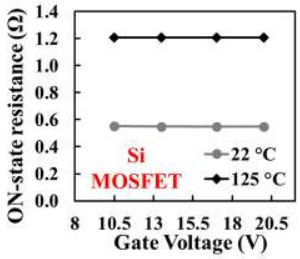
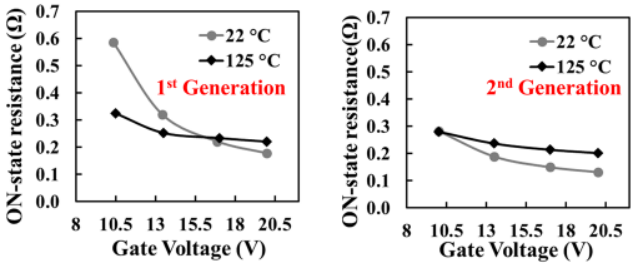


Fig. 3 ON-state resistance as a function of the gate voltage at 22 °C and 125 °C for a 1200 V Si MOSFET.

Depending on the SiC MOSFET generation and the improved channel resistance, the impact of the gate voltage will be different. This is shown in Fig. 4(a) for a 1200 V 1st generation planar SiC MOSFET, where a clear PTC is observed for gate voltage values greater than 16 V and a NTC is observed for lower V_G values. Fig. 4(b) shows the $R_{DS\text{-}ON}$ as function of V_{GS} for a 1200 V 2nd generation planar SiC MOSFET which has PTC for the whole range of driving gate voltage values.



(a) (b)

Fig. 4 ON-state resistance as a function of the gate voltage at 22 °C and 125 °C for a 1200 V SiC MOSFET. (a) First Generation, (b) Second generation

The zero-temperature coefficient (ZTC) point is the bias condition where the MOSFET $R_{DS\text{-}ON}$ is temperature invariant. The ZTC point is where the NTC of the effective mobility is balanced by the NTC of the threshold voltage hence, total $R_{DS\text{-}ON}$ of the MOSFET is temperature invariant. The ZTC point is approximately 16 V for the 1st generation device whereas it is approximately 10.5 V for the 2nd generation device, as shown in Fig. 4.

This TSEP is particularly relevant as it has been proposed in different publications like [12, 38]. Its applicability to SiC MOSFETs will have to be evaluated carefully given the BTI challenges mentioned in the previous section.

C. *Body diode voltage.*

The voltage of a PN junction is a well-known TSEP for

silicon and silicon carbide devices. It is widely used for determining the junction temperature during power cycling [39] in the case of MOSFET body diodes. The forward voltage V_F of a PiN diode in the ON-state is given by the sum of the junction voltages ($V_j(p^+n)$ and $V_j(nn^+)$) and the drift layer voltage V_{drift}, as given in (4) [40].

$$V_F = V_j(p^+n) + V_{drift} + V_j(nn^+) \quad (4)$$

The temperature dependency of the forward voltage of a PiN diode is determined by the temperature coefficients of the different elements defining V_F. The drift layer voltage V_{drift} has a PTC due to decreased carrier mobility from increased phonon scattering, whereas the junction voltages $V_j(p^+n)$ and $V_j(nn^+)$ have a NTC due to increased carrier concentration from thermally induced bandgap narrowing [40]. Furthermore, the junction voltages are independent of current while the drift layer voltage increases with current [40]. This TSEP is mainly used at low currents and in this situation, V_F is mainly determined by the junction voltages, as defined in (5) [40], where k is the Boltzmann's constant, T is temperature, q is the fundamental charge, p_L is the hole concentration, n_R is the electron density and n_i is the intrinsic carrier concentration.

$$V_F = V_j(p^+n) + V_j(nn^+) = \frac{kT}{q} ln \frac{p_L n_R}{n_i^2} \quad (5)$$

As the intrinsic carrier concentration increases with temperature, at low currents the forward voltage of a PiN diode decreases with temperature [40]. Considering the body diode of a SiC MOSFET, one of its peculiarities is that it requires a negative voltage to fully close the channel, resulting on 3rd quadrant characteristics which are gate voltage dependent [29, 39-41]. This is shown in Fig. 5, which presents the measured forward voltage as function of the applied gate voltage at ambient temperature (22 °C) for different SiC MOSFETs and a Si MOSFETs. Due to the wide bandgap properties, V_F is higher for SiC PiN diodes [40]. However, the accurate forward voltage of the SiC PN junction body diode is not measured until the channel is fully closed by applying a sufficient negative gate voltage. When V_{GS}=0, during conduction of a reverse current there is partial channel conduction due to the body effect [41] hence the measured forward voltage of the body diode is lower than the true value (around 1.5 V). As the magnitude of the negative gate voltage is increased and more current flows through the body diode, the forward voltage increases, as shown in Fig. 5. At a gate voltage around -5 V, the channel is fully closed and the current flows only through the body diode. In this situation, the measured forward voltage, around 3 V, corresponds to a SiC PN junction. This phenomenon is not observed in the evaluated Si MOSFET, whereas in SiC MOSFETs, the body effect is more evident because of the high V_{SD} compared to silicon (due to the wide bandgap) [41].

The calibrated temperature sensitivity of the body diode voltage (V_{SD}) of a SiC MOSFET is shown in Fig. 6. The selected device is a 650 V SiC Trench MOSFET and the sensing current I_{SD} was 50 mA. The voltage was measured at V_{GS}=0 (partial channel conduction) and V_{GS}=-10 V (no channel conduction). The impact of V_{GS} on V_{SD} and its temperature sensitivity is clearly observed [41], resulting in two different calibration curves.

The channel conduction when V_{GS}=0 will be affected by BTI-induced V_{TH} shifts; hence it is important to assess its impact on the use of this parameter as TSEP.

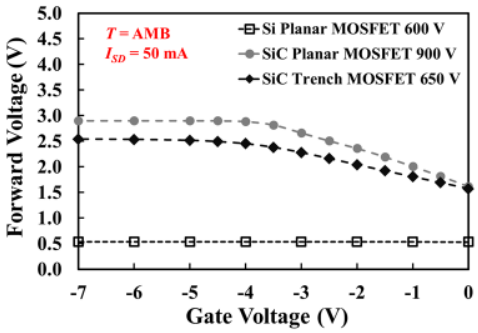


Fig. 5 Body diode voltage for different Si and SiC MOSFETs as function of the gate voltage. Ambient temperature, I_{SD}= 50 mA

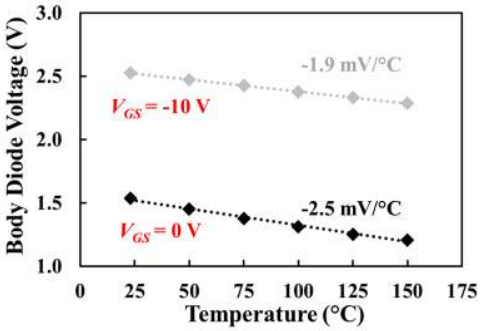


Fig. 6 Forward voltage of the body diode of a 650 V SiC trench MOSFET as a function of temperature for different gate voltages. I_{SD}=50 mA

D. *Switching rate of the drain current*

The switching rate of the drain current dI_{DS}/dt is a TSEP for SiC MOSFET which was analyzed in detail in [37, 42], where it was shown that the turn-ON dI_{DS}/dt increases with temperature. Its temperature sensitivity can be analyzed using (6) [42], where β is the MOSFET gain factor, which is given by $\beta = \mu_n C_{OX} W/L_{CH}$ [40].

$$\frac{d^2 I_{DS}}{dtdT} = \frac{dV_{GS}}{dt}\left(\beta \left|\frac{dV_{TH}}{dT}\right| - (V_{GS} - V_{TH}) \left|\frac{d\beta}{dT}\right|\right) \quad (6)$$

From (6), the parameters contributing to the temperature sensitivity of dI_{DS}/dt are dV_{TH}/dT and $d\beta/dT$. In (6) the absolute value of both parameters is used; hence the negative temperature coefficient of V_{TH} tends to increase dI_{DS}/dt while the negative temperature coefficient of β tends to reduce dI_{DS}/dt. The temperature sensitivity of β is determined by the effective mobility μ_n and in the case of SiC MOSFETs, due to its reduced temperature sensitivity compared to silicon devices [36], dV_{TH}/dT dominates $d\beta/dT$. Hence, the turn-ON current switching rate increases with temperature in SiC MOSFETs. More details are given in [42]. Fig. 7 shows the drain current transients during turn-ON of a 650 V SiC trench MOSFET at different temperatures, which were measured using a conventional double pulse test setup [43]. The gate voltage V_{GS}

and gate resistance R_G used for characterization were selected to maximize the temperature sensitivity of dI_{DS}/dt, as described in [37]. Fig. 7 clearly shows how the switching rate increases with temperature.

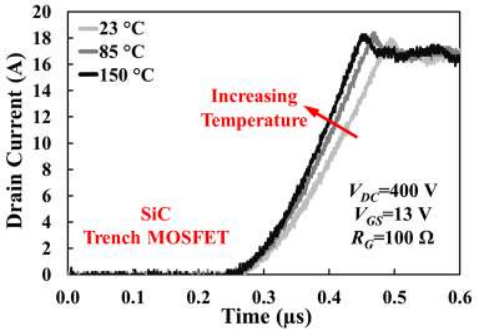


Fig. 7 SiC trench MOSFET. Drain current transients during turn-ON at different temperatures

In silicon MOSFETs, the turn-ON switching transient of the drain current rates tend either to be temperature invariant or decrease with temperature [42, 44] while in silicon IGBTs the turn-ON transient shows a characteristic double temperature coefficient due to the different temperature coefficients of the threshold voltage and the plasma formation required for conductivity modulation in IGBTs [45]. As these transient characteristics are affected by the value of V_{TH}, it will be important to characterize the impact of BTI.

E. Gate plateau during turn-ON

As a result of the temperature sensitivity of V_{TH} and dI_{DS}/dt, the gate voltage plateau V_{GP} has also a well-defined temperature sensitivity in SiC MOSFETs [42]. The gate voltage plateau can be defined as the gate-source voltage value at which the drain current reaches the load current I_{LOAD} during turn-ON. Its value is given by (7) and it is also affected by the value of the load current [30].

$$V_{GP} = V_{TH} + \sqrt{\frac{I_{LOAD} L_{CH}}{\mu_n C_{OX} W}} \tag{7}$$

The load current is determined by the converter operation and topology. For example, in an inverter the load current is sinusoidal, and the transistor will switch at different drain current values during one load cycle. The peak sinusoidal current will also change if the output power varies. In a buck converter, if the output power is fixed, the switched drain current can be considered constant. However, variations of the output power and the converter operation mode will affect its value. Hence, in order to use TSEPs that depend on the load current, measurement sequences will be required, like in [46].

Fig. 8 shows the gate voltage transient during turn-ON of a SiC trench MOSFET at different temperatures, where it is clearly observed that V_{GP} decreases with temperature. As this TSEP is load dependent, it is also worth to analyze the impact of the load current on the temperature sensitivity of V_{GP}. This has been evaluated for load currents of 10 A and 20 A using the SiC trench MOSFET and the results are shown in Fig. 9. The selected gate voltage is 18 V, for allowing enough gate voltage overdrive.

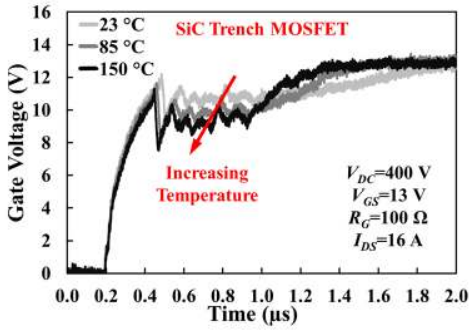
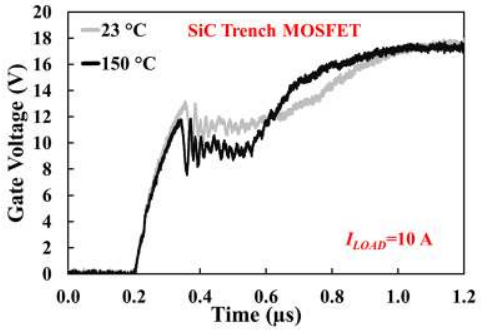
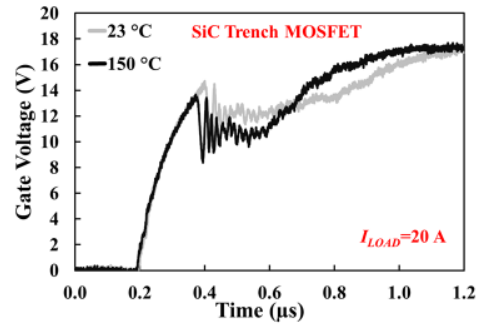


Fig 8 SiC trench MOSFET. Gate voltage transients during turn-ON at different temperatures



(a)



(b)

Fig. 9 SiC trench MOSFET. Impact of load current on the temperature sensitivity of gate voltage plateau. (a) I_{LOAD} = 10 A, (b) I_{LOAD} = 20 A

The variation of V_{GP} as function of temperature and I_{LOAD} is shown in Table II. The results in this table indicate that the temperature sensitivity of V_{GP} decreases with increasing load current. This can be explained by analyzing (7), as the reduction of V_{TH} is compensated by the dependency of the square-root term on the load current.

TABLE II: IMPACT OF LOAD CURRENT ON THE TEMPERATURE SENSITIVITY OF THE GATE VOLTAGE PLATEAU

I_{LOAD} (A)	V_{GP} at 23 °C (V)	V_{GP} at 150 °C (V)	Sensitivity (mV/°C)
10	11.25	9.56	-13.29
20	11.92	10.74	-9.29

Another way of characterizing the gate plateau is the gate current transient, where a gate current plateau I_{GP} is also observed. The gate current transients are shown in Fig. 10, and it has the opposite temperature sensitivity to the gate voltage plateau since it increases with temperature [42]. It should however be noted that using V_{GP} and I_{GP} as TSEPs come with

great difficulty since the plateau duration is shortened as the switching rates are increased. Furthermore, the transient waveforms become obscured by high frequency ringing when the MOSFETs are switched with high dI_{DS}/dt and dV_{DS}/dt.

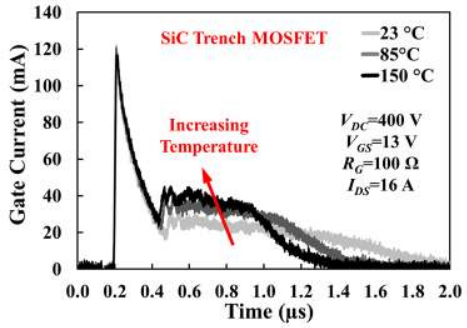


Fig 10 SiC trench MOSFET. Gate current transients during turn-ON at different temperatures

III. Bias Temperature Instability And Threshold Voltage Measurement in SiC MOSFETs

A. BTI characterization in SiC MOSFETs

Before evaluating the impact of BTI on TSEPs, it is important to make some remarks regarding V_{TH} measurement after gate stress in SiC MOSFETs. As stated previously, the gate oxide reliability of SiC MOSFETs has been one of the main fabrication issues [13]. The higher defect density in the SiO_2/SiC interface [13, 17] together with the reduced band offsets to the dielectric [17, 47] make the gate dielectric interface and BTI in SiC MOSFET more complex. The mechanisms of BTI in SiC MOSFETs [16] are the same as in silicon devices. However, considering the measurement of V_{TH} after V_{GS} stress removal, several features have been identified, including the dependency of the V_{TH} shift on the stress voltage, stress duration and temperature [17, 48-50]. However, there are certain peculiarities that make the case of BTI in SiC MOSFET a challenge.

Firstly, the recovery of V_{TH} after stress removal [17, 21, 25]. Once the gate bias is removed, there is a fast recovery of V_{TH} as the traps are released [16]. Traps with time constants ranging from several µs to ks have been identified [21, 51], which are responsible for a fast-transient recovery and more permanent V_{TH} shift. Secondly, the measurement technique also has an impact of the measured V_{TH} [17, 52, 53]. Factors affecting the measured V_{TH} value are the gate voltage sweep direction, the measurement speed and the interruption of the stress and stress reapplication [16, 17, 54]. More information about the different techniques is available [16], which reviews the different methodologies proposed in the literature for characterization of V_{TH} shifts in SiC MOSFETs.

The sweep direction of the measurement reveals a hysteresis phenomenon in the V_{TH} of SiC MOSFETs [17]. When V_{TH} is measured in the upward sweep of V_{GS} (moving from accumulation to inversion) the threshold voltage is lower than when it is measured in the downward sweep (from inversion to accumulation). This is caused by charged traps in the interface and it is specific to SiC MOSFETs due to the higher defect density [17]. These traps have a short capture/emission time, within a switching period [17, 51]. This V_{TH} hysteresis is recoverable and does not affect circuit operation according to [16, 17, 21].

Large V_{TH} hysteresis and changes of ON-state resistance were detected in [16], where high frequency (50 kHz) AC gate bias tests were used. In [16] it is reported that this large recoverable shift should not have any substantial impact on the performance of the device, but it will be important to select the appropriate negative gate voltage for turning-OFF the device, as it can affect the lifetime of the MOSFET [55]. Recent investigations [56] have been able to capture the impact of BTI in a converter leg operation using shoot-through currents in the range of several hundreds of microseconds.

The recovery of V_{TH} after stress removal can also, have implications in the qualification of devices [57], since there can be long delay times between stress application and post-stress measurement. A delay independent technique based on a preconditioning sequence [54] does not measure fully recoverable shifts and minimizes the dependency of the measurement on the delay time. Hence it is able to capture the application relevant V_{TH} shift, attributed to traps within the oxide. These traps have long capture/emission time constants [17]. In [17] different commercial devices were characterized using the preconditioning technique, where the results indicate that some vendors have MOSFETs more prone to BTI-induced shifts, including a wide range of V_{TH} shift for the same stress.

B. Gate stress and V_{TH} shifts in SiC MOSFETs

To illustrate the concept of V_{TH} shift, accelerated high temperature gate bias stresses have been performed on commercially available devices. The stress and recovery schematic circuits are shown in Fig. 11.

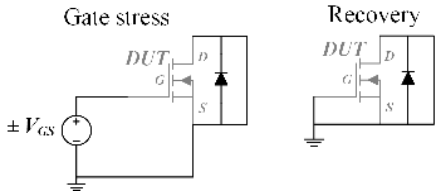


Fig. 11 Stress and recovery circuits for gate bias stress tests

The transfer characteristics of the devices were obtained using a curve tracer model 371B from Tektronix at ambient temperature before stress and after a relaxation period of 16 hours with the gate and source terminals shorted (V_{GS}=0). This recovery time is use for characterizing only the more permanent long-term V_{TH} shift, as described previously and easing the stress/recovery/characterization sequence. Fig. 12 shows the pre-stress and post-stress transfer characteristics of a 650 V silicon IGBT, measured at ambient temperature, 16 hours after stress removal. The stress values were +40 V for the PBTI evaluation and –40 V for NBTI evaluation. The duration of the stress was 1 hour at a temperature of 150 °C. The results in Fig. 12 show no apparent V_{TH} shift on the transfer characteristics of the IGBT. In the case of SiC MOSFETs, the threshold voltage shift caused by BTI, increases with the gate voltage applied to the device [16]. Using the SiC trench MOSFET, cumulative gate stresses have been applied for evaluating both PBTI and NBTI [58]. The stress voltage,

duration and temperature are shown in Table III, whereas the measured pre- and post-stress transfer characteristics are shown in Fig. 13 and Fig. 14.

The stresses were cumulative, with two initial stages of the same stress magnitude. These V_{GS} stresses are higher than the recommended values but are deemed suitable for explaining the concept of BTI-induced V_{TH} shifts. The selected stress voltages are based on stress voltages used in [20, 50]. In [59] the authors use V_{GS} voltages twice the rated value, which is 18 V in the case of the device evaluated in this paper, for pre-screening the oxide quality.

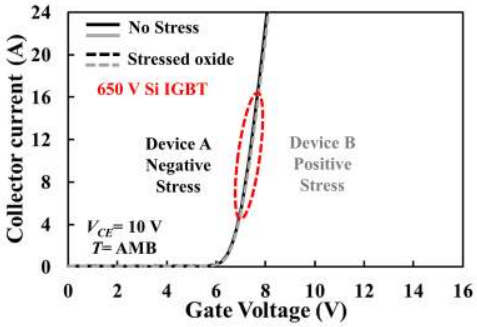


Fig. 12 Si IGBT. BTI impact on transfer characteristics.

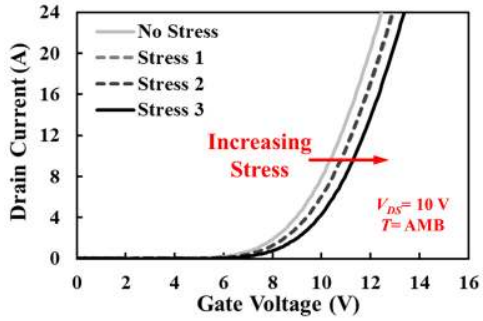


Fig. 13 SiC Trench MOSFET. Impact of PBTI on the transfer characteristics

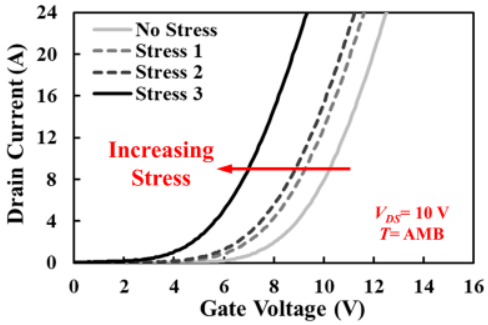


Fig. 14 SiC Trench MOSFET. Impact of NBTI on the transfer characteristics

TABLE III: CUMULATIVE GATE STRESS FOR EVALUATION OF BTI [58]

	PBTI	NBTI
Stress 1	35V, 150 °C, 30 minutes	- 35V, 150 °C, 30 minutes
Stress 2	35V, 150 °C, 30 minutes	- 35V, 150 °C, 30 minutes
Stress 3	40V, 150 °C, 30 minutes	- 40V, 150 °C, 30 minutes

The results in Fig. 13 and Fig. 14 show that the threshold voltage shift is directly proportional to the stress voltage and it is more apparent for the negative gate stresses, as expected for N-channel MOSFETs [60]. The higher impact of NBTI has been reported in [61, 62], with improvements in NBTI performance if the manufacturing process is optimized [47, 62]. Studies in [16] reported a high concentration of traps with small capture/emission times for NBTI compared with PBTI, but further studies are required to identify the physical nature of the defects causing the BTI-induced V_{TH} shifts [16, 21].

IV. THRESHOLD VOLTAGE INSTABILITY AND TSEPS IN SIC MOSFETS

Some challenges regarding instrumentation and real time measurement of junction temperature using TSEPs in SiC MOSFETs were evaluated in [12], however the objective of this section is evaluating how BTI will affect the performance and accuracy of TSEPs for determining the junction temperature of SiC MOSFETs. This evaluation has been performed using a 650 V SiC Trench MOSFET, which was subjected to accelerated positive and negative gate stresses. The stresses applied were +40 V for 1 hour at 150 °C for the evaluation of PBTI and -40 V for 1 hour at 150 °C for the evaluation of NBTI. The devices were characterized before stress and after stress removal, following a recovery time of 16 hours with the gate and source shorted (V_{GS}=0). The pre- and post-stress transfer characteristics are shown in Fig. 15, showing a PBTI-induced V_{TH} shift of +0.79 V and a NBTI-induced V_{TH} shift of -2.61 V. The V_{TH} was extracted from the transfer characteristics using the Current-to-Square-Root-of-Transconductance method [63].

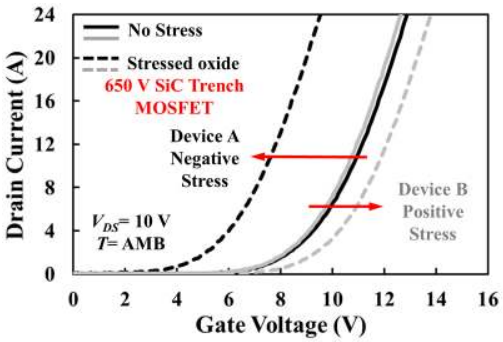


Fig. 15 SiC Trench MOSFET. Transfer characteristics of the devices subjected to BTI stress tests for TSEP characterization

The main objective of this investigation is characterizing the impact of the V_{TH} shift on TSEPs rather than characterizing the reliability of the device or determining the peak shift after stress removal. The long recovery of 16 hours has been selected for minimizing the impact of the recoverable shift on characteristics measured after stress removal, hence characterizing a more permanent V_{TH} shift.

A. BTI and ON-state resistance

As described in section II, in SiC power MOSFETs, the channel resistance R_{CH} has an important contribution to the total $R_{DS\text{-}ON}$. Since R_{CH} is affected by the value of V_{TH}, it is important to characterize the impact of BTI on the output characteristics of SiC power MOSFETs. This has been done using the stressed devices shown in Fig. 14. Fig. 16 shows the measured pre-stress and post-stress output characteristics of the SiC trench

MOSFET subjected to PBTI stress. The output characteristics were measured at ambient temperature using a curve tracer Tektronix 371B. The results in Fig. 16 show a shift of the output characteristics to the right, indicating an increase of the ON-state resistance. The contribution of R_{CH} is higher at low gate voltage values, hence the more apparent shift of the output characteristics observed at V_{GS}=12 V. The calculated ON-state resistance extracted from the output characteristics is shown in Fig. 17, where it is shown that the impact of BTI is more apparent at higher currents, when the device is driven at lower V_{GS} values.

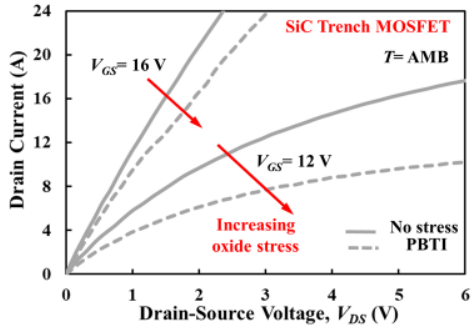


Fig. 16 SiC trench MOSFET. Output characteristics pre- and post- PBTI stress

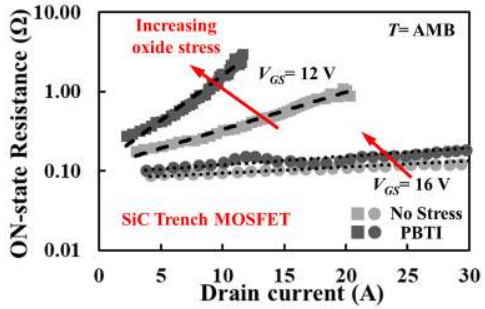


Fig. 17 SiC trench MOSFET. $R_{DS\text{-}ON}$ as a function of current for PBTI stress

The output characteristics for the NBTI stress are shown in Fig. 18. In this case, a clear shift leftwards is observed, indicating the reduction of the $R_{DS\text{-}ON}$.

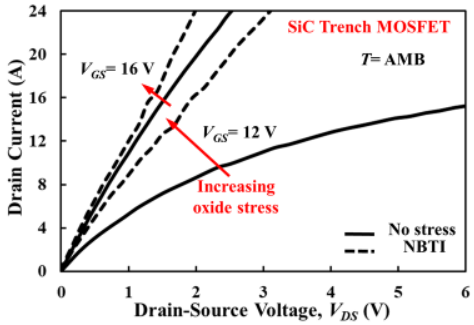


Fig. 18 SiC trench MOSFET. Output characteristics pre- and post- NBTI stress

The calculated $R_{DS\text{-}ON}$ extracted from the output characteristics is shown in Fig. 19. As it was the case of the PBTI stress, the reduction of the ON-state resistance becomes more apparent when the device is driven at low V_{GS} values and the current is increased.

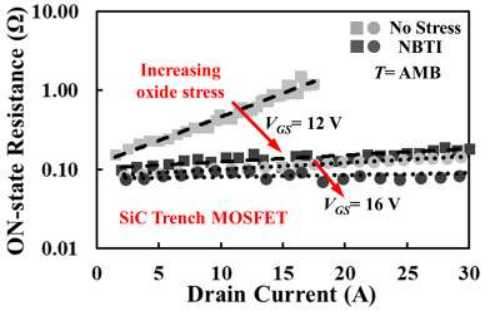
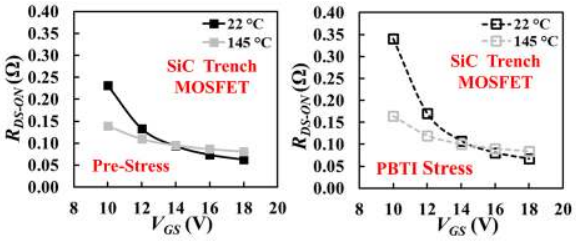


Fig. 19 SiC trench MOSFET. $R_{DS\text{-}ON}$ as a function of current for NBTI stress

The results presented in Fig. 16 to Fig. 19 clearly indicate that $R_{DS\text{-}ON}$ is affected by BTI. As the $R_{DS\text{-}ON}$ is a parameter that is usually monitored to indicate damage of the packaging during power cycling tests, this change of resistance may have a considerable impact on the evaluation of the measured results. In some cases, for monitoring the degradation of the packaging elements independently of temperature, it can be considered to operate in the ZTC point [64]. However, the change of the partial contribution of the channel resistance due to BTI in SiC MOSFETs will also affect the ZTC point of $R_{DS\text{-}ON}$. This has been evaluated for both PBTI and NBTI stresses, characterizing the $R_{DS\text{-}ON}$ of the SiC trench MOSFET as a function of the gate voltage before and after stress.

Fig. 20(a) shows the pre-stress $R_{DS\text{-}ON}$ as function of V_{GS}, whereas Fig. 20(b) shows the same characteristics post-PBTI stress. In both cases the resistance was measured using a current of 50 mA, thereby $R_{DS\text{-}ON}$ was characterized in the ohmic region.



(a) (b)

Fig. 20 SiC Trench MOSFET. $R_{DS\text{-}ON}$ as function of V_{GS} at 22 °C and 145 °C. (a) Before stress, (b) After PBTI stress

From the results in Fig. 20, PBTI causes an increase of the ZTC point from 14 V to around 15 V and a clear increase of $R_{DS\text{-}ON}$ of the device in NTC region. Moreover, the temperature sensitivity of the ON-state resistance has also increased in the NTC region.

The impact of PBTI on the accuracy of $R_{DS\text{-}ON}$ as temperature sensor is shown in Fig. 21, at both ambient temperature and 145 °C. This figure shows that the impact of BTI is minimized when R_{DSON} is measured at high V_{GS} due to the reduced contribution of R_{CH} to the total R_{DSON}. Increasing the contribution of R_{CH} to the total R_{DSON} (by reducing V_{GS}) makes the impact of BTI on $R_{DS\text{-}ON}$ more apparent, resulting in lower accuracy of $R_{DS\text{-}ON}$ as temperature indicator at low V_{GS} values.

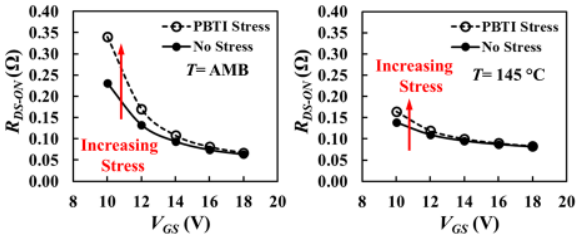


Fig. 21 SiC Trench MOSFET. Impact of PBTI on the ON-state resistance as function of the gate voltage. (a) Ambient temperature (b) 145 °C

For the recommended gate voltage of 18 V, at ambient temperature (22 °C) R_{DS-ON} increases +5.7%, whereas at 145 °C the increase is +2.7 %. When the device is driven with a gate voltage of 10 V, at ambient temperature the increase of R_{DS-ON} is +47%, compared with +18.1% at 145 °C Hence, the impact of PBTI is less apparent high temperature.

The results for the NBTI stress are shown in Fig. 22. Fig. 22(a) shows the pre-stress measured ON-state resistance as function of the gate voltage while Fig. 22(b) shows the post NBTI stress measured values.

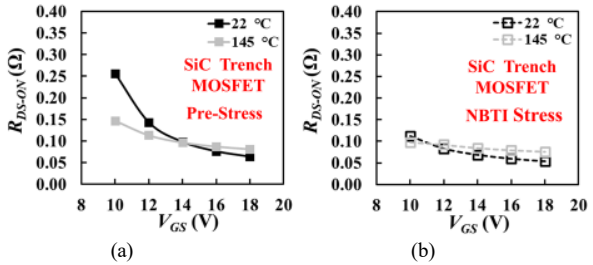


Fig. 22 SiC Trench MOSFET. R_{DS-ON} as function of V_{GS} at 22 °C and 145 °C. (a) Before stress, (b) After NBTI stress

For the NBTI stress, a clear shift of the ZTC can be observed, reducing from around 14 V before stress to approximately 11 V after stress. The impact of NBTI on the use of R_{DS-ON} as temperature indicator is shown in Fig. 23.

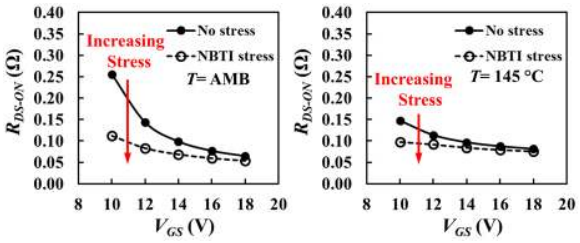


Fig. 23 SiC Trench MOSFET. Impact of NBTI on the ON-state resistance as function of the gate voltage. (a) Ambient temperature (b) 145 °C

Similar to the case of PBTI, the results for the NBTI stress in Fig. 23 show that the impact of the V_{TH} shift on the ON-state resistances is more apparent at low gate voltages, where the contribution of the R_{CH} is higher. For the recommended gate voltage of 18 V, at ambient temperature (22 °C) R_{DS-ON} decreases –16.5%, whereas at 145 °C the reduction is -6.4%. When the device is driven with a gate voltage of 10 V, the reduction of R_{DS-ON} at ambient temperature is -56.2%, whereas at 145 °C it is -33.5%. Hence, as in the case of PBTI, the impact of NBTI is less apparent at high temperature.

The higher variation of R_{DS-ON} after NBTI stress indicates that the negative gate stress had a higher impact on the gate oxide reliability for the evaluated SiC trench MOSFET.

An interesting option, from the point of view implementing of condition monitoring, can be measuring both the MOSFET resistance (affected by BTI) and the resistance of the wirebonds (not affected by BTI), as proposed in [65]. To implement this, it is only required having access to a to a Kelvin source terminal. Nevertheless, the challenge of accurately measuring the junction temperature of SiC MOSFETs using R_{DS-ON} remains.

B. BTI and switching rate of the drain current

The shift of the transfer characteristics due to BTI shown in section III indicates a clear impact on the dynamic/transient characteristics of SiC MOSFETs. Hence it is important to assess the impact of BTI on dynamic TSEPs like the switching rate of the drain current.

To that end, the turn-ON transients were measured before and after stress for the devices subjected to PBTI and NBTI stresses as shown in Fig. 15.

The switching transients before and after stress are shown in Fig. 24 and Fig. 25, for PBTI and NBTI respectively. The measurements were performed at ambient temperature, using a gate voltage V_{GS} of 13 V and a gate resistance R_G of 100 Ω.

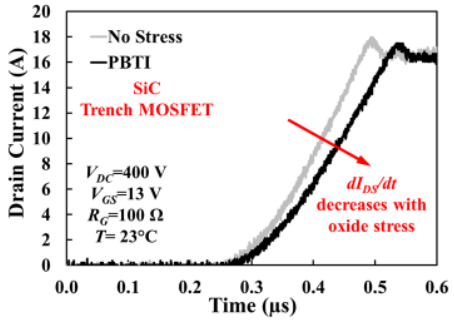


Fig.24 SiC Trench MOSFET – Impact of PBTI on the drain current turn-ON transient

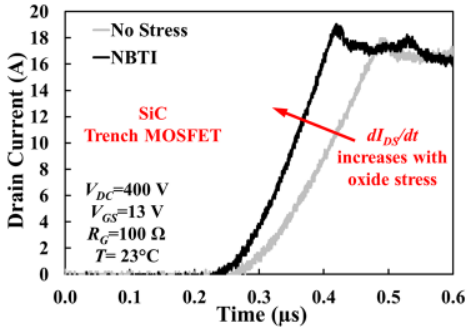


Fig. 25 SiC Trench MOSFET – Impact of NBTI on the drain current turn-ON transient

The results for the PBTI stress in Fig. 24 show a clear reduction of the switching rate, together with a shift rightwards of the drain current turn-ON transient. In the case of the NBTI stress, Fig. 25 shows a leftwards shift in the turn-ON transient together with a clear increase of the switching rate. Comparing Fig. 24 and Fig. 25, the impact of NBTI is more apparent. The differences on the measured dI_{DS}/dt are summarized in

Table IV. The results in Table IV clearly show that the impact of NBTI is higher.

TABLE IV SIC TRENCH – IMPACT OF BTI ON THE MEASURED *DRAIN CURRENT SWITCHING RATE* DURING TURN-ON
(V_{GS}=13 V, R_G=100 Ω, I_{DS}=16 A, T= 23 °C)

	Switching Rate Before Stress (A/µs)	Switching Rate After Stress (A/µs)	Difference (%)
PBTI	83.9	73.4	-12.6
NBTI	84.9	115.4	+35.9

The measurements show a considerable impact of BTI on the switching transients, especially in the case of NBTI. This is the result of highly accelerated stress tests, but it is worth to remark that BTI may have negative consequences in the use of the switching rate as junction temperature indicator. This is shown for the PBTI stress in Fig. 26, where the calibration of dI_{DS}/dt as function temperature indicator is shown. The reduction of dI_{DS}/dt caused by PBTI indicates that this relationship is no longer valid. The trend is observed for both V_{GS}=13 V and V_{GS}=17 V.

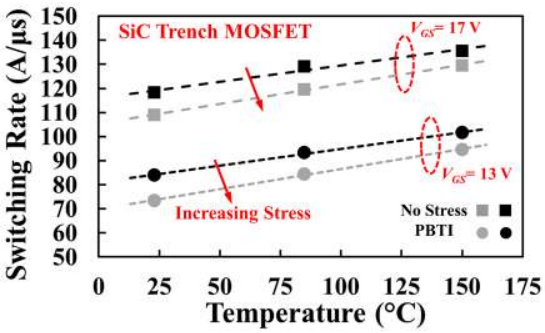


Fig. 26 Impact of PBTI on the calibration of the drain current switching rate as TSEP. SiC trench MOSFET. R_G=100 Ω, I_{DS}=16 A

Furthermore, an important observation is that due to this shift, the measured transient could be the same for two different temperatures. This is shown in Fig. 27, where it can be observed that the transient at 85°C is equal to the transient at 150°C for the device subjected to PBTI stress.

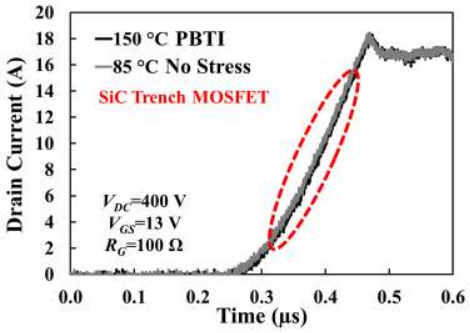


Fig. 27 SiC Trench MOSFET – Overlapping turn-ON current transients at different temperatures caused by PBTI

C. BTI and gate plateau

Similar to the switching rate of the drain current during turn-ON, the gate voltage plateau V_{GP} is also affected by BTI since it is a V_{TH} dependent TSEP. The gate voltage transients were measured at a temperature of 23 °C, for the devices subjected to PBTI and NBTI stresses and the results are shown in Fig. 28 and Fig. 29 respectively. Fig.28 shows the increase of V_{GP} after PBTI stress due to the higher V_{TH}, whereas the reduction of V_{GP} is clearly observed in Fig. 29 for the NBTI stress.

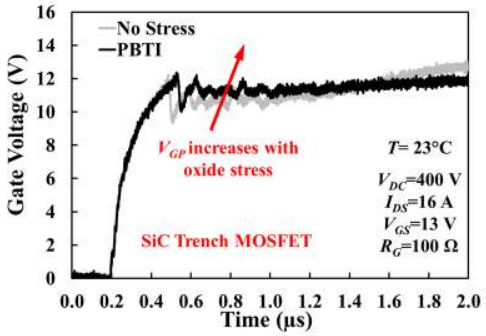


Fig. 28 SiC Trench MOSFET. Impact of PBTI on the gate voltage turn-ON transient.

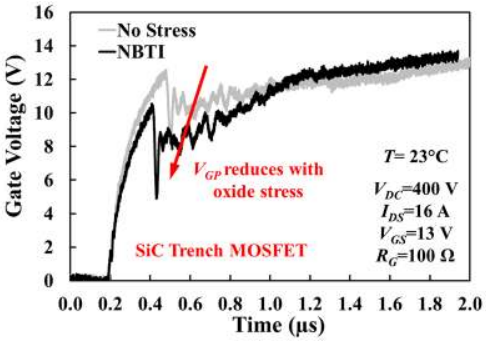


Fig. 29 SiC Trench MOSFET. Impact of NBTI on the gate voltage turn-ON transient.

As in the case of the drain current transients, it is also possible to obtain the same V_{GP} for different temperatures, as the results in Fig. 30 show. Hence, the occurrence of BTI can cause TSEPs to report a wrong temperature. These gate voltage transients correspond to the drain current transients in Fig. 27. The gate current plateau I_{GP} is also affected by BTI. In the case of positive gate stress, its value reduces as shown in Fig. 31.

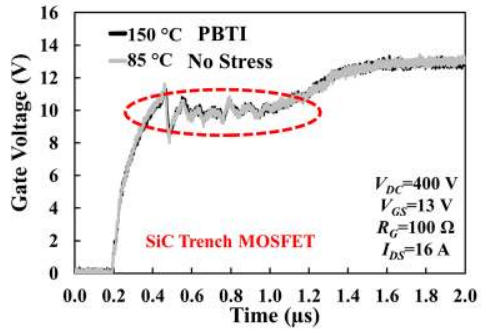


Fig. 30 SiC Trench MOSFET. Overlapping gate voltage turn-ON transients at different temperatures caused by PBTI

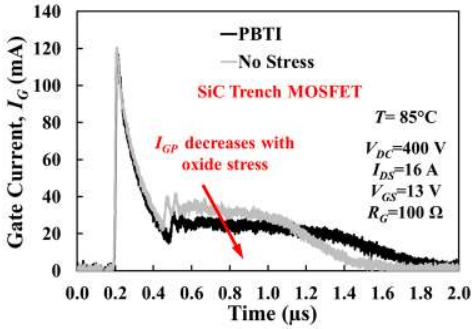


Fig. 31 SiC Trench MOSFET. Impact of PBTI on the gate current turn-ON transient

D. BTI and body diode voltage

To evaluate the impact of BTI on V_{SD} as a TSEP, the cumulative stresses in section III.B were used for both PBTI and NBTI evaluation. The forward voltage V_{SD} was characterized as TSEP after the 16-hour recovery period, at both V_{GS} = 0 V and V_{GS} = -4 V, using a sensing current I_{SD} of 50 mA. The results are shown in Fig. 32 for PBTI and Fig. 33 for NBTI.

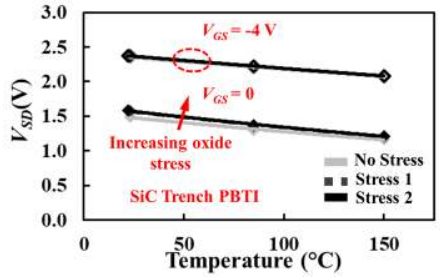


Fig. 32 SiC Trench MOSFET. Impact of PBTI on V_{SD}. (I_{SD}=50 mA)

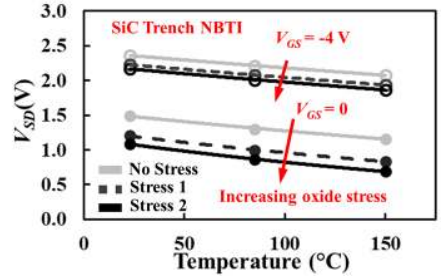


Fig. 33 SiC Trench MOSFET. Impact of NBTI on V_{SD} (I_{SD}=50 mA)

When V_{GS}=0 V, the results in Fig. 32 show a corresponding increase of V_{SD} due to the positive shift of V_{TH} caused by PBTI. However, as was already demonstrated in[39], when the device is biased with V_{GS}=-4 V, the impact of the positive shift is minimized and the accuracy of V_{SD} as TSEP is not affected. In the case of NBTI, as presented in Fig. 33, a higher negative voltage would be required to fully close the channel, as the rated gate voltage does not eliminate the impact of NBTI.

The impact of BTI on this TSEP is highly relevant to power cycling, where the calibration of V_{SD} as temperature indicator will be affected by the gate bias stress during the test. Power cycling methodologies where the device is biased with a negative voltage for junction temperature measurement have been proposed in the literature [39, 66]. An option to overcome the impact of BTI during power cycling can be the use of fiber optic sensors [67], but its application to condition monitoring will be limited.

An important observation from Fig. 32 and Fig. 33 is that for a known temperature *T,* the shift of V_{SD} can be used as a cursor of BTI degradation. A novel methodology using this relationship was evaluated in [41, 58, 68], where it was shown that it is able to capture the peak shift of V_{TH} and subsequent recovery after stress removal.

V. Conclusions

BTI is a reliability concern in SiC MOSFETs compared with Si MOS-gated devices. BTI in SiC MOSFETs is a challenging issue, as a fast and recoverable V_{TH} shift coexists with a more permanent V_{TH} drift. The threshold voltage V_{TH} drift resulting from gate bias stress will affect the electrical parameters of the SiC MOSFET.

Using accelerated stress tests, which capture the more permanent BTI-induced V_{TH} drift, the impact of PBTI and NBTI on the most common TSEPs for SIC MOSFETs has been evaluated. It is shown that the accuracy of the TSEPs is affected and the calibration relationships are no longer valid, as it is possible to measure the same value for two different temperatures. This will clearly affect the effectiveness of condition monitoring based on TSEPs for SiC MOSFETs.

The impact of BTI-induced shifts is more apparent when the devices are driven with low gate voltages, as the contribution of the channel resistance is higher. There are methods for eliminating or minimizing the impact of the BTI-induced V_{TH} shift, like the use of a negative gate voltage when using the body diode voltage or using high gate voltages when measuring the ON-state resistance. It is also shown that BTI-induced V_{TH} shifts affect the dynamic TSEPs, like the switching rate of the drain current, hence it will affect the switching losses and converter operation.

As BTI is a reliability challenge in SiC MOSFETs, monitoring the impact of the V_{TH} shift on the electrical parameters could be used for implementing BTI degradation monitoring techniques.

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