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# Bidirectional Three-Level Stacked Neutral-Point-Clamped Converter for Electric Vehicle Charging Stations

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**ABSTRACT** Electric vehicles (EVs) powered by batteries and other energy storage devices (ESDs), e.g., ultracapacitors, are expected to play an important role in the development of a more sustainable future. In this context, charging stations (CSs) are supposed to become the main sources of energy for charging the batteries, being strongly dependent on power electronic converters. This paper analyzes a bidirectional single-phase, three-level stacked neutral-point-clamped (3L-SNPC) converter for CS applications, which may behave as a rectifier or an inverter depending on the power flow direction. Besides, the derived analysis can be easily extended to the development of a three-phase version. Considering that the CS is capable of integrating the utility grid and renewable energy sources, it is possible to absorb or inject energy into the ac grid with high power factor and reduced harmonic content of the current. The main advantages of the bidirectional topology are the existence of a three-level voltage waveform across each leg and the neutral point, while filtering requirements are reduced when compared with typical two-level structures used in EV CSs; the voltage stresses on all semiconductors are equal to half of the total dc-link voltage; power factor is nearly unity in any operation mode; and the voltages across the dc-link capacitors are balanced. The thorough design of the power and control stages is presented, as well as experimental results from a laboratory prototype are discussed in detail.

**INDEX TERMS** Bidirectional converters, charging stations, electric vehicles, resonant controller.

## I. INTRODUCTION

Considering the imminent need to reduce the greenhouse gas emissions, as well the eventual depletion of fossil fuels, it is expected that internal combustion engine vehicles (ICEVs) will be replaced by electric vehicles (EVs) in a near future. The widespread use of EVs is also inserted in a more complex scenario involving microgrids and the smart grid concept, thus bringing major challenges to many research fields [1], [2].

Being an eco-friendly choice for transportation, plug-in electric vehicles (PEVs) equipped with batteries can be employed as both mobile energy storage devices (ESDs) and generators capable of supplying the energy demand of buildings if necessary [3]. In this context, fast and reliable charging is an essential feature that must be taken into account for the successful large-scale utilization of EVs [4]. This process also depends on distinct aspects, e.g., a cquisition cost and technological evolution of ESDs, charging algorithms, infrastructure in terms of existing charging stations (CSs), among others [5].

The practical implementation of CS topologies relies strongly on power electronic converters considering that battery chargers can be directly supplied by either a common dc link in dc microgrids or indirectly through ac-dc converters connected to the ac mains [6]. A thorough review on the state-of-the-art of CSs for EVs is presented in [7], being classified as off-board and on-board. It is clearly evidenced that the wide availability of CSs may lead to reduced energy storage requirements and costs associated with on-board chargers.

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Thus, the development of off-board topologies based on several energy sources is of great interest since batteries can be charged more quickly [8].

The work developed in [9] proposes a two-stage CS configuration composed of a three-phase interleaved boost rectifier and a bidirectional three-level asymmetrical dc-dc converter. In this case, the dimensions of the filter elements required by the front-end stage are reduced owing to the interleaved operation. In order to minimize the complexity of the control system implementation in the front-end stage, a single-stage architecture employing a 24-pulse thyristor rectifier is suggested in [10] as a possible solution to minimize the harmonic content of the ac input current, although a bulky low-frequency phase-shift transformer is required. An interleaved ac-dc boost converter cascaded with an isolated dc-dc full-bridge topology based on a high-frequency transformer is also described in [11] as a prominent solution to achieve reduced size, weight, and volume. It is worth mentioning that high efficiency results since the switching losses in the active switches of the dc-dc converter operate under zero voltage switching (ZVS) condition. The use of wide-bandgap semiconductors in EV CSs is also addressed in [12], in which gallium nitride (GaN) and silicon (Si) semiconductors are paralleled in order to achieve both superior switching performance and affordable cost associated with high-current capability in a hybrid approach.

The integration of renewable energy sources with CS topologies is also an interesting choice. For instance, photovoltaic (PV) modules can be used to provide part of the energy required to charge the EVs, thus contributing to the minimization of power system loading. The batteries can be charged by either the modules or the utility grid, or even by both sources simultaneously. Besides, part of the generated power can be injected into the grid depending on the load demand. For instance, the architecture introduced in [13] consists of a PV CS based on a three-phase hybrid converter, which integrates an isolated dc-dc converter and a three-phase inverter for grid connection with low component count, but only few results obtained from a small-scale prototype are presented and discussed. A Z-source inverter (ZSI) is also employed in [14] as a solution to reduce the number of conversion stages in a PV-based approach, being this topology able to provide voltage boost and dc-ac power conversion.

This work proposes an architecture of EV CS based on the integration of distinct energy sources, i.e., PV modules and the utility grid. A bidirectional power converter, which is capable of operating as a rectifier or an inverter, is also described in detail as part of this structure. It is also worth mentioning that SAE J1772 standard defines two charging levels: AC Level 1 (120 Vac with currents ranging from 12 A to 16 A) and AC Level 2 (208-240 Vac for currents up to 80 A). In this context, the analyzed converter is classified as AC Level 1.

In order to preserve power quality indices associated with the ac grid, proportional plus resonant (PR) control is employed so that it is possible to regulate the dc-link voltage and also emulate the behavior of a resistive load by imposing a nearly sinusoidal waveform to the current. A detailed design procedure is presented and an experimental prototype is developed to evaluate the converter performance and validate the theoretical assumptions.

## II. PROPOSED TOPOLOGY

Fig. 1 shows the block diagram of a possible CS architecture, which relies on the use of renewable energy sources, the conventional ac grid to charge the batteries, and a backup power source represented by a diesel generator. Dc-dc converters are associated with each set of PV modules to supply power to a common dc link, which is responsible for charging the EVs. Good design flexibility exists while aggregating distributed energy resources and ESDs to the system, which are essentially related to dc currents and voltages and do not demand synchronization with the ac grid or cause reactive power flow. Another potential application lies in the possibility to supply distinct loads in residential and industrial environments, e.g., lamps, electric ovens, and universal motors, which can be directly connected to the symmetrical dc link with rated voltages of 230 V or 460 V without using battery chargers. The number of conversion stages can be reduced as a consequence, thus implying higher efficiency. Otherwise individual battery chargers can be employed to provide distinct dc voltage levels to several loads.

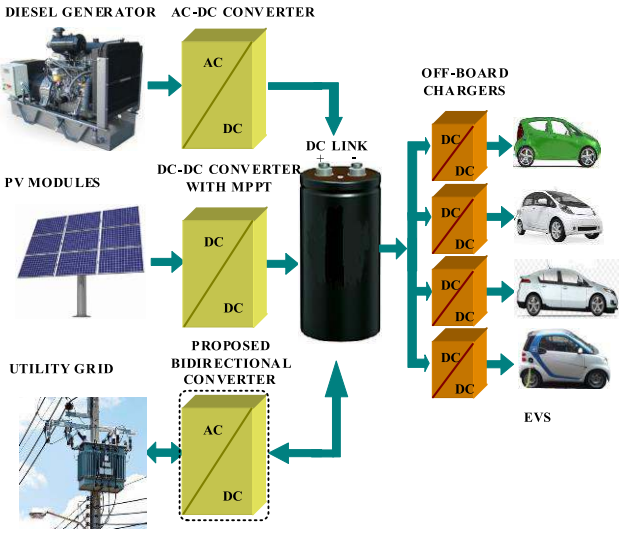


**FIGURE 1.** EV CS integrating the ac utility grid, PV modules, and a diesel generator.

It can be seen that a bidirectional power converter must also be used to control the grid current according to the energy demand. Many topologies can be chosen for this purpose, e.g., a bidirectional two-phase interleaved converter [15]. However, the voltage stress across the switches is equal to the dc-link voltage, what may lead to the use of metal oxide semiconductor field effect transistors (MOSFETs) with high voltage ratings and cost. In this case, conduction losses will

increase as a consequence since such semiconductors typically present high drain-source on-resistance.

Other suitable topologies for CS applications can also be found in the literature. A three-phase three-level neutral point clamped (3L-NPC) inverter is presented in [16], which employs 12 active switches. Besides, the capacitor voltage unbalance is of major concern and requires the use of complex and costly control schemes. According to [17], the three-level neutral stacked point clamped (3L-SNPC) and the three-level active stacked neutral point clamped (3L-ASNPC) inverters introduced in [18] and [19], respectively, present improved performance over traditional 3L-NPC ones due to the increase of the apparent switching frequency and better total loss balancing. The authors also propose a modified 3L-SNPC structure based on the use of insulated gate bipolar transistors (IGBTs) associated with only two MOSFETs operating at high frequency to minimize the switching losses. A similar configuration is also analyzed in [20]. Unfortunately, the component count in [17], [20] is still high when compared with the 3L-SNPC inverter.

It is also worth mentioning that the topologies presented in [17]–[20] do only perform ac-dc power conversion and bidirectional versions of the aforementioned converters were not presented so far. Considering good tradeoffs between the number of components and efficiency, the 3L-SNPC structure proposed in [18] was adopted to provide bidirectional power flow capability, resulting in the structure shown in Fig. 2. Besides, it allows charging independent batteries or even injecting power into the ac grid in EV CS applications, what was not investigated so far in the literature.

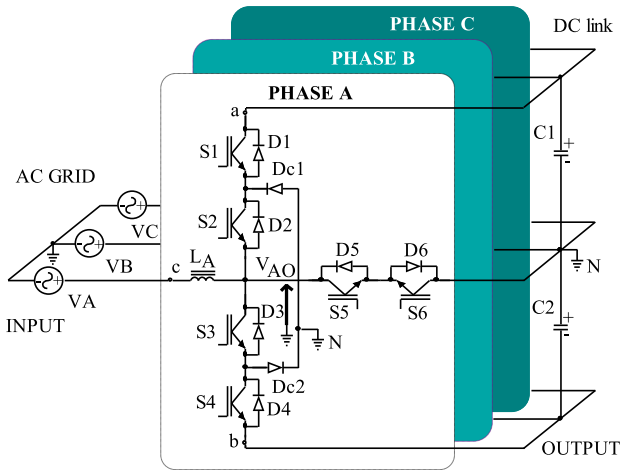


**FIGURE 2.** Three-phase bidirectional 3L-SNPC converter.

The proposed bidirectional converter is composed of clamping diodes $D_{c1}\ldots D_{c6}$; active switches $S_1\ldots S_{18}$ and their respective body diodes $D_1\ldots D_{18}$; storage inductors $L_A\ldots L_C$; dc-link capacitors $C_1$ and $C_2$; ac voltage sources $V_A$, $V_B$, $V_C$ corresponding to the phase voltages; and a dc voltage source that represents the dc link so that it is possible to evaluate the capability to provide bidirectional power flow. For this purpose, only phase A is analyzed as shown in Fig. 2, considering that the cell was formerly introduced in [18]. In this case, three control loops are required to shape the currents through the inductors, balance the voltages across the capacitors, and regulate the dc-link voltage, resulting in bidirectional power flow capability and high power factor.

The phase-disposition sinusoidal pulse width modulation (PD-SPWM) is typically employed in NPC-based topologies [21]. However, this technique must be modified in the case of the converter shown in Fig. 2 in order to provide bidirectional power flow. This is why $S_5$ and $S_6$ have been added to the converter, behaving as a bidirectional switch for this purpose. Since the dc link is composed of two capacitors $C_1$ and $C_2$, two carriers are necessary as represented in Fig. 3. In this case, only two switches are allowed to be on at the same time, while the remaining ones remain off according to Fig. 4. Switches $S_1$ and $S_2$ are only turned on when the modulator is greater than the carrier $V_{saw1}$ during the positive half cycle. Otherwise, switches $S_3$ and $S_4$ will be turned on when the modulator is less than the carrier $V_{saw2}$ during the negative half cycle. Analogously, switches $S_5$ and $S_6$ will be driven together when switches $S_1$ and $S_4$ are simultaneously off.

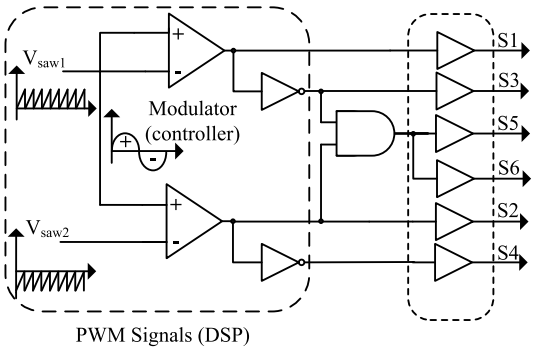


**FIGURE 3.** PD-SPWM and generation of the drive signals.

## III. DESIGN EXAMPLE

Table 1 summarizes the specifications used in the design of the power stage elements considering a single-phase version of the 3L-SNPC topology. It is also worth mentioning that the converter is designed to process one third of the total power required by its three-phase counterpart.

### A. PRELIMINARY CALCULATION

Parameter $\alpha$ corresponds to the ratio between the peak grid voltage and half of the total output voltage, i.e.:

$$\alpha = \frac{\sqrt{2}\cdot V_A}{(V_o/2)} = \frac{\sqrt{2}\cdot 127}{(460/2)} = 0.78 \tag{1}$$

The peak grid current $I_{Apk}$ is given by:

$$I_{Apk} = \frac{\sqrt{2}\cdot P_o}{\eta\cdot V_A} = \frac{\sqrt{2}\cdot 2000}{0.97\cdot 127} = 22.95\text{A} \tag{2}$$

The average output current $I_o$ is:

$$I_o = \frac{P_o}{V_o} = \frac{2000}{460} = 4.35\,\text{A} \tag{3}$$

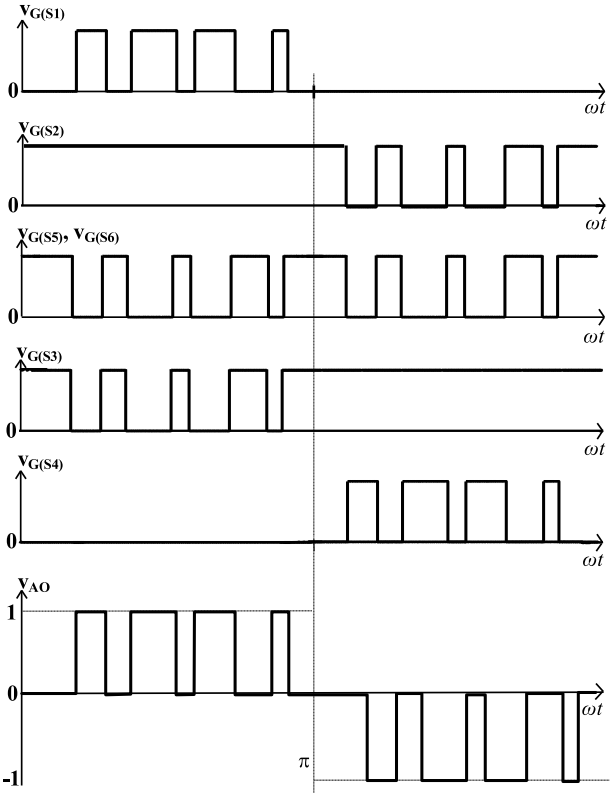


**FIGURE 4.** Drive signals of switches $S_1 \ldots S_6$.

**TABLE 1.** Design specifications for the single-phase version of the converter.

| Parameter | Specification |
|---|---|
| Rms grid voltage | $V_A$=127 V |
| Grid frequency | $f_g$=60 Hz |
| Total dc-link voltage | $V_o$=460 V |
| Output power | $P_o$=2 kW |
| Switching frequency | $f_s$=25 kHz |
| Input voltage variation | ±20% |
| Theoretical efficiency | $\eta$=97% |

### B. BOOST INDUCTOR

The boost inductance is given by:

$$L_A = \frac{(V_o/2)}{4 \cdot f_s \cdot \Delta I_{\max}} = \frac{(460/2)}{4 \cdot 25 \cdot 10^3 \cdot 4.59} = 501\mu\text{H} \quad (4)$$

where $\Delta I_{max}$ is the maximum peak-to-peak ripple of the inductor current.

In this case, $L_A = 500\ \mu$H is adopted.

### C. STRESSES ON THE ACTIVE SWITCHES

The maximum voltages across all switches correspond to half of the total dc-link voltage, i.e.:

$$V_{S1\ldots S6(\max)} = \frac{V_o}{2} = \frac{460}{2} = 230\text{V} \quad (5)$$

When the converter operates in rectifier mode, the currents through switches $S_1$ and $S_4$ are null. On the other hand, the average and rms currents through $S_2$, $S_3$, $S_5$, and $S_6$ are given by (6) and (7), respectively.

$$I_{S2,S3,S5,S6(avg)} = I_{Apk} \cdot \frac{1}{2} \cdot \left(\frac{1}{\pi} - \frac{\alpha}{4}\right) = 22.95 \cdot \frac{1}{2} \cdot \left(\frac{1}{\pi} - \frac{0.78}{4}\right) = 1.42\text{A} \quad (6)$$

$$I_{S2,S3,S5,S6(rms)} = I_{Apk} \cdot \frac{1}{2}\sqrt{\left(\frac{1}{4} - \frac{2 \cdot \alpha}{3 \cdot \pi}\right)} = 22.95 \cdot \frac{1}{2}\sqrt{\left(\frac{1}{4} - \frac{2 \cdot 0.78}{3.\pi}\right)} = 3.34\text{A} \quad (7)$$

However, when the converter operates in inverter mode, the average and rms currents through $S_1$ and $S_4$ are given by:

$$I_{S1,S4(avg)} = I_{Apk} \cdot \frac{\alpha}{4} = 22.95 \cdot \frac{0.78}{4} = 4.47\text{A} \quad (8)$$

$$I_{S1,S4(rms)} = I_{Apk} \cdot \sqrt{\frac{2 \cdot \alpha}{3 \cdot \pi}} = I_{Apk} \cdot \sqrt{\frac{2 \cdot \alpha}{3 \cdot \pi}} = 9.33\text{A} \quad (9)$$

### D. STRESSES ON THE ANTIPARALLEL DIODES OF THE ACTIVE SWITCHES

The reverse voltage across all diodes is:

$$V_{A\_D1\ldots D6(PIV)} = \frac{V_o}{2} = \frac{460}{2} = 230\ \text{V} \quad (10)$$

The average and rms currents through $D_5$, $D_6$, $D_{c1}$, and $D_{c2}$ are given by (11) and (12), respectively.

$$I_{D5,D6,Dc1,Dc2(avg)} = I_{Apk} \cdot \frac{1}{2} \cdot \left(\frac{1}{\pi} - \frac{\alpha}{4}\right) = 22.95 \cdot \frac{1}{2} \cdot \left(\frac{1}{\pi} - \frac{0.78}{4}\right) = 1.42\text{A} \quad (11)$$

$$I_{D5,D6,Dc1,Dc2(rms)} = I_{Apk} \cdot \frac{1}{2}\sqrt{\left(\frac{1}{4} - \frac{2 \cdot \alpha}{3 \cdot \pi}\right)} = 22.95 \cdot \frac{1}{2}\sqrt{\left(\frac{1}{4} - \frac{2 \cdot 0.78}{3.\pi}\right)} = 3.34\text{A} \quad (12)$$

The average, rms, and peak currents through the antiparallel diodes $D_1$, $D_2$, $D_3$ and $D_4$ are obtained from (13), (14), and (15), respectively.

$$I_{A\_D1\ldots D4(avg)} = \frac{I_{Apk} \cdot \alpha}{4} = 4.47\ \text{A} \quad (13)$$

$$I_{A\_D1\ldots D4(rms)} = I_{Apk} \cdot \sqrt{\frac{2 \cdot \alpha}{3 \cdot \pi}} = 9.33\ \text{A} \quad (14)$$

$$I_{A\_D1\ldots D4(pk)} = I_{Apk} \cdot = 22.95\ \text{A} \quad (15)$$

### E. OUTPUT FILTER CAPACITORS

Capacitors $C_1$ and $C_2$ are responsible for keeping the dc-link voltage constant, being determined as:

$$C_1 = C_2 \geq \frac{P_o \cdot \Delta t}{2 \cdot (V_o^2 - V_{o(\min)}^2)} = \frac{2000 \cdot 8.33 \cdot 10^{-3}}{2 \cdot (230^2 - 225.4^2)} = 3.98\ \text{mF} \quad (16)$$

where $\Delta t$ is the hold-up time and $V_{o(\min)}$ is the minimum value assumed by the dc-link voltage.

The output filter capacitors are assumed to be $C_1 = C_2 = 3.92$ mF, represented by seven 560-$\mu$F capacitors connected in parallel. The equivalent series resistance (ESR) of the association is $R_{se} = 22.85$ m$\Omega$.

## IV. CONTROL SYSTEM

In order to achieve power factor correction (PFC), there are some consolidated techniques available in the literature, e.g., one cycle control [22] and average current mode control [23]. The PR control has the ability to track a sinusoidal reference, resulting in null steady-state error, while Fig. 5 shows the block diagram that represents the implementation of such approach. It can be seen that three loops are required to keep high power factor, minimized harmonic content of the grid current, regulated dc-link voltage, and balanced voltages across the output filter capacitors.

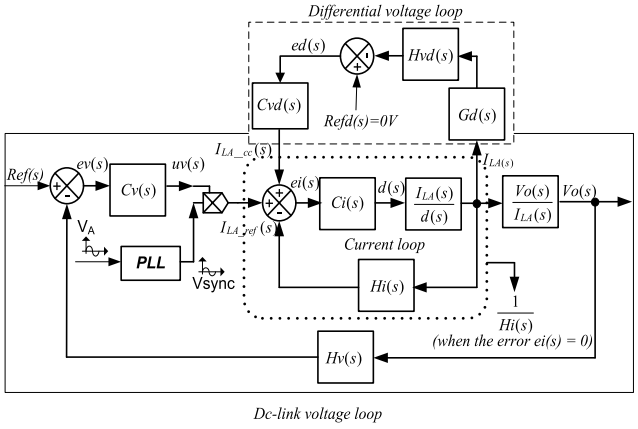


**FIGURE 5.** Block diagram of the control system.

The internal current loop is composed of PR controller $C_i(s)$, which is designed from the classical proportional-integral (PI) controller and modifies the control signal $d(s)$ properly so that the input current is nearly sinusoidal and remains in phase with the grid voltage. On the other hand, the external voltage loop employs controller $C_v(s)$, which provides the current loop with a sinusoidal reference signal to be imposed to the current so that the dc-link voltage remains regulated. Finally, the differential voltage loop is represented by controller $C_{vd}(s)$, being responsible for keeping the voltages across capacitors $C_1$ and $C_2$ balanced as desired. In fact, the controller adds a small dc component to the reference signal of the current loop for this purpose. The detailed design procedure for such controllers is presented in the forthcoming sections employing the K factor as described in [24].

Table 2 defines the main parameters for the design of the current loop. Besides, according to [25], the equivalent circuit shown in Fig. 6 can be employed to simplify the small-signal modeling of the 3L-SNPC converter. Subscript "eq" is adopted for the representation of the converter elements in terms of equivalent components in the

**TABLE 2.** Parameters employed in the current loop design.

| Parameter | Specification |
|---|---|
| Peak-to-peak voltage associated with the sawtooth carriers | $V_d$=5 V |
| Pulse width modulator gain | $F_m(s)$=0.2 |
| Hall-effect current sensor gain | $K_{hall}$ =0.001 |
| Shunt resistance connected to the current sensor output | $R_{shuntx}$=100 Ω |
| Inductor current gain | $H_i(s)$=0.1 V/A |

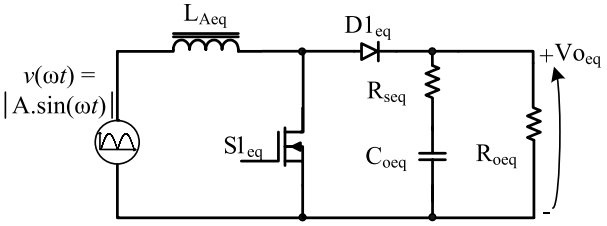


**FIGURE 6.** Equivalent circuit of the proposed converter used in the control system design.

circuit, i.e., inductor $L_{A(eq)}$; switch $S_{1(eq)}$; diode $D_{1(eq)}$; output filter capacitor $C_{o(eq)}$ and its respective ESR $R_{se(eq)}$; and load resistor $R_{o(eq)}$. From the design specifications of the original converter, the equivalent parameters in Table 3 can be obtained.

**TABLE 3.** Parameter specifications of the equivalent converter.

| Parameter | Specification |
|---|---|
| Rated rms input voltage | $V_A$=127 V |
| Range of the rms phase voltage | $V_{A(\min)}$=102 V – $V_{A(\max)}$=152 V |
| Ratio between the output voltages of the proposed 3L-SNPC and the equivalent converter | $r_v=V_o/V_{o(eq)}$=2 |
| Total output voltage | $V_{o(eq)}=V_o/r_v$=230 V |
| Input filter inductor | $L_{A(eq)}=L_A$=500 µH |
| Switching frequency | $f_{s(eq)}=f_s$=25 kHz |
| Switching period | $T_{s(eq)}=T_s$=40 µs |
| Output power per phase | $P_o$=2 kW |
| Average duty cycle | $D_{(eq)}=D$=0.5 |
| Inductor series resistance | $R_w$=100 mΩ |
| Output filter capacitance | $C_{o(eq)}=C_o\cdot r_v^2$=15.68 mF |
| ESR of the output filter capacitor | $R_{se(eq)}=R_{se}/r_v^2$=5.71 mΩ |
| Load resistance | $R_{o(eq)}=R_o/r_v^2$=26.45 Ω |

### A. INTERNAL CURRENT LOOP

First, it is necessary to obtain the control-to-inductor current transfer function, which is given by (17) [26].

$$G_i(s) = \frac{I_{LA}(s)}{d(s)} = \frac{(V_o/2)}{s \cdot L_A + R_w} \tag{17}$$

where $R_w$ is the inductor series resistance.

In digital control systems, the time delay associated with the performed calculations $T_d$ must be considered. This effect can be represented in terms of a simple first-order Padé approximation in the form:

$$G_d(s) = \frac{1}{T_d \cdot s + 1} \tag{18}$$

The following parameters are also considered in the design:

$$F_m(s) = V_d^{-1} \tag{19}$$

$$H_i(s) = K_{hall} \cdot R_{shunt} \tag{20}$$

The open-loop transfer function for the current loop can then be obtained as:

$$TFOL_{iu}(s) = F_m(s) \cdot G_i(s) \cdot G_d(s) \cdot H_i(s) \tag{21}$$

The PR controller is represented by the following expression:

$$C_i(s) = k_p + \frac{2 \cdot k_i \cdot \omega_c \cdot s}{s^2 + 2 \cdot \omega_c \cdot s + \omega_0^2} \tag{22}$$

where $k_p$ and $k_i$ are the proportional and integral gains, respectively; and $\omega_c$ and $\omega_0$ are the crossover angular frequency and resonance angular frequency, respectively.

Parameter $k_p$ can be tuned similarly to a conventional PI controller, thus defining the dynamic behavior of the system, bandwidth, phase margin, and gain margin [27]. On the other hand, parameter $k_i$ has little influence on the loop bandwidth and represents the controller gain. According to [27], it is possible to determine $k_p$ and $k_i$ from a conventional PI controller. Considering that it has one pole at the origin of the complex plane and adopting the pole and zero cancellation approach, the open-loop transfer function of the compensated loop can be simply given by:

$$TFOL_{ic}(s) = \frac{K_{PI} \cdot B}{s \cdot (s + a)} \tag{23}$$

where $K_{PI}$ is the gain for the PI controller to be determined. Besides, parameters $B$ and $a$ are given by:

$$B = \frac{F_m \cdot H_i \cdot V_o}{T_d} \tag{24}$$

$$a = \frac{1}{T_d} \tag{25}$$

In order to obtain fast transient response without overshoot, the PI controller must be tuned so that the closed-loop poles are in the real axis and placed exactly in the middle of the root locus as shown in Fig. 7. It can then be stated that the closed-loop poles of the current loop will always be in the left half-plane, while stability is achieved for any value of $K_{PI}$ in (23).

The value of $K_{PI}$ that leads the poles to the same position defined as $a/2$ is [28]:

$$K_{PI} = \frac{a^2}{4 \cdot B} = \frac{\left(1.667 \cdot 10^4\right)^2}{4 \cdot 76666.7} = 905.73 \tag{26}$$

According to the adopted procedure, the transfer function representing the PI controller can be written in the form:

$$C_{PI}(s) = K_{PI} \cdot \left(\frac{s \cdot L_A + R_w}{s}\right) \tag{27}$$

Thus, it is possible to calculate $k_p$ and $k_i$ as follows:

$$k_p = K_{PI} \cdot L_A = 0.45 \tag{28}$$

$$k_i = K_{PI} \cdot R_w = 90.57 \tag{29}$$

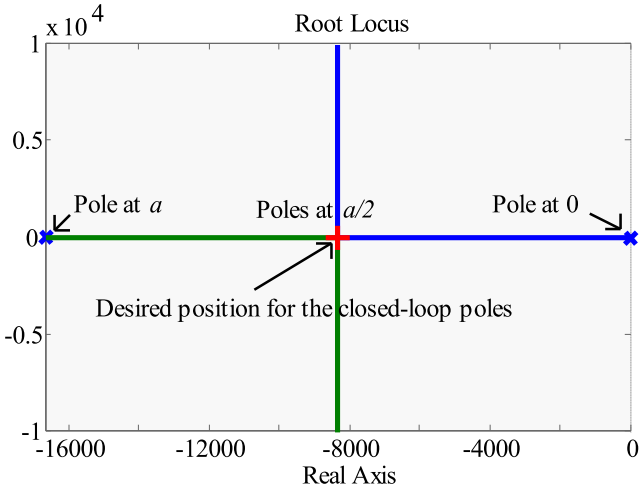


**FIGURE 7.** Root locus of the current loop associated with the PI controller.

Considering $\omega_c = 0.1$ Hz and $\omega_0 = 2 \cdot \pi \cdot f_g = 377$ rad/s, the resulting Bode diagrams of the PR controller and the closed-loop transfer function of the compensated system are represented in Fig. 8.

Fig. 8 (a) shows that the controller gain is high at $f_g = 60$ Hz, while the phase angle is null. In other words, the controller is able to ensure that the current remains nearly in phase with the grid current, as high power factor is obtained as a consequence. Besides, Fig. 8 (b) denotes that the current through $L_A$ is in phase with the sinusoidal reference signal considering that the phase angle is null in this case. Besides, the gain remains constant at 20 dB for frequencies up to 1 kHz, thus providing fast response. The closed-loop response of the current loop is fast enough so that the current follows a sinusoidal reference at 60 Hz. Thus, it can be simplified in the form of $1/H_i(s)$, which is a constant value as represented in Fig. 8 (b).

The close-loop poles of the whole system were also determined for stability analysis purposes. Fig. 9 shows the three existing poles when $R_{o(eq)}$ is varied. It can be stated that the system is stable when the load power varies because the poles remain in the left-half plane.

### B. EXTERNAL VOLTAGE LOOP

Since the current loop is inherently faster than the voltage one, its respective transfer function can be simplified in the form [29]:

$$A(s) = (H_i(s))^{-1} = 10 \tag{30}$$

The gain of the Hall-effect voltage sensor manufactured by LEM is:

$$H_v(s) = 5/400 = 12.50 \cdot 10^{-3} \tag{31}$$

Finally, the open-loop transfer function of the voltage loop is given by:

$$TFOL_{vu}(s) = A(s) \cdot Z(s) \cdot H_v(s) \tag{32}$$

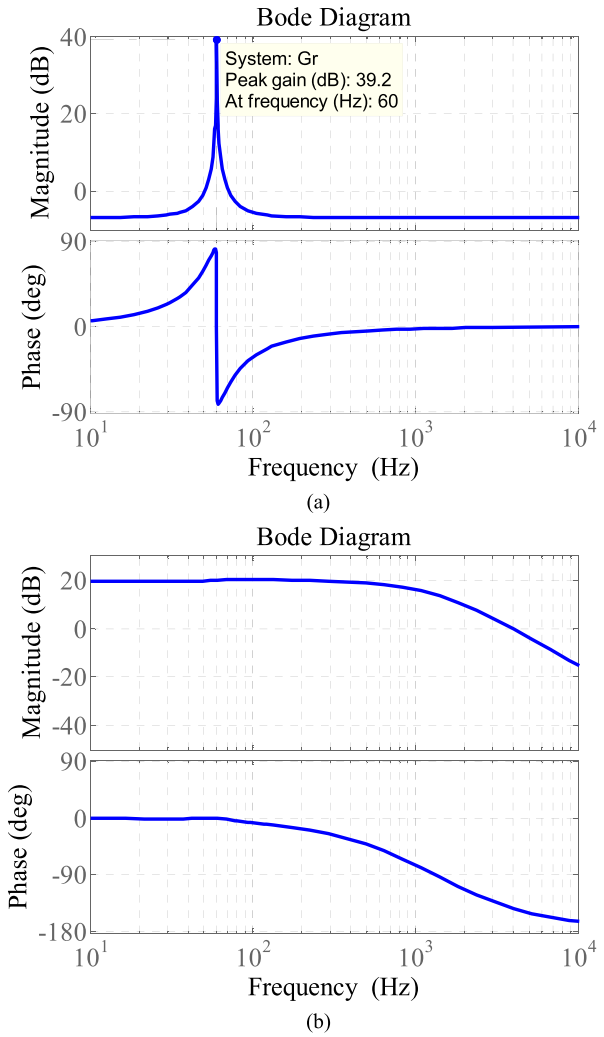


**FIGURE 8.** (a) Bode plot of the PR controller, (b) Bode plot of the closed-loop transfer function for the current loop.

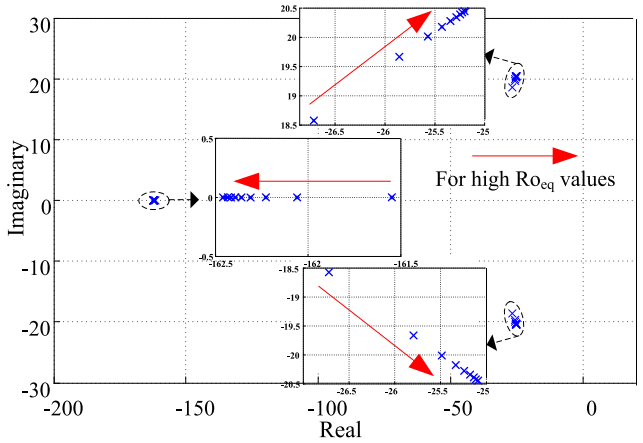


**FIGURE 9.** Closed-loop poles for 10 values of $R_{o(eq)}$.

where $Z(s)$ is:

$$Z(s) = \left[(1-D)\cdot\frac{R_{oeq}\cdot R_{seq}}{R_{oeq}+R_{seq}}\right]\cdot\left(\frac{s+\frac{1}{R_{seq}\cdot C_{oeq}}}{s+\frac{1}{C_{oeq}\cdot(R_{oeq}+R_{seq})}}\right) \quad (33)$$

The crossover frequency has been chosen as $f_{cv} = f_g/6 = 10$ Hz, while the phase margin is 60°. The resulting transfer function of $C_v(s)$ is:

$$C_v(s) = \frac{10.86\cdot 2\cdot\pi\cdot 2.97.}{s\cdot\left(\frac{s}{2\cdot\pi\cdot 33.70}+1\right)}\cdot\left(\frac{s}{2\cdot\pi\cdot 2.97}+1\right) \quad (34)$$

### C. DIFFERENTIAL VOLTAGE LOOP

Controlling the differential voltage is performed indirectly through the current loop, as a dc component can be added to the reference signal of the loop responsible for controlling $I_{LA}(s)$. Consequently, it is possible to maintain equal voltages across the dc-link capacitors even when unbalanced loads are supplied by the converter. Considering the ESRs of the capacitors, the transfer function of the inductor current to the differential voltage can be obtained as [24]:

$$Z_d(s) = \frac{V_{dif}(s)}{I_{LA}(s)} = \frac{0.5\cdot R_o\cdot(R_{se}\cdot C_o\cdot s+1)}{0.5\cdot(R_o+R_{se})\cdot C_o\cdot s+1} \quad (35)$$

The open-loop transfer function is given by:

$$TFOL_{vdsc}(s) = A(s)\cdot Z_d(s)\cdot H_v(s) \quad (36)$$

The bandwidth of the differential voltage loop must be significantly narrower than the capacitor voltage ripple frequency so that the reference signal for the current loop is not distorted. Therefore, the crossover frequency is chosen as $f_{cvd} = 5$ Hz and the phase margin is 60°, as the transfer function for controller $C_{vd}(s)$ becomes:

$$C_{vd}(s) = \frac{0.69\cdot 2\cdot\pi\cdot 1.85}{s\cdot\left(\frac{s}{2\cdot\pi\cdot 13.50}+1\right)}\cdot\left(\frac{s}{2\cdot\pi\cdot 1.85}+1\right) \quad (37)$$

The designed analog controllers can be discretized using the bilinear transform considering that the sampling frequency is equal to the switching frequency. The resulting controllers are then embedded in a digital signal processor (DSP) so that operation with high power factor and low harmonic distortion is ensured. Fig. 10 represents the main functions of the DSP as associated with the digital control system.

## V. EXPERIMENTAL RESULTS

In order to validate the theoretical assumptions, a 2-kW experimental prototype was implemented and thoroughly evaluated considering the specifications given in Table 3 and the components listed in Table 4. Fig. 11 shows the experimental setup used in the tests, where the complex programmable logic device (CPLD) and DSP, drivers, power stage, laptop, among other components are evidenced. A three-phase transformer is used to provide isolation and an rms voltage of 127 V to the single-phase version of the topology assessed in the laboratory.

Protection devices, electromagnetic interference (EMI) filters, circuit breakers, and varistors are also included in the prototype. All voltage and current signals measured by the sensors are properly conditioned and filtered to mitigate noise and avoid anti-aliasing in the DSP. Besides, shielded cables are used to prevent interference in the control circuit. In order to implement the digital control system, Experimenter Kit

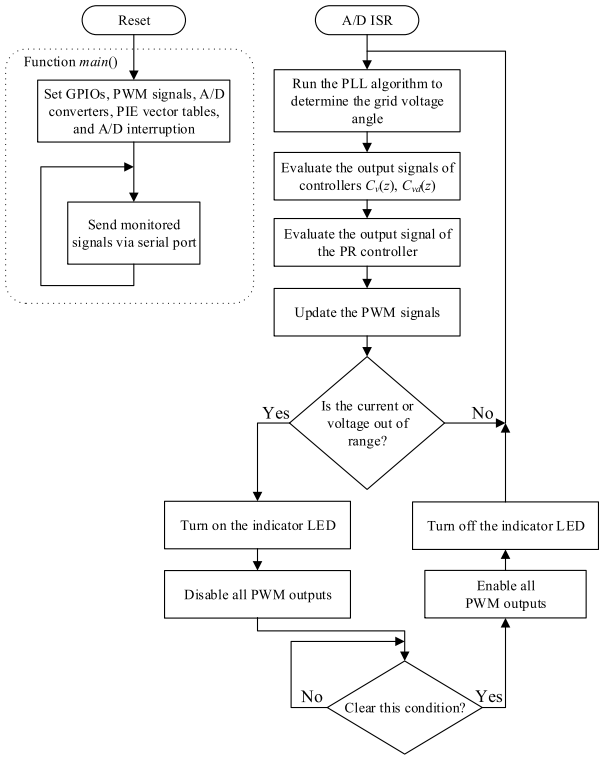


**FIGURE 10.** Flowchart of the digital control system.

**TABLE 4.** Components used in the experimental prototype.

| Component | Specification |
|---|---|
| Drivers of switches $S_1$…$S_2$ and $S_3$…$S_4$ | 02×2SC0108T2G0 |
| Drivers of switches $S_5$-$S_6$ | 01×2SC0106T2A1 |
| Switches $S_1$…$S_6$ | IGBTs STGW80V60DF |
| Diodes $D_{c1}$, $D_{c2}$ | 02×30EPH06 |
| Sensor for measuring the grid voltage and the dc-link voltages | 03×Hall-effect sensors LV25-P |
| Sensor for measuring the grid current | 01×Hall-effect sensors LA55-P |

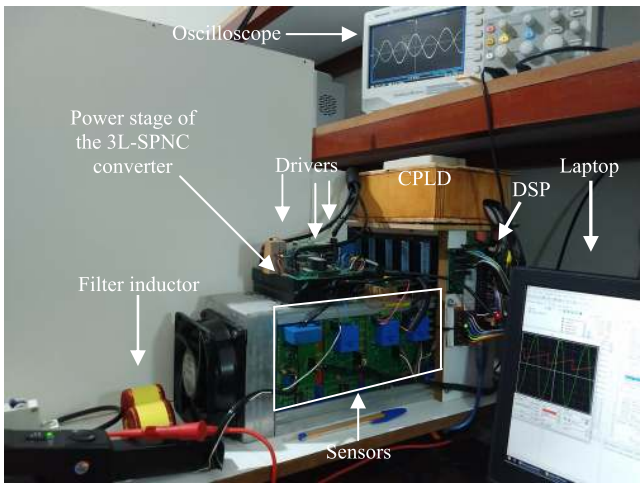


**FIGURE 11.** Experimental setup.

associated with DSP TMS320F28335 was employed. CPLD EPM240T100C5N was adopted to generate the drive signals of switches $S_5$ and $S_6$, as well as monitor the behavior of the PWM signals and eventual failure warnings associated with the drivers.

The experimental prototype was evaluated considering the operation in both rectifier and inverter modes. A detailed discussion on the results is provided as follows.

### A. OPERATION IN RECTIFIER MODE

Fig. 12 shows the waveform corresponding to voltage $v_{AO}$ as represented in Fig. 2, which has three levels as expected and is in accordance with the adopted modulation strategy.

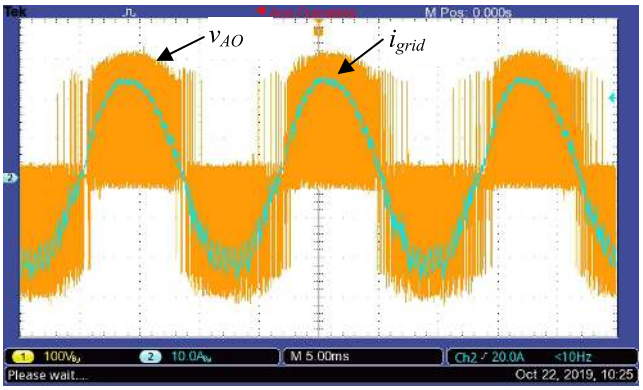


**FIGURE 12.** Three-level voltage $v_{AO}$ and phase current at the rated power condition in rectifier mode.

Fig. 13 presents the phase voltage and the current drawn from the grid. It can be stated that the current is sinusoidal and remains in phase with the voltage, resulting in a power factor of 0.9951 and total harmonic distortion (THD) of 2.03% considering the first 40 harmonic components.

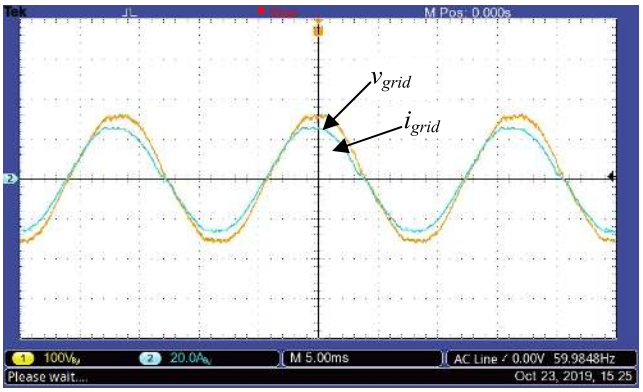


**FIGURE 13.** Grid voltage and grid current at the rated power condition in rectifier mode.

Fig. 14 shows the dynamic behavior of the converter when load steps from 50% to 100% of the rated power and vice-versa occur. In either case, the dc-link voltage remains regulated at about 460 V in steady-state condition, while the grid current is nearly sinusoidal.

A detailed view of the output voltage and grid current during the positive and negative load steps is also provided in Fig. 15.

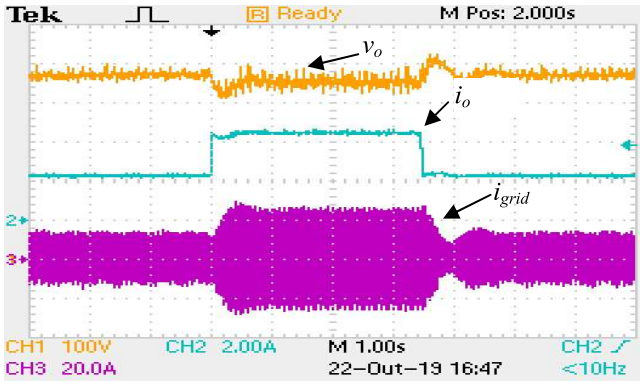


**FIGURE 14.** Behavior of the dc-link voltage and grid current during positive and negative load steps in rectifier mode.

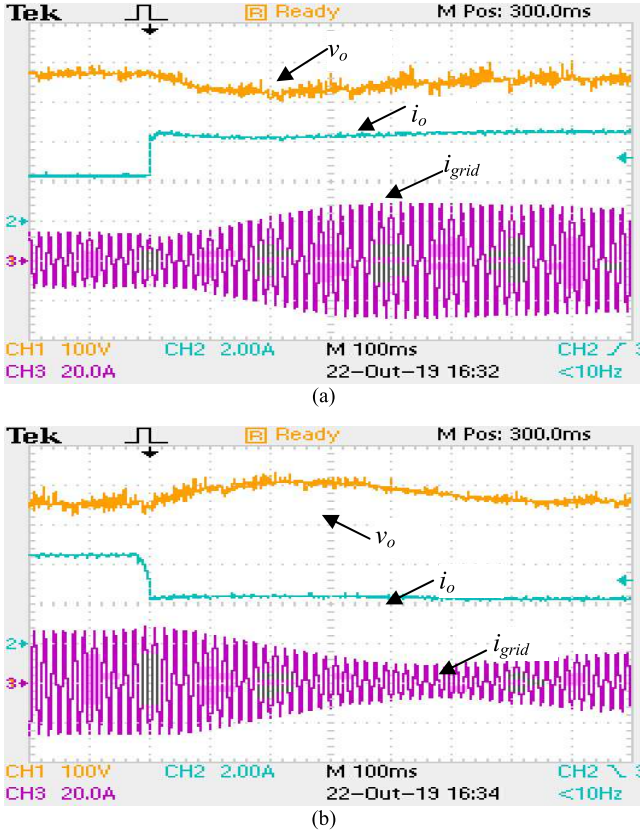


**FIGURE 15.** Detailed view of the dc-link voltage and grid current in rectifier mode: (a) load step from 50% to 100% of the rated power, (b) load step from 100% to 50% of the rated power.

Fig. 16 shows the behavior of the current THD, power factor, and efficiency as a function of the output power, which are equal to 2.03%, 0.9951, and about 92.5% at the rated load condition, respectively. It can be stated that the harmonic distortion of the input current is low over the entire power range, while both the power factor and efficiency are high.

The harmonic content of the grid current at the rated load condition up to the 40$^{th}$ order is shown in Fig. 17. It is observed that 3$^{rd}$ harmonic is the most dominant component

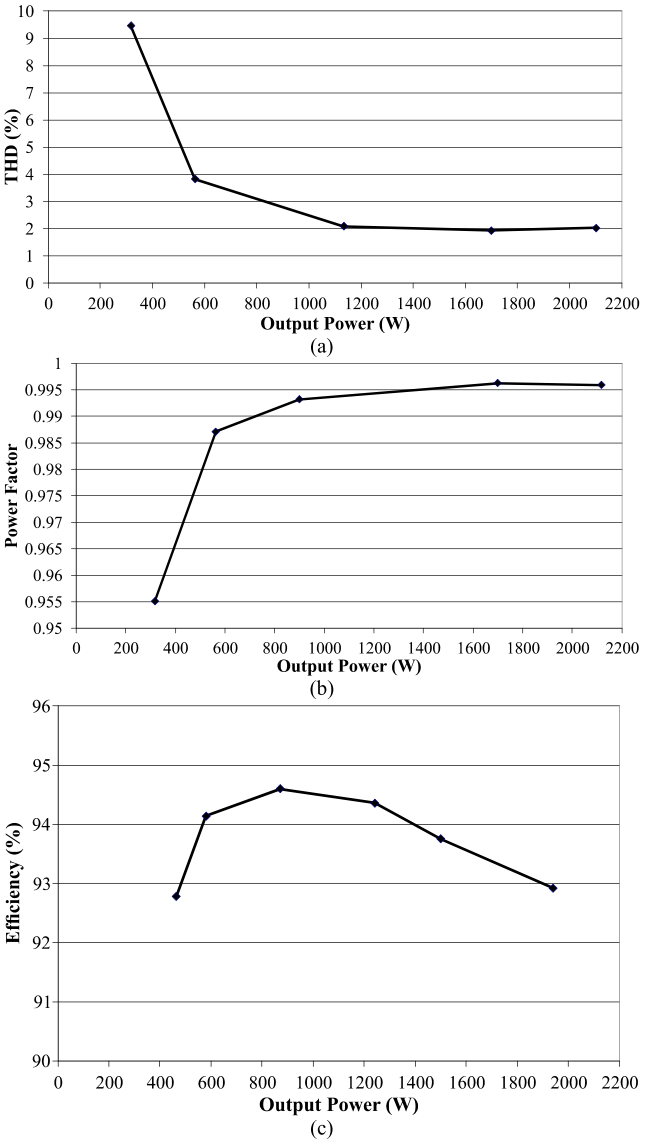


**FIGURE 16.** Converter performance over a wide load range in rectifier mode: (a) THD, (b) power factor, (c) efficiency.

and corresponds to 1.08% of the fundamental, i.e., 0.245 A, thus denoting that the adopted control strategy is capable of providing sinusoidal currents. Besides, all limits established by standard IEC 61000-3-2 for class A equipment are strictly respected.

The losses in the power stage components of the single-phase topology considering the operation at the rated power are shown in Fig. 18. The overall losses are equal to 85.24 W and were determined using the methodology described in [30]–[32]. The major portions are associated with the conduction losses in the body diodes and the inductor losses.

### B. OPERATION IN INVERTER MODE

Fig. 19 presents the waveform of voltage $v_{AO}$, which also has three levels as a consequence of the adopted modulation

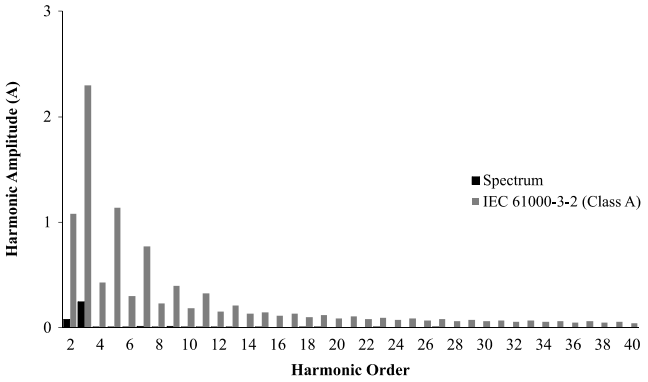


**FIGURE 17.** Harmonic spectrum of the grid current at the rated load condition in rectifier mode.

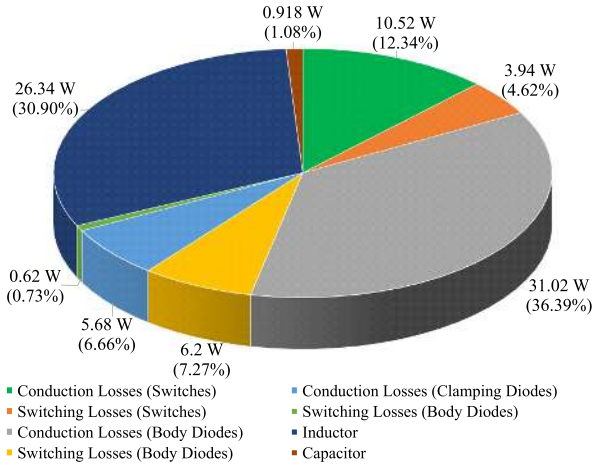


**FIGURE 18.** Loss breakdown at the rated load condition in rectifier mode.

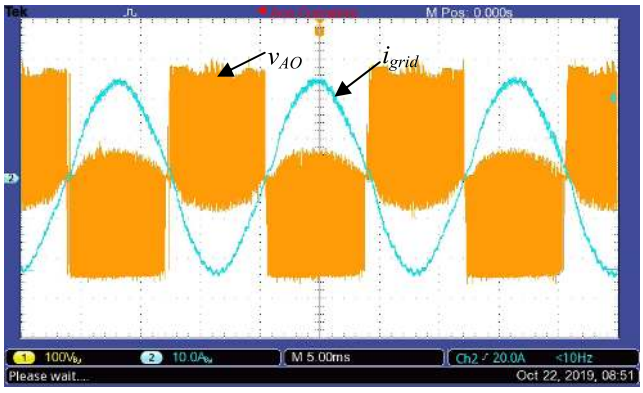


**FIGURE 19.** Three-level voltage $v_{AO}$ and phase current at the rated power condition in inverter mode.

strategy, thus allowing minimizing the dimensions of inductor $L_A$. In inverter mode, the current is phase-shifted by 180° with respect to the grid voltage as shown in Fig. 20. The current shape is also sinusoidal, which is due to the use of a PR controller.

Fig. 21 represents the THD of the current injected into the grid, power factor, and efficiency as a function of the output power, which are lower than 3%, nearly unity, and higher

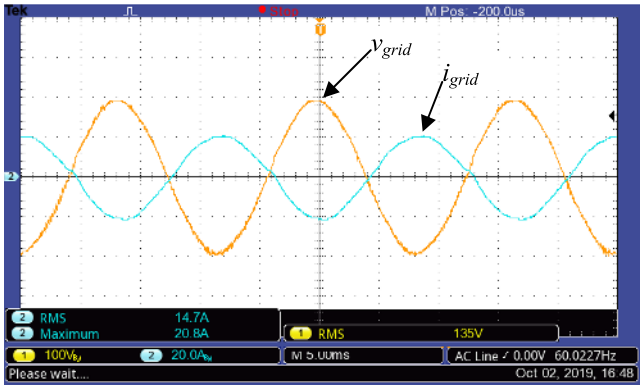


**FIGURE 20.** Grid voltage and grid current at the rated power condition in inverter mode.

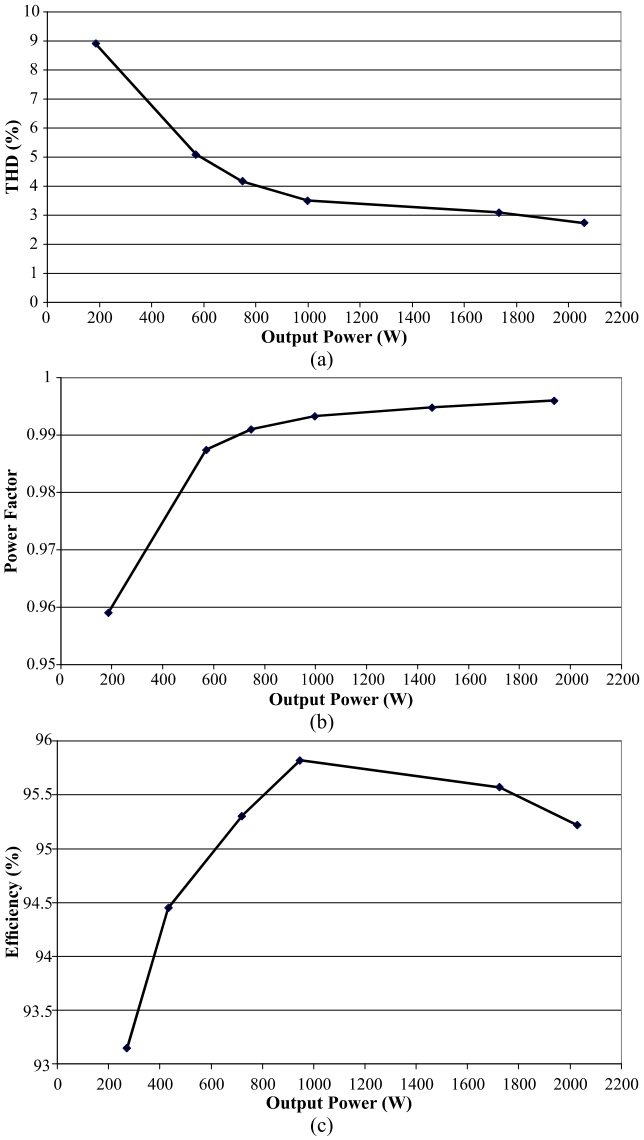


**FIGURE 21.** Converter performance over a wide load range in inverter mode: (a) THD, (b) power factor, (c) efficiency.

than 95% at the rated load condition, respectively. Besides, the converter is capable of ensuring a sinusoidal shape to the current over a wide load range as expected.

Fig. 22 corresponds to the harmonic content of the grid current at the rated load condition. Once again, the most dominant component is the 3rd harmonic, being equal to 1.97% of the fundamental, i.e., 0.37 A. However, all the remaining components remain lower than 0.5%, thus demonstrating that the grid current is nearly sinusoidal. The converter operation is also in accordance with standard IEC 61000-3-2 for class A equipment.

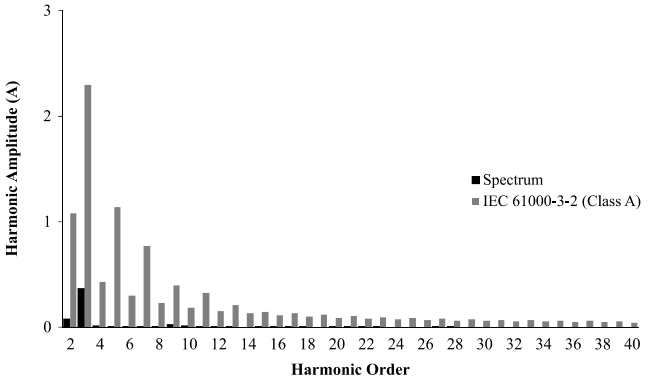


**FIGURE 22.** Harmonic spectrum of the grid current at the rated load condition in inverter mode.

The loss breakdown at the rated power is also shown in Fig. 23, while the overall losses are 96.47 W in inverter mode [30]–[32]. The major portions are due to the conduction losses in the active switches and the inductor losses.

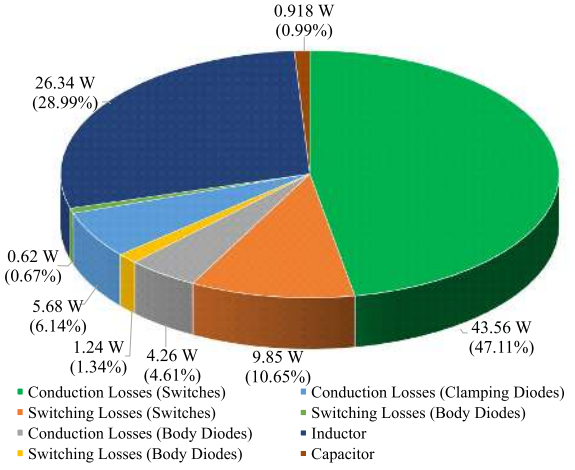


**FIGURE 23.** Loss breakdown at the rated load condition in inverter mode.

### C. POWER FLOW DIRECTION

Fig. 24 presents a detailed view of the transition from inverter to rectifier mode, thus demonstrating the bidirectional power flow capability of the converter. It can be stated that the settling time of the dc-link voltage is about 300 ms, while the grid current remains nearly sinusoidal during this time interval. Besides, it takes almost eight cycles of the grid voltage so that the power flow inversion occurs.

The power flow when the converter changes from rectifier to inverter mode is shown in Fig. 25. Once again, it takes nearly 300 ms so that the dc-link voltage remains regulated in steady-state condition. About eight cycles of the grid voltage are also required for the power flow inversion in this case.

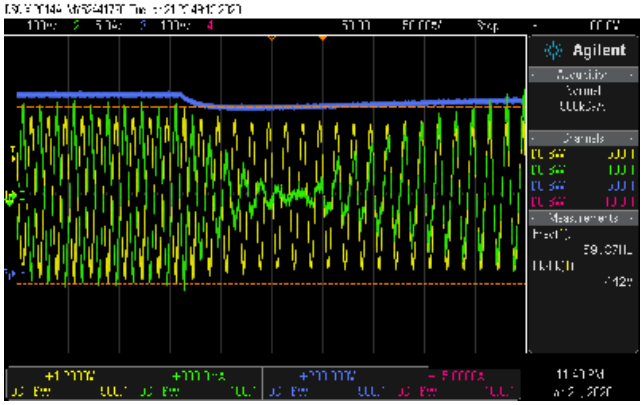


**FIGURE 24.** Detailed view of the grid voltage (yellow), grid current (green), and dc-link voltage (blue) during the transition from inverter to rectifier mode.

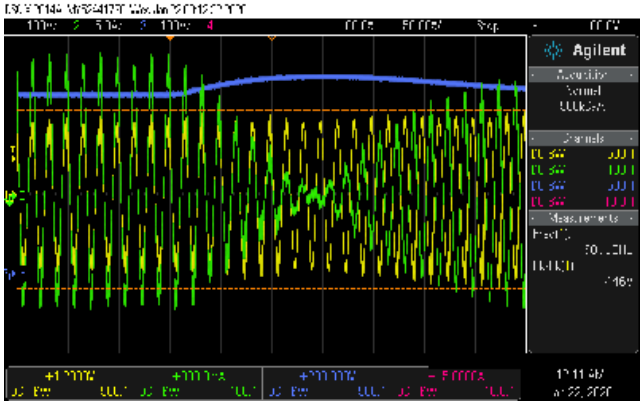


**FIGURE 25.** Detailed view of the grid voltage (yellow), grid current (green), and dc-link voltage (blue) during the transition from rectifier to inverter mode.

## VI. CONCLUSION

A 3L-SNPC topology for EV CSs has been proposed in this work. Besides, a possible CS architecture is described, which allows the integration of the utility grid and renewable energy sources, e.g., PV and wind, where the energy surplus can be injected into the ac grid, thus contributing to the distributed generation scenario.

The main advantages addressed to the converter include the operation with high power factor, bidirectional power flow capability, as well as reduced current and voltage stresses on the semiconductors, which are quite important for practical applications involving off-board battery chargers. A step-by-step design procedure has been presented, which includes the power stage elements, modulation strategy, and control system.

Experimental results have demonstrated that the converter presents good performance when operating in both rectifier and inverter modes, thus justifying the choice of the PD-SPWM technique. Even though a single-phase topology has been developed, it is reasonable to state that the same

analysis can be promptly extended to a three-phase version, especially because the phases are associated with a common neutral point in wye configuration.

The transition between the operating modes occurs naturally considering that the dc-link voltage remains properly regulated and monitored by the control system. Power quality indices are maintained within acceptable levels due to the use of a PR controller, which is capable of providing a sinusoidal reference to the grid current so that it remains in phase with the voltage even at low power levels. This controller is designed based on a conventional PI counterpart, as a design methodology is described in detail.

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