# Bifurcation Behavior of SPICE Simulations of Switching Converters: A Systematic Analysis of Erroneous Results

Xiaoqun Wu, Siu-Chung Wong, *Member, IEEE*, Chi K. Tse, *Fellow, IEEE*, and Junan Lu

***Abstract*—The SPICE simulation program is widely used as a brute force simulator for analyzing and designing switching power converters. Results from SPICE are mostly useful, but their integrity is sometimes questionable as erroneous results could be obtained which may not reflect the true behavior of the circuits being simulated. Various parameters in SPICE are crucial in controlling the convergence and accuracy of the simulated results, e.g., relative error tolerance and maximum integration step size. In this paper, we study the system consisting of the SPICE simulation algorithm and the circuit being simulated. Specifically, we describe the generation of flawed solutions in terms of bifurcation of the system under parameter variations. Erroneous results have been collected for different relative error tolerances, maximum integration step sizes, and parasitic inductance and capacitance. These flawed solutions can be analyzed in terms of the manifestation of period-doubling bifurcation and chaotic behavior under variation of selected simulation parameters. This paper provides a systematic approach to rationalizing the behavior of the SPICE simulator, its practical significance being in the identification of the ranges of simulation parameters for which flawed solutions can be produced.**

***Index Terms*—Bifurcation, circuit simulation, power electronics, SPICE, switching converters.**

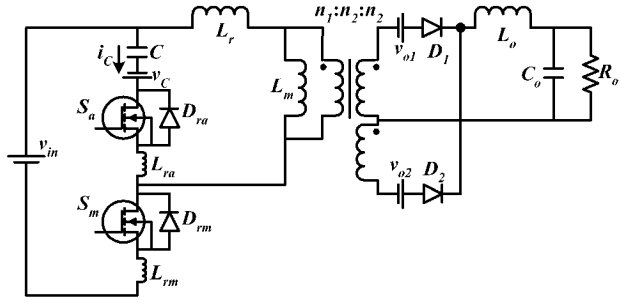


Fig. 1. Asymmetrical half-bridge forward converter.

TABLE I
SIMULATION TIMES FOR DIFFERENT VALUES OF RELTOL AND TMAX

| RELTOL | TMAX | Simulation time |
|---|---|---|
| 0.005 | default | 5.780 s |
| 0.02 | 10 ns | 17.766 s |
| 0.002 | 1 ns | 151.904 s |

## I. INTRODUCTION

PROPER models and reliable simulations are indispensable to the analysis and design of power electronics circuits [1]. SPICE is among the most widely used simulation tools which provide design information such as circuit operation, stability, transient performance, device stresses, etc. [1]–[5]. Transient analysis using SPICE is the most popular method for studying the large-signal behavior of switching converters. Switching converters, being nonlinear and time-varying, can be difficult to simulate using SPICE [6]–[8], the most commonly encountered problem being *convergence*. To overcome the convergence problems, engineers often resort to trial-and-error types of adjustment of simulation parameters, such as relaxing the relative error tolerance and increasing the maximum step size. Furthermore, *flawed* or *erroneous results* may be generated, giving wrong or misleading design information [9]. It is thus of interest to study the way in which the SPICE simulator fails to give correct results. So far, very little work has been reported to address the dynamics of the simulation process from a system viewpoint (i.e., treating the simulator that imitates the dynamics of the switching converter as a dynamical system and its parameters as system/bifurcation parameters), and to study the effects on the integrity of the results obtained. In this paper we investigate the SPICE simulator and its dynamical behavior in terms of possible bifurcations from stable operation. (See [10]–[15] for some previous study of bifurcations in power electronics, and [16]–[18] for a survey of the recent research in nonlinear dynamics of power converters.) We wish to know what parameters control the integrity of the results and how flawed results normally develop as system parameters are changed. The purpose is to understand the dynamics of SPICE simulations, leading to a more informed use of SPICE in the design of switching converters.

In Section II, we first describe a switching converter and some typical simulation results from SPICE. We will give three sets of simulation results in Section II-B. These results show different behaviors of the same circuit, under the same circuit condition

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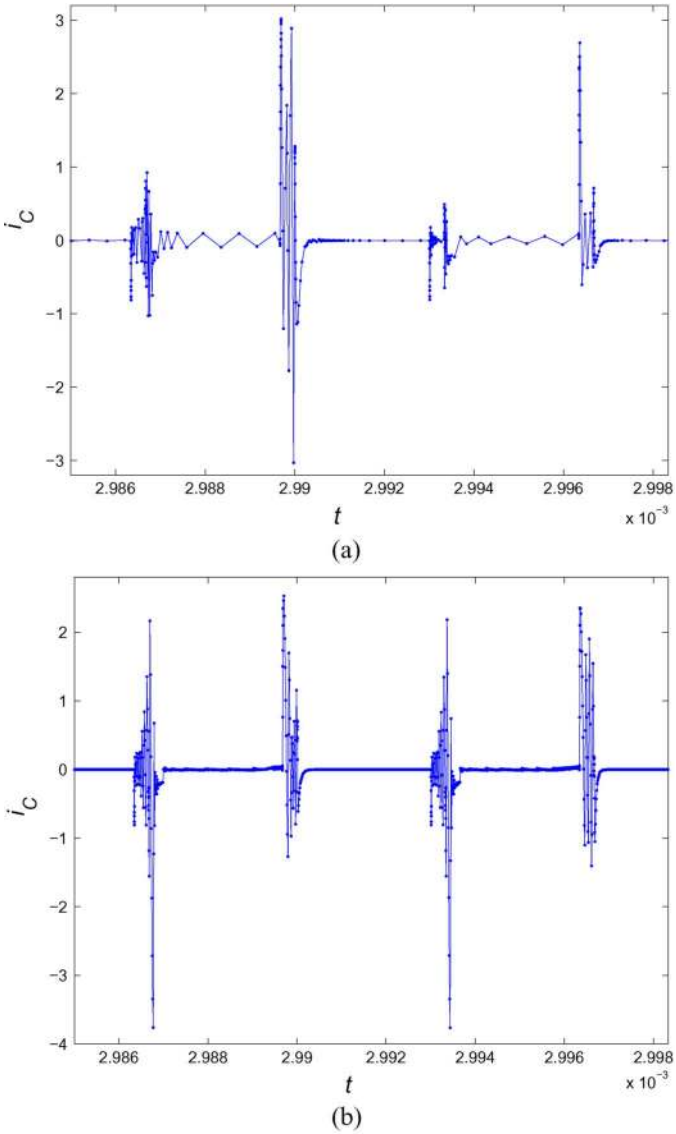


Fig. 2. Flawed simulation results of $i_C$ with: (a) $\mathrm{RELTOL} = 0.005$ and default TMAX and (b) $\mathrm{RELTOL} = 0.02$ and $\mathrm{TMAX} = 10$ ns.

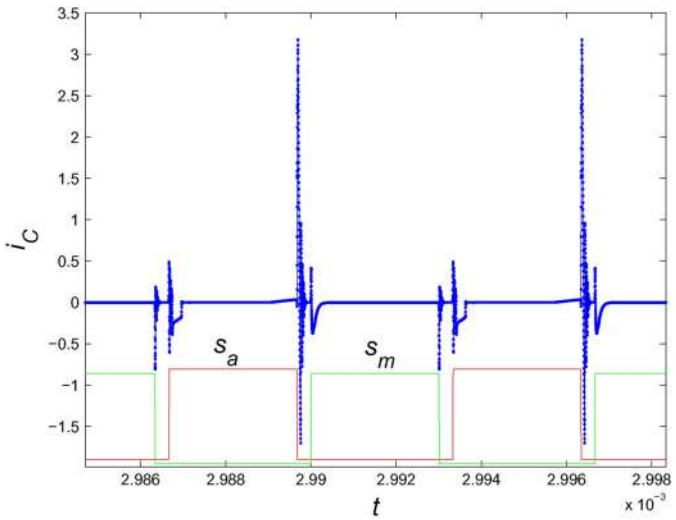


Fig. 3. Improved simulation result of $i_C$ with $\mathrm{RELTOL} = 0.002$ and $\mathrm{TMAX} = 1$ ns.

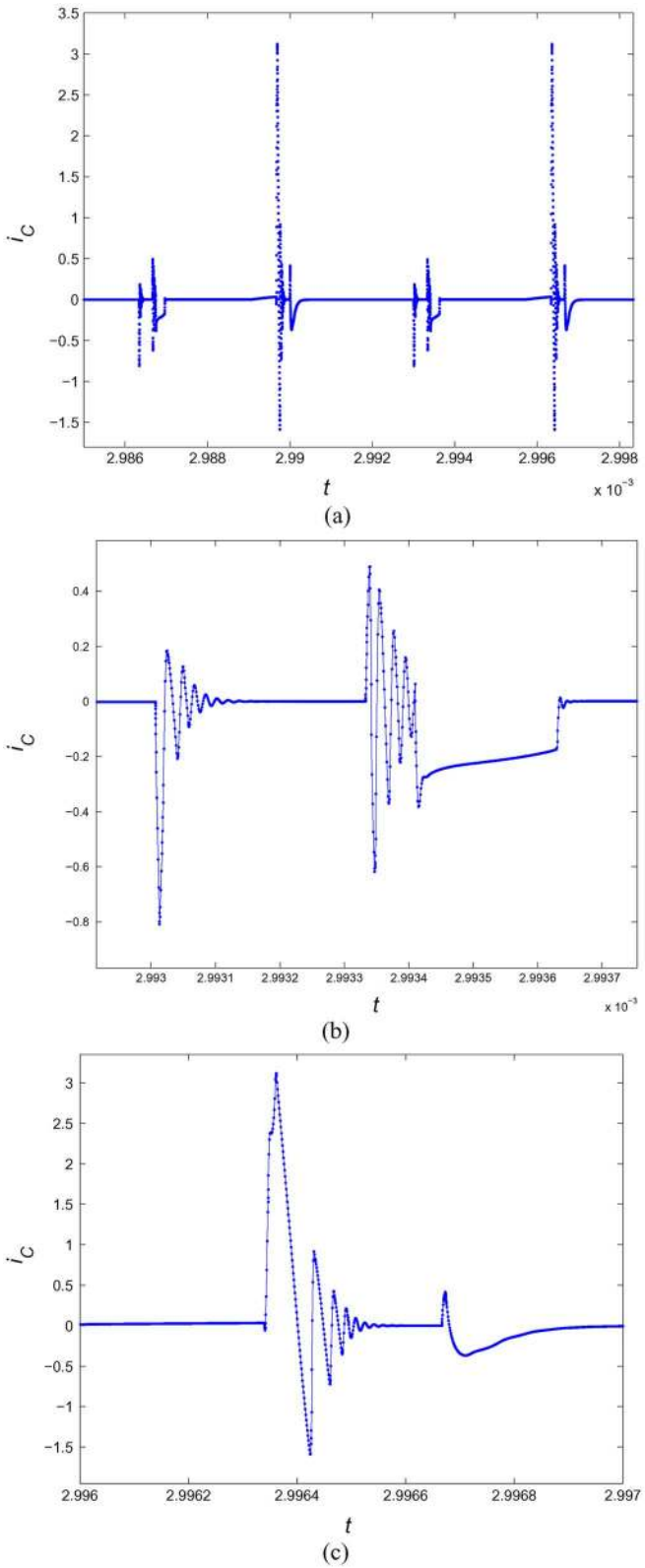


Fig. 4. (a) "Correct" simulation of $i_C$ with $\mathrm{RELTOL} = 0.001$, $\mathrm{TMAX} = 1$ ns and $\mathrm{METHOD} = \mathrm{Gear}$. (b)–(c) Close-up views.

but with different simulator's parameters. We treat the SPICE algorithm and the switching converter as a nonlinear dynamical system [19] and study the effects of the simulator's parameters, relative error tolerance (RELTOL), maximum

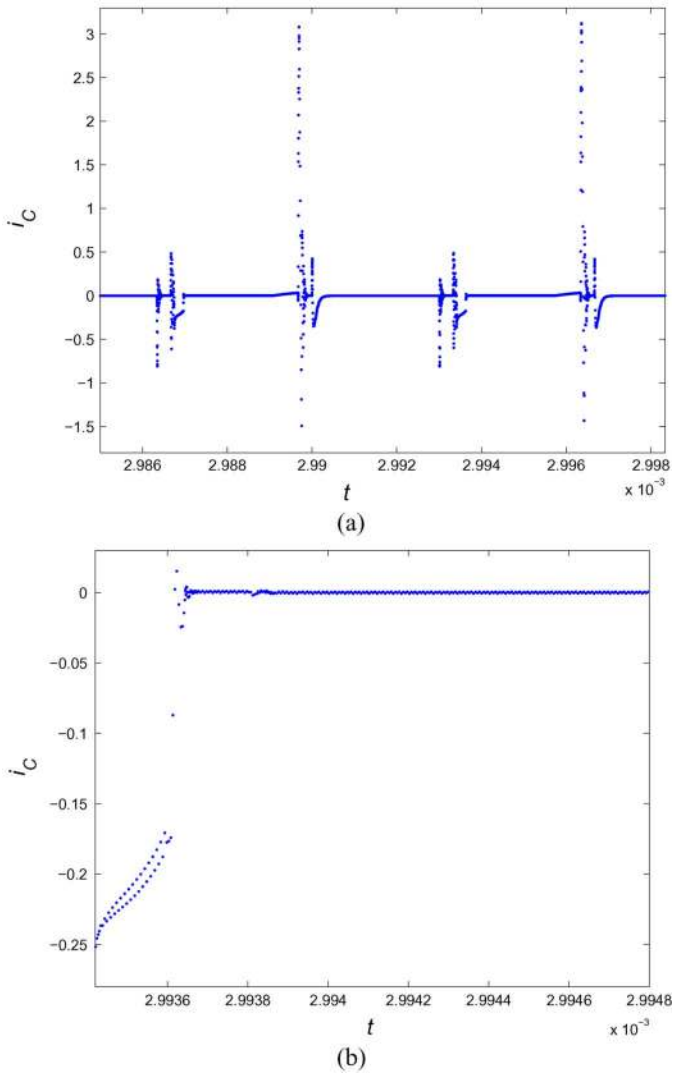


Fig. 5. (a) Flawed periodic operation of $i_C$ with $\mathrm{RELTOL} = 0.001$ and (b) close-up view.

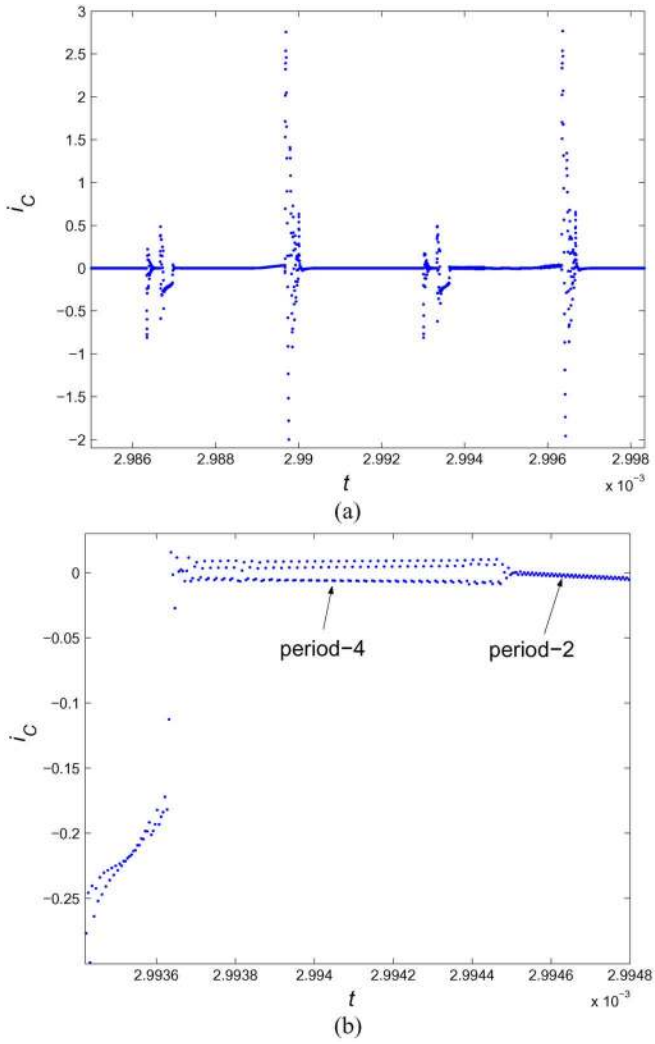


Fig. 6. (a) Flawed periodic operation of $i_C$ with $\mathrm{RELTOL} = 0.01$ and (b) close-up view.

step size (TMAX), parasitic inductors $L_{ra}, L_{rm}$, and parasitic capacitance $C_{jo}$, on the simulator's outputs. One of the circuit variables is chosen as the output. The simulated outputs of the system for different values of RELTOL are reported in Section III-A, those for different values of TMAX are reported in Section III-B, and those for varying parasitic inductance and capacitance are reported in Section III-C. We illustrate in Section IV the different operation boundaries in the system parameter space within which correct or flawed results are produced. Finally, we conclude our findings in Section V.

## II. SPICE Simulation of Switching Converters

We consider the half-bridge forward converter shown in Fig. 1, [20], [21]. SPICE has been found very useful in identifying the number of states of operation, zero-voltage switching conditions, device stresses, and sensitivity of this circuit. In the following study, we will use SPICE to verify the operational waveforms of the circuit and our purpose is to find out whether SPICE would faithfully reproduce the correct information and under what conditions it would fail to do so. Furthermore, as we are interested in knowing the integrity of SPICE in simulating the correct waveforms, we are not concerned here with the problem of convergence associated with the presence of a feedback loop. We thus omit such a feedback loop and focus on openloop simulations which are often performed by engineers in order to inspect the operational waveforms.

### A. Circuit Description

The circuit in Fig. 1 can be described in a SPICE netlist file, as shown in the Appendix. Dummy sources $v_C, V_{o1}$ and $V_{o2}$ are added for the measurement of current. The transformer is assumed ideal. Parasitic source-pin-inductors $L_{ra}$ and $L_{rm}$ of the MOS switches are added for more accurate waveform calculations. $D_{ra}$ and $D_{rm}$ are body diodes of the MOS transistors. The two diodes can also be shunted by external fast switching diodes to improve the efficiency.

Steady-state (or near steady-state) waveforms can be obtained by running transient analysis in SPICE for a sufficiently long period of time. Usually, steady-state waveforms can be assumed when there is no significant change of the waveforms in two

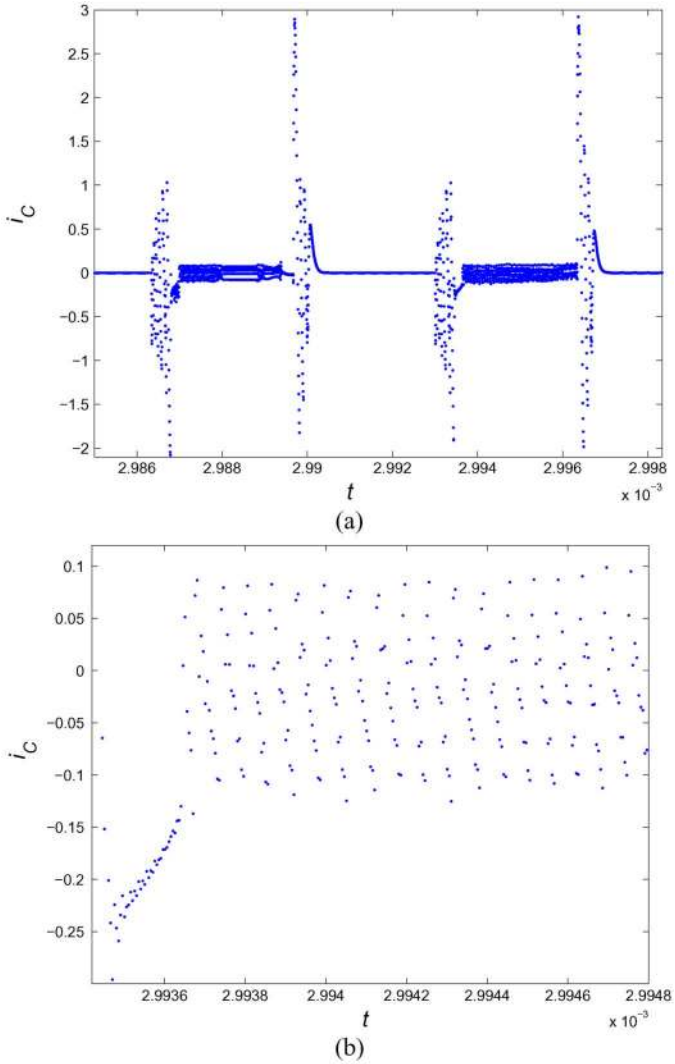


Fig. 7. (a) Flawed periodic operation of $i_C$ of longer period with $\mathrm{RELTOL} = 0.1$ and (b) close-up view.

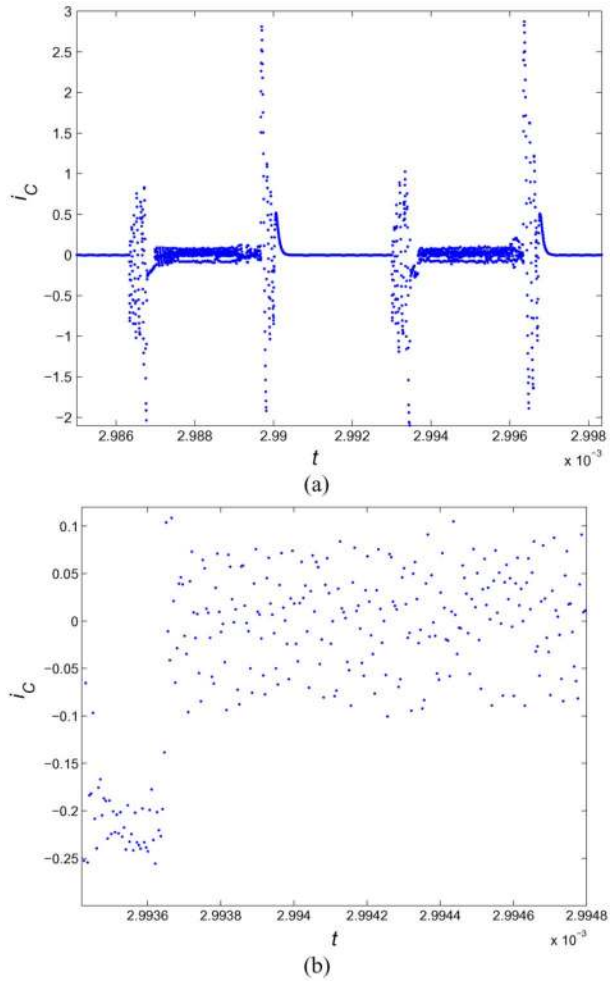


Fig. 8. (a) Flawed chaotic operation of $i_C$ with $\mathrm{RELTOL} = 0.2$ and (b) close-up view.

consecutive switching periods. A typical transient analysis command is as follows:

$$\texttt{TRAN TSTEP TSTOP} \langle\, \texttt{TSTART} \langle\, \texttt{TMAX} \,\rangle\rangle$$

where TMAX is the maximum step size used by SPICE. As a default, the program chooses either TSTEP or (TSTOP-TSTART)/50.0, whichever is smaller. The calculation of steady-state waveforms can be speeded up by using the optional UIC (use initial conditions) keyword at the end of the .TRAN statement. Also, near steady-state voltages and currents values are inserted using "IC = ..." at the end of the elements or using the .IC control line for various initial node voltages obtained from previous solutions.

### *B. Erroneous Simulation Results: Beyond Speed-Accuracy Tradeoff*

It is generally believed that simulation speed and convergence can be improved dramatically by relaxing the requirement of simulation tolerance [6]. We have measured the simulation time for three sets of simulation tolerances and controls, as shown in Table I. Figs. 2 and 3 show the corresponding simulated waveforms.

For comparison, we also present in Fig. 4 the "correct" (practically consistent) waveforms of $i_C$ with a tighter simulation control, i.e., $\mathrm{RELTOL} = 0.001, \mathrm{TMAX} = 1$ ns and the integration method is Gear. We observe a rather large discrepancy in the simulated results for different simulator's parameters. This clearly shows that the simulator's parameters do not only control the speed-accuracy tradeoff, but may also be crucial in determining whether correct or flawed results would be produced. It is thus useful to study the dynamics of the system consisting of the SPICE simulation algorithm that imitates the dynamics of the switching converter.

Since we are primarily concerned with system stability in relation to the SPICE parameters (RELTOL and TMAX), and the circuit parameters (parasitic inductors $L_{ra}, L_{rm}$ and capacitance $C_{jo}$ of body diodes $D_{ra}$ and $D_{rm}$), we will focus on variation of these parameters. From the simulation results based on the netlist shown in the Appendix, we observe period-doubling bifurcation and chaotic behavior in some intervals of time during a switching cycle. In the following, we choose the current $i_C$, as shown in Fig. 1, as the system output for the purpose of identifying the instability phenomena.

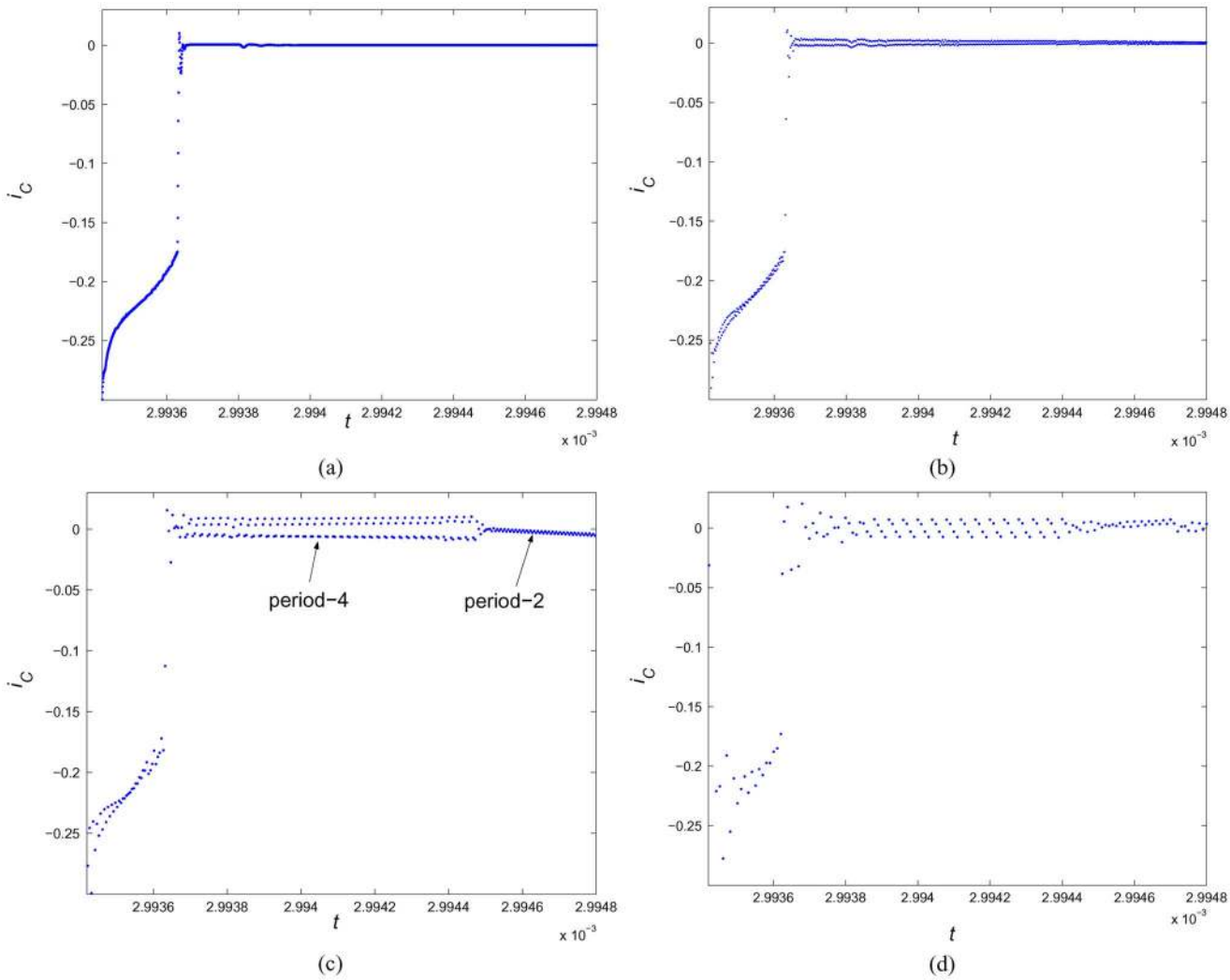


Fig. 9. (a) "Correct" simulation of $i_C$ with $\mathrm{TMAX} = 0.5$ ns; (b) flawed period-2 operation of $i_C$ with $\mathrm{TMAX} = 2$ ns; (c) flawed period-4 operation of $i_C$ with $\mathrm{TMAX} = 5$ ns; (d) flawed periodic operation of $i_C$ with $\mathrm{TMAX} = 10$ ns.

## III. Period-Doubling Bifurcation of SPICE Results

### A. Varying RELTOL

In this section, we present a detailed inspection of the effect of varying RELTOL. In these simulations, TMAX is fixed at 5 ns. The simulated results with varying RELTOL are shown in Figs. 5 to 8.

Fig. 5 plots the waveform of $i_C$ in two switching cycles with $\mathrm{RELTOL} = 0.001$. An erroneous period-2 subharmonic operation is observed, as shown in the close-up view in Fig. 5(b). Fig. 6 shows period-2 and period-4 operation (also erroneous) in some intervals of a switching cycle with $\mathrm{RELTOL} = 0.01$. Also, Fig. 7 shows erroneous periodic operation of longer periods with a larger RELTOL. Finally, Fig. 8 displays erroneous chaotic operation with $\mathrm{RELTOL} = 0.2$.

In general, we observe that the simulation results become more "unstable" (in the sense that more erroneous answers are produced) as we increase RELTOL.

### B. Varying TMAX

We now look at the effect of varying TMAX. For simplicity, we keep RELTOL at 0.01, and display the close-up views in some interval of a switching cycle.

Fig. 9(a) displays the "correct" simulated operation of $i_C$ with $\mathrm{TMAX} = 0.5$ ns. When TMAX is relaxed to 2 ns, an erroneous period-2 operation is observed, as shown in Fig. 9(b). When we further increase TMAX, we observe period-2 and period-4 operations, as shown in Fig. 9(c) and (d).

Thus, we observe that the simulation results again become progressively more "unstable" as TMAX is increased. Again, by "unstable" we mean that the simulation results do not converge to the correct results.

### C. Varying Parasitic Inductance and Capacitance

Since parasitic inductors $L_{ra}, L_{rm}$ and parasitic capacitance $C_{jo}$ of the body diodes of the MOS transistors may also affect the simulated results, we now look at the effect of varying these parasitic elements. In the following simulations, TMAX is fixed

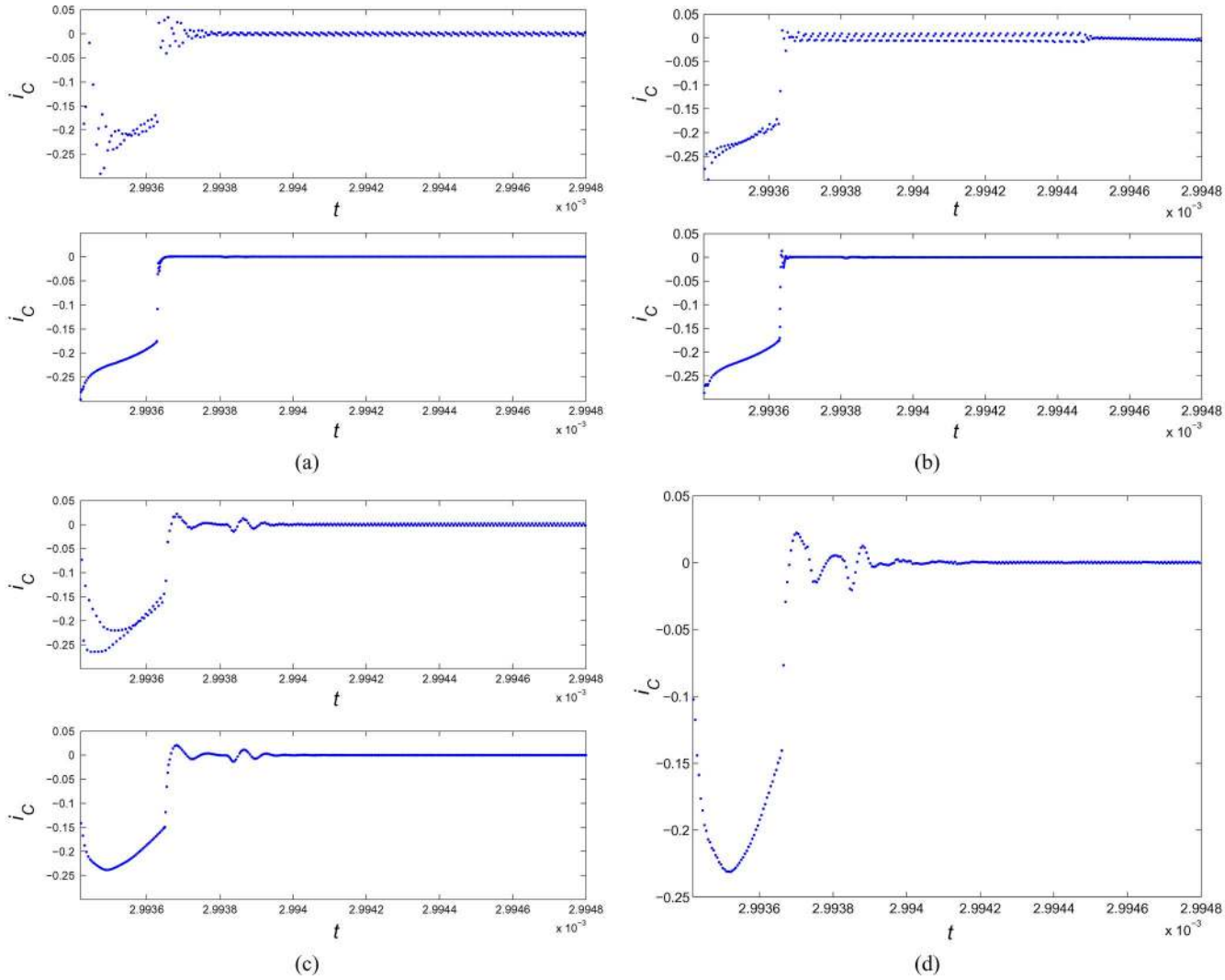


Fig. 10. Simulated waveforms of $i_C$ with different $L_{ra}$ and $L_{rm}$, and $C_{jo} = 83.2$ pF. (a) $L_{ra} = L_{rm} = 1$ nH. Upper panel: flawed periodic operation with $\mathrm{RELTOL} = 0.01$; lower panel: "correct" result with $\mathrm{RELTOL} = 0.001$ and $\mathrm{METHOD} = \mathrm{Gear}$. (b) $L_{ra} = L_{rm} = 5$ nH. Upper panel: flawed periodic operation with $\mathrm{RELTOL} = 0.01$; lower panel: "correct" result with $\mathrm{RELTOL} = 0.001$ and $\mathrm{METHOD} = \mathrm{Gear}$. (c) $L_{ra} = L_{rm} = 80$ nH. Upper panel: flawed periodic operation with $\mathrm{RELTOL} = 0.01$; lower panel: correct result with $\mathrm{RELTOL} = 0.001$ and $\mathrm{METHOD} = \mathrm{Gear}$. (d) "Correct" simulation with $L_{ra} = L_{rm} = 150$ nH and $\mathrm{RELTOL} = 0.01$.

at 5 ns. For simplicity, we only display the close-up views in some intervals of a switching cycle.

Fig. 10 shows the simulated results for different values of $L_{ra}$ and $L_{rm}$, and $C_{jo} = 83.2$ pF. The upper panels of Fig. 10(a) to (c) display erroneous period-2 and period-4 waveforms of $i_C$ for relatively small values of inductance with $\mathrm{RELTOL} = 0.01$. For comparison, we also show in the lower panels the "correct" simulated results with a tighter numerical control, i.e., $\mathrm{RELTOL} = 0.001$ and $\mathrm{METHOD} = \mathrm{Gear}$. Increasing the parasitic inductance to 150 nH, we obtain the "correct" result, as shown in Fig. 10(d). Thus, we observe that the simulation results become more "stable" as $L_{ra}$ and $L_{rm}$ are increased.

Fig. 11 shows the simulated results for different values of parasitic capacitance $C_{jo}$, while $L_{ra}$ and $L_{rm}$ are kept at 5 nH. The upper panels of Fig. 11(a) to (c) display erroneous periodic waveforms of $i_C$ for relatively small values of $C_{jo}$ with $\mathrm{RELTOL} = 0.01$. Increasing the capacitance to 400 pF, period-2 operation is observed, as shown in Fig. 11(c). The corresponding "correct" results for different values of $C_{jo}$ are also presented in the lower panels in Fig. 11(a) and (c) for the purpose of comparison. Further increasing $C_{jo}$ to 2400 pF, we obtain the "correct" result, as shown in Fig. 11(d). Thus, the simulation results again become more "stable" as the parasitic capacitance is increased.

## IV. Application: Identification of Operation Boundaries

Of engineering importance is the ranges of parameters that correspond to different types of results, flawed and correct. To address this issue, we need to identify the operation boundaries in some appropriate parameter space. We have performed a large number of simulations for different sets of parameters, which enable operation boundaries to be identified. It should be noted

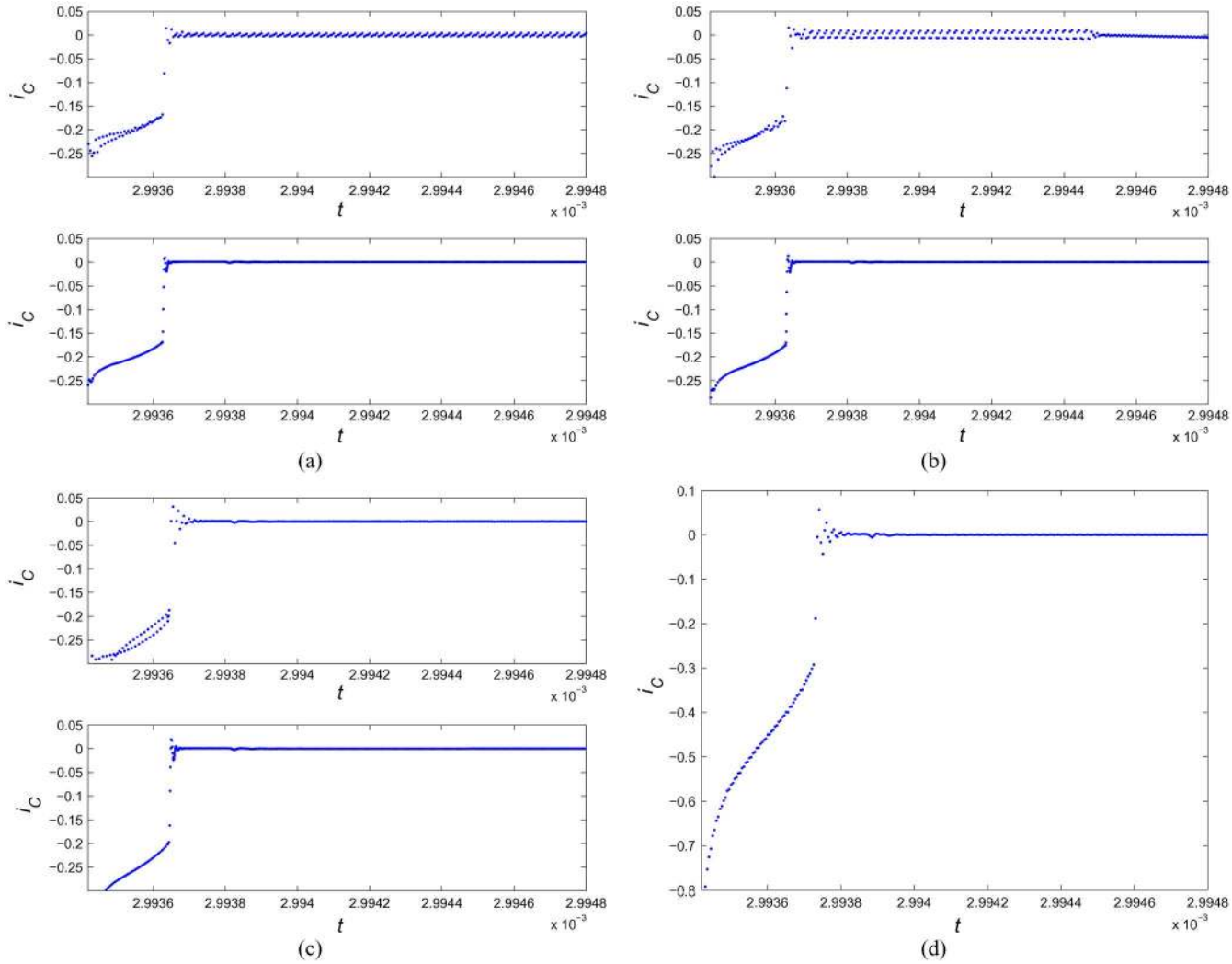


Fig. 11. Simulated waveforms of $i_C$ with different $C_{jo}$, and $L_{ra} = L_{rm} = 5$ nH. (a) $C_{jo} = 15$ pF. Upper panel: flawed periodic operation with $\mathrm{RELTOL} = 0.01$; lower panel: "correct" result with $\mathrm{RELTOL} = 0.001$ and $\mathrm{METHOD} = \mathrm{Gear}$. (b) $C_{jo} = 83.2$ pF. Upper panel: flawed periodic operation with $\mathrm{RELTOL} = 0.01$; lower panel: "correct" result with $\mathrm{RELTOL} = 0.001$ and $\mathrm{METHOD} = \mathrm{Gear}$. (c) $C_{jo} = 400$ pF. Upper panel: flawed periodic operation with $\mathrm{RELTOL} = 0.01$; lower panel: "correct" result with $\mathrm{RELTOL} = 0.001$ and $\mathrm{METHOD} = \mathrm{Gear}$. (d) "Correct" simulation with $C_{jo} = 2400$ pF and $\mathrm{RELTOL} = 0.01$.

that although numerical results are presented here for a particular circuit, the general procedure is applicable to any circuit to yield similar information.

Fig. 12(b) and (c) displays the boundaries of operations in the 2-D parameter space of $\log_{10}$RELTOL versus $L_{ra}, L_{rm}$ and $C_{jo}$. Here, we observe that the simulated results become generally more "stable" as the parasitic inductance and capacitance are increased. The correct-flawed simulation boundaries in the space of parasitic capacitance versus parasitic inductance for different values of RELTOL are shown in Fig. 12(d), where TMAX is fixed at 5 ns. For a certain value of RELTOL, we find that the numerically obtained boundary curves are generally consistent with the curve $LC = \alpha_i$, where $\alpha_i$ is a constant. The correct simulated results should then correspond to the region Fig. 12(a) displays the boundaries of operations in the 2-D parameter space of $\log_{10}$RELTOL versus TMAX. It can be observed that the simulated results become more "unstable" as TMAX and RELTOL are increased, which is consistent with the observations made earlier in Sections III-A and III-B defined by $LC > \alpha_i$. Since the parasitic resonant frequency is given by

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

the above observation clearly indicates that for given values of RELTOL and TMAX, there is a critical parasitic resonant frequency $f_c$ below which the simulated results are correct. Fig. 13 displays the 3-D boundary surface in the 3-D space of the parasitic resonant frequency, RELTOL and TMAX. In this figure, correct simulations correspond to the region below the surface and erroneous simulations correspond to system parameters above the surface.

From the above results, we clearly see that correct simulation results can only be obtained if the simulation parameters are chosen within the region where the system (SPICE) does not bifurcate into period-2, other longer periodic or chaotic or-

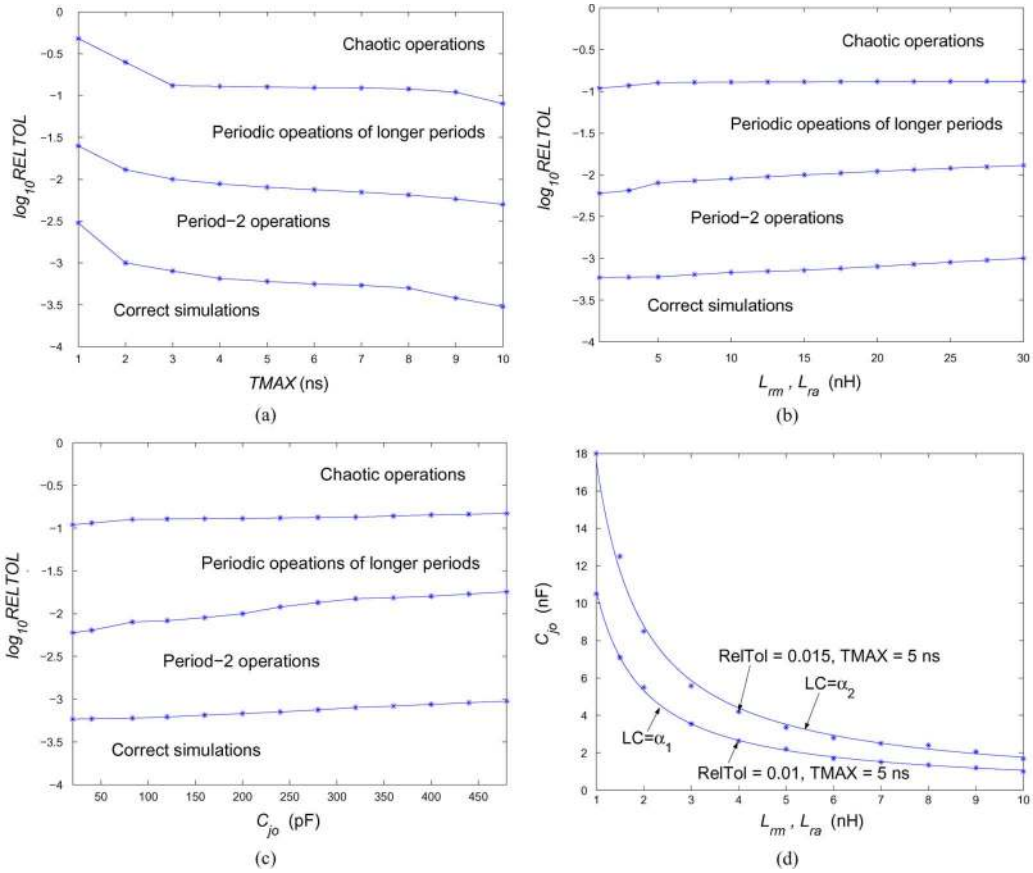


Fig. 12. Boundaries of operations in 2-D parameter space of (a) $\log_{10}$RELTOL versus TMAX; (b) $\log_{10}$RELTOL versus parasitic inductance; (c) $\log_{10}$RELTOL versus parasitic capacitance; (d) parasitic capacitance versus parasitic inductance for two different values of RELTOL. Simulation of "correct" results corresponds to region above the curves.

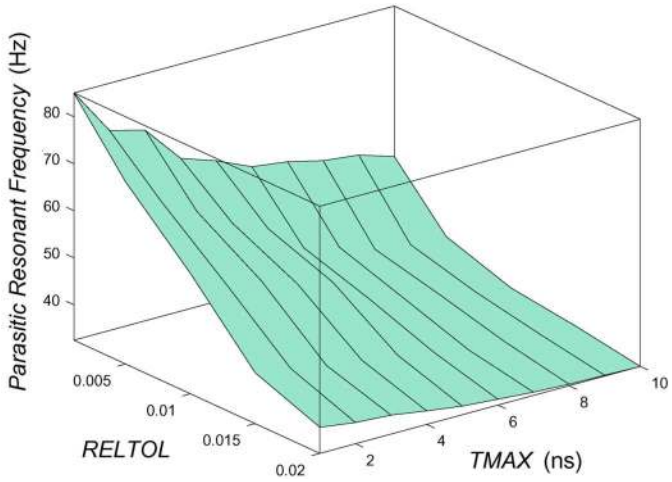


Fig. 13. Correct-flawed simulation boundary surface. "Correct" simulated results correspond to the area below the surface.

bits. It should be noted that although the boundary curves will be different if different circuit parameters are used, the general trend of the stability behavior should remain unchanged. Thus, an effective strategy for obtaining correct answers from SPICE is to choose TMAX and RELTOL appropriately in conjunction with the sizes of the circuit parasitics, as explained earlier.

## V. CONCLUSION

The SPICE simulator, along with the switching converter it imitates, has been studied in terms of the bifurcation behavior of the simulated results. A dynamical system viewpoint is taken to examine the SPICE simulated results for different parameter values. It has been found that SPICE exhibits period-doubling bifurcation and chaos when parameters are not properly chosen, giving erroneous results which do not reflect the true behavior of the circuits being simulated. Our main conclusion is that SPICE is itself a dynamical system which is controlled by a number of parameters whose variations cause the simulated results to manifest various behaviors. We also find that the system's behavior is affected by the parasitic resonant frequency of the circuit. In this paper, we have considered four parameters in particular, namely, relative error tolerance, maximum step size, parasitic inductance, and parasitic capacitance. We have performed a thorough investigation which identifies various system parameters that affect the integrity of the simulation results and the parameter boundaries that define a region in which trustworthy results can be guaranteed. The results obtained here can facilitate parameter selection for guaranteeing correct operations. Finally, it should be noted that our study has explained the convergence problem of SPICE from a system's viewpoint, treating SPICE itself as a system which may exhibit complex behavior when its parameters are changed. In particular, for the given circuit under study, we have observed period-doubling bifurcation as the key

mechanism through which SPICE loses stability and bifurcates into period-2 orbits. When the circuit being simulated is a different one, SPICE may exhibit other bifurcation behaviors. The possibilities, like in any other nonlinear system, are rich. This remains the key difficulty in deriving a universal solution for solving SPICE's stability problems.

## APPENDIX
## SPICE NETLIST

```
.PARAM   f = 150 e3
.PARAM   T = 1/f
.PARAM   d = 0.45
.PARAM   dT = T*d
.PARAM   fT = T*(d)
.PARAM   f1T = (T + dT - fT)/2
.PARAM   rise = T/1e3
.PARAM   n = 19
*        Please note that original spice3 does not
         support .PARAM macro,
*        we use .PARAM macro here for better
         readability.
Vin      nss 0 DC 120
Vc1      nc1 0 DC 0 Pulse 0 12 0 {rise}
         +{rise}
         +{dT}
         +{T}
Rc1      nc1 nc11 5
Vc2      nc2 n2 DC 0 Pulse 0 12 {f1T}
         +{rise}
         +{rise}
         +{fT}
         +{T}
Rc2      nc2 nc22 5
C        nss n1c 165n
Vc       n1 n1c 0
Lr       nss n3 30u
Lm       n3 n2 150u IC = 1
RLm      n3 n2 10k
Mm       n2 nc11 n2m n2m Sma L = 2uW = .64
Ma       n1 nc22 n2a n2a Sma L = 2uW = .64
Drm      n2m n2 Dma
Dra      n2a n1 Dma
Lra      n2 n2a 5n
Lrm      0 n2m 5n
Bp1      n3 n2 i = i(Vo1)/{n}
Bp2      n3 n2 i = -i(Vo2)/{n}
Bout1    0 n4 v = (v(n3) - v(n2))/{n}
Bout2    0 n5 v = (v(n2) - v(n3))/{n}
Vo1      n6 n4 0
Vo2      n7 n5 0
D1       n6 n8 Dout
D2       n7 n8 Dout
Lo       n8 no 4u IC = 16
Co       no 0 990u IC = 5
Ro       no 0 0.32
.MODEL   Sma NMOS level = 3VTO = 3.697KP =
         20.68u GAMMA = 0PHI = .6RD =
         .02108RS = .4508IS = 202.9f JS = 0
         +PB = .8CBD = 366.5pCJ = 0CJSW =
         0CGSO = 950pCGDO = 300pCGBO =
         0 + TOX = 100nXJ = 0DELTA =
         0ETA = 0U0 = 0
.MODEL   Dma D IS = 7.27pRS = 22.4mBV =
         200IBV = 10.0uCJO = 83.2pM =
         0.333N = 0.700TT = 36.0n
.MODEL   Dout D IS = 0.5fCJO = 1400pBV =
         100M = 0.5VJ = 0.2TT = 1n
.TRAN    10n 3000u 2980u TMAX UIC
.OPTION  RELTOL = ***
.END
.CON-
TROL
RUN
.ENDC
```

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