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Binary Hybrid Multilevel Inverter-Based Grid Integrated Solar Energy Conversion System With Damped SOGI Control

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ABSTRACT This paper presents a binary hybrid multilevel inverter (BHMLI) based grid-connected solar energy conversion system (SECS), controlled by damped second-order generalized integral (DSOGI). The BHMLI architect has a cascaded half-bridge array, which modifies the DC-link of the H-bridge of the voltage source inverter, and results in approximate reference waveform. It reduces the dV/dt of the H-bridge switches and improves output waveform quality. The DSOGI control damps the oscillations and overshoots and provides longer service period of low power switches at transient conditions. It is implemented in the multilevel inverter application for the first time in literature. The SECS is designed to inject active power to the grid, and also mitigates the harmonic and reactive power demands of the load. The cascading of 'n' half-bridges and one H-bridge generate $(2^{(nC1)} - 1)$ output voltage levels. The maximum power extraction from solar photovoltaic (PV) array is achieved through incremental conductance (IC) algorithm based maximum point tracking (MPPT) operation of the DC-DC converter. An isolated single-input multiple-output single-ended primary inductance converter (SIMO-SEPIC) realizes it. SECS with 15-level BHMLI is analyzed with extensive simulation as well as with a hardware prototype. Moreover, the shunt active filter functionality of the system at various load conditions are verified and maintained the grid power quality within the IEEE-519 standard throughout the operation. The laboratory developed setup is tested for 5 kW, 400 V, three-phase system, and the experimental analysis at steady-state and dynamic variations of load-side and insolation variations validate the theoretical claims.

INDEX TERMS Multilevel inverter, SIMO-SEPIC, solar PV, power quality.

I. INTRODUCTION

The rapid growth of electrical energy demand as well as the requirement of clean and free energy for environmental safety, give a spotlight to the renewable energy (RE) based power generation, and it is increasing globally at a fast scale. The solar photovoltaic (PV) systems are gaining more attraction among grid integrated RE technologies [1]. The advantages such as long life, ease of installation, rooftop applications, free and abundant energy, clean energy production, noiseless operation, absence of moving parts and less maintenance are the vital advantages of solar PV. The efficient power transfer from the solar PV to the distribution grid with is the modern research trend.

The grid-connected solar inverters avoid bulky battery banks and save space and cost. A conventional two-level (2L) inverter-based solar energy conversion system (SECS) is reported in [2], where a controller of modified proportional-resonant (M-PR) is operating both in stand-alone as well as grid-connected modes. The primary advantages are circuit and switching simplicity. The peak-peak current ripple in the 2L inverter is analyzed and compared with the multilevel inverter (MLI) in [3], and some pulse width modulation (PWM) schemes for reducing the

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current ripple is also reported. The higher switching stress limits the application of 2L to low power. Moreover, the higher switching frequency and complex filters reduce the efficiency and introduce electromagnetic interference (EMI) issues to nearer power and communication lines.

The grid-synchronization part of SECS is carried out by voltage source inverters (VSI), and the MLIs are introduced to overcome the demerits of 2L inverters. These are classified as neutral point clamped (NPC), flying capacitor clamped (FCC) and cascaded H-bridge (CHB). The features and power loss distribution of a three-level (3L) stacked neutral point clamped MLI is analyzed for the first time with solar PV applications in [4]. However, the THD is reduced, but the topology needs a larger number of switches for a 3L output. The literature in [5] addresses the unbalanced fault conditions of a 3L-NPC, during a fault, it generates errors and introduces a delay in the power system because of the intricate design or the neglected negative-sequence component of the grid. An FCC-MLI is reported in [6], [7] where the study focuses on the control side of the grid-connected power conditioning unit. The number of capacitors and semiconductor devices increase the cost, size and complexity. The capacitor voltage unbalancing is another issue. Hence it is less appealing to find the application for FCC-MLI. The CHB inverters are a prevalent MLI, and it provides a highly modular topological structure and higher power transfer capabilities. However, it requires a large number of switches for higher output voltage levels and isolated DC sources. It is well used for PV applications and reported in [8], and it is in conjunction with a SEPIC converter. The power and energy balance among the H-bridges of a CHB-MLI are crucial, and various PWM techniques are reported recently by addressing that issue [9]. Numerous as good as ever MLI topologies are now and again reporting these days for PV applications. The principle fascination is that the solar panel management acknowledges the demand for isolated DC sources in MLIs. Kamal Al Haddad et al. reports the packed-U-cell MLI topology, and it offers high-energy conversion quality using a lesser number of capacitors and power switches. It is modified and reported for PV applications in [10]. The paper [11] is an MLI based on two isolated 2L inverters, which are connected to the grid through a three-phase transformer having open-end windings on the inverter side, realizes a 3L-MLI. A nine-level, grid-connected inverter for PV application, based on two CHBs with different dc-link voltages is reported in [12]. An additional FCC-MLI structure is necessary for this topology, and this will prompt unequal voltage levels. Therefore, a supplementary voltage balancing circuit is essential, that results in over component count. A modified cascaded grid-connected MLI and the topology comprises of a bidirectional switch included to the standard CHB-MLI [13]. It adds additional switching and conduction losses and also increases the circuit complexity. An asymmetrical MLI presented for operating under wide dc-link voltage variation consists of a level doubling network connected in series with a full-bridge [14]. The interconnection of such units increases the number of output voltage levels. An improved CHB-MLI is reported in [15], by reducing the leakage currents and hipe the efficiency, and it shows low switching and conduction losses. An asymmetric CHB-MLI based on trinary DC sources is reported in [16]. It is a single-sourced 27-level MLI. A modular multilevel single-delta bridge-cell inverter is reported in [17] intended for utility-scale PV systems. An asymmetrical cascaded MLI with individual DC-DC converters fed from asymmetric power PV panels is published in [18]. The separate maximum power point tracking (MPPT) algorithms are implemented for different panels. However, the output voltage levels are high, but the complex control will slow down the dynamic performance of the system. A three-level step-up converter for improving the power conversion efficiency by lowering the voltage stress as well as balancing of the dc-link capacitor voltages is connected to the three-level inverter is presented in [3]. Additional voltage balancing is implemented, and the MLI is incapable of self-regulating the DC bus. The modified H-bridge-based MLI given in [19], includes two legs, a usual two-level leg and a T-type leg. The T-type is a modified 2L leg but connected to the split DC-link mid-point through a bidirectional switch. An asymmetrical CHB-MLI reported in [20] has the DC source asymmetry generated through a high-frequency DC-DC converter, and this will increase the overall component count, conduction losses and system complexity. A hybrid nine-level MLI [21] uses a PWM technique for nine-level voltage output. The reduced switch count is the main attraction of the topology, ten switches for nine levels. The globally accepted two stage SECS has more stability than single stage SECSs, because, the maximum power extraction and DC-link voltage stabilization are done by DC-DC converter part. Therefore, it is necessary to use an efficient, flexible and simple DC-DC converter to interface between PV and VSI.

A buck-boost DC-DC converter is presented in ref. [22] for PV applications. The wide range of voltage regulation capability is the advantage. It needs only one buck-boost stage for voltage regulation by employing the reconfiguration of the switching stage with a smooth transition between the modes. A new class of converters based on capacitor link DC-DC converters-Cuk, SEPIC, and Zeta converters-that operates under the critical conduction mode has been reported [23]. An auxiliary circuit is used to get zero-current and zero-voltage switching for all the switches during the transitions. The value of dv/dt and EMI issues and voltage ringing across the switches are reduced. A high gain DC-DC converter is reported by combining the switched capacitor and regenerative boost configuration [24], but the device count is increased. A control scheme for the boost converter operated with a grid-connected PV system is reported in [25]. The MPPT, as well as limited power point tracking control schemes, are employed in the boost converter. Since the inability of the boost converter to withstand wide range duty ratio is not addressed. A high gain DC-DC converter with the coupled inductor and intermediate capacitors

are used to achieve high gain [26]. To recover the leakage energy and to alleviate the voltage spikes, a clamped circuit is used. A review is reported with differential power processing converter technology in [27], and the ability of SEPIC converter for wide duty ratio control and acceptance in SECS technology is also discussed. The MPPT operation of DC-DC converter requires flexibility to buck and boost operation and must be stable at wide duty ratios.

The traditional hill climb algorithm based MPPTs such as perturb and observe (P&O) and incremental conductance (IC) algorithms provide better results at steady state. Still, the dynamic response at partial shading conditions is inadequate [28]. It has been improved by adaptive techniques such as fuzzy logic control, particle swarm optimization, artificial neural network, etc. give accurate MPPT during adverse insolation conditions. The genetic algorithm, as well as some evolved techniques, exhibits superior performance and also have the facility to add or remove constraints [29]. But these complex algorithms reduce the speed of a larger system. Therefore, for a large grid-connected solar energy conversion systems are using modified accurate hill-climbing techniques to improve the overall dynamic performances [30].

Another inevitable part of the SECS is grid synchronization control. A linear quadratic regulator based solar energy conversion system is reported in [31]. The adaptive sliding mode control scheme is reported in the literature for current control in grid integration of PV system [32]. It is less accurate, and power calculation steps are tedious. A second-order general integral (SOGI) based phase-locked-loop is presented in [33], and it shows poor damping at oscillations and overshoots. Therefore, it causes component failure. A two-stage solar PV system with a damped second-order generalized integral (DSOGI) algorithm is reported in [34]. The fundamental active power components of load currents are extracted for evaluating the reference grid currents. By using the appropriate damping factor, the grid current-control eliminates the overshoots and provides a steady response. Moreover, it gives a fast and accurate operation.

In this paper, the DSOGI controller is implemented to control a binary hybrid MLI by which real power control, reactive power control, harmonic elimination and source current balancing are verified. This paper is organized in such a way that the solar energy conversion system is described in Section II. The control part is explained in Section VI followed by the modeling of SECS in Section III. The simulation results and experimental validation are given in Section VII and Section VIII, then the conclusions are in Section IX.

II. CONFIGURATION OF GRID CONNECTED SECS

The configuration of the three-phase solar energy conversion system is shown in Fig. 1. A nonlinear, unbalanced load is connected at the point of common coupling (PCC). An RC ripple filter to eliminate the voltage ripples due to MLI switching is also connected at the PCC. This paper reports a fifteen-level binary hybrid multilevel inverter in SECS. It has an array of three half-bridge converters (hBC), feeding from

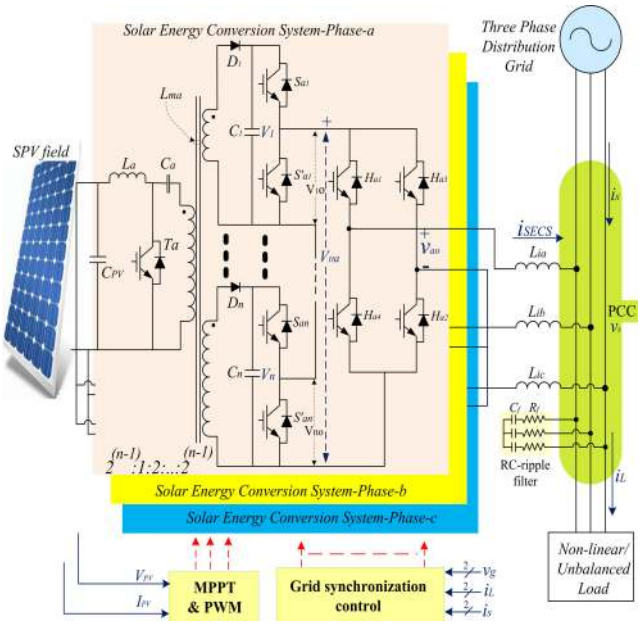

FIGURE 1. Circuit configuration of the solar energy conversion system.

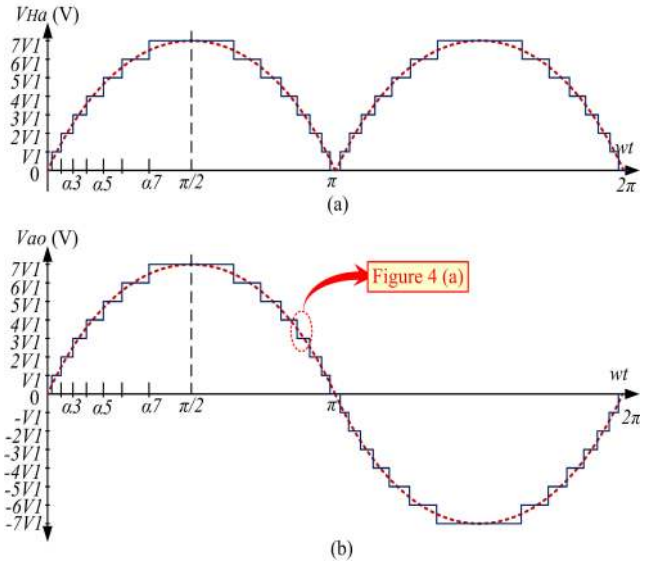

FIGURE 2. Expected output voltage waveforms of the SECS (a) half-bridge array output voltage V_{Ha} (b) fifteen level output voltage V_{ao}.

isolated DC-sources V_1, V_2 and V_3, in the ratio of 1 : 2 : 4 respectively. The operation of hBC switches S_{a1}, S'_{a1}, S_{a2}, S'_{a2}, S_{a3} and S'_{a3} is modulated for unipolar stepped voltage at the H-bridge input of phase-a is V_{Ha} (or with low switching frequency level shifted pulse width modulation), as shown in Fig. 2 (a). The H-bridge switches $H_{a1} - H_{a4}$ switched at the fundamental frequency, and produce desired AC output voltage, which is depicted in Fig. 2 (b).

The centralised solar PV field is feeding SIMO-SEPIC for three-phase balanced power injection, it is designed to provide isolated DC sources for the hBCs in each phase, and it controlled by IC algorithm based MPPT. T_a, L_a

and C_a are semiconductor switch, primary side inductance and primary side capacitors of the SIMO-SEPIC, respectively. The multi-winding transformer is designed with a turns ratio of 4 : 1 : 2 : 4.

The relation between the output voltage levels and number of half-bridges is derived as,

$$l_n = 2^{(n+1)} - 1 \tag{1}$$

where, n is the number of hBCs in phase-a.

The number of power electronic switches in one phase is determined as,

$$S_n = 2n + 4 \tag{2}$$

The positive voltage levels in the output voltage of phase-a V_{ao} are, V_1, $2V_1$, $3V_1$, $4V_1$, $5V_1$, $6V_1$ and $7V_1$. Similar negative voltage levels and a zero level are contained in a complete cycle of output voltage as depicted in Fig. 2 (b). The fundamental output voltage waveform is shown in the diagram, and the expression is derived by Fourier series analysis.

Due to the quarter wave symmetry along the x-axis, both Fourier coefficients A_0 and A_n are zero [38]. The expression for fundamental output voltage is,

$$v_{ao1}(\omega t) = \frac{4V_1}{\pi} S_f \sin(\omega t) \tag{3}$$

where, S_f is the switching factor, calculated by using MATLAB Simulink Mathfunction as,

$$S_f = \sum_{k=1}^{7} \cos(\alpha_k) \tag{4}$$

V_1 is the output voltage step magnitude and α_1 to α_7 are the switching angles, as depicted in Fig. 2.

The system efficiency is calculated by considering the power losses P_L as,

$$\begin{aligned} P_{out} &= P_{in} - P_L \\ P_L(total) &= P_{sl} + P_{cl} + P_{osl} + P_{gl} \end{aligned} \tag{5}$$

where, P_{Ltotal} is the total power loss, P_{sl} is the switching losses, P_{cl} is the conduction losses; P_{osl} is the OFF state losses and P_{gl} is the gate losses.

The upper hBC switches, S_{a1}, S_{a2} and S_{a3} are operated to introduce the respective DC sources to the output, and the lower hBC switches S'_{a1}, S'_{a2} and S'_{a3} are operated to circumvent the respective DC sources from the output voltage waveform. The upper and lower switches of single hBC are complimentary in operation. The output voltage levels are considered as modes for the explanation. Some of such operating modes, Mode-I of $0V_1$ output, Mode-VI of $5V_1$ and Mode-VII of $7V_1$ are delineated in Figs. 3 (a)-(c). Moreover, the H-bridge switches are controlled by zero-crossing detection of the fundamental frequency reference waveform. The overall switching combinations for the fifteen discrete output voltage levels are depicted in TABLE 1.

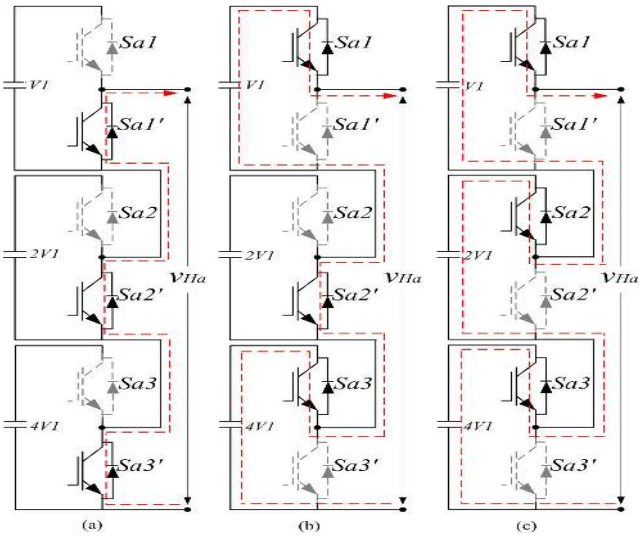

FIGURE 3. Modes of operations and current path in hBCs (a) Mode I: $0V_1$ (b) Mode VI: $5V_1$ (c) Mode VIII: $7V_1$.

TABLE 1. Switching combinations for output voltage levels.

Sl. No.	V_{ao}	S_{a1}	S'_{a1}	S_{a2}	S'_{a2}	S_{a3}	S'_{a3}	$\frac{H_{a1}\&H_{a2}}{H_{a3}\&H_{a4}}$
1	V_1	1	0	0	1	0	1	1
2	$2V_1$	0	1	1	0	0	1	1
3	$3V_1$	1	0	1	0	0	1	1
4	$4V_1$	0	1	0	1	1	0	1
5	$5V_1$	1	0	0	1	1	0	1
6	$6V_1$	0	1	1	0	1	0	1
7	$7V_1$	1	0	1	0	1	0	1
8	$0V_1$	0	1	0	1	0	1	1
9	$-V_1$	1	0	0	1	0	1	0
10	$-2V_1$	0	1	1	0	0	1	0
11	$-3V_1$	1	0	1	0	0	1	0
12	$-4V_1$	0	1	0	1	1	0	0
13	$-5V_1$	1	0	0	1	1	0	0
14	$-6V_1$	0	1	1	0	1	0	0
15	$-7V_1$	1	0	1	0	1	0	0

III. SECS DESIGN

Voltage rating of n^{th} hBC IGBT switch is,

$$V_{sn} = V_n + V_{mn} \tag{6}$$

where, V_n is the DC-link voltage of n^{th} hBC and V_m is the maximum overshoot allowed (10 % of V_n).

Three half bridges, with isolated DC-sources in the ratio of 1 : 2 : 4 are cascaded as shown in Fig. 3. Therefore, the voltage rating of H-bridge switch V_H is,

$$V_H = 7V_1 + V_{mH} \tag{7}$$

where, V_{mH} is, 10 % of $7V_1$.

Current rating of n^{th} hBC IGBT switch is,

$$I_{sn} = 1.25(I_{SECSmp} + I_r) \tag{8}$$

where, I_{SECSmp} is the peak of maximum output current through the one phase of the SECS. I_r is the maximum ripple current allowed (5 %).

Where, I_{SECSmp} is the sum of active and reactive currents (maximum possible with this practical inverter).

The multiplication factor 1.25 is used in (8) to incorporate the safety factor. Current rating of H-bridge switches are same as that of hBC switches.

The DC-link capacitors C_1, C_2 and C_3 at input of hBCs (generally call C_n) are designed as [39],

$$C_n = \frac{6V_{no}(ai_{SECSmp})t}{(V_{nmax}^2 - V_{nmin}^2)} \tag{9}$$

where, V_{no} is the rms value of n^{th} hBC output voltage, a is the overloading factor (1.2), t time to be which the DC-link voltage to be recovered, V_{nmax} is maximum possible and V_{nmin} is the minimum DC-link voltage of n^{th} hBC.

The magnitude of interfacing inductance L_i is designed based on the active power rating of SECS as,

$$L_i = \frac{V_{sa}V_{ao1}sin\delta}{P_{SECS}\omega} \tag{10}$$

The magnitude of δ is selected by the active power sharing, and it is evaluated by the control algorithm. P_{SECS} is the active power rating of the SECS and ω is the fundamental grid frequency in rad/s.

Voltage relation of the SIMO-SEPIC is derived as,

$$V_1 + V_2 + V_3 = MV_{PV} \tag{11}$$

where, $M = \frac{D}{(1-D)}$, D is the switching duty ratio of switch T_a and V_{PV} is the input voltage across C_{PV}.

The inductance value of L_a is derived as [8],

$$L_a = \frac{V_{PVmin}D_{max}}{\Delta I_{PV}f_{ss}} \tag{12}$$

where, D_{max} is considered as 0.8 at continuous conduction mode, and the isolating transformer inductance also reduces the current ripple, therefore, to get a minimum possible L_a, ΔI_{PV} is considered as 15 % of I_{PV}. f_{ss} is the switching frequency of T_a. V_{PVmin} is the minimum PV voltage at which converter operates satisfactorily to generate isolated outputs.

$$V_{PVmin} = \frac{1}{M_{max}} r \times V_{sec\ min} \tag{13}$$

where,

$$M_{max} = \frac{D_{max}}{(1 - D_{max})} \tag{14}$$

and

$$r = \frac{N_s}{N_p} \tag{15}$$

N_s is the total number of secondary windings and N_p is the total number of primary windings. $V_{sec\ min}$ is the minimum value of cumulative DC-link voltages, $7V_{1min}$. V_{1min} is derived from the relation between the fundamental grid voltage (v_{sab}) and inverter output voltage derived in (3). To acheve, power transfer from SECS to the grid PCC,

$$\widehat{v_{ao1}} = 1.1\widehat{v_{sa}} \tag{16}$$

$$V_{1min} = 1.1\frac{\pi}{4S_f}\sqrt{\frac{2}{3}}V_{sab} \tag{17}$$

The factor 1.1 is considered to account voltage drops at various parts of the SECS as well as to maintain, V_{ao} to be higher than V_{sa}.

The output voltage across the n^{th} secondary winding of SIMO-SEPIC V_n is derived as [8],

$$V_n = M\frac{N_{sn}}{N_p}V_{pv} \tag{18}$$

where, N_p is the primary and N_{sn} is the n^{th} secondary turns of multi winding transformer.

Individual DC-link voltages generated by SIMO-SEPIC at the out terminals are derived from (18) as,

$$V_1 = M\frac{V_{pv}}{4} \tag{19}$$

$$V_2 = M\frac{V_{pv}}{2} \tag{20}$$

$$V_3 = MV_{pv} \tag{21}$$

The design of T_a is,

$$V_{rms} = 2(V_{in} + V_{out}) = 2(V_{PV} + 4V_1) \tag{22}$$

$$I_{rms} = \frac{2}{\sqrt{3}}(I_{in} + I_{out}) = \frac{2}{\sqrt{3}}(\frac{I_{pv}}{3} + I_o) \tag{23}$$

where, I_o is the output current of the converter,

$$I_o = \frac{V_{PV}I_{PV}}{7V_1} \tag{24}$$

The Diode in the secondary side of the winding also has the same voltage and current ratings of IGBT switch [11].

IV. EFFICIENCY CALCULATION

The efficiency of the BHMLI is evaluated by using (25)

$$\eta_{BHMLI} = \frac{P_{in} - P_{loss}}{P_{in}} \tag{25}$$

where, P_{in} is the total input power of BHMLI. P_{loss} is the total loss of every semiconductor devices during conduction (P_{lc}), blocking (P_{loff}) and switching (P_{ls}) states. Where, P_{loff} is due to reverse leakage current, and it is practically negligible, and therefore, loss associated with leakage current is also omitted [35]. The instantaneous conduction losses through the diode and transistor are evaluated as [36],

$$P_{lcS} = [V_S + R_S i_{SECS}^{\gamma}(t)]i_{SECS}(t) \tag{26}$$

$$P_{lcD} = [V_D + R_D i_{SECS}(t)]i_{SECS}(t) \tag{27}$$

P_{lcS} is the conduction loss of the IGBT switch, V_S and R_S are the ON-state voltage drop and ON-sstate resistance of BHMLI switches, γ is the constant governed by the IGBT characteristics. P_{lcD} is the conduction loss of IGBT diode. V_D and R_D are the forward voltage drop and On-state resistance of the diode. The current through each semiconductor

TABLE 2. Device count comparison of MLIs.

MLI topology	Number of output voltage levels	Isolated Dc sources	Power electronic switches	Clamping diodes	Total capacitors
NPC-MLI	15	1	28	84	7
FCC-MLI	15	1	28	0	56
Symmetrical CHB-MLI	15	7	28	0	0
Hybrid CHB-MLI	15	3	12	0	0
BHMLI	15	3	10	0	0

device at an instant is same as the instantaneous magnitude of output current ($i_{SECS}(t)$).

The average conduction loss is estimated from (26) and (27) as,

$$P_{lc-avg} = \frac{1}{\pi}\int_0^{\pi} [\{h_s(t)V_S + h_D(t)V_D\}i_{SECS}(t) + h_S(t)R_S\, i_{SECS}^{\gamma+1}(t) + h_D(t)R_D\, i_{SECS}^{2}(t)]d(\omega t) \tag{28}$$

where, $h_S(t)$ and $h_D(t)$ are the instantaneous number of IGBT switches and number of diodes in conduction. The total switching loss is calculated by summing up the individual switching loss of each switch from TABLE 1. The switching voltage and currents at the transition intervals of ON state to OFF-state and back are linearly approximated [36]. The total power loss during turn-ON and turn-OFF duration is evaluated as [37],

$$\sum_{j=1}^{2n+4}[\frac{1}{6}V_{o,j}I(t_{on}+t_{off})f_j] \tag{29}$$

V. COMPARATIVE ANALYSIS OF BHMLI WITH CONVENTIONAL MLI TOPOLOGIES

The component count and conduction loss are the main concerns in MLI topologies. Therefore, a comparative analysis of the BHMLI with other classical topologies and binary cascaded H-bridge MLI are carried out, based on the number of components used. The conventional DCMLI, FCMLI and CHBMLI are considered. A binary hybrid CHBMLI with source ratio same as BHMLI is also included in the analysis. The comparison results are depicted in TABLE 2. The various MLIs are considered with the same output voltage levels. The BHMLI and CHB require isolated DC-sources, but comparing the power electronic switches, BHMLI has the least. Also, it reduces the burden of the pulse generation unit and also reduces the gate driver circuits. More than that, it reduces the conduction and switching losses. Besides, BHMLI does not require any clamping diodes or flying capacitors. Therefore, BHMLI is expected to give an efficient operation in SECS application.

VI. CONTROL OF THE SYSTEM

Fig. 4 (a) shows a portion of steady state expected output voltage at $+3V_1$ voltage level. The hBC switches S_{a1}, S_{a2} and S'_{a3} are turned ON along with H-bridge switches H_{a1} and H_{a2}. During this level, V_1 and V_2 are turned ON and V_3 is

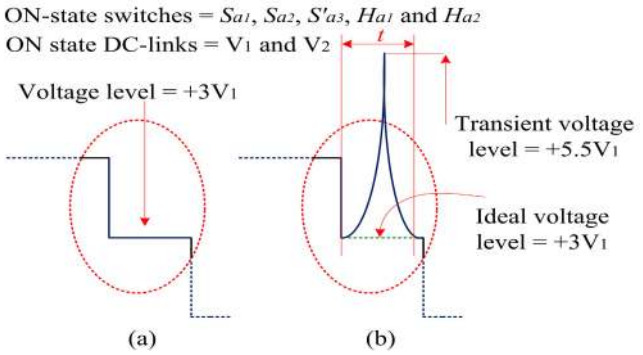

FIGURE 4. Zoomed view of portion marked in Fig. 2 (b), (a) steady state (b) voltage overshoot for time *t*.

bypassed. According to equation (6), the hBC switch S_{a1} and S'_{a1} are rated at $1.1V_1$, S_{a2} and S'_{a2} are rated at $2.2V_1$, S_{a3} and S'_{a3} are rated at $4.4V_1$ and H-bridge switches at $7.7V_1$. Therefore, if a voltage transient appeared at t with magnitude $+6V_1$ as depicted in Fig. 4 (b), hBC switches damages, and leads to overall system failure. Similar analysis can be carried out in current states also. Hence, a sophisticated, perfectly damped control algorithm is required to eliminate the overshoots and oscillations in voltages and currents at load side, grid side and PV side fluctuations. A DSOGI control reported for conventional two level inverter in [34], is implemented on the BHMLI for satisfactory SECS operation.

A. BHMLI CONTROL USING DAMPED SOGI

The PV power available at the BHMLI input is transferred to the utility side by the damped second-order generalized integral based control [34]. It is designed to deliver active power to the grid from solar PV panels and also mitigate harmonic as well as reactive power requirements of load and thereby keeping the grid power quality standards. The overall control block diagram is depicted in Fig. 5. The two-phase quantities are sensed from the three-phase three-wire system, and the third phase parameters are estimated to reduce the number of sensors. Two line-line grid voltages v_{sab} and v_{sbc}, load currents i_{La} and i_{Lb} and the grid currents i_{sa} and i_{sb} are sensed.

The three-phase grid phase-voltages are estimated from line-voltages which are passed through individual bandpass filters tuned at 314 rad/s as,

$$\begin{pmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 2 & 1 \\ -1 & 1 \\ -1 & -2 \end{pmatrix}\begin{pmatrix} v_{sab} \\ v_{sbc} \end{pmatrix} \tag{30}$$

The load current and grid current os phase$-c$ are estimated as,

$$i_{sc} = -(i_{sa} + i_{sb}); \quad i_{Lc} = -(i_{La} + i_{Lb}). \tag{31}$$

The amplitude of average phase voltage is estimated as,

$$V_t = \sqrt{(2/3)(V_{sa}^2 + V_{sb}^2 + V_{sc}^2)} \tag{32}$$

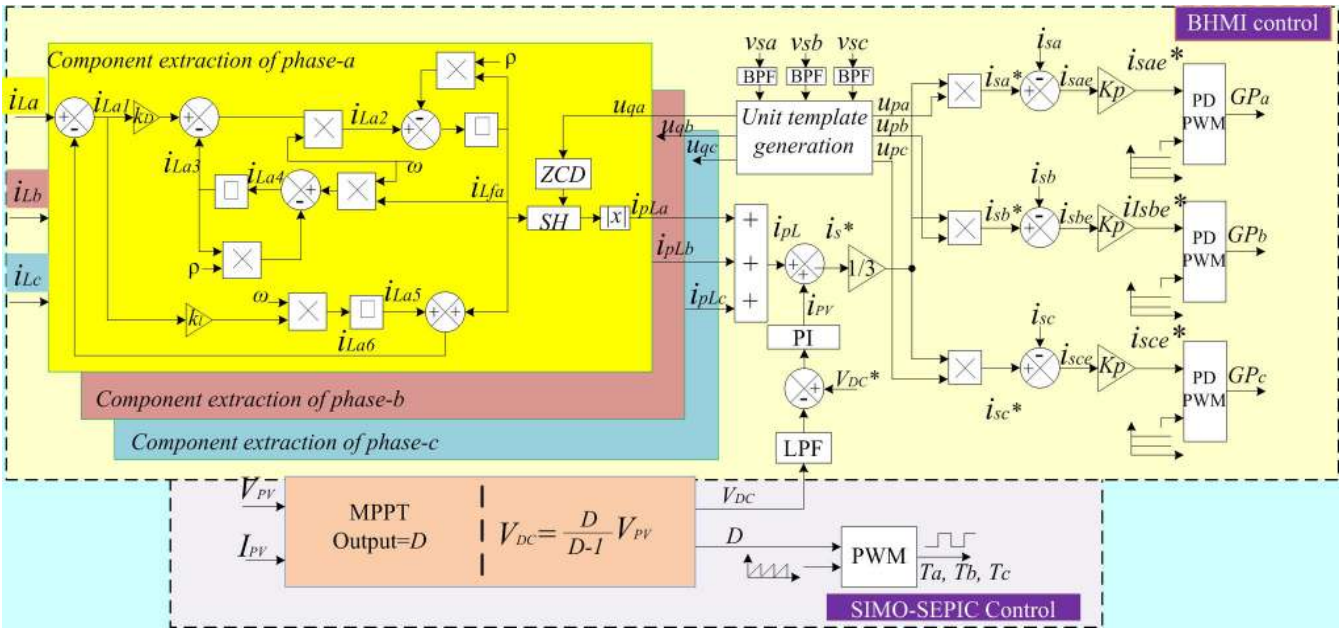

FIGURE 5. Control block diagram of SECS.

The unit in-phase templates are generated from (30) and (32) as,

$$u_{pa} = \frac{1}{3V_t} v_{sa}; \quad u_{pb} \frac{1}{3V_t} v_{sb}; \quad u_{pc} \frac{1}{3V_t} v_{sc}. \tag{33}$$

The unit quadrature components are also estimated as,

$$\begin{pmatrix} u_{qa} \\ u_{qb} \\ u_{qc} \end{pmatrix} = \frac{1}{2\sqrt{3}} \begin{pmatrix} -2u_{pb} + u_{pc} \\ -3u_{pa} + u_{pb} - u_{pc} \\ 3u_{pa} + u_{pb} - u_{pc} \end{pmatrix} \tag{34}$$

The intermediate DSOGI control signals are evaluated as [34],

$$i_{La1} = i_{La} - i_{La6} \tag{35}$$

$$i_{La2} = \omega(k_D i_{La1} - i_{La3}) \tag{36}$$

$$i_{La3} = \int i_{La4} \tag{37}$$

$$i_{La4} = i_{Lfa}\omega - i_{La3}\rho \tag{38}$$

$$i_{La5} = \int k_l \omega i_{La1} \tag{39}$$

$$i_{La6} = i_{Lfa} + i_{La5} \tag{40}$$

The constants, k_D, k_l and ρ are calculated by Routh Hurwitz (RH) stability analysis of the control transfer function, and it is derived as,

$$F_{DSOGI}(s+\rho) = \frac{\omega(s+\rho)}{(s+\rho)^2 + \omega^2} \tag{41}$$

where the Zero-order hold is transformed into $\frac{1-e^{-Ts}}{s}\frac{1}{s^2+1}$ and the unit template of the sine wave is transformed to $\frac{1}{s^2+1}$. Where ω =314. Damping factor ρ is selected as 0.5. According to RH criterion of stability, The characteristic equation (CE) satisfy necessary conditions such as no missing terms and no sign changes. The stability analysis of the DSOGI controller is evaluated and compared with the traditional SOGI algorithm. It is found that the poles and zeros are aligned at the left-hand side of the imaginary axis in the pole-zero plot. As it is a frequency fixed tuning algorithm, the slight allowable variations in the grid frequencies are accommodated by spreading the bandwidth accordingly. Therefore, the selection of damping factor must be a trade-off between tuning capacity, speed of response, overshoot-damping and flexibility with frequency variation.

The performance of the DSOGI control algorithm for the fundamental load component extraction of load current at $\omega = 314\ rad/s$ is evaluated by bode plot analysis, and it provides higher attenuation below and above ω. Hence, fine fundamental component tuning is ensured.

The fundamental load current component i_{Lfa} is passed through the sample and hold circuit, and it is triggered by the zero-crossing pulses of quadrature unit templates of grid voltage. The absolute value gives the active component of the load current. The total active load current component is evaluated as,

$$i_{pL} = i_{pLa} + i_{pLb} + i_{pLc} \tag{42}$$

The reference of individual grid current amplitudes are estimated as,

$$I_s^* = \frac{1}{3}(I_{pL} + I_{PV}^* - I_{pf}) \tag{43}$$

where, I_{PV}^* is the DC-link regulation output, derived as [32],

$$I_{PV}^* = k_{pr}(V_1^* - V_{1avg}) + k_{ir}(V_1^* - V_{1avg}) \tag{44}$$

k_{pr}, k_{ir} are the proportional and integral constants of PI controller. V_1^* is the reference DC-link voltage evaluated

from (17), and

$$V_{1avg} = \frac{V_1 + V_2 + V_3}{7} \tag{45}$$

I_{pf} is the PV feed-forward used to improve the dynamic performance of the system, and it enhances faster PI control operation. It is derived as,

$$I_{pf} = \frac{2P_{PV}}{3V_t} \tag{46}$$

P_{PV} is the output PV power,

$$P_{PV} = V_{PV} \times I_{PV} \tag{47}$$

The reference grid currents are estimated as,

$$i_{sa} = I_s^* \times u_{pa}; \quad i_{sb} = I_s^* \times u_{pb}; \quad i_{sc} = I_s^* \times u_{pc} \tag{48}$$

It is compared with the sensed grid currents, and the error is passed through a current controller to produce three-phase inverter switching references i_{sae}^*, i_{sbe}^* and i_{sce}^* respectively. It is fed to gate pulse generation unit, and the BHMLI gate pulses are produced.

In order to calculate the switching angles of the MLI, α_k is the k^{th} switching angle as shown in Fig. 2.

The selective harmonic elimination and other complicated switching angle calculation algorithms are not used here. Because, sometimes, the SECS is required to inject harmonics and reactive power to the PCC for the considered load. Seven carrier signals are used, and compared with the reference signal. Current references 1 to 7 are the constants with amplitudes 0.5 V_1, 1.5 V_1, 2.5 V_1, 3.5 V_1, 4.5 V_1, 5.5 V_1 and 6.5 V_1 respectively. The crossing point of reference signal and the carrier signal in the x-axis is evaluated using MATLAB Simulink relational operator. The corresponding switching pulses with angles α_1 to α_7 are feed into the respective switches (TABLE 1). This quarter wave switching pulse generation program is continued in the entire cycle, and it is the switching angle calculation method.

B. MPPT CONTROL

The efficient PV power transfer is achieved in the SECS by using incremental conductance algorithm based MPPT controller. It is comparatively simple and fast [34]. Power drawn from the PV panel, P_{pv} is calculated by sensing PV voltage v_{pv} and PV current i_{pv} as given in (47).

At the maximum power point (MPP),

$$\frac{dP_{pv}}{dv}(MPP) = 0 = v_{MPP}\frac{di_{pv}}{dv_{pv}}(MPP) + i_{MPP} \tag{49}$$

The conductance,

$$g_{mpp} = \frac{|di_{pv}|}{|dv_{PV}|}(MPP) = \frac{i_{MPP}}{v_{MPP}} \tag{50}$$

The IC of PV is $g_{ac} = \frac{|di_{pv}|}{|dv_{pv}|}$. But, the PV absolute conductance, $g_{DC} = \frac{i_{pv}}{v_{pv}}$ [34].

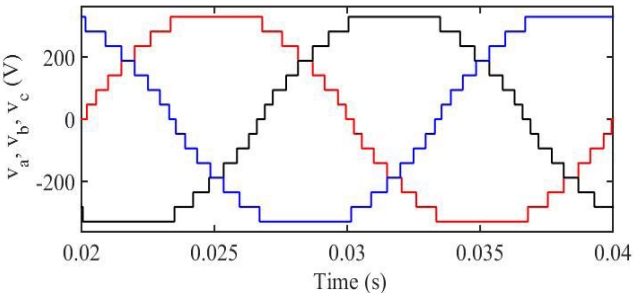

FIGURE 6. Fifteen level three-phase BHMLI output voltages.

From the equation (50),

$$v_{pv} < v_{MPP} \Rightarrow g_{ac} < g_{DC} \tag{51}$$

$$v_{pv} > v_{MPP} \Rightarrow g_{ac} > g_{DC} \tag{52}$$

The IC algorithm evaluates the MPP operating pint and produces the duty cycle D as output. The PWM with a triangular carrier wave gives switching pulses to the SEPIC switches T_a, T_b, and T_c.

VII. SIMULATION RESULTS AND DISCUSSIONS

The simulation analysis of this system is carried out in MATLAB/Simulink platform. The system parameters are depicted in Appendix A. The BHMLI generates 15-level output voltage waveforms, as shown in Fig. 6. The three-phase voltage output waveform of SECS has the peak voltage as 325 V, and the frequency is 50 Hz. The system is designed in a way that, the SECS supporting the nonlinear load demand, connected at the PCC and the remaining power is delivered to grid at rated insolation (1000 W/m^2). Fig. 7 shows the waveforms of irradiation level I_{rr}, PV output voltage V_{PV}, PV output current I_{PV}, output PV power P_{PV}, three-phase grid voltages v_s, grid currents i_s, load currents i_L and SECS currents i_{SECS} at various operating conditions in single frame, and the detailing is as follows.

A. STEADY STATE OPERATION OF SECS WITH BALANCED NONLINEAR LOAD AT CONSTANT IRRADIATION

The steady-state behaviour of the SECS is analysed with applying a balanced non-linear load at the PCC. The irradiation level is kept at 1000 W/m^2, and the waveforms are depicted before 1.98 s of Fig. 7. SECS feeding power to load and the grid. Therefore, the grid currents are 180^0 out-of-phase from the phase-voltages. One can witness that the grid currents are maintained sinusoidal and balanced. Therefore, the steady-state operation of SECS is found to be satisfactory.

B. DYNAMIC PERFORMANCE OF SECS WITH UNBALANCED LOAD CONDITION

A load unbalance introduced by thrown-off of the lad at phase$-a$ at 1.98 s as shown in Fig. 7. During this, load transition, P_{PV} remains constant. Therefore, the balanced

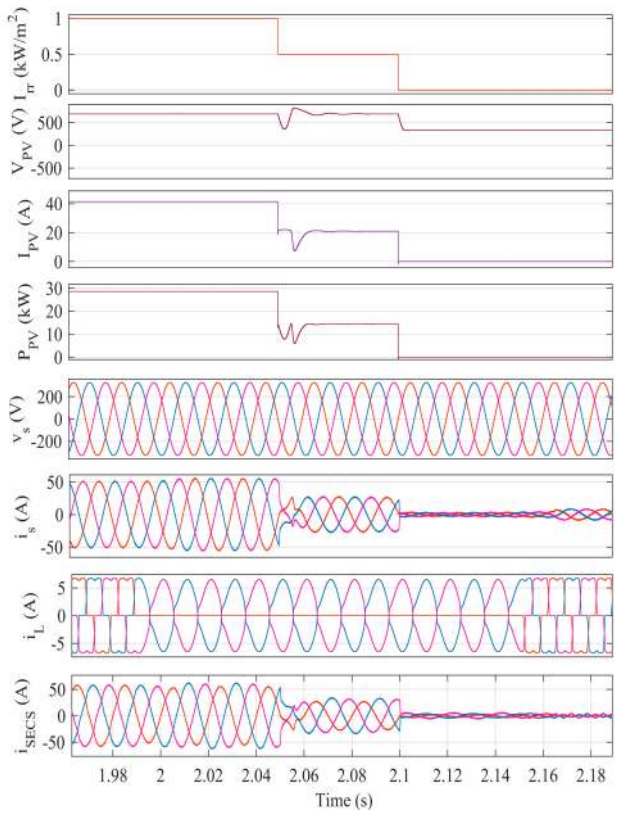

FIGURE 7. Dynamic performance of SECS at various operating conditions, I_{rr}, V_{PV}, I_{PV}, P_{PV}, v_s, i_s, i_L and i_{SECS}.

grid currents are increased. The load single-phasing is made ineffective in the grid by unbalanced operation of SECS; therefore, i_{SECS} are unbalanced. The grid current increases suddenly and attains the steady-state within a cycle duration. The sudden load removal does not create any overshoots and oscillations in any part of the system, and it validates the effect of the damped controller. The fast, steady-state achievement of the system parameters are also witnessed in this analysis. Similar satisfactory performance is also observed during load restoration at 2.15 s. Moreover, the grid currents and voltages are balanced and sinusoidal.

C. PERFORMANCE OF SECS UNDER VARIABLE IRRADIATIONS

The irradiation level is changed to observe the system behaviour. For that, at 2.05 s, the solar irradiation is reduced from 1000 to 500 W/m^2. It affects V_{PV}, but it maintained nearly constant. I_{PV} reduced to nearly half, and therefore, it is reflected in P_{PV}. The insolation variation with unbalanced load reduces the SECS output, and it is witnessed in the waveforms of i_{SECS}. As the grid is accepting power from SECS, it also reduced and settled nearly half of the rated. One can witness it in i_s. Further, the irradiation is reduced to zero-level to examine the system performance at unbalanced load at 2.1 s, as shown in Fig. 7. AS I_{rr} reaches zero, I_{PV} is reduced to zero, but there is a small value V_{PV} can

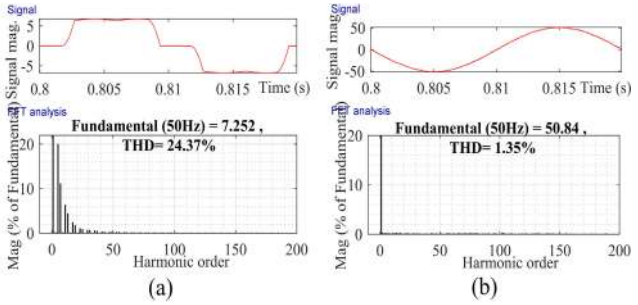

FIGURE 8. Harmonic spectra and THD of (a) load current (b) grid current.

be observed due to charged capacitor C_{PV}. P_{PV} becomes zero, instantly, and it reflected in i_{SESC}. It fails to mitigate the active demand of unbalanced nonlinear load, and it is drawn from the grid. During these transitions, the system performance is satisfactory, and the speed of steady-state attainment is also found satisfactory. Moreover, during the unbalanced, zero-insolation condition, the SECS performs as an active shunt filter and provides balanced sinusoidal and in-phase grid currents with the respective phase-voltages.

The harmonic analysis of the system parameters is depicted in Fig. 8. Fig. 8 (a) shows the harmonic spectrum of load current, and the THD is 24.3 % with 7.52 A fundamental amplitude. The current injected to the grid from the SECS has a THD of 1.3 % with amplitude 50.8 A fundamental as shown in Fig. 8 (b). The grid current and voltage harmonic magnitudes are maintained within the IEEE-519 standard. Therefore, the theoretical claim of the BHMLI based grid-connected SECS for power quality improvement is validated.

As a summary, the simulation analysis of the system provides satisfactory steady-state and dynamic performances at various load and irradiation conditions.

VIII. EXPERIMENTAL VALIDATION

A hardware prototype of the solar energy conversion system is developed in the laboratory with 5 kW, 400 V, 50 Hz three-phase grid-connected solar energy conversion system. SECS provides active power to the grid after meeting the load demands. The 15-level BHMLI is developed by using IGBT switches with protection driver., and the DSOGI and MPPT controls are realized by using dSPACE Micro Lab Box-1202. The waveforms are observed in digital storage oscilloscope (DSO), scope meter and power quality (PQ) analyzer. The design values of the system parameters are depicted in Appendix B.

The BHMLI output voltage waveforms of the experimental set are depicted in Fig. 9. The uni-polar output voltage waveform at the H-bridge input V_{Ha} is shown in Fig. 9 (a) and the fifteen level output voltage waveform is depicted in Fig. 9 (b). The performance of SECS is analyzed for various load side and irradiation variations, and the results are depicted in the following sub-sections.

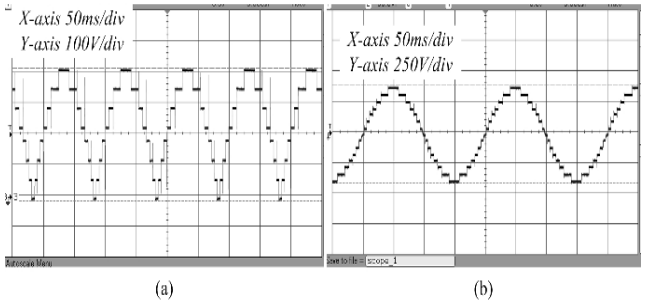

FIGURE 9. Fifteen-level BHMLI output voltage waveforms of phase−*a* (a) V_{Ha} (b) v_{ao}.

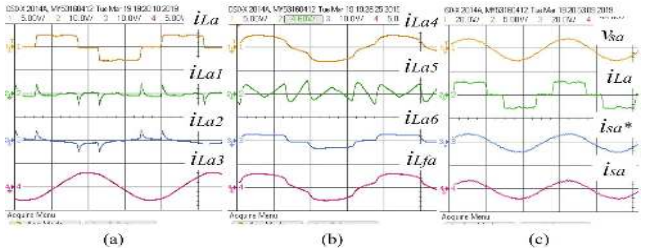

FIGURE 10. Internal signals of the DSOGI control algorithm (a) i_{La}, i_{La1}, i_{La2} and i_{La3} (b) i_{La4}, i_{La5}, i_{La6} and i_{Lfa} (c) v_{sa}, i_{La}, i^*_{sa} and i_{sa}.

A. INTERMEDIATE SIGNALS OF DSOGI BASED GRID CONTROL

The intermediate signals of the DSOGI based control algorithm with a nonlinear load is shown in Fig. 10. The load current waveform i_{La}, the derived signals i_{La1}, i_{La2} and i_{La3} are given in Fig. 10 (a). Fig. 10 (b) depicts the waveforms of i_{La4}, i_{La5}, i_{La6} and i_{Lfa}. The grid voltage V_{sa}, load current i_{La}, grid current reference i^*_{sa} and the actual grid current i_{sa} are shown in Fig. 10 (c). From the figures, one can witness the sinusoidal fundamental grid current reference i^*_{sa}, with same phase that of v_{sa}.

B. STEADY STATE PERFORMANCE OF SECS WITH LINEAR BALANCED LOAD

At constant irradiation and a balanced linear local load, the performance of SECS is analyzed, and the results are depicted in Fig. 11. The SECS delivers 4.82 kW active power, and the load draws 2.7 kW. The remaining power is fed to the grid without altering the grid power qualities. The voltage and current waveforms of the grid during the SECS operation is expressed in Fig. 11 (a). Fig. 11 (b) shows the linear load current of phase−*a* and the SECS current waveform is in Fig. 11 (c). The three-phase power injected to the grid by the SECS is shown in Fig. 11 (d). Load power is displayed in Fig. 11 (e), and Fig. 11 (f) demonstrate the SECS power. From these test results, it is clear that the performance of SECS with a linear balanced load is found satisfactory. Moreover, it keeps the grid power quality standards.

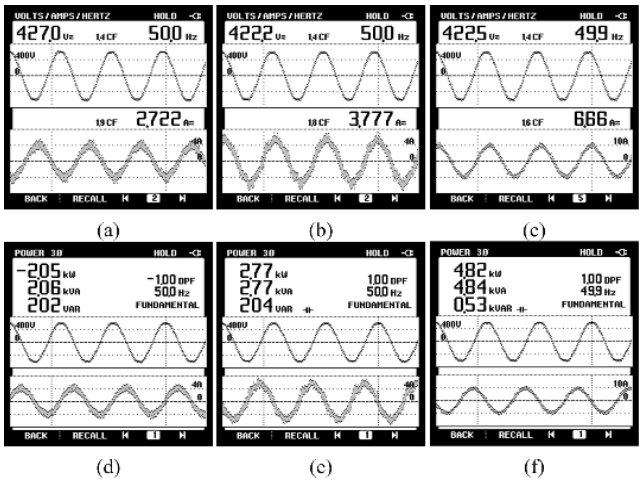

FIGURE 11. Test results of SECS under linear and balanced load (a)-(c) v_{sab} with i_{sa}, i_{La} and i_{SECSa} (d) grid power P_s (e) load power P_L (f) SECS power P_{SECS}.

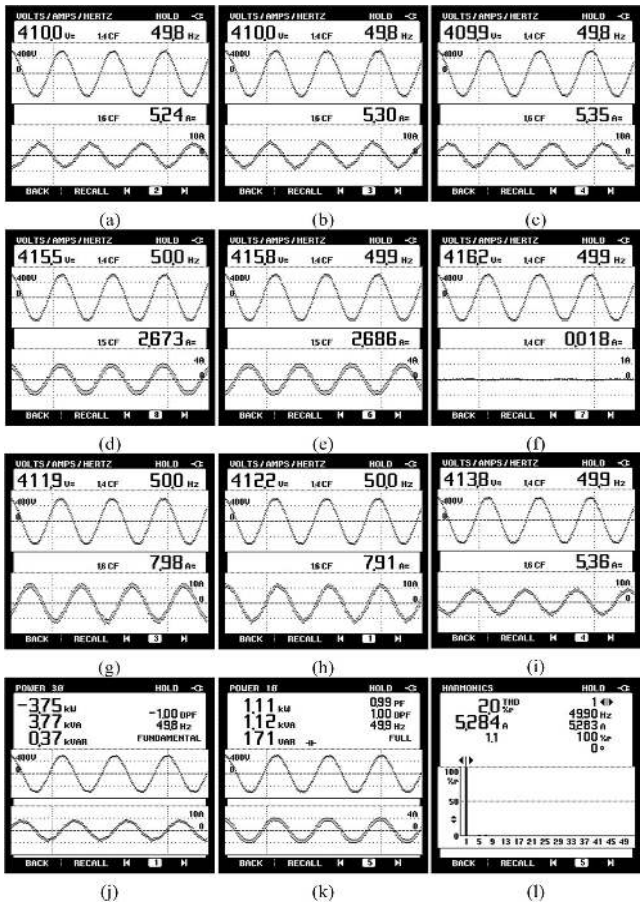

FIGURE 12. Performance of SECS under linear unbalanced load (a)-(c) v_{sab} with i_{sa}, i_{sb} and i_{sc} (d)-(f) v_{sab} with i_{La}, i_{Lb} and i_{Lc} (g)-(i) v_{sab} with i_{SECSa}, i_{SECSb} and i_{SECSc} (j) grid power P_s (k) single phase load power (l) harmonic spectrum of i_{sa}.

C. PERFORMANCE OF SECS WITH LINEAR UNBALANCED LOAD

Fig. 12 exhibits the test results of the system under linear unbalanced loads. It is clear in Figs. 12 (a)-(c) that the

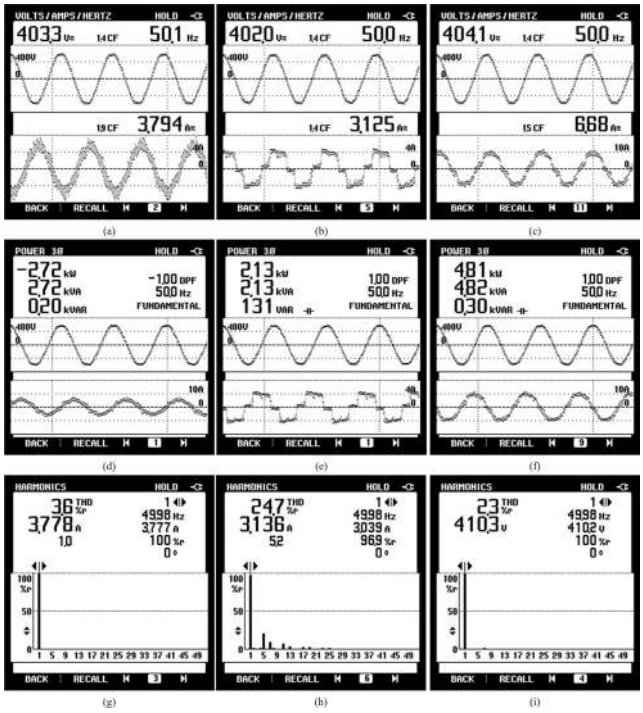

FIGURE 13. Test results of SECS under non-linear balanced load (a)-(c) v_{sab} with i_{sa}, i_{La} and i_{SECS} (d) grid power P_s (e) load power P_L (f) SECS power P_{SECS} (g)-(i) harmonic spectra of i_{sa}, i_{La} and i_{SECS}.

three-phase grid currents are balanced and sinusoidal stable under unbalanced load condition. The load current waveforms are depicted in Figs. 12 (d)-(f). The load unbalance realized by disconnecting one of the load phases. The unbalanced operation of the SECS for grid current balancing is achieved, and the waveforms are shown in Figs. 12 (g)-(i). The three-phase balanced, active power is injected to the grid at unity power factor, and zero reactive power is explored in Fig. 12 (j). The single-phase load power is given in Fig. 12 (k) and the grid current harmonics limit is within the IEEE-519 standard [40], as witnessed in Fig. 12 (l). Therefore, the performance of the system at the unbalanced load condition is verified.

D. PERFORMANCE OF SECS UNDER BALANCED NON-LINEAR LOAD

The test results of SECS at balanced non-linear load condition are depicted in Fig. 13. Figs. 13 (a)-(c) show the waveforms of v_{sab} with i_{sa}, i_{La} and i_{SECS}. It is realized that the grid current is sinusoidal and in phase with the grid phase voltage. The three-phase grid power, load power and SECS power are shown in Figs. 13 (d)-(f). It shows the unity power factor operation in grid power. SECS delivers power to the grid and the non-linear load. Figs. 13 (g)-(i) depict the harmonic spectra of i_{sa}, i_{La} and v_{sab}. From the results, it is clear that the SECS mitigates the non-linear load with 24.7 % THD and the grid current and voltage THDs are maintained within the IEEE-519 standards [40].

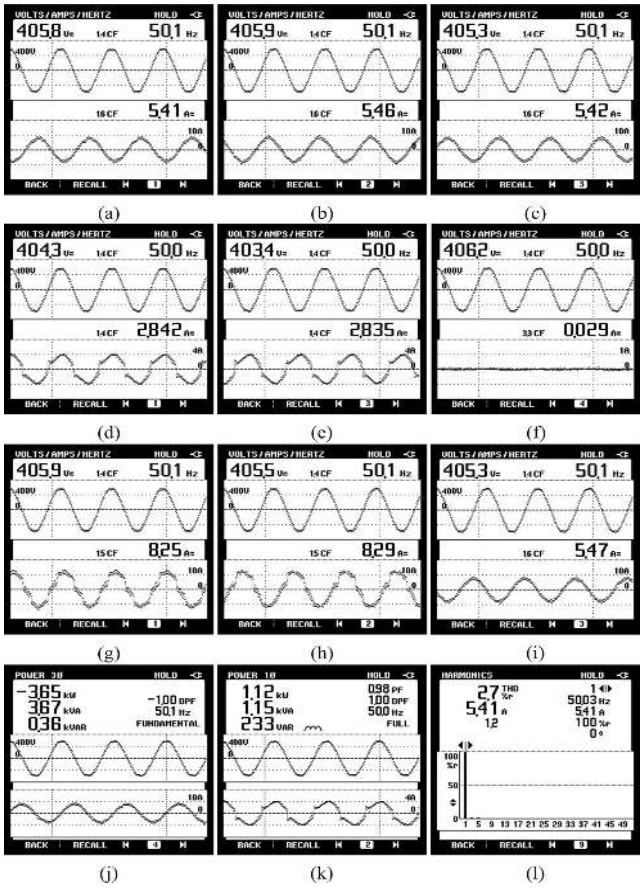

FIGURE 14. Results of SECS operation with non-linear unbalanced load (a)-(c) v_{sab} with i_{sa}, i_{sb} and i_{sc} (d)-(f) v_{sab} with i_{La}, i_{Lb} and i_{Lc} (g)-(i) v_{sab} with i_{SECSa}, i_{SECSb} and i_{SECSc} (j) grid power P_s (k) load power P_L (l) harmonic spectrum of i_{sa}.

E. PERFORMANCE OF SECS WITH NON-LINEAR UNBALANCED LOAD

Fig. 14 exhibits the performance results of SECS under non-linear unbalanced loads. It is clear in Figs. 14 (a)-(c) that the three-phase grid currents are balanced, sinusoidal and steady at non-linear unbalanced load. The load current waveforms are depicted in Figs. 14 (d)-(f). The three-phase load unbalancing is realized by opening one of the load phases. The unbalanced operation of the SECS for grid current balancing is visualized in Figs. 14 (g)-(i). The three-phase balanced, active power injected to the grid at a unity power factor, as shown in Fig. 14 (j). The single-phase load power is given in Fig. 14 (k) and the grid THD is within the five percentage limit [40], as shown in Fig. 14 (l).

F. PERFORMANCE OF SIMO-SEPIC

The Solar PV field is directly coupled to the SEPIC converter, which is controlled for tracking MPP. The three isolated DC outputs voltages and currents of the SEPIC V_1, I_1, V_2, I_2, V_3 and I_3 are shown in Figs. 15 (a)-(c). Individual output power through the output ports of SIMO-SEPIC P_1, P_2 and P_3 are shown in Figs. 15 (d)-(f). The PV output voltage and current waveforms V_{PV} and I_{PV} are depicted in Fig. 15 (g), and power is shown in Fig. 15 (h).

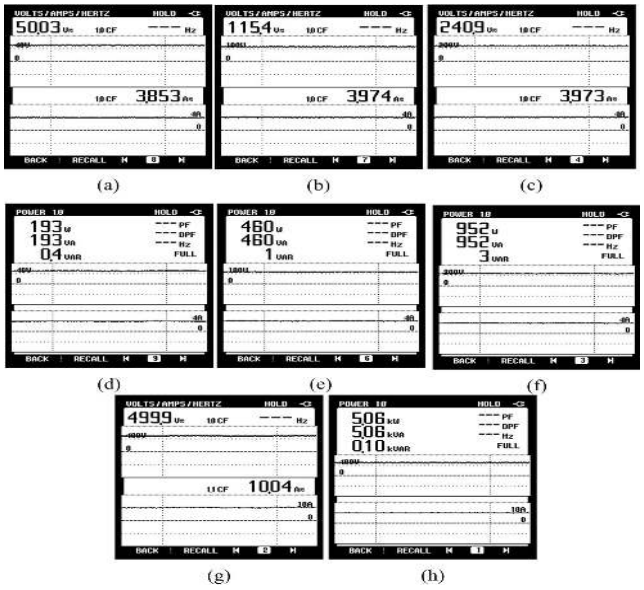

FIGURE 15. Test results of SIMO-SEPIC (a) V_1, I_1 (b) V_2, I_2 (c) V_3, I_3 (d) P_1 (e) P_2 (f) P_3 (g) V_{PV}, I_{PV} (h) P_{PV}.

G. DYNAMIC PERFORMANCE OF SECS UNDER SUDDEN IRRADIATION VARIATIONS

The performance of SECS is tested at sudden insolation variations, and the results with waveforms of V_{PV}, I_{PV}, V_1, V_2, v_{sa}, i_{sa}, i_{sb} and i_{sc} are shown in Fig. 16. The sudden irradiation fall with constant load condition reduces the PV power, and the corresponding dip is visible in I_{pv}. But the SIMO-SEPIC output voltages V_1 and V_2 are maintained nearly constant, which is presented in Fig. 16 (a). The reduction in three-phase balanced grid current injection is witnessed along with the grid voltage v_{sa} in Fig. 16 (b). The test of SECS with sudden irradiation rise is carried out, and the corresponding variations are shown in Fig. 16 (c). As the PV power increases with irradiation rise, the increment in the three-phase balanced grid current is visible in Fig. 16 (d). Therefore, during sudden irradiation variations, the DC-link voltage is maintained at steady, and the overshoots and oscillations in grid parameters are eliminated, it also counted as the merit of SIMO-SEPIC controlled by IC-MPPT.

H. DYNAMIC PERFORMANCE OF SECS AT SUDDEN LOAD VARIATIONS

The dynamic behaviour of SECS with a sudden load variation is tested and the waveforms of v_{sa}, i_{La}, i_{Lb} and i_{Lc}, i_{sa}, i_{sb} and i_{sc} are depicted in Fig. 17. One phase of the three-phase nonlinear is disconnected suddenly, and the load current waveforms with a grid phase-voltage are shown in Fig. 17 (a). With sudden load single phasing, load-power is dropped. Then that much power is injected to the grid. One can witness a balanced and in-phase grid currents and its variations in Fig. 17 (b). The waveforms of sudden load restoration with a grid phase-voltage are shown in Fig. 17 (c) and the corresponding grid power decrement is visible in Fig. 17 (d). During the transient conditions, the SECS operation is found to be satisfactory, and the peak overshoots are eliminated without compromising the speed of operation by the control algorithm. It is the evidence of damped SOGI performance in BHMLI for component safety.

The photograph with descriptions of the experimental setup developed in the laboratory is shown in Fig. 18. A dSPACE Micro-Lab-Box is used for realizing the control part, and it is marked as 1 in Fig. 18. 2 is a solar array simulator with 10 kW capacity, it has seven individual panels, 3 is digital storage oscilloscope, used to evaluate the gate pulses and internal control signals. The dSPACE is controlled through a MATLAB interfacing PC, which is marked as 4. 5 is a multimeter, 6 is the power supply for the switch protection driver and 7, 14 and 15 are the IGBT modules, which is the

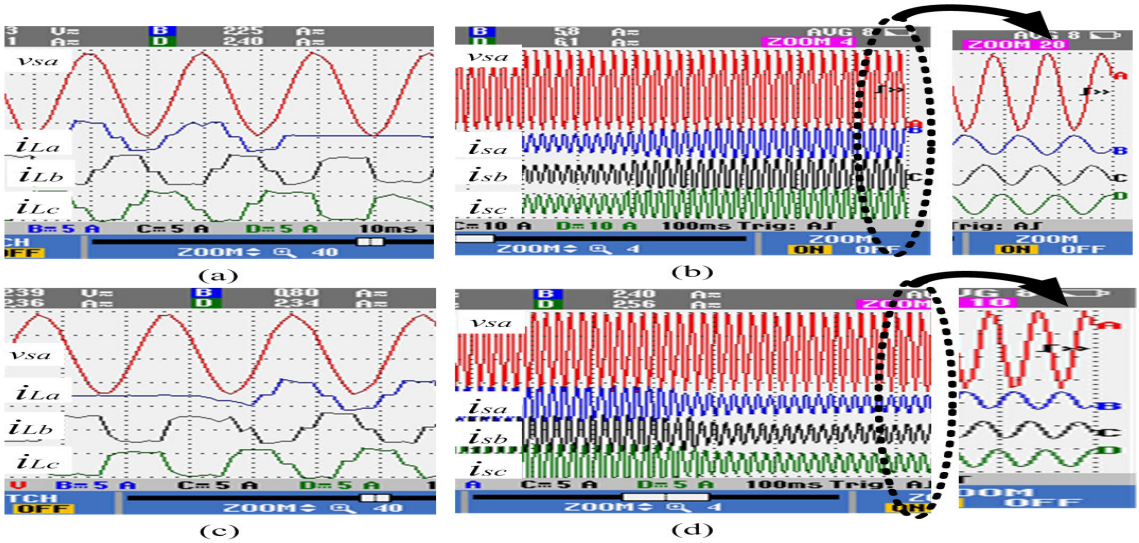

FIGURE 16. Test results of SECS at sudden irradiation variations (a)-(b) sudden Irradiation fall (c)-(d) insolation rise, waveforms of V_{PV}, I_{PV}, V_1, V_2, v_{sa}, i_{sa}, i_{sb} and i_{sc}.

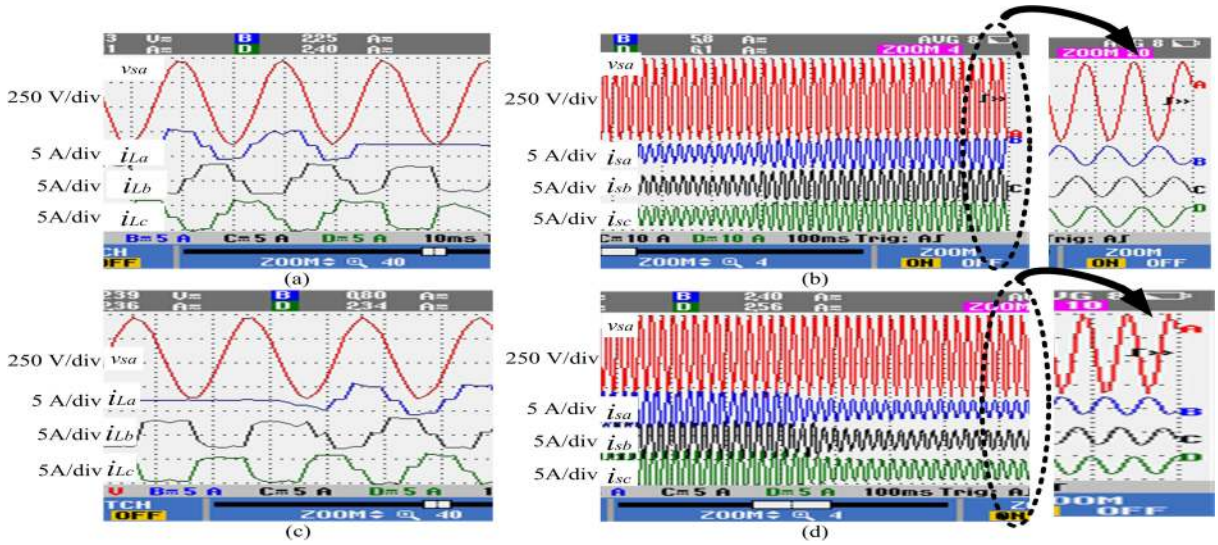

FIGURE 17. Dynamic behavior of SECS at sudden load variations (a)-(b) sudden load unbalancing (c)-(d) load balancing, waveforms of v_{sa}, i_{La}, i_{Lb}, i_{Lc}, i_{sa}, i_{sb} and i_{sc}.

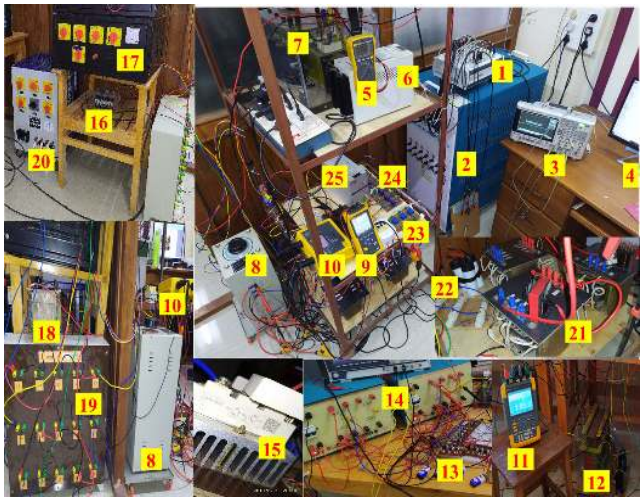

FIGURE 18. Experimental setup of the grid connected SECS 1. dSPACE micro-lab box 2. solar array simulator 3. DSO 4. dSPACE controlling PC 5. DC-link monitor 6. supply for protection driver 7. H-bridges 8. three-phase grid 9. PQ analyzer 10. power logger 11. scope meter 12. multi winding transformer 13. gate driver circuit 14. H-bridges and hBCs 15. hBC 16-18. nonlinear load and DC side impedance 19-20. linear RL load 21. interfacing inductors 22. RC ripple filter 23. voltage sensors 24. current sensors 25. supply unit for sensors.

part of BHMLI. 8 is the three-phase autotransformer, used as distribution grid. 9 and 10 are power quality analyzer and power logger, used to evaluate the grid power quality and parameter readings. 11 is a scope meter with isolated channels used to catch the dynamic performance of the system. 12 is the SIMO-SEPIC DC-DC converter with isolating transformer and 13 is the optocoupler driver circuits for the gate pulses. 16 is an uncontrolled diode bridge rectifier used as a nonlinear load in the experiment, and 17 and 18 are the variable resistive and inductive loads connected at the DC-side of the rectifier. 19 and 20 are the variable inductive and resistive load used as a linear load. 21 is the interfacing inductor, 22 is the RC ripple filter connected at the PCC, 23 and 24 are the voltage and current sensors used for the control, and its supply unit is in 25.

IX. CONCLUSION

A grid-connected solar energy conversion system, based on a binary hybrid multilevel inverter is designed and tested in this literature. The fifteen-level BHMLI is realized by ten semiconductor switches and three binary weighted isolated DC-sources. The advantages of the reduced component count, reduced device rating and lower switching frequency are validated in this work. The acceptability of damped SOGI control in BHMLI for eliminating the overshoots and oscillations during load side fluctuations are tested and found satisfactory. Therefore, the low rated components are made safer in the adverse operating conditions. The single input multiple output SEPICs in each phase, connected to the common PV field realizes a balanced power transfer to the grid. It also provided the isolated DC-sources for BHMLI operation and stabilized the DC-link voltages during sudden PV output variations. Moreover, it achieves a fast, maximum power point tracking during the dynamic insolation variations by using incremental conductance algorithm. The extensive analysis in the experimental setup proves the satisfactory SECS integration to the grid during adverse operating conditions. It mitigates the harmonic demand and active power of load and validates the shunt achieve filter functionality during the entire operation. A balanced, sinusoidal and in-phase grid currents are achieved, at dynamic load and PV variations. Therefore, SECS operation maintains the grid power quality within the IEEE-519 standard.

APPENDIXES

APPENDIX A

DSOGI control: $\omega = 314\ rad/s$; $k_D = 1.4$; $k_1 = 1.2$; $\rho = 0.42$

Simulation parameters:

Grid: Three-phase, 50 Hz, 400 V

PV: $V_{oc} = 700$ V; $I_{sc} = 60$ A; $P_{MPP} = 28$ kW (at 1000 W/m^2 insolation) and 14 kW (at 500 W/m^2 insolation)

SECS: $L_i = 6$ mH; $C_{PV} = 2200\ \mu$F; $V_{DCmin} = 650$ V

SIMO-SEPIC: $L_a = 3.2$ mH; $C_a = 10\ \mu$F; $L_m = 2$ mH; $f_{ss} = 10$ kHz.

BHMLI: $V_1 = 75$ V; $V_2 = 150$ V; $V_3 = 300$ V; $C_1 = 47\ \mu$F;

$C_2 = 33\ \mu$F; $C_3 = 22\ \mu$F.

RC ripple filter: $R_f = 10\ \Omega$, $C_f = 10\ \mu$F.

Load: Three-phase diode bridge rectifier load with 10.48 Ω DC-side impedance.

APPENDIX B

Hardware parameters:

Grid: Three-phase, 50 Hz, 400 V.

PV: $V_{oc} = 600$ V; $I_{sc} = 15$ A; $P_{MPP} = 5$ kW.

SECS: $L_i = 6$ mH; $C_{PV} = 2200\ \mu$F; $V_{DCmin} = 650$ V.

SIMO-SEPIC: $L_a = 4$ mH; $C_a = 10\ \mu$F; $L_m = 36$ mH; $f_{ss} = 8$ kHz.

BHMLI: $V_1 = 60$ V; $V_2 = 120$ V; $V_3 = 240$ V; $C_1 = 47\ \mu$F;

$C_2 = 33\ \mu$F; $C_3 = 22\ \mu$F.

RC ripple filter: $R_f = 10\ \Omega$, $C_f = 10\ \mu$F.

Load: Linear reactive 65 Ω impedance per phase and non-linear three-phase diode bridge rectifier with 150 Ω DC-side impedance.

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