Purdue University
Purdue e-Pubs

Birck and NCN Publications | Birck Nanotechnology Center

4-2011

Bipolar Integrated Circuits in 4H-SiC

Shakti Singh
Birck Nanotechnology Center, Purdue University, shakti@purdue.edu

James A. Cooper
Birck Nanotechnology Center, Purdue University, cooperj@purdue.edu

Follow this and additional works at: http://docs.lib.purdue.edu/nanopub

Part of the Nanoscience and Nanotechnology Commons

Singh, Shakti and Cooper, James A., "Bipolar Integrated Circuits in 4H-SiC" (2011). *Birck and NCN Publications.* Paper 1035.
http://dx.doi.org/10.1109/TED.2011.2107576

This document has been made available through Purdue e-Pubs, a service of the Purdue University Libraries. Please contact epubs@purdue.edu for additional information.

Bipolar Integrated Circuits in 4H-SiC

Shakti Singh and James A. Cooper, *Fellow, IEEE*

***Abstract*—Due to its wide band gap, 4H-SiC is potentially capable of sustained operation at temperatures well above 600 °C, but current devices are limited to lower temperatures by the stability of the metallization and passivation layers. SiC bipolar transistors are capable of operation at temperatures above 300 °C, as they do not have an oxide layer under high electric field and hence do not suffer from oxide reliability issues. In this paper, we describe bipolar digital integrated circuits on semi-insulating 4H-SiC that operate over a wide range of supply voltage and temperature, demonstrating the potential of SiC for high-temperature small-scale integrated-circuit applications.**

***Index Terms*—High-temperature integrated circuits (ICs), silicon carbide (SiC), SiC ICs, smart power, transistor–transistor logic (TTL).**

I. Introduction

SILICON CARBIDE (SiC) is a wide-band-gap semiconductor that offers significant performance advantages in applications requiring high voltages and/or high temperatures. 4H-SiC has a band gap of 3.25 eV, which is three times larger than that of silicon. The wider band gap gives SiC an avalanche breakdown field that is about five times larger than that of silicon, making it ideal for power-switching devices [1]–[3]. The wider band gap also results in an intrinsic temperature well above 600 °C, allowing high-temperature operation [4], [5]. The thermal conductivity of SiC is twice as high as silicon, enabling SiC devices to dissipate more internally generated heat [2]. SiC has an electron saturation velocity that is about twice as high as that of silicon [6], [7], whereas the electron mobility in 4H-SiC is about 60% that of silicon.

Generally, SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) cannot be reliably operated at temperatures above about 200 °C, due to issues with oxide reliability [8], although some recent work have extended the operational temperature of SiC MOSFETs and logic circuits using such MOSFETs to beyond 200 °C [9]–[11]. Since bipolar transistors (bipolar junction transistors, BJTs) do not utilize a gate oxide that is stressed by high electric fields, they are not subject to the same temperature restrictions as MOSFETs. This makes BJTs more suitable for high-temperature applications. In spite of all the aforementioned advantages, SiC BJTs suffer from degradation in electrical performance over time at both room and high temperatures [12]. This is caused by the development of stacking faults in the low-doped collector regions [12], [13] and/or the increase in the surface recombination in the base–emitter region [14]. However, recent work has demonstrated progress in the long-term operational stability of SiC BJT [15].

Manuscript received September 1, 2010; revised November 27, 2010; accepted January 3, 2011. Date of publication February 10, 2011; date of current version March 23, 2011. This work was supported by the Defense Advanced Research Projects Agency Robust Integrated Power Electronics Program under Grant FA8650-05-1-7203, which was administered by the Air Force Research Laboratory. The review of this paper was arranged by Editor J. D. Cressler.

The authors are with the School of Electrical and Computer Engineering and the Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: shakti@purdue.edu; cooperj@purdue.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2011.2107576

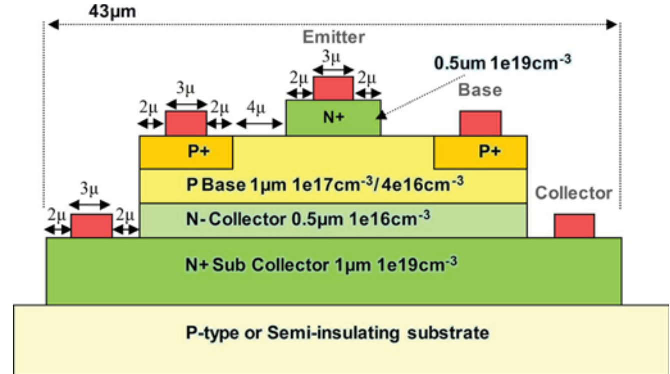

Fig. 1. Structure, dimensions, and doping of the BJT used for simulation purposes. Dimensions and the doping of the fabricated device slightly differ from the simulated structure.

The first bipolar digital integrated circuits (ICs) in 4H-SiC were simple transistor–transistor logic (TTL) gates operating on a 15-V supply voltage, with propagation delays of more than 100 ns at room temperature [16]. In this paper, we report an improved and optimized design with propagation delays of only 9.8 ns at room temperature. All circuits operate over a wide range of supply voltage and at temperatures ranging from room temperature to over 300 °C.

II. Simulation and Design

Fig. 1 shows the structure and dimensions of the BJTs (without the metal interconnect levels) used for simulation purposes. All layers in the BJT are epitaxially grown to avoid lower minority carrier lifetimes associated with implanted layers. Two types of substrates are compared: 1) p-type 4H-SiC and 2) semi-insulating 4H-SiC. Semi-insulating substrates minimize collector–substrate capacitance, leading to faster switching times for the ICs.

The BJTs are optimized by 2-D numerical simulations using MEDICI [17]. Both steady-state and transient simulations are performed to determine the base doping that provides the best combination of current gain and switching speed.

Design rules of 2 μm/3 μm (alignment tolerance/feature size) are used for the transistor. Pursuant to the design rules, all contacts are at least 3 μm wide and are at least 2 μm away from the edges of mesas to allow for misalignment during processing. The p+ base contact implant is kept 4 μm away from the emitter edge in order to minimize the effect on current gain [18].

0018-9383/$26.00 © 2011 IEEE

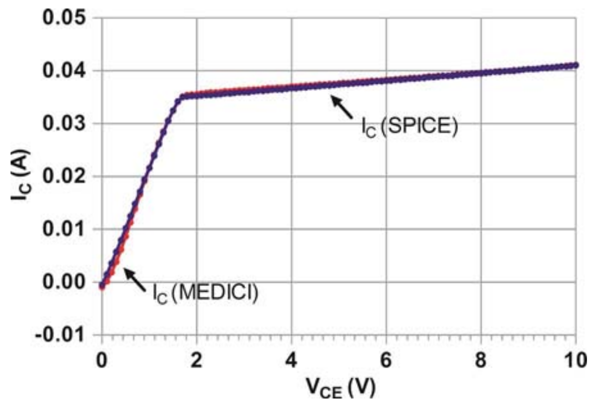

Fig. 2. SPICE fitting of I_C–V_{CE} for a 100-μm BJT for $I_B = 1$ mA.

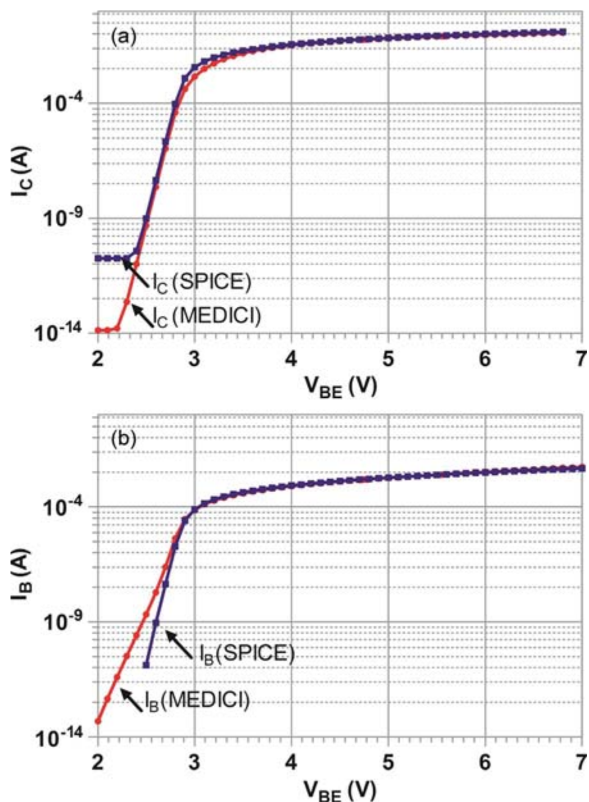

Fig. 3. SPICE fitting of (a) I_C–V_{BE} and (b) I_B–V_{BE} for a 100-μm BJT.

Circuit designs are optimized using SPICE [19]. To simulate circuits in SPICE, an appropriate model for the BJT is needed. SPICE model parameters are initially generated by treating MEDICI simulations as "experimental data" and fitting the SPICE model to the MEDICI "data." Comparisons of SPICE and MEDICI models are shown in Figs. 2 and 3. In Fig. 3, the agreement is poor at low I_C and I_B values. This is, in part, due to the inability of SPICE to accurately model recombination current. For circuit design, this is not critical since, for low I_B values, the BJT is essentially cut off. The complete set of fitted curves and final model parameters are given in [20].

Many different bipolar IC families have been developed in silicon. In this paper, we consider two particular families: 1) TTL and 2) Schottky TTL (STTL). For STTL, two different circuit configurations are examined. The first configuration is the conventional Schottky TTL circuit, whereas the second configuration, which is called "STTL as TTL," is essentially the standard TTL circuit with Schottky diodes across each transistor. The performance of each design is evaluated using a basic inverter gate with the following goals: 1) it must exhibit adequate noise margins when loaded by a fan-out of ten similar gates and 2) a chain of such gates must be optimized for minimum propagation delay. Optimization is complicated, because the circuit configuration that gives the best dc characteristics may not be the fastest. Hence, both dc and transient performance are simultaneously evaluated. The SPICE circuit simulator is used to optimize the inverter design in all technologies. The basic power supply voltage V_{CC} is chosen as 15 V, compared with 5 V for silicon TTL, due to the higher forward diode drop in wide-band-gap semiconductors.

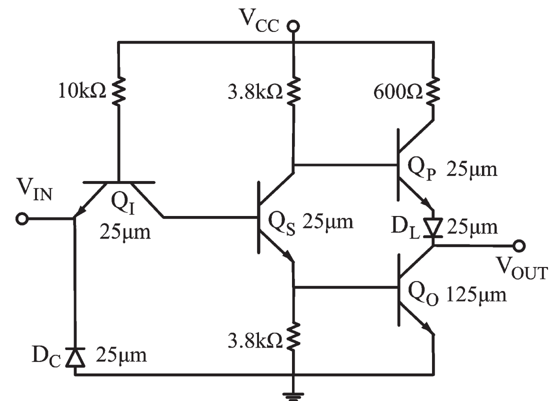

Fig. 4. Circuit diagram of the optimized TTL inverter.

Fig. 4 shows the circuit diagram of the TTL inverter with resistor and transistor values optimized for a fan-out of ten (FO-10), best dc noise margins, and lowest propagation delay. The length of all transistors, except the output transistor, is set at 25 μm. The output transistor is made 125 μm long to support a fan-out of ten. When the values of the resistors are adjusted, the areas of all transistors are scaled by the same ratio to maintain the same current density. The biggest drawback of this approach is degradation in noise margins, particularly logic-low noise margin at higher fan-outs. The solution is to make the output transistor larger than other transistors. This allows us to reduce resistor values to decrease the propagation delay without degrading the dc performance of the circuit.

Fig. 5 shows the circuit configuration of an optimized STTL inverter circuit. For the "STTL as TTL" design, the values of the resistors are carried over from the TTL design. Fig. 6 shows the voltage transfer characteristic (VTC) of the optimized TTL and STTL FO-10 inverter circuits. The stable operating points are the lowest and highest intersection points of the normal and the inverted VTC curves.

Fig. 7 shows the simulated propagation delay of an FO-10 inverter for four different designs. The optimized TTL and Schottky TTL designs (with semi-insulating substrates) display comparable propagation delays. Because of the additional complexity in fabricating STTL circuits and the minimal performance improvement, it was decided to pursue the optimized TTL design. The expected propagation delay for this configuration is 2.98 ns.

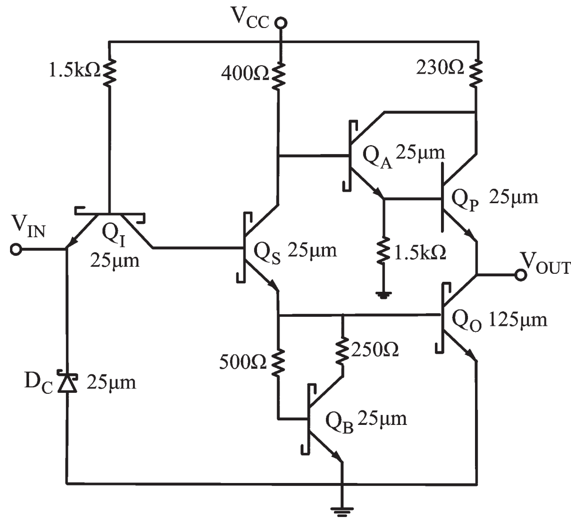

Fig. 5. Circuit diagram of the optimized STTL inverter.

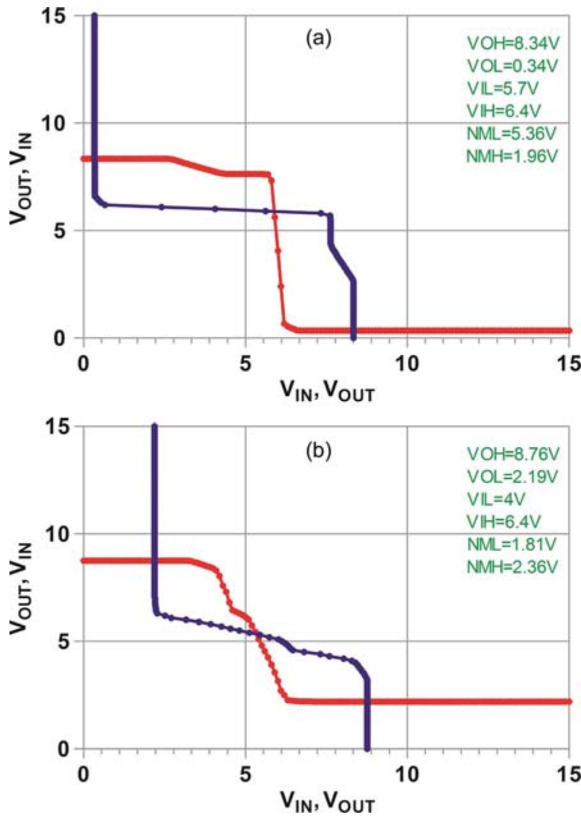

Fig. 6. Simulated VTCs for the optimized F-10 (a) TTL inverter and (b) STTL inverter.

III. Fabrication

All devices and circuits are fabricated on 50-mm wafers with n+/p/n-/n+ epilayers ($0.65\ \mu\text{m} - 1.2 \times 10^{19}\ \text{cm}^{-3}/1.1\ \mu\text{m} - 1 \times 10^{17}\ \text{cm}^{-3}/0.54\ \mu\text{m} - 8 \times 10^{15}\ \text{cm}^{-3}/1\ \mu\text{m} - 1 \times 10^{19}\ \text{cm}^{-3}$) on semi-insulating 4H-SiC substrates.

To characterize the performance of SiC TTL designs, additional gates and more complex ICs are fabricated, including a half-adder, an 11-stage ring oscillator, a string of ten inverters in series, and a D-type flip-flop.

Starting with the epitaxial wafer, Ti/Ni (10 nm/100 nm) is deposited as a masking material, and 0.7–0.78 μm of SiC is

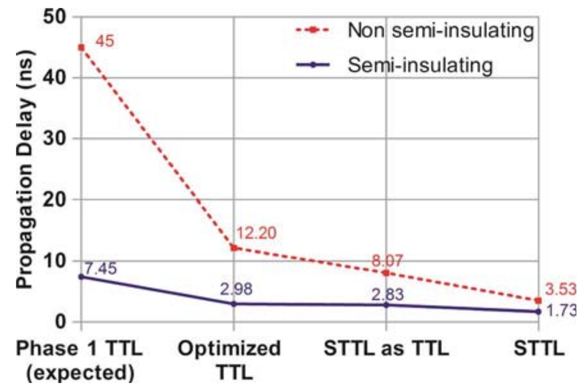

Fig. 7. Simulated propagation delays for F-10 inverter in all circuit technologies.

selectively removed by reactive-ion etching (RIE) in SF_6 to form the emitter fingers. For the p+ base contact, Ti/Au (10 nm/ 600 nm) is evaporated and patterned to form an implant mask, and Al is implanted at 650 °C at a dose of $1.05 \times 10^{15}\ \text{cm}^{-2}$. Following the implant, a graphite cap is formed on the sample to prevent roughening of the surface during the implant anneal, and the dopants are activated by annealing at 1600 °C for 20 min in argon. To form the base mesa, Ti/Ni (10 nm/150 nm) is deposited and patterned as an etch mask, and 1.6–1.7 μm of SiC is removed by RIE in SF_6. To isolate each BJT, the collector epilayers are patterned by RIE using Ti/Ni/PR as a mask.

To minimize surface recombination, several hundred angstroms of metal–oxide–semiconductor-quality oxide is grown by pyrogenic oxidation at 1150 °C for 3.5 h, followed by a two-hour anneal in NO at 1175 °C [21]. Using photoresist as a masking material, contact windows are opened in the oxide using RIE and buffered hydrofluoric acid (BHF). This is followed by deposition of contact metals (70-nm Ni for n-type and 34-nm/ 167-nm Ti/Al for p-type), using e-beam evaporation. The contacts are then annealed at 1000 °C for 2 min in vacuum.

A first intermediate dielectric (ILD), which is 0.5 μm thick, is formed by low-temperature oxidation (LTO). Next, windows are opened in the ILD to deposit top metal. Fifteen-nanometer Ti and 250 nm of Al are sputtered to form the first layer of metal interconnect. A second ILD is then deposited by LTO. In order to connect the first layer of interconnect to the second, vias are opened using RIE and wet etching, using photoresist as an etch mask. Finally, Ti/Au (15 nm/250 nm) is sputtered to form the second-level interconnect. Fig. 8 shows scanning electron microscope (SEM) images of some of the completed devices and circuits.

IV. Results and Discussion

The dc characteristics of the transistors and circuits are measured using an HP-4156 semiconductor parameter analyzer. The transient response of circuits is characterized using an Agilent-33220A waveform generator and a Tektronix-TDS5032B digital phosphor oscilloscope with a Tektronix P6245 low-capacitance (< 1 pF) field-effect-transistor probe. All measurements are obtained at wafer probe using a hot chuck with maximum temperature of 355 °C.

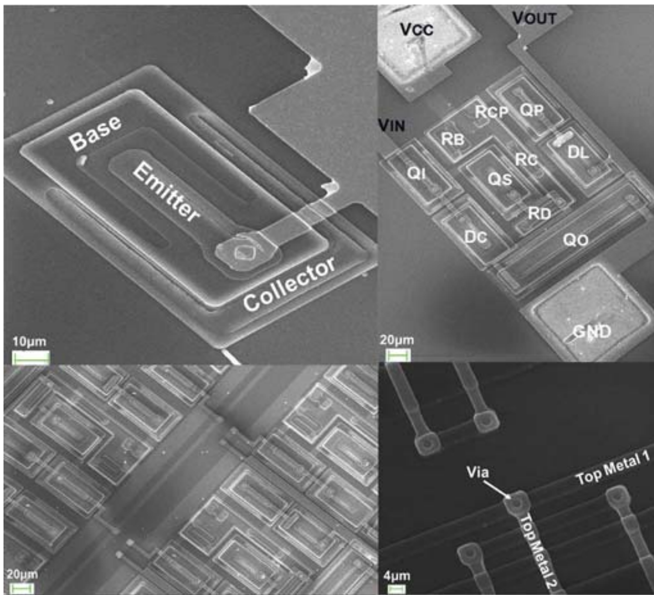

Fig. 8. SEM photographs of (clockwise, from top left) a 25-μm stand-alone BJT, a TTL inverter, metal lines, and portion of a demonstration IC.

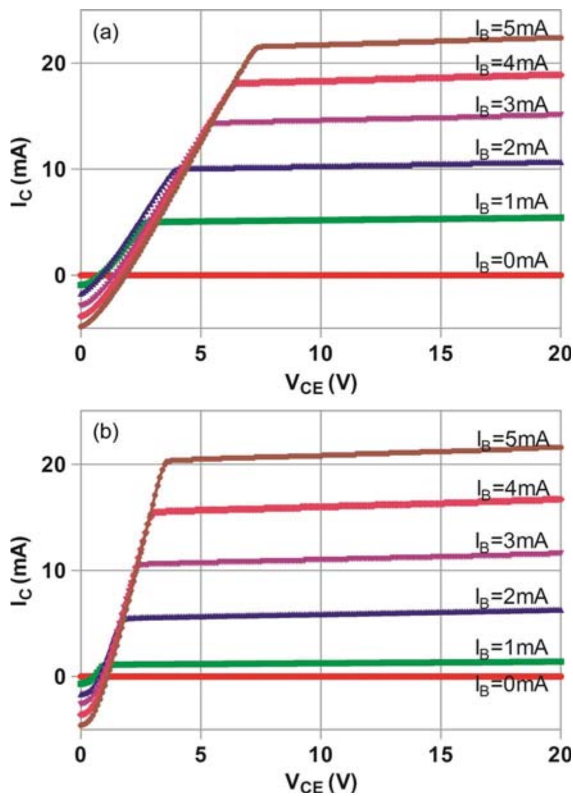

Fig. 9. I_C–$V_{\rm CE}$ plots for (a) the 25-μm BJT and (b) the 125-μm BJT.

The sheet resistivities ρ_s of the emitter, collector, and base epilayers, which was obtained using transmission-line-method measurements, are 250, 216, and 21 300 Ω, respectively. The resistivities $\rho_{\rm cn}$ of the emitter, collector, and base contacts are 2.35×10^{-5}, 2.06×10^{-5}, and 1.8×10^{-3} $\Omega\cdot\text{cm}^2$, respectively.

Fig. 9 shows the dc current–voltage characteristics of the fabricated 25- and 125-μm BJT, and Fig. 10 displays the Gummel plots for the same transistors. A peak dc current gain of 5.6 is observed for the 25-μm BJT, and a peak gain of 4.7

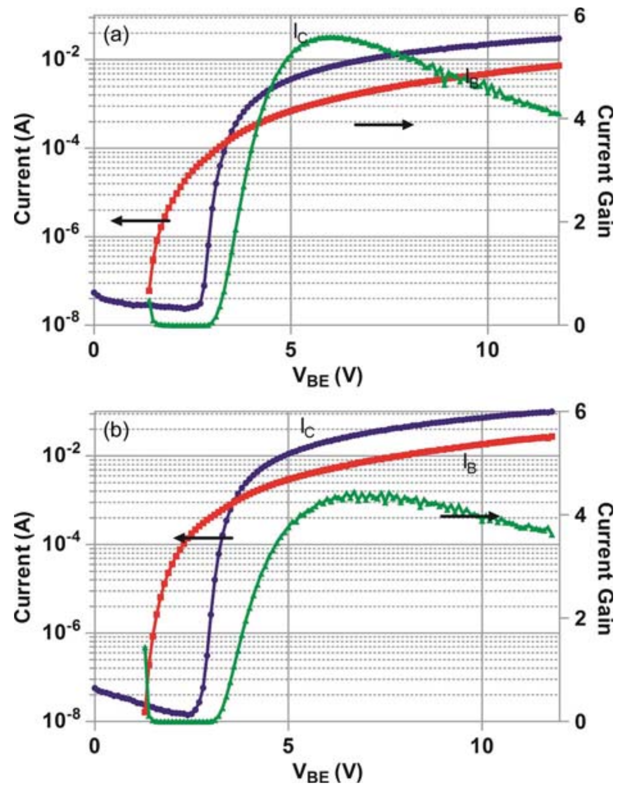

Fig. 10. Room-temperature Gummel plots for (a) the 25-μm BJT and (b) the 125-μm BJT.

is observed for the 125-μm BJT. These results are much lower than the value (~42) predicted by MEDICI simulations. The two transistors have similar current levels due to the similar current gains.

Current gain depends on a number of factors, including the doping and thickness of the base and the emitter, minority carrier lifetime in these regions, and surface recombination at the top of the base and sidewalls of the emitter. It is highly sensitive to surface recombination velocity, and the actual value may differ from the value assumed in the simulations. Surface recombination on the etched sidewalls at the emitter–base boundary plays a major role in determining the current gain, and its effects are well documented in the literature (specifically, current gain is inversely proportional to surface recombination).

The current gain may be limited by the quality of the SiC-SiO_2 interface. Recent studies have shown that passivation by dry oxidation in an N_2O ambient gives rise to high current gain in a BJT due to reduced surface recombination [22]. As calculated from the Gummel plots, the ideality factors for the base currents in our devices are ~2.9 for the 25-μm BJT and ~2.2 for the 125-μm BJT; such high ideality factors strongly suggest that the base current is dominated by recombination.

Another possible explanation for the low current gain is recombination in the implanted p+ base contact regions [18]. In the simulations, the electron and hole lifetimes were assumed to be 0.26 and 0.3 μs in all regions of the device. In the fabricated BJT, the lifetimes in the p+ implanted region will likely be much lower due to lattice damage caused by ion implantation. To investigate this, additional simulations were performed with dimensions, dopings, and contact resistances

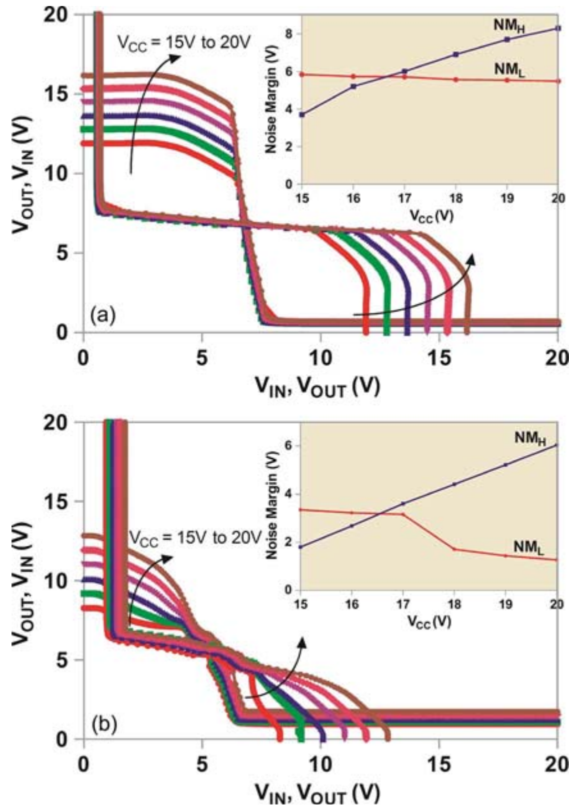

Fig. 11. VTC at room temperature as $V_{\rm CC}$ goes from 15 to 20 V for (a) the FO-1 inverter and (b) the FO-10 inverter. The inset shows the variation of noise margins with respect to $V_{\rm CC}$ for both inverters.

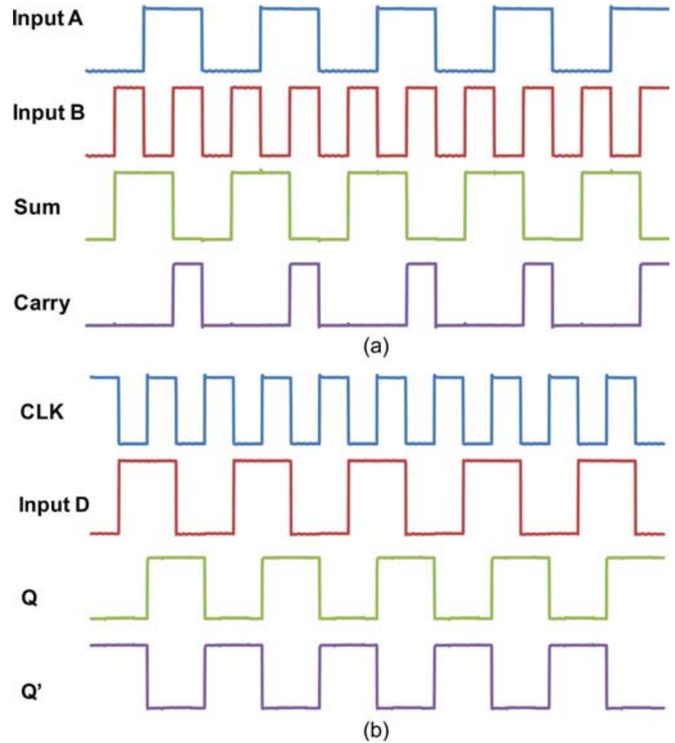

Fig. 12. Logical functionality of (a) the half adder and (b) the D flip-flop.

set to those measured in the fabricated BJT. It was noticed that, when the lifetime in the p+ implant region is reduced to 1.5 ns, the current gain decreases to $\sim$6. This suggests that base contact recombination alone may account for the low gain in the fabricated devices.

The low current gain may also be exacerbated by the "emitter size effect." This effect is caused by edge recombination that becomes dominant when the emitter area-to-periphery ratio decreases. Many studies have shown that, as the emitter width decreases, the gain also decreases [23]–[25]. Hence, for narrow emitter widths, it becomes much more important to improve the interface between SiC and $\rm SiO_2$. The width of the emitter in our BJTs is 7 μm, which is narrow enough for this effect to play a key role in limiting the current gain.

Fig. 11 shows the VTC at room temperature and different supply voltages for both FO-1 and FO-10 inverters. For both inverters, $V_{\rm OH}$ almost linearly increases with $V_{\rm CC}$, whereas $V_{\rm OL}$ only slightly increases. The inset in Fig. 11 shows the variation in noise margins with changing power supply voltage for both the inverters. As the power supply voltage is increased, the output-high noise margin NM_H almost linearly increases with $V_{\rm CC}$, whereas the output-low noise margin NM_L slightly decreases. For the FO-1 inverter, NM_H increases from 3.7 to 8.3 V, and NM_L decreases from 5.8 to 5.5 V, as $V_{\rm CC}$ goes from 15 to 20 V. For the FO-10 inverter, NM_H increases from 1.8 to 6 V, and NM_L decreases from 3.3 to 1.3 V, as $V_{\rm CC}$ goes from 15 V to 20 V. As apparent from the figure, both inverters exhibit adequate noise margins over the entire range of power supply voltages and are in good agreement with the simulated results.

All individual gates and demonstration ICs operate as expected. Fig. 12 illustrates the logical functionality of two such ICs, i.e., the half-adder and D flip-flop.

Device and circuit performance are evaluated at two elevated temperatures, i.e., 150 °C and 355 °C. In the case of BJT, for a fixed base current, the current gain decreases with increasing temperature. The measured peak current gain for the 25-μm transistor is 5.6 at 23 °C, 4.5 at 150 °C, and 3.8 at 355 °C. For the 125-μm transistor, the peak gain is 4.7 at 23 °C, 3.8 at 150 °C, and 2.8 at 355 °C. The decrease in gain is expected since SiC n-p-n BJTs have a negative temperature coefficient of current gain, which is caused by an increase in the ionization of aluminum acceptors in the base and reduced emitter injection efficiency [26], [27].

Fig. 13 displays the variation in noise margins for both inverters as a function of power supply voltage and temperature. For a given $V_{\rm CC}$, both the output-high voltage and output-low voltage increase with temperature. The increase in output-high voltage leads to an increase in NM_H, whereas the increase in output-low voltage leads to a decrease in NM_L. Fig. 14 demonstrates that the inverters still exhibit adequate noise margins, even at high temperatures, with the lowest noise margin being the NM_L of the F-10 inverter at 355 °C.

Propagation delay is measured using the 11-stage ring oscillator circuit. The ring oscillator consists of an odd number of inverters (11 in this case) in a circular chain, where the output of the last inverter is fed back in to the first inverter. Fig. 14 shows the output characteristic of the ring oscillator at $V_{\rm CC} = 20$ V at three temperatures. At room temperature, the ring oscillator exhibits high and low logic levels of about 14 and 0.4 V, respectively (13.6-V logic swing). The rise and fall times are determined to be 26 and 23 ns, respectively. The

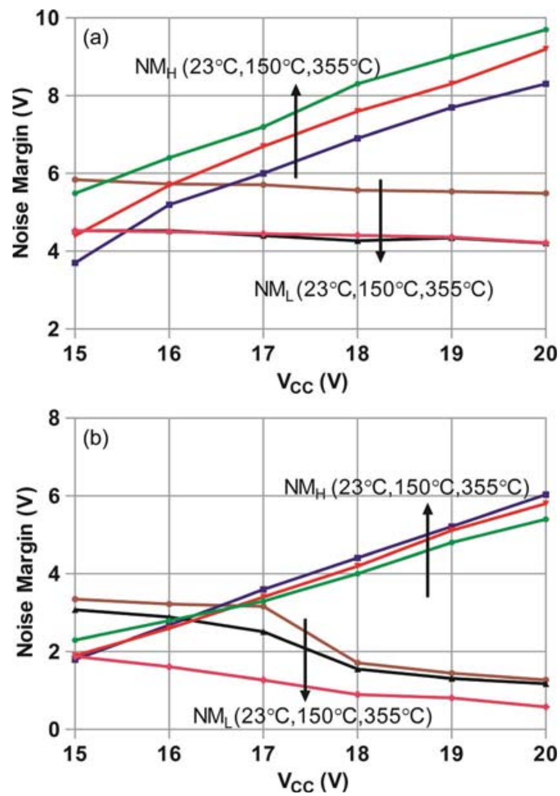

Fig. 13. Noise margins as V_{CC} goes from 15 to 20 V and at $T = 23$ °C, 150 °C, and 355 °C for (a) the FO-1 inverter and (b) the FO-10 inverter.

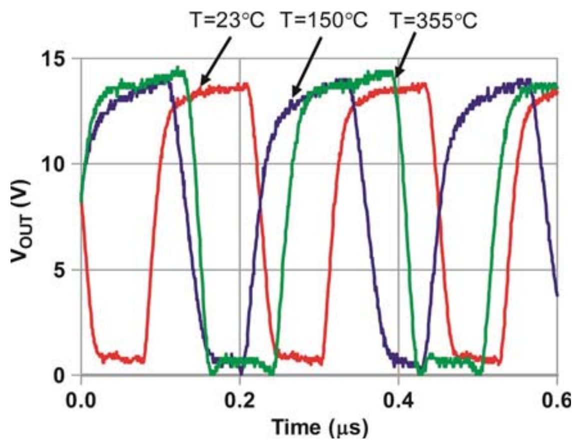

Fig. 14. Output characteristic of the 11-stage ring oscillator at three temperatures.

oscillation frequency of the oscillator is about 4.63 MHz, and the calculated stage delay is 9.8 ns at room temperature. The fabricated circuit runs about 3.3 times slower than predicted by SPICE. This discrepancy can be attributed to the low current gain in the fabricated devices. Current gain is an important parameter in determining how quickly base charge is removed from the BJT during switching. The value of current gain used in the simulation was 42, whereas the experimental value of current gain is only 5.6 and 4.7 for the 25- and 125-μm BJTs, respectively. A lower current gain increases the time for charge accumulation or removal. Hence, to speed up the circuits, it is imperative to have a higher current gain.

The delay almost linearly increases with temperature (9.8 ns at 23 °C, 10.3 ns at 150 °C, and 11.7 ns at 355 °C), and the oscillation is 19% slower at 355 °C than at room temperature. As stated earlier, current gain determines the speed of charge removal from the base, and since the current gain decreases with temperature, it is expected that the delay will increase.

In spite of the low current gain, these delays are comparable to those of silicon TTL circuits ($\sim$10 ns) and are an order of magnitude lower than our first 4H-SiC bipolar ICs [16]. The ring oscillator waveforms remain robust at high temperatures, demonstrating the potential of SiC bipolar ICs for small-scale high-temperature application.

V. Conclusion

In this paper, we have described the design and fabrication of second-generation 4H-SiC bipolar ICs and characterized their operation as a function of temperature and power supply voltage. All devices and circuits are functional over a range of supply voltages and temperature, in spite of low current gains. We attribute the low current gain to a high surface recombination and short minority carrier lifetime in the implanted p+base contact regions, in combination with narrow emitter fingers (emitter size effect). Propagation delays are an order-of magnitude lower than the best previous results and compare well with those of silicon TTL. Further investigations are required to establish the long-term stability and reliability of this technology.

Acknowledgment

The authors would like to thank Dr. J.-Y. Lee for valuable technical advice and Dr. K. Matocha of GE Global Research for deposition of the intermediate-layer dielectrics.

References

[1] J. W. Palmour, R. Singh, R. C. Glass, O. Kordina, and C. H. Carter, Jr., "Silicon carbide for power devices," in *Proc. IC's-ISPSD*, May 26–29, 1997, pp. 25–32.

[2] P. G. Neudeck and C. Fazi, "Positive temperature coefficient of breakdown voltage in 4H-SiC pn junction rectifiers," *IEEE Electron Device Lett.*, vol. 18, no. 3, pp. 96–98, Mar. 1997.

[3] C. M. Johnson, N. G. Wright, M. J. Uren, K. P. Hilton, M. Rahimo, D. A. Hinchley, A. P. Knights, D. J. Morrison, A. B. Horsfall, S. Ortolland, and A. G. O'Neill, "Recent progress and current issues in SiC semiconductor devices for power applications," *Proc. Inst. Elect. Eng.—Circuits Devices Syst.*, vol. 148, no. 2, pp. 101–108, Apr. 2001.

[4] P. G. Neudeck, "Progress towards high temperature, high power SiC devices," in *Institute of Physics Conference Series: Compound Semiconductors 1994*, H. Goronkin and U. Mishra, Eds. Bristol, U.K.: IOP Publishing, 1995, pp. 1–6.

[5] J. J. Liou and A. Kager, "Theoretical prediction of the performance of Si and SiC bipolar transistors operating at high temperatures," *Proc. Inst. Elect. Eng.—Circuits Devices Syst.*, vol. 140, no. 4, pp. 289–293, Aug. 1993.

[6] W. V. Müench and E. Pettenpaul, "Saturated electron drift velocity in 6H silicon carbide," *J. Appl. Phys.*, vol. 48, no. 11, pp. 4823–4825, Nov. 1977.

[7] I. A. Khan and J. A. Cooper, Jr., "Measurement of high-electron transport in silicon carbide," *IEEE Trans. Electron Devices*, vol. 47, no. 2, pp. 269–273, Feb. 2000.

[8] M. M. Maranowski and J. A. Cooper, Jr., "Time-dependent-dielectric-breakdown measurements of thermal oxides on n-type 6H-SiC," *IEEE Trans. Electron Devices*, vol. 46, no. 3, pp. 520–524, Mar. 1999.

[9] L. C. Yu, G. T. Dunne, K. S. Mathocha, K. P. Cheung, J. S. Suehle, and K. Sheng, "Reliability issues of SiC MOSFETs: A technology for high temperature environments," *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 4, pp. 418–426, Sep. 2010.

[10] K. Matocha, P. Losee, A. Gowda, E. Delgado, G. Dunne, R. Beaupre, and L. Stevanovic, "Performance and reliability of SiC MOSFETs for high-current power modules," in *Proc. 13th ICSCRM*, Nuremberg, Germany, Oct. 11–16, 2009, pp. 1123–1126.

[11] M. Le-Huu, F. F. Schrey, M. Grieb, H. Schmitt, V. Häublein, A. J. Bauer, H. Ryssel, and L. Frey, "NMOS logic circuits using 4H-SiC MOSFETs for high temperature applications," in *Proc. 13th ICSCRM*, Nuremberg, Germany, Oct. 11–16, 2009, pp. 1143–1146.

[12] A. Agarwal, S. Krishnaswami, J. Richmond, C. Capell, S. H. Ryu, J. Palmour, B. Geil, D. Katsis, C. Scozzie, and R. E. Stahlbush, "Influence of basal plane dislocation induced stacking faults on the current gain in SiC BJTs," in *Proc. ICSCRM*, Pittsburgh, PA, Sep. 18–23, 2005, pp. 1409–1412.

[13] L. Farese, G. Malm, M. Domeij, and M. Östling, "Experimental study of degradation in 4H-SiC BJTs by means of electrical characterization and electroluminescence," in *Proc. 13th ICSCRM*, Nuremberg, Germany, Oct. 11–16, 2009, pp. 1037–1040.

[14] Y. Gao, A. Q. Huang, Q. Zhang, S. Krishnaswami, and A. K. Agarwal, "Analysis of operational degradation of SiC BJT characteristics," in *Proc. 19th IC's-ISPSD*, May 27–31, 2007, pp. 121–124.

[15] A. O. Konstantinov, M. Domeij, C. Zaring, I. Keri, J. O. Svedberg, K. Gumaelius, M. Östling, and M. Reimark, "Operation of silicon carbide BJTs free from bipolar degradation," in *Proc. 13th ICSCRM*, Nuremberg, Germany, Oct. 11–16, 2009, pp. 1057–1060.

[16] J.-Y. Lee, S. Singh, and J. A. Cooper, "Demonstration and characterization of bipolar monolithic integrated circuits in 4H-SiC," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1946–1953, Aug. 2008.

[17] *Medici Two-Dimensional Device Simulation program User Manual*, version 2002.4, Synopsis Inc., Mountain View, CA, Feb. 2003.

[18] C.-F. Huang and J. A. Cooper, Jr., "High current gain 4H-SiC NPN bipolar junction transistors," *IEEE Electron Device Lett.*, vol. 24, no. 6, pp. 396–398, Jun. 2003.

[19] L. W. Nagel, "SPICE2: A program to simulate semiconductor circuits," Univ. California, Berkeley, CA, Memo UCB/ERL M520, 1975.

[20] S. Singh, "High-performance TTL bipolar integrated circuits in 4H-SiC," Ph.D. dissertation, School of Elect. Comput. Eng., Purdue Univ., West Lafayette, IN, 2010.

[21] C.-Y. Lu, J. A. Cooper, T. Tsuji, G. Y. Chung, J. R. Williams, K. McDonald, and L. C. Feldman, "Effect of process variations and ambient temperature on electron mobility at the SiO_2/4H-SiC interface," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1582–1588, Jul. 2003.

[22] H.-S. Lee, M. Domeij, C.-M. Zetterling, M. Ostling, F. Allerstam, and E. O. Sveinbjornsson, "Surface passivation oxide effects on the current gain of 4H-SiC bipolar junction transistors," *Appl. Phys. Lett.*, vol. 92, no. 8, pp. 082 113-1–082 113-3, Feb. 2008.

[23] Y. Gao, A. Q. Huang, S. Krishnaswami, A. K. Agarwal, and C. Scozzie, "Emitter size effect in 4H-SiC BJT," in *Proc. CES/IEEE 5th IPEMC*, Aug. 14–16, 2006, vol. 1, pp. 1–4.

[24] W. Liu and J. S. Harris, "Diode ideality factor for surface recombination current in AlGaAs/GaAs heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 39, no. 12, pp. 2726–2732, Dec. 1992.

[25] M. Domeij, H.-S. Lee, E. Danielsson, C.-M. Zetterling, M. Ostling, and A. Schoner, "Geometrical effects in high current gain 1100-V 4H-SiC BJTs," *IEEE Electron Device Lett.*, vol. 26, no. 10, pp. 743–745, Oct. 2005.

[26] S.-H. Ryu, A. K. Agawal, R. Singh, and J. W. Palmour, "1800 V NPN bipolar junction transistors in 4H-SiC," *IEEE Electron Device Lett.*, vol. 22, no. 3, pp. 124–126, Mar. 2001.

[27] Y. Tang, J. B. Fedison, and T. P. Chow, "An implanted-emitter 4H-SiC bipolar transistor with high current gain," *IEEE Electron Device Lett.*, vol. 22, no. 3, pp. 119–120, Mar. 2001.

Shakti Singh received the B.S., M.S., and Ph.D. degrees in electrical and computer engineering from Purdue University, West Lafayette, IN, in 2000, 2003, and 2010, respectively, specializing in electronic devices in wide band-gap semiconductors, particularly silicon carbide.

He is currently an Assistant Professor of electronic engineering with Khalifa University of Science, Technology, and Research, Abu Dhabi, UAE.

James A. Cooper (S'66–M'69–SM'85–F'93) received the Ph.D. degree from Purdue University, West Lafayette, IN, in 1973.

From 1973 to 1983, he was a member of the technical staff with Bell Laboratories, Murray Hill, NJ, where he was the Principal Designer of AT&T's first microprocessor and investigated the nonlinear transport in silicon inversion layers. Since 1983, he has been with the faculty of Purdue University, where he is currently the Jai N. Gupta Professor of electrical and computer engineering. From 2001 to 2006, he served as the Founding Codirector of Birck Nanotechnology Center in Purdue University's Discovery Park. His research at Purdue University has centered on semiconductor device physics and characterization, focusing primarily on III-V materials and silicon carbide. His group pioneered the development of the SiC double-diffused metal–oxide–semiconductor (DMOS) power transistors and developed the process currently used for self-aligned short-channel power DMOS field-effect transistors. He has coauthored over 250 technical papers and conference presentations and five book chapters. He is the holder of 14 U.S. patents. He has graduated 26 Ph.D. and 10 M.S. thesis students. He served as the Associate Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES from 1983 to 1986, as a Guest Editor of the 1999 and 2008 special issues of the IEEE TRANSACTIONS ON ELECTRON DEVICES, and as a member of the editorial board of the *IEEE Proceedings* from 2004 to 2009.