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Bipolar ReRAM Based Non-Volatile Flip-flops for Low-Power Architectures

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***Abstract*—Resistive Random Access Memories (ReRAMs) fabricated in the back-end-of-line are a promising breakthrough for including permanent retention mechanisms in embedded systems. This low-cost solution opens the way to advanced power management schemes. In this paper, we propose novel design architecture of a non-volatile flip-flop based on Bipolar ReRAMs (Bi-RNVFF). Compared to state-of-the-art Data-Retention flip-flop (with Balloon latch), the proposed design is 25% smaller due to 6T structure compared to the 8T structure of Data-Retention flip-flop. Moreover, being non-volatile, the proposed architecture exhibits a zero leakage. Whereas, Data-Retention Flip-Flop consume ~3.2µW in sleep mode (leakage) for a 10K Flip-Flop design implemented in 22nm FDSOI technology. Our simulation results show that Bi-RNVFF is a true alternative for future Low power applications adding Non-Volatility without significant burdening of the existing architectures.**

I. INTRODUCTION

Ultra low power circuits are mandatory for next-generation mobile applications. Many design techniques have been deployed to reduce dynamic power consumption at all the levels: clock-gating at design-time, gate sizing, multi-V_T transistors and body biasing at implementation-time, voltage and frequency scaling when the application is running [1]. However, advanced technologies, used for high-performance processing units, exhibit significant power dissipation in idle/standby modes due to high current leakage, which can be up to ~40% of active mode energy [2][3] in idle circuits. To overcome this issue, local power gating has been introduced [4]. However, when sub-circuits are powered down, the data saved in the local registers (Flip-Flops) are lost. The subsequent power budget for saving/restoring this information limits this energy saving strategy in applications with long idle periods. This issue currently has been addressed using data-retention flip-flop known as Balloon Flip-Flop consisting of high-V_{th} transistors based retention cell (balloon latch) connected to the slave stage of a flip-flop. The schematic of the data-retention flip-flop using balloon latch is reproduced from [5] in Fig 1. In this architecture the Sleep Control signal transition to low disconnects the FF from ground. The recent data at the slave latch is latched on to balloon latch consisting of high-V_{th} cross-coupled inverters with constant power supply and ground network. Considering a 10K flip-flops design, with a low-power FDSOI 22nm Technology, a small but significant power of ~3.2µW is consumed.The integration of Non-Volatile Flip-Flop (NVFF) in SoC (System on Chip) is a novel solution to overcome the virtual ground line leakage. Recent studies have explored the possibility to introduce non-volatility as distributed memory cells. The solutions have used different technologies, such as:

- FeRAM, which present fast timing but a limited scalability [6].
- MRAM, with fast timing but presents some major challenges with respect to integration due to the complexity of the MRAM stack [7] [8].
- Unipolar ReRAMs is reported in [9], however this solution is limited due to instability in switching characteristics [10] at present maturity of technology.

In this work, we propose a new Non-Volatile Flip-Flop based on Bipolar Oxide Resistive switching (Bi-RNVFF for Bipolar

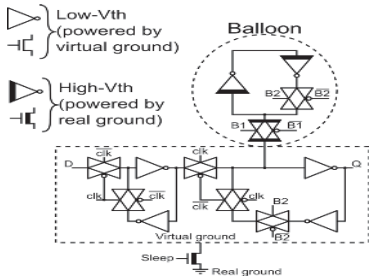

Figure 1: Architecture of Data-Retention Flip-Flop with Balloon Latch used with power gating technique (redrawn from [5])

ReRAM NVFF). This design solution takes full benefit of technology development, i.e. simple ReRAM material stack

compatible with standard CMOS materials combined with low-power advanced CMOS process of Fully Depleted Silicon on Insulator (FDSOI). The content of this paper is organized as follows; a brief overview of the Bipolar ReRAM technology and compact model used to realize the design of the Bi-NVFF is explained in section II, section III presents the proposed new architecture description and operation. Section IV presents simulation results. We conclude with Results and discussion.

II. Bipolar Oxide-Based Resistive RAM

A. *Bipolar ReRAM Technology*

Resistive switching phenomenon is observed in several transition metal oxides such as TiO_2, HfO2 CuxO, NiO, ZnO and some perovskite oxides. Two distinct states exist namely: A High Resistance State (HRS) and a Low Resistance State (LRS)- which initially attained with a high voltage forming process on a pristine device ($V_{forming} > V_{set}$), leading to subsequent reversible HRS to LRS switching at V_{set} and LRS-to-HRS at V_{reset}. Fig 2. shows the integration scheme of this new device in BEOL of CMOS process flow. The relatively simple device structure compatible with the traditional CMOS process flow, high scalability and fast operating speeds are some of the advantages in favor of ReRAMs [11].

B. *Compact Model Based on Self-Consistent Physical Model*

The Bipolar ReRAM is modeled through physical mechanisms used for set and reset operations in the devices. The electric field-induced migration of oxygen vacancies within the switching layer is the broadly accepted physical phenomenon in these devices [12] [13]. The compact model used for simulations accounts for both set and reset operations embedded into a single equation, which modulates resistance based on the diameter (φ) of the conduction pathways in the oxide given by:

$$\frac{d\varphi}{dt} = \frac{\varphi_{max} - \varphi}{\tau} e^{-\frac{E_a - q.\alpha.V_{cell}}{\kappa_b.T}} - \frac{\varphi}{\tau} e^{-\frac{E_a - q.\alpha.V_{cell}}{\kappa_b.T}} \qquad (1)$$

Where τ represents the creation/destruction rate, E_a the activation energy and V_{cell} the cell voltage. This model is verified with quasi-static and dynamic experimental data correlation before implementation in electrical circuit simulators. The model is calibrated to experimental data of [14] consisting of material stack (TiN(25nm)/HfO_2(10nm)/ Ti(10nm) / TiN(50nm). The Fig. 3a validates a good matching between experimental I-V curves and the simulation of the model. To program a bipolar ReRAM cell, a voltage ramp is needed. To perform a realistic circuit analysis, an important requirement of the model is to take in account the dynamics of the programming signals. Experimental data show a variation in the set voltage for various ramp rates and the model accounts for this observation. Fig. 3b shows the evolution of the set voltage V_{set} as a function of the ramp speed and the simulated results. This plays an important role in choosing the right ramp speeds to confine the voltage regimes allowed for a given technology through Process Design Kit (PDK). For example, in our case the PDK supports up to 1.2V for logic operation. Hence using this result (Fig. 3b) we can deduce the ramp speeds at which we should operate to faithfully set at 1.2V.

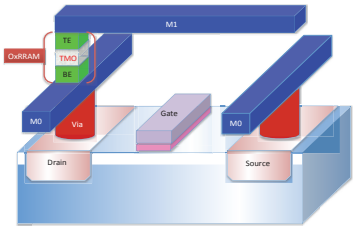

Figure 2. Schematic showing ReRAM device in BEOL. The OxRERAM consists of Metal-Insulator-Metal (MIM) structure with Transition Metal Oxide (TMO) sandwiched between Top Electrode (TE) and Bottom Electrode (BE) contacts. It is co-habitat with a via in Back End of Line (BEOL) integrated with Front Of Line (FEOL) select transistor in a standard CMOS process flow

III. Bi-NVFF Architecture, Design and Operating Principal

Using the ReRAM compact model described in the previous section a new Flip-Flop architecture is simulated. The basic idea distills down to using two Bipolar Oxide ReRAMs along with control transistors together called NVM_L and NVM_R in the Flip-Flop as shown in Fig. 4: the non-volatile elements are connected in the slave part of the classical Flip-Flop structure. Each NVM block consists of three transistors for controlled programming of ReRAM. The transistors sandwiching the ReRAM also enable to impose

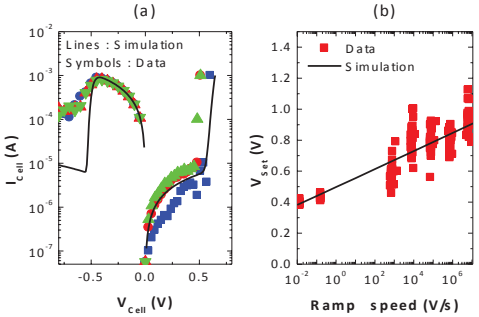

Figure 3. (a) I-V characteristic measured on actual devices [14] and corresponding simulation using a bipolar physical model. (b) Set voltage as a function of the programming ramp [14].

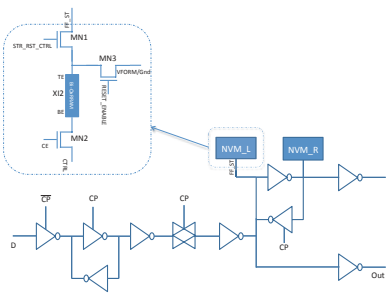

Figure 4: Bi-RNVFF architecture with non-volatile block based on ReRAM with ReRAMs in slave state.

compliance current limit on the memory cell.

A. Operating Principal

The sequence of operations followed for successful operation of this architecture is as described in Fig. 5. The operation follows phases namely: Normal Operation, Save, Restore and Reset of ReRAMs.

1) Normal Operation

This mode is the classical operation of master slave Flip-Flop, where the data on the input is latched in the master stage at active low clock signal and in the subsequent transition of the clock is pushed on to the slave of the Flip-Flop to be available at the output. During this phase of the operation all the control signals (STR_RST_CTRL, CE, RESET_ENABLE, CTRL) governing the NVM blocks are disabled hence the NVM blocks are completely isolated and

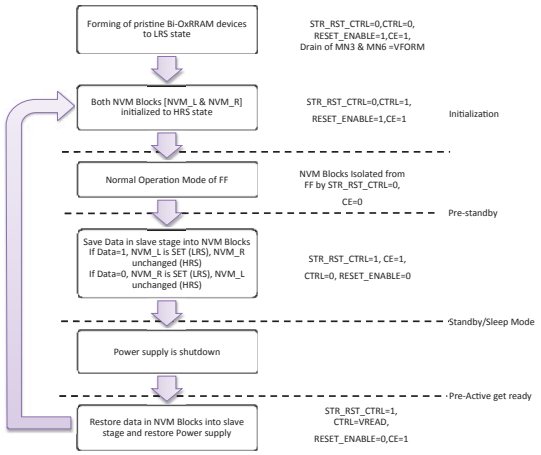

Figure 5: Sequential flow of operations required for transitions between Normal and Sleep/Standby Modes with Bi-NVFF.

ReRAMs remain in their HRS state.

2) Save Operation

This operation is initiated by the control signals STR_RST_CTRL ='1',CE ='1' and CTRL ='0' guiding logic state present in the slave latch on to the ReRAMs, for example: when slave has latched a '1' the ReRAM in NVM__L block is SET (LRS state), since a positive bias is applied between its top (TE in Fig. 2) and bottom (BE in Fig. 2) electrodes. The NVM_R block remains unchanged (HRS state) since the voltage applied between TE and BE is equal to 0V. In essence the NVM_L in LRS state and NVM_R in HRS state together representing the logic state of '1' faithfully saved into NVM blocks. Following the completion of this event the Flip-Flop can be completely powered-down owing to the information stored in Non-Volatile Memories.

3) Restore and Reset Operation

During Restore, using control signals STR_RST_CTRL='1', CE ='1', CTRL ='1' and RESET_ENABLE ='0' the logic is restored into the slave latch for resumption of Normal Operation accompanied by the V_{DD} restoration to normal value. This is in effect a read operation on the ReRAM. The presence of complementary logic of the NVM_L and NVM_R assists the acceleration of logic restoration process onto the slave stage. The restoration phase is followed by resetting of both the NVM blocks using control signals STR_RST_CTRL='0', CE='1', CTRL='1' and RESET_ENABLE ='1', wherein both the NVM blocks are applied with a negative bias between their top and bottom electrodes driving both the ReRAMs to HRS state.

IV. Simulation Results and Discussion

To validate the Bi-RNVFF functionality, the full structure is simulated under electrical simulator using a CMOS-FDSOI 22nm Low Power design kit and the bipolar model fitted to Resistive RAM devices described in [14]. V_{DD} is nominal for the technology and is set to 1.2V during all modes of operation except during power-off when it is brought down to 0V. All modes of operation are simulated for input value of D='1' and D='0'. The complete timing diagrams for the case of input D=1 is shown in Fig. 6.

As stated in Fig. 5, the path between transistor MN3, ReRAM and transistor MN2 is employed to perform forming of pristine ReRAM, which imposes their sizing (forming demands high current surge but is performed only once).

A. Timing Metrics

The basic Flip-Flop timing parameters are *clock-to-output* (*Clk-Q*) delay, *setup* and *hold* times. These parameters indicate the system-level performance termed as Flip-Flop delay (also known as *Latency*) and *internal race immunity*. The *Clk-Q* delay is the delay measured from active clock edge to the output. *Setup* and *hold* times are defined as data to clock offsets that correspond to a *10%* increase in the *Clk-Q* delay from its nominal or stable delay as shown in Fig. 7. The setup and hold time values of the standard FF (without Balloon), Balloon FF (Fig. 1) and Bi-NVFF (Fig. 4) are tabulated in Table I. An input and output transition constraints of 4ps (0-100%) and an output load of 0.43fF have been used to obtain these values. The values show that there is feeble degradation due to the cumulative capacitances of the additional transistors in Balloon FF and Bi-NVFF compared to Standard FF. But the values of Bi-NVFF are still comparable to standard FF and lower than Balloon FF.

B. Power and Area impact

For performing a fair comparison, we used the same FDSOI technology used for our structure with the design proposed in the Fig. 1. When the balloon latch is switched to sleep mode we obtained a leakage current of 0.33nA through sleep transistor. This value is small due to state-of-the-art FDSOI technology used that minimizes the leakage. When we extrapolate this to a reasonable design of 10K FF design, it results in leakage power of ~3.2μW, which is significant, compared to *zero* for the proposed solution. The proposed solution [6T] alleviates the silicon-footprint by 25% compared to a balloon latch of 8T. Since the ReRAMs occupy the non-active BEOL of the real estate. The current limitation of the proposed design is due to the ramp speed, which leads to higher power consumption during the set and reset operations, compared to balloon latch. However, these operations will be performed rarely compared to the idle time duration in mobile applications.

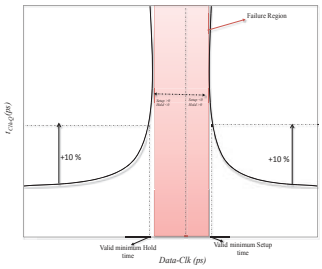

Figure 7: Definition for setup and hold times [15].

Table I. Timing Metrics under Normal Operation of FFs

Circuit Technique	*Clk-Q Delay* [a] *(ps)*	*Setup* [a] *(ps)*	*Hold* [a] *(ps)*
Standard FF	42.473	8.9895	-3.1
Balloon FF	45.677	10.4	-2.95
Bi-NVFF	43.057	9.5225	-3.05

a) C load =0.431F and rise and fall constraints of 4ps (0=100%) on *D* and *Clk*

V. CONCLUSION

This work presented a novel architecture of NVFF using Bi-ReRAMs for the first time. The complete structure was validated in CMOS 22nm FDSOI technology for all the operating scenarios (forming, save and restore). The proposed design reduces a) area over-head by 25% when compared with Balloon Flip-Flop solution b) the stand-by leakage power to zero, c) comparable timing metrics and d) adds Non-Volatility. Applications with long idle modes and fast recovery requirements can have high power benefits when using the proposed technological solution.

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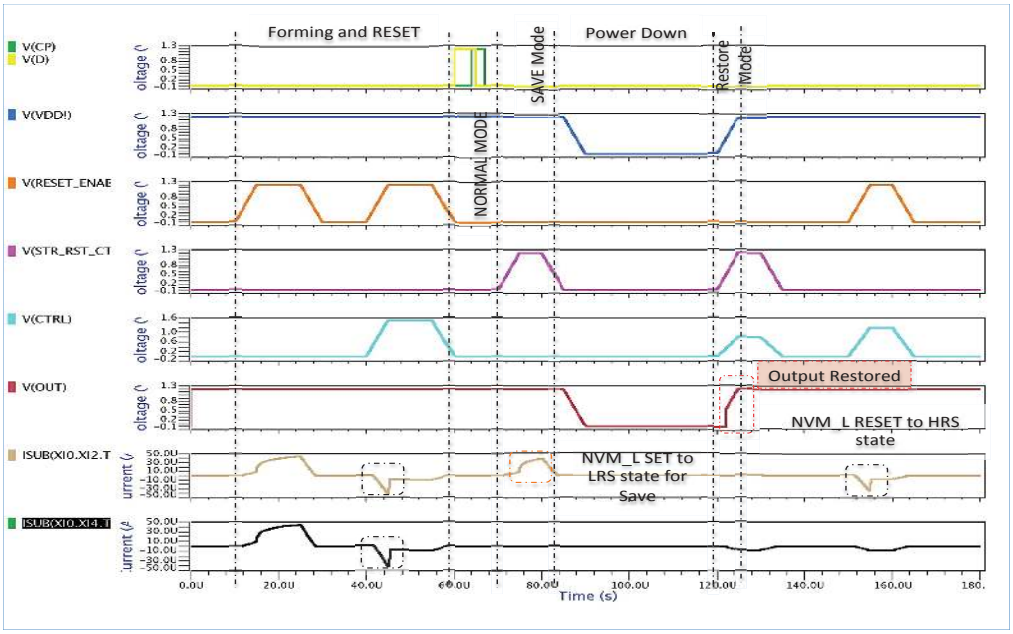

Figure 6: Bi-RNVFF architecture with Non-volatile block based on ReRAM with ReRAMs in slave state for Data = 1