# Bit-stream signal processing and its application to communication systems

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**Abstract:** The paper describes a digital circuit technique to process directly bit-stream signals from sigma–delta modulation based analogue-to-digital converters and the application of the technique to communication systems. The newly developed adder and multiplier are fundamental processing circuit modules. Using the fundamental modules and up/down counters, other circuit modules, such as oscillators, dividers and square root circuits, can also be realised. Signal processors built from the modules have three advantages over multi-bit Nyquist rate processors. First, single-bit/multibit converters are not needed at the inputs of the processors because the arithmetic modules directly process the bit-stream signals. Secondly, the physical areas for routing the signals among the circuit modules are small since they are in the form of a bit-stream. Thirdly, the processors are built from a smaller number of logic gates than conventional Nyquist rate processors because of the simple structure of the circuit modules. As an application of the technique to digital signal processing for communications, a QPSK demodulator is presented. In addition to circuit simulations of the demodulator, a useful linear analysis to estimate the influence of the noise components contained in the outputs from the circuit modules on the steady-state demodulation performance is explained.

## 1 Introduction

Sigma–delta ($\Sigma\Delta$) modulation has become a popular technique for analogue-to-digital (A/D) and digital-to-analogue (D/A) conversion in recent years. This is because $\Sigma\Delta$ modulator circuits are structured simply with low-accuracy analogue parts. The $\Sigma\Delta$ modulated single-bit or short-bit signals are converted into multibit signals at the inputs of conventional digital signal processors (DSP) at the Nyquist sampling rate. Thus, currently usable types of digital systems with $\Sigma\Delta$ based A/D and D/A converters need single-bit/multibit conversion hardware including decimation and interpolation circuits. In the DSP block, large numbers of logic gates are used for multibit arithmetic circuits, especially multipliers. Moreover, multibit signal lines occupy large routing areas. Therefore, the DSP systems must be implemented on large and high-cost LSI chips.

To reduce logic gates and routing areas, approaches have been proposed for specific-purpose signal processing. One of these is for IIR digital filters [1]. In the filters every multibit multiplier is replaced by a $\Sigma\Delta$ modulator and a sign-reverse circuit to perform bit-stream conversion and multiplication of the bit-stream signal by a multibit coefficient. Digital neural networks using pulse density or pulse width modulation [2] are other examples of simplified signal processing circuits for pattern recognition or classification. These approaches are useful for their specific applications but are not always available directly for different applications. On the other hand, bit-serial architecture has been employed in various kinds of digital signal processors for many years to save logic gates. However, it is not easy to schedule efficiently the sequence of operating modes of each circuit module in systems tasked to carry out sophisticated processing.

This paper describes a digital circuit technique for DSP hardware and its application to communication systems. The circuit technique is called bit-stream signal processing (BSSP) in this paper. In BSSP systems signals are represented in the form of a single-bit stream. The bit-stream signals are directly supplied to and obtained from novel arithmetic circuits without being converted into multibit signals. Thus, decimation after $\Sigma\Delta$-based A/D conversion and interpolation before $\Sigma\Delta$ based D/A conversion are unnecessary. Furthermore, the arithmetic circuits can be built from a small number of logic gates. Therefore, the BSSP technique reduces both signal routing areas and logic gates.

## 2 Fundamental arithmetic circuits

### 2.1 Bit-stream adder

The adder performs the following operation for two $\Sigma\Delta$ modulated bit-stream signals $x(n)$, $y(n)$ $(= \pm 1)$, $n$: time index:

$$z(n) = \begin{cases} (x(n) + y(n))/2 & \text{if } x(n) = y(n) \\ q(n) & \text{if } x(n) \neq y(n) \end{cases} \quad (1)$$

where $q(n)$ $(= \pm 1)$ is a single-bit state in the adder, changing every time when $x(n) \neq y(n)$, i.e.

$$q(n) = \begin{cases} q(n-1) & \text{if } x(n) = y(n) \\ -q(n-1) & \text{if } x(n) \neq y(n) \end{cases} \quad (2)$$



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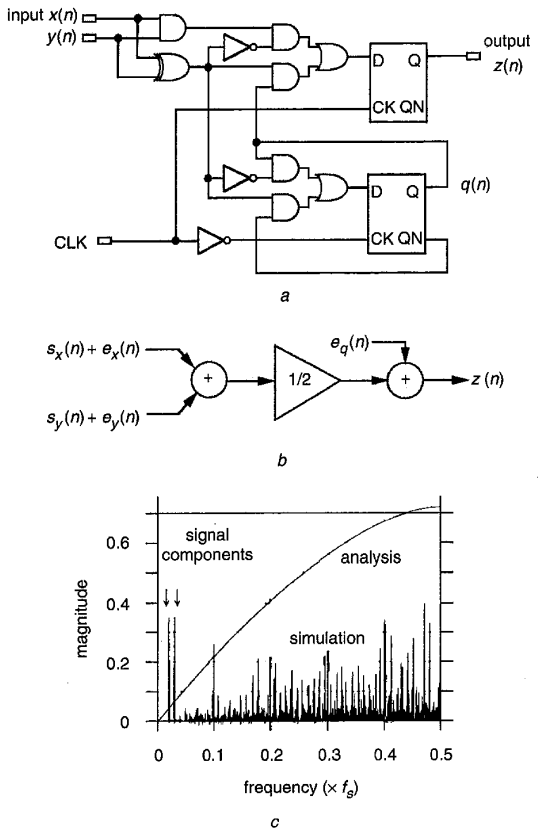


**Fig. 1** *Bit-stream adder*
*a* Circuit
*b* Equivalent model
*c* Output spectral density

Then, the sum $z(n)$ is a bit-stream output taking values $+1$ or $-1$. Fig. 1*a* shows a digital circuit realisation of (1) and (2). High and low levels of signals in the circuit correspond to $+1$ and $-1$.

Fig. 1*b* shows an equivalent circuit of the adder. Input signals $x(n)$, $y(n)$ are composed of pure signal components $s_x(n)$, $s_y(n)$ and $\Sigma\Delta$ modulation noise $e_x(n)$, $e_y(n)$, that is

$$\begin{aligned} x(n) &= s_x(n) + e_x(n) \\ y(n) &= s_y(n) + e_y(n) \end{aligned} \tag{3}$$

Another noise source $e_q(n)$ generated by the action of $q(n)$ is a bipolar signal given by

$$e_q(n) = \begin{cases} 0 & \text{if } x(n) = y(n) \\ q(n) & \text{if } x(n) \neq y(n) \end{cases} \tag{4}$$

First, consider the spectral density $E(\omega)$ of the modulation noise components $e_x(n)$, $e_y(n)$. According to [3], it is obtained by the following approximate equation when the inputs are modulated by first-order $\Sigma\Delta$ loops with two-level quantisation $\pm\delta/2$ and the quantisation error is treated as white noise having equal probability of lying anywhere in the range $\pm\delta/2$:

$$E(\omega) = 2e_{rms}\sqrt{\frac{2}{f_s}}\sin\left(\frac{\omega}{2f_s}\right), \quad e_{rms} = \delta/\sqrt{12} \tag{5}$$

where $\delta$ is quantisation spacing and $f_s$ is sampling frequency Secondly, consider the power spectrum density (PSD) of the bipolar noise $e_q(n)$. Suppose that the signal components $s_x(n)$, $s_y(n)$ are slowly varying and their magnitudes are less than $\delta/2$. Then, the probability that $x(n) = y(n)$ at time index $n$ is given by

$$p_q(n) = \frac{1}{2}\left(\frac{2s_x(n)}{\delta}\frac{2s_y(n)}{\delta} + 1\right) \tag{6}$$

From (2) and (4), it is found that $e_q(n)$ cannot be equal to $e_q(n-m)$ when they are not zero and $e_q(n-i) = 0$ for all $i \in \{i \mid 1 \leq i < m,\ m \geq 1\}$. Therefore, the auto-correlation $r(m)$ of $e_q(n)$

$$r(m) = \frac{1}{N}\sum_{n=0}^{N-1} e_q(n)e_q(n-m), \quad \begin{matrix} N\text{: long time interval} \\ \text{(integer)} \end{matrix} \tag{7}$$

can be represented as follows:

$$r(0) = \frac{1}{N}\sum_{n=0}^{N-1}(1 - p_q(n))$$

$$r(1) = -\frac{1}{N}\sum_{n=0}^{N-1}(1 - p_q(n))(1 - p_q(n-1)) \tag{8}$$

$$r(m) = -\frac{1}{N}\sum_{n=0}^{N-1}\left\{(1 - p_q(n))\left[\prod_{i=1}^{m-1}(2p_q(n-i) - 1)\right](1 - p_q(n-m))\right\}, \quad m \geq 2$$

The PSD of $e_q(n)$ is obtained by the Fourier transform of (8). Since the correlation $r(m)$ is considered to be an even function with respect to $m$, the PSD is represented as follows:

$$R(\omega) = r(0) + 2\sum_{m=1}^{\infty} r(m)\cos(\omega m/f_s) \tag{9}$$

Then, the PSD $P_a(\omega)$ of the total noise in the output signal $z(n)$ is computed by summing (5) and (9),

$$P_a(\omega) = R(\omega) + |E(\omega)|^2/2 \tag{10}$$

Fig. 1*c* shows the output spectral density obtained both by the analytical method and by circuit simulation. Input signal components $s_x(n)$, $s_y(n)$ are sinusoidal waves $0.02f_s$ and $0.03f_s$ in frequency and $0.7 \times (\delta/2)$ in amplitude. The analytical method estimates the output noise to be larger than the result of the circuit simulation due to the assumption that the input signal components vary slowly enough for (6) and (8) to be satisfied, and due to the rough approximation (5) of the spectral density of the input noise $e_x(n)$, $e_y(n)$.

## 2.2 Bit-stream multiplier

One of the representations of the arithmetic product of two bit-stream signals $x(n)$ and $y(n)$ is given by

$$\left[\frac{1}{L}\sum_{i=n-L+1}^{n} x(i)\right]\left[\frac{1}{L}\sum_{j=n-L+1}^{n} y(j)\right] \tag{11}$$

where $L$ (integer) is a time interval. Direct computation of the expression, however, requires a multibit multiplier. In order for the multibit multiplier to be removed, the multiplication is considered as follows: let (11) be expanded as

$$\frac{1}{L^2}\sum_{i,j=n-L+1}^{n} x(i)y(j) \tag{12}$$

Exclusive-OR gates are applied to the multiplication of the signal levels of bit-streams $x(i)$ at time $i$ and $y(j)$ at $j$, and previously introduced bit-stream adders to the summation of the subproducts $x(i)y(j)$. The circuit computing (12) is shown in Fig. 2*a* for $L = 4$. The total number of logic gates needed for the multiplier is about 400. It is almost equal in circuit scale to a 6-bit parallel multiplier.

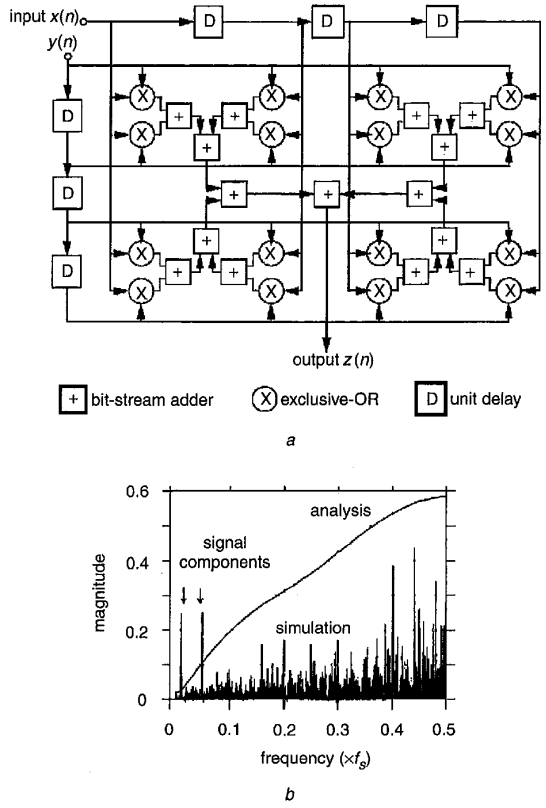


**Fig. 2** *Bit-stream multiplier*
*a* Block diagram
*b* Output spectral density

Next, we estimate the noise contained in the output signal using the equivalent model of the adder circuit shown in Fig. 1*b*. The average values of all the inputs to the adders used in the multiplier are assumed to be $s_x(n)s_y(n)$ around time $n$ because every adder outputs half of the sum of the two input signals, and their signal components $s_x(n)$, $s_y(n)$ vary slowly. Then, the PSD $R(\omega)$ of the bipolar noise $e_q(n)$ in all the adders is obtained identically. With the further assumption that the bipolar noise $e_q(n)$ in each adder is independent of the bipolar noises in other adders, we can estimate the PSD $P_{m,q}(\omega)$ of the output noise component which is attributed to the actions of the states $q(n)$ in all adders as follows:

$$P_{m,q}(\omega) = R(\omega) \sum_{k=0}^{2M-1} \frac{1}{2^k}, \quad 2^M = L \tag{13}$$

Factoring (12) backward to (11), substituting (3) into (11), and using (13), we obtain the total spectral density $S_m(\omega)$ of the output signal as follows:

$$\begin{aligned} S_m(\omega) =& (H(\omega)S_x(\omega)) * (H(\omega)S_y(\omega)) \\ &+ (H(\omega)S_x(\omega)) * (H(\omega)E_y(\omega)) \\ &+ (H(\omega)E_x(\omega)) * (H(\omega)S_y(\omega)) \\ &+ (H(\omega)E_x(\omega)) * (H(\omega)E_y(\omega)) \\ &+ E_q(\omega)\sqrt{\sum_{k=0}^{2M-1} \frac{1}{2^k}} \end{aligned} \tag{14}$$

$$H(\omega) = \frac{1}{L}\sum_{m=0}^{L-1} \exp(-j\omega m/f_s)$$

$$|E_q(\omega)|^2 = R(\omega)$$

where '$*$' is the convolution operator, and $S_x(\omega)$, $S_y(\omega)$, $E_x(\omega)$ and $E_y(\omega)$ are the Fourier transforms of $s_x(n)$, $s_y(n)$, $e_x(n)$ and $e_y(n)$. The first term is the desired product in the frequency domain. The second, third and fourth terms are regarded as noise components. Fig. 2*b* shows the output spectrum obtained by (14) and by the circuit simulation for $L = 4$ when two $\Sigma\Delta$ modulated sinusoidal inputs whose signal components are $0.02f_s$ and $0.03f_s$ in frequency and $0.7 \times (\delta/2)$ in amplitude are given. Equation (14) has the tendency to make the noise power larger than the circuit simulation because the theoretically estimated noise of the adders of which the multiplier consists is larger than the noise observed in the circuit simulation.

## 3 Circuit modules

### 3.1 Integrator and digital $\Sigma\Delta$ modulator

When a bit-stream signal $x(n)$ controls count-up/down of an $m$-bit (with $m$ integer) counter clocked at the bit-stream rate, the signal is integrated in the counter. Let the $m$-bit content of the counter be denoted by $w(n)$. The transfer function between $x(n)$ and $w(n)$ in the $z$-domain is given by

$$\frac{W(z)}{X(z)} = \frac{z^{-1}}{1 - z^{-1}} \tag{15}$$

The $m$-bit counter content can be converted into bit-stream form by the digital $\Sigma\Delta$ modulator shown in Fig. 3. Replacing the signum function block by a constant multiplier $1/K$ and a white noise source, the modulator is linearised as follows:

$$Y(z) = \frac{z^{-1}}{K} W(z) + E(z) \tag{16}$$

where the term $E(z)$ is the differential of the white noise,

$$E(z) = \frac{1}{\sqrt{3}}(1 - z^{-1}) \tag{17}$$

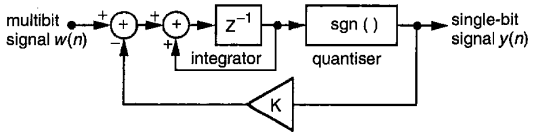


**Fig. 3** *First-order digital sigma–delta modulator*

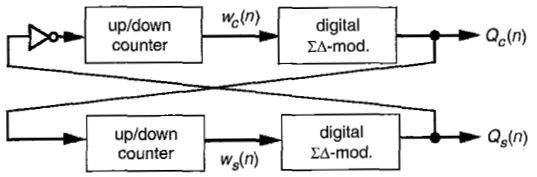


**Fig. 4** *Sigma–delta based oscillator*

### 3.2 ΣΔ-based oscillator

The oscillator shown in Fig. 4 consists of two digital ΣΔ modulators with feedback gain $K$ and two up/down counters with upper and lower limits $\pm A$, $1 \ll A < K$. The following linearised equation in terms of its state $w_c(n)$ is derived by using (15) and (16):

$$\left((1-z^{-1})^2 + \frac{z^{-4}}{K^2}\right) W_c(z) = (z^{-1} - z^{-2}) E_s(z) + \frac{z^{-3}}{K} E_c(z) \tag{18}$$

where $E_c(z)$ and $E_s(z)$ are $z$-transforms of the two ΣΔ modulation noises given by (17). The equation in terms of $w_s(n)$ is similarly derived. We investigate the autonomous behaviour of the oscillator based on the equation. The characteristic roots of the above equation lie at positions $Z_o$ given by

$$\begin{aligned} |Z_o| &= 1 + \varepsilon, \quad 0 < \varepsilon \ll 1 \\ \angle Z_o &\approx \pm 1/K \end{aligned} \tag{19}$$

in the complex plane. Taking into account the counter limit $A$ and the root location $Z_o$, it is expected that $w_c(n)$ is a sinusoidal wave that is $1/2\pi K$ in frequency and $A$ in amplitude. Since one state $w_c(n)$ ($w_s(n)$) is regarded as the integral of another state $-w_s(n)$ ($w_c(n)$), the phase difference between the two states is $\pi/2$.

The phase of the oscillation can be controlled by adjusting the feedback gain $K$. Suppose that the gain $K$ is increased or decreased by $\Delta K$ from $K_o$ depending on a single-bit control signal $c(n)$. Then, the oscillation phase $\theta(n)$ at time $n$ is

$$\theta(n) = \sum_{i=0}^{n} \frac{1}{K_o - \Delta K \cdot c(i)} \approx \frac{n}{K_o} + \frac{\Delta K}{K_o^2} \sum_{i=0}^{n} c(i) \tag{20}$$

The second term of the right-hand side of the equation is the phase variation $\Delta\theta(n)$ caused by the control signal $c(n)$. Their relation in the $z$-domain is given by

$$\Delta\theta(z) = \frac{\Delta K}{K_o^2} \frac{z^{-1}}{1 - z^{-1}} C(z) \tag{21}$$

From the above investigations and the consideration that $|E_c(z)|$, $|E_s(z)| \ll K$, the outputs $Q_c(n)$ and $Q_s(n)$ can be approximated to ΣΔ modulated sinusoidal signals whose phase is controlled by $c(n)$,

$$\begin{aligned} Q_c(n) &\approx \frac{A}{K} \cos\left(\frac{1}{K_o}\left(n + \frac{\Delta K}{K_o}\sum_{i=0}^{n} c(i)\right)\right) + e_c(n) \\ Q_s(n) &\approx \frac{A}{K} \sin\left(\frac{1}{K_o}\left(n + \frac{\Delta K}{K_o}\sum_{i=0}^{n} c(i)\right)\right) + e_s(n) \end{aligned} \tag{22}$$

where $e_c(n)$ and $e_s(n)$ are inverse $z$-transforms of $E_c(z)$ and $E_s(z)$.

### 3.3 ΣΔ-based digital filter

Fig. 5 shows a schematic diagram of a first-order digital lowpass filter (LPF) [1] with a first-order digital ΣΔ modulator. Input $x(n)$ and output $y(n)$ are bit-stream signals. As mentioned in Section 1, it needs no multibit multipliers. Using the linear approximation (16) of the digital ΣΔ modulator, the following relations are obtained among the input $x(n)$, ΣΔ modulation noise, the state $w(n)$,

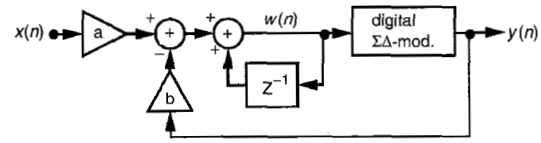


**Fig. 5** *First-order digital sigma–delta based lowpass filter*

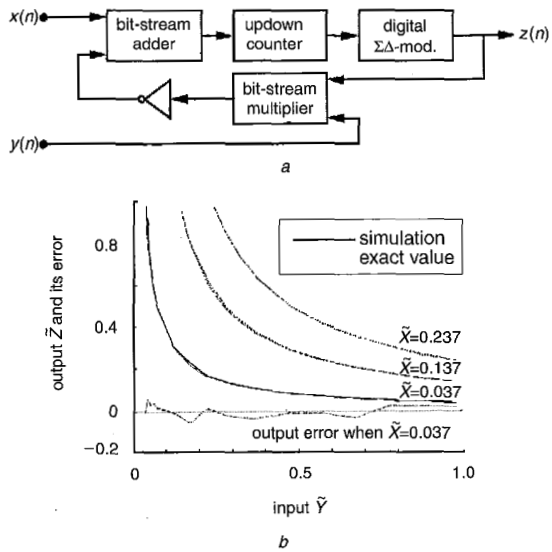


**Fig. 6** *Bit-stream divider*
*a* Block diagram
*b* Input/output characteristics

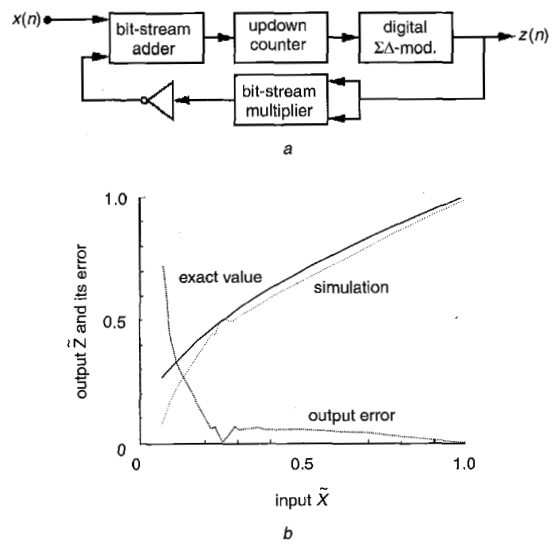


**Fig. 7** *Bit-stream square root circuit*
*a* Block diagram
*b* Input/output characteristics

and the output $y(n)$ in the $z$-domain:

$$W(z) = \frac{a}{1-\left(1-\frac{b}{K}\right)z^{-1}}X(z) + \frac{-b}{1-\left(1-\frac{b}{K}\right)z^{-1}}E(z) \quad (23)$$

$$Y(z) = \frac{\frac{a}{K}z^{-1}}{1-\left(1-\frac{b}{K}\right)z^{-1}}X(z) + \frac{1-z^{-1}}{1-\left(1-\frac{b}{K}\right)z^{-1}}E(z) \quad (24)$$

### 3.4 Bit-stream divider

Fig. 6*a* shows a schematic diagram of a divider whose inputs and output are in bit-stream form. It has the circuit scale of 1K logic gates. If the delays and noise of the output from its bit-stream adder and multiplier are neglected, the circuit operation is expressed by the following nonlinear difference equation:

$$z(n+1) = z(n) + \{x(n) - y(n)z(n)\}/(2K) \quad (25)$$

where $x(n)$ and $y(n)$ are inputs, $z(n)$ is the output and $K$ denotes the feedback gain of the digital $\Sigma\Delta$ modulator. When the average $\tilde{Y}$ of $y(n)$ is positive, it is found from (25) that the output average $\tilde{Z}$ converges to $\tilde{X}/\tilde{Y}$, where $\tilde{X}$ stands for the average of $x(n)$. The convergent output values of the divider are plotted in Fig. 6*b*. The average values $\tilde{X}$, $\tilde{Y}$ and $\tilde{Z}$ in the Figure are obtained by the $\Sigma\Delta$-based LPFs in Fig. 5 with $a = b = 0.001$. The output errors (exact value − simulated output $\tilde{Z}$)/(exact value), are also shown in the Figure.

### 3.5 Bit-stream square root circuit

The behaviour of the square root circuit in Fig. 7*a* is also governed by the following difference equation in terms of input $x(n)$ and output $z(n)$:

$$z(n+1) = z(n) + \{x(n) - z(n)^2\}/(2K) \quad (26)$$

When the average $\tilde{X}$ of input $x(n)$ is positive, the output average $\tilde{Z}$ converges to the square root of $\tilde{X}$. Its input/output characteristics are plotted in Fig. 7*b*.

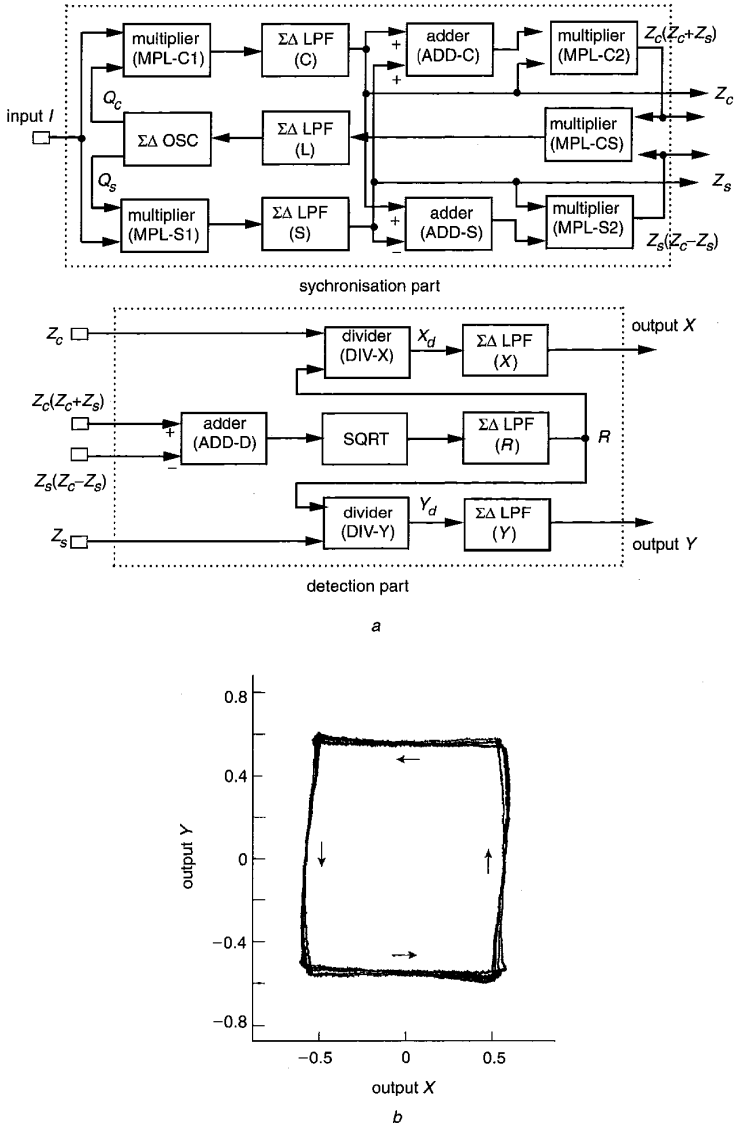


**Fig. 8** *QPSK demodulator*
*a* Block diagram
*b* Output constellation

## 4 Application to a communication system

In this Section a QPSK demodulator is presented as an application of BSSP to communication systems. Intended to be applied to the A/D conversion in high speed communication systems, $\Sigma\Delta$-based A/D converters and decimation filters using superconductive Josephson device technology have been proposed in recent years [4, 5]. The fact that BSSP systems can be built from small numbers of logic gates may also make it possible to implement all parts of the DSP in high-speed, low-power, but low-density superconductive Josephson chips. When BSSP is applied to lower speed communications, such as digital subscriber line communications, the processing circuits can be implemented using conventional CMOS technology.

### 4.1 BSSP for QPSK demodulation

Fig. 8*a* shows a QPSK demodulator built from the previously introduced bit-stream arithmetic circuits and circuit modules. The synchronisation part tracking the QPSK carrier is a kind of Costas loop. It contains a $\Sigma\Delta$-based oscillator and $\Sigma\Delta$-based lowpass filters in addition to the bit-stream arithmetic circuits. The phase of the oscillation is controlled by the bit-stream output of the loop filter $\Sigma\Delta$-LPF(L). About 6.5 K logic gates are consumed by the synchronisation part.

In the phase detection part, square root and divider circuits normalise output magnitude. Thus, the detector is equipped with automatic gain control. This phase detection part consists of 6 K logic gates.

A Nyquist rate processor equivalent to the demodulator requires 20 multibit multipliers. About 15 K gates were used for the multipliers when their bit length is 8 bits.

Circuit simulation were carried out under the conditions shown in Table 1. An example of the output signal is presented as constellation plots in Fig. 8*b*. The outputs $X$ and $Y$ of the filters $\Sigma\Delta$ LPF(X),(Y) are the multibit states corresponding to the state $w(n)$ in Fig. 5. In Fig. 8*b*, the outputs are normalised by the feedback gain $K$ of the digital $\Sigma\Delta$ modulators in the filters and plotted for $10^5$ sampling intervals.

### 4.2 Linear steady-state analysis

A linear approximation model of the demodulator is built to estimate analytically the influence of the $\Sigma\Delta$ modulation noise and the bipolar noise in the adders and multipliers on the steady-state performance of the demodulator. The bit-stream adders, up/down counters for integrating bit-stream signals, digital $\Sigma\Delta$ modulators, and $\Sigma\Delta$-based LPFs are already linearised as in previous sections.

The multipliers MPL-C2,MPL-S2,MPL-CS in the synchronisation part, MPL-X,MPL-Y in the dividers and MPL-R in the square root circuit are linearised as follows since their input signal components are in equilibrium after the phase shift of the carrier:

$$\Delta z(n) \approx x_o \cdot (h * \Delta y(n)) + (h * \Delta x(n)) \cdot y_o + e_q(n)\sqrt{\sum_k \frac{1}{2^k}}$$

or

$$\Delta Z(z) \approx x_o \cdot (H(z)\Delta Y(z)) + (H(z)\Delta X(z)) \cdot y_o + E_q(z)\sqrt{\sum_k \frac{1}{2^k}} \quad (27)$$

**Table 1: Specification of the QPSK demodulator**

| Item | Specification |
|---|---|
| Sampling frequency | $f_S = 1$ |
| | Waveform: $\Sigma\Delta$ modulated sinusoidal wave |
| Input carrier | Frequency $f_C = 0.002$ |
| | Amplitude $I_O = 0.9(\times\delta/2\sqrt{2})$ |
| Phase shift interval | 5000 samples |
| | Centre frequency $1/2\pi\ K_o = 2.015 \times 10^{-3}$ |
| $\Sigma\Delta$-based oscillator | Variable frequency range $\Delta K/K_o = 0.0506$ |
| | Amplitude $A/K_o = 0.95$ |

| $\Sigma\Delta$ LPF characteristics | order | cut-off frequency | gain |
|---|---|---|---|
| (C) | 1 | $2.0 \times 10^{-3}$ | 1 |
| (S) | 1 | $2.0 \times 10^{-3}$ | 1 |
| (L) | 1 | $2.0 \times 10^{-3}$ | 8 |
| (R) | 1 | $2.0 \times 10^{-3}$ | 3 |
| (X) | 1 | $2.0 \times 10^{-4}$ | 1 |
| (Y) | 1 | $2.0 \times 10^{-4}$ | 1 |

The operator $h*$ stands for averaging $L$ samples. Its $z$-transform $H(z)$ is given by the second equation of (14). The variation $\Delta x(n)$ and $\Delta y(n)$ of the inputs includes the small variation of signal components from $x_o$ and $y_o$ and the noise components caused by the bit-stream conversions. The output variation $\Delta z(n)$ contains the noise, the third term of (27), whose power spectrum is given by (13).

Then, the linear models of the dividers and the square root circuit can also be built since all the circuit modules constituting them have been linearised.

As we will see later, the noise components in $\Sigma\Delta$ modulated input carrier $I(n)$ and in the outputs $Q_c(n)$, $Q_s(n)$ of the $\Sigma\Delta$-based oscillator are transformed into the noise given by the sum of the second, third, and fourth terms in (14) and moved to the outputs of the multipliers MPL-C1,MPL-S1. Then, the oscillator is represented by only one linear (21).

Next, we estimate the output variation of multipliers MPL-C1 and MPL-S1 when the input carrier $I(n)$ and the $\Sigma\Delta$-based oscillator shift their phase $\theta_I$ and $\theta_L$ slightly by $\Delta\theta_I$ from $\theta_o + (\pi/2)i$, $i = 0, 1, 2, 3$ and by $\Delta\theta_L$ from $\theta_o$. When the signal components $s_i(n)$, $s_c(n)$ and $s_s(n)$ of the input carrier $I(n)$ and the oscillator outputs $Q_c(n)$, $Q_s(n)$ are given by

$$s_i(n) = I_o(\cos\theta_I + \sin\theta_I)$$

$$s_c(n) = \frac{A}{K}\cos\theta_L \quad (28)$$

$$s_s(n) = \frac{A}{K}\sin\theta_L$$

the variations $\Delta z_c(n)$, $\Delta z_s(n)$ of the signal components of the

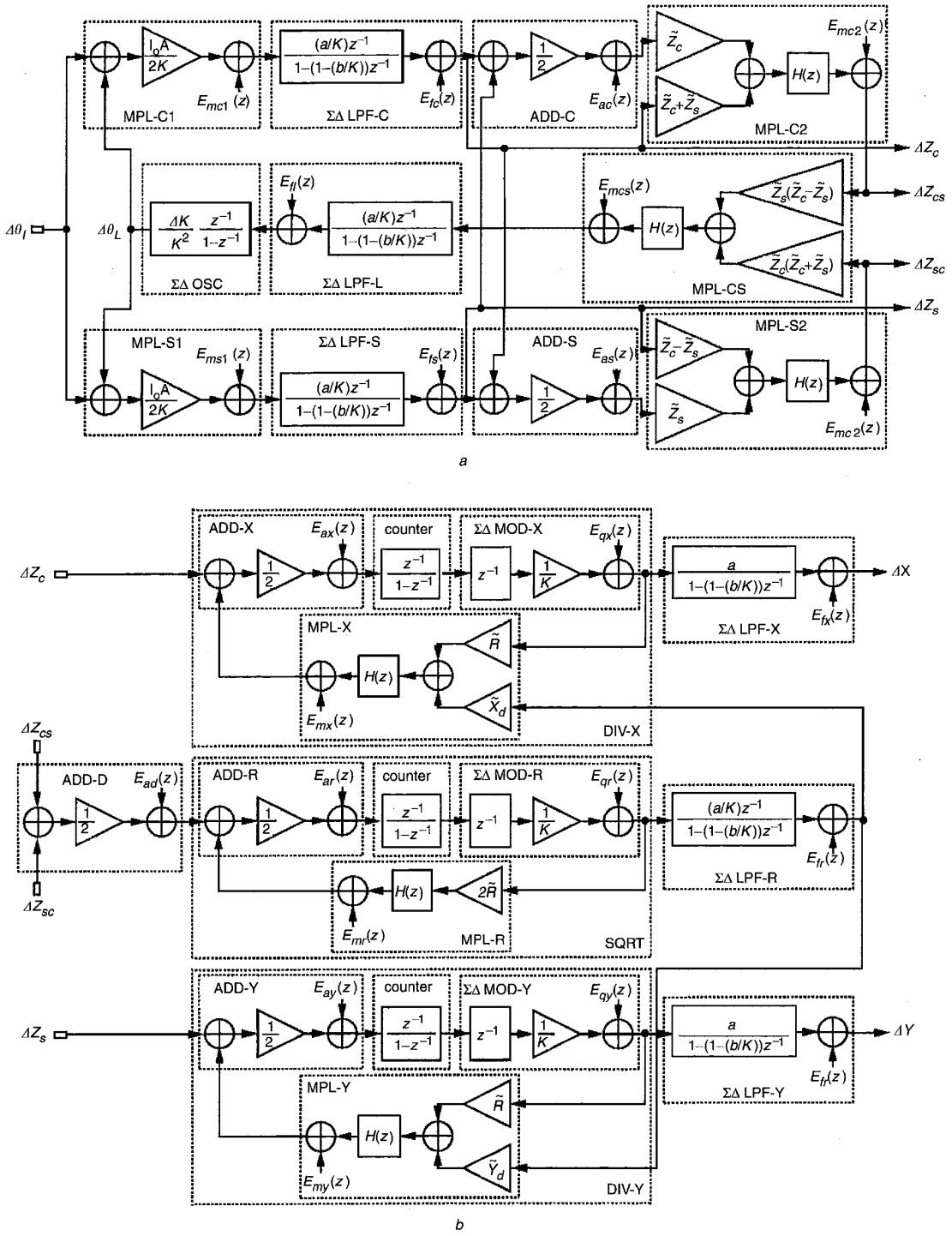


**Fig. 9** *Linear approximation model of the QPSK demodulator*
*a* Synchronisation part
*b* Detection part

multiplier outputs are as follows:

$$\Delta z_c(n) = d_c(i)\frac{I_o A}{2K}(\Delta\theta_I - \Delta\theta_L)$$

$$\Delta z_s(n) = d_s(i)\frac{I_o A}{2K}(\Delta\theta_I - \Delta\theta_L) \qquad (29)$$

$$(d_c(i), d_s(i)) = (+1,-1),(-1,-1),(-1,+1),(+1,+1) \quad \text{for } i = 0,1,2,3$$

From (14), the output noise components of the multiplier MPL-C1 are given by

$$H(z)S_i(z) * H(z)E_c(z) + H(z)E_i(z) * H(z)S_c(z) + H(z)E_i(z) * H(z)E_c(z) + E_q(z)\sqrt{\sum_k \frac{1}{2^k}} \qquad (30)$$

where $E_i(z)$ and $E_c(z)$ are the $z$-transforms of the $\Sigma\Delta$

modulation noise components of $I(n)$ and $Q_c(n)$. The output noise components of MPL-S1 are similarly represented.

The block diagram of the linear model of the demodulator is shown in Fig. 9. In the Figure, the constant multipliers $\tilde{Z}_c, \tilde{Z}_s, \tilde{R}, \tilde{X}_d, \tilde{Y}_d$ denote the steady signal components of the signals $Z_c$, $Z_s$, $R$, $X_d$, $Y_d$ in Fig. 8*a* for example. The noise sources in the linear model was clarified as follows: the noise sources $E_{mc1}$, $E_{ms1}$ in multipliers MPL-C1, MPL-S1 are derived as in (30). The noise sources in the adders and other multipliers are given by, respectively (9) and (13). The noise sources in the $\Sigma\Delta$ modulators are given by (17). The noise sources in $\Sigma\Delta$ LPF are represented by the second term of (23) or of (24), depending on the form of the filter outputs, multibit or bit-stream.

Using the linear model, the total influence of all the noise sources on the steady phase jitter of the oscillator is estimated as shown in Fig. 10, where the oversampling ratio is the ratio of the sampling frequency $f_s$ to the carrier frequency $f_c$. Setting the ratio higher decreases the noise power in the signal band. Accordingly, the phase jitter also decreases. However, the curve obtained by the circuit simulation shows that the jitter cannot be lower than a certain level since the multipliers generate harmonics at $2f_c$ and higher in frequency, while the analytical curve continues to decline because the effect is removed by linearisation.

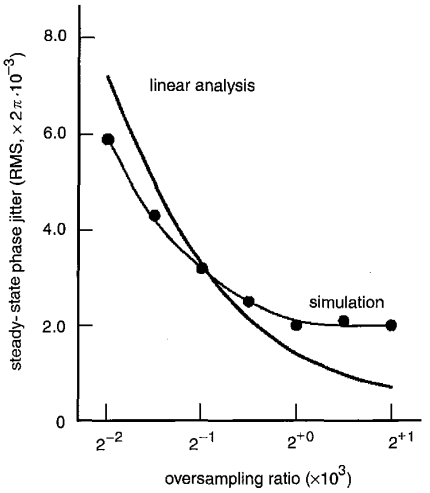


**Fig. 10** *Steady-state RMS jitter of the phase of the sigma–delta based oscillator in the demodulator*

## 5 Conclusions

The bit-stream signal processing technique reduces the large number of logic gates and data lines in a hardware implementation because of the simple arithmetic circuits and one routing line for one signal. The BSSP and bit-serial processing provide the possibility to implement DSP systems on LSI chips using neither high-precision analogue elements nor heavy multibit digital arithmetic units.

Application systems are considered from the following points of view: the first is the influence of $\Sigma\Delta$ modulation noise on system performance. Bit-stream signals from $\Sigma\Delta$ modulators or the arithmetic circuits inherently contain quantisation errors. However, from the circuit simulation in Section 2, it was found that the proposed arithmetic circuits can provide sums and products keeping the dynamic range of 30 dB in the signal band from DC to 1/64 of the sampling frequency. The large noise power in the higher frequency band is attenuated by integrators or lowpass filters. Therefore, BSSP will be especially useful when bit-stream adders and multipliers are used together with integrators or filters. The quantitative estimation of the influence of such noise on system performance is made by a similar linear analysis to that presented in Section 4.2. The second point is the dynamical characteristics, including the stability of systems in which divider and square root circuits are used. Since the circuits are dynamical systems represented by the nonlinear difference equations given in Section 3, their output transient time is much longer than the sampling interval. In some applications there may be concerns about whether transient outputs affect the dynamic characteristics. This transient problem is to be the subject of future research.

## 6 Acknowledgments

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