IEEE Asian Solid-State Circuits Conference
November 12-14, 2007 / Jeju, Korea

Bitwise Competition Logic for Compact Digital Comparator

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***Abstract*—In this paper, we present a Bitwise Competition Logic (BCL) for the high performance and area efficient digital comparator. It compares two integer numbers using the location of the first 1 from the MSB, without arithmetic computations. The detail circuits to implement BCL, pre-encoder and selection logics are explained. The implemented BCL comparator shows 16%, 38% and 30% improved result in propagation delay, transistor count, and physical area compared to the other types of comparators. Measurement waveforms of fabricated BCL comparator verify its feasibility and functionality.**

I. Introduction

The digital comparator is one of the most basic and essential components in digital systems. It is widely used in many fundamental processes of computing and communication including sorting and searching data [1]-[2]. And it is heavily used in data intensive applications such as image processing and 3D graphics [3]-[4]. Therefore, a digital comparator should be optimized carefully to build fast and efficient system.

A primitive way of designing digital comparator is to exploit a parallel adder. However parallel adder includes unnecessary arithmetic function over comparison, physical implementation becomes rather complicate. Besides, it is only useful when the length of comparator input is short. As another way, a comparator can be implemented based on the equation which flattens compare function directly. However, this approach is also suitable for comparators whose length of input is short. As the length of inputs increases, not only its implementation complexity but also required resources like transistor count and power are also increased dramatically. And the speed of comparator is saturated. To solve this, several works for high performance and area efficient comparators have been proposed recently [5]-[8]. C.-C. Wang proposed ANT dynamic logic for high performance [5] and high fan-in dynamic circuit for low transistor count [8]. C.-H. Huang exploited the priority encoder based algorithm and used MODL in circuit to decrease logic depth [6]. And S.-W. Cheng employed modified 1's complement principle and conditional sum adder scheme for efficient implementation [7]. All above works design comparator based on arithmetic equations of long number comparison and improve performance with own proposed logic circuits. In this approach, the efficiency of comparator is dependent on conciseness of arithmetic expression and performance of logic circuits which build up the equation. Although this approach improves performance, the implemented comparators are still complicated because the arithmetic equation they rely on has a base complexity. Therefore, a new approach for comparing operation is required to achieve further improvements on designing high performance and area efficient comparator.

In this paper, we propose a compact digital comparator based on an algorithm which has no arithmetic computation. It decides the larger one by detecting which has the earlier first 1 from the MSB after pre-encoding of inputs. To implement this into the circuits, Bitwise Competition Logic (BCL) is newly proposed. As a result, implemented BCL comparator achieves improvements not only in transistor count, but also in propagation delay and physical area. BCL comparator is fabricated in 0.18μm CMOS process and its operations are verified by chip measurement.

This paper is organized as follows. Chapter II describes a proposed algorithm for two integer number comparison. In chapter III, implementation of BCL comparator and its detailed circuits are explained. In chapter IV, performance comparisons with conventional works will be discussed. After that, the implementation and measurement results will be shown in chapter V. Lastly, conclusion of this paper will be made in chapter VI.

II. Proposed Algorithm

The size of two long binary numbers can be easily compared by identifying the locations of the first 1 from the MSB: The one that has the first 1 in more significant position is the larger. In case that the locations of the first 1 are the same in both numbers, the decision is postponed to the lower bit where only one input has 1 in that bit position.

Proposed comparison algorithm exploits above easy and intuitive method. Fig. 1 represents the flow chart of algorithm. At first, pre-encoders encode two input numbers bit by bit as the truth tables shown in table I. Pre-encoder A makes the output high only when input A is 1 and input B is 0 and pre-encoder B do encoding in the opposite way. Therefore pre-encoding removes cases that 1s exist in the same bit position

TABLE I. Truth tables of pre-encoders

A \ B	0	1
0	0	0
1	**1**	0

(a) $A^* = A \cdot \overline{B}$

A \ B	0	1
0	0	**1**
1	0	0

(b) $B^* = \overline{A} \cdot B$

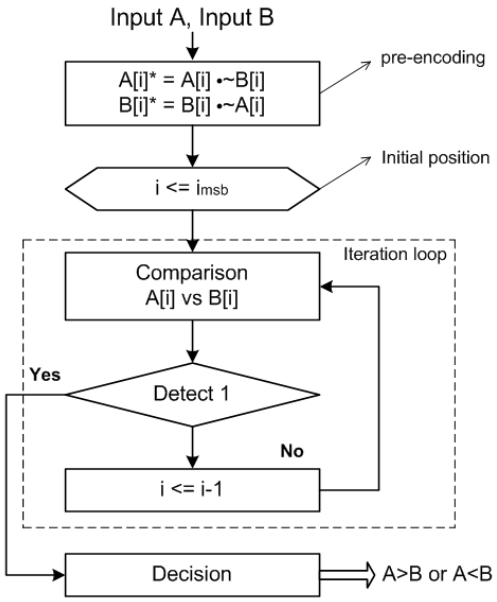

Fig. 1. Flow Chart of Proposed Algorithm

and allows that only one input has 1 in any bit. After pre-encoding, the size order of two numbers can be determined easily by detecting the earlier first 1 from the MSB without postponing decision to lower bits. To detect the first 1, two bits in same bit position are compared repeatedly bit by bit from the MSB. Next summarizes the comparison algorithm.

Step1. Input A and B are pre-encoded into A* and B* each.
Step2. Bit comparison is performed (initial = MSB)
Step3. If 1 is detected, that input is decided to be the larger.
Step4. If no 1 is detected, move to next lower bit and repeat from step 2 until find the first 1.

To give a simple example of proposed algorithm, 4-bit unsigned number comparison is presented in Fig. 2. In this case, input A is decided to be the larger because it has the first 1 from the MSB in more significant bit than input B after pre-encoding.

III. Bitwise Competition Logic (BCL)

A digital comparator which implements above algorithm consists of pre-encoders and bitwise competition logic (BCL). Pre-encoders encode each bit of two inputs from A[i] and B[i] into (A[i] • ~B[i]) and (~A[i] • B[i]) respectively in front of BCL. They prevent the logic failures of BCL occurred when both inputs have 1s in the same bit position. BCL, a main block of comparator, is devised to detect which has the earlier first 1 from the MSB in two binary numbers. It just locates two inputs from the MSB to the LSB and races each bit from the MSB, motivated from S.-J. Lee's RALA [9], to achieve fast operation and minimal transistor count implementation.

Fig. 3 describes BCL circuit diagram and its operation for 8-bit inputs. In BCL, there are two parallel lines named A line and B line which are pre-charged to VDD initially. Then, START signals are activated sequentially to trigger each bit of pre-encoded signals to the lines from the MSB to LSB. To generate START signals with a constant interval time, simple inverter chain is used. The interval time between START

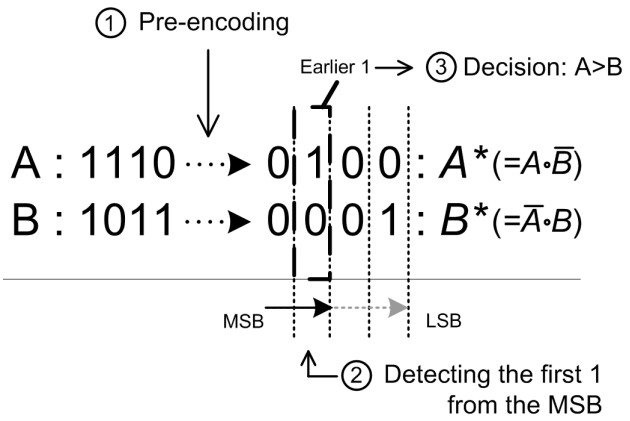

Fig. 2. The comparison of two 4-bit unsigned numbers

signals is made by two inverters and it is about 100ps in 0.18μm process. If any triggered pre-encoded signal is 1, the path from the corresponding line to GND is connected and the voltage of the line goes down abruptly. Otherwise, when no 1 is triggered, there is no change in both lines. And decision logic, at the right end of the lines, senses the line that firstly goes down and keeps the result until the bitwise competitions end. As shown in Fig. 4, the circuit of decision logic is based on the circuit of sense amplifier except transistor N1 and N2. N1 and N2 receive feedbacks from the output signals and disable further input of the small number to preserve only the first decision or the input of large number. For example, the timing diagram of Fig. 3 illustrates BCL's whole operations in case that pre-encoded input A* and B* are 00000010 and 00000001

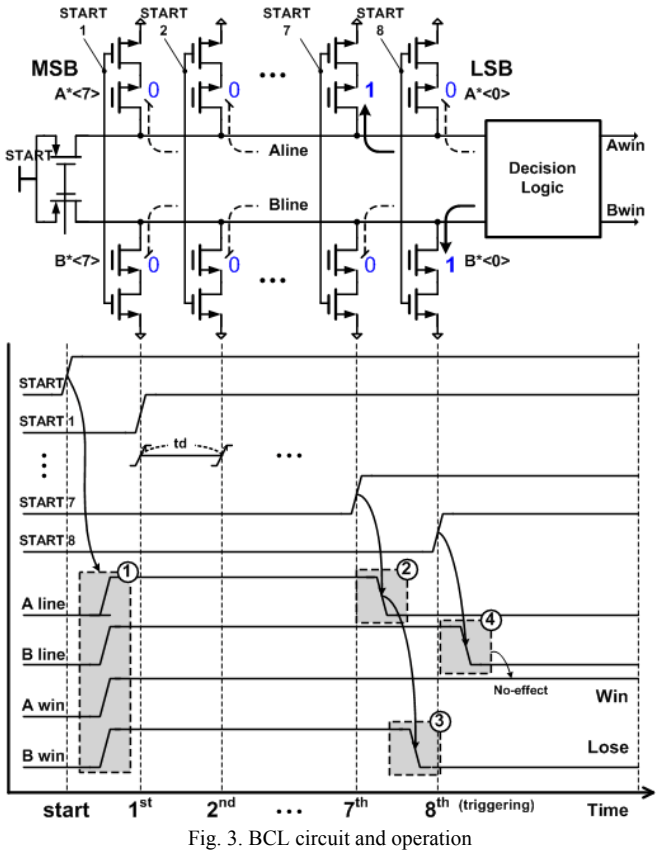

Fig. 3. BCL circuit and operation

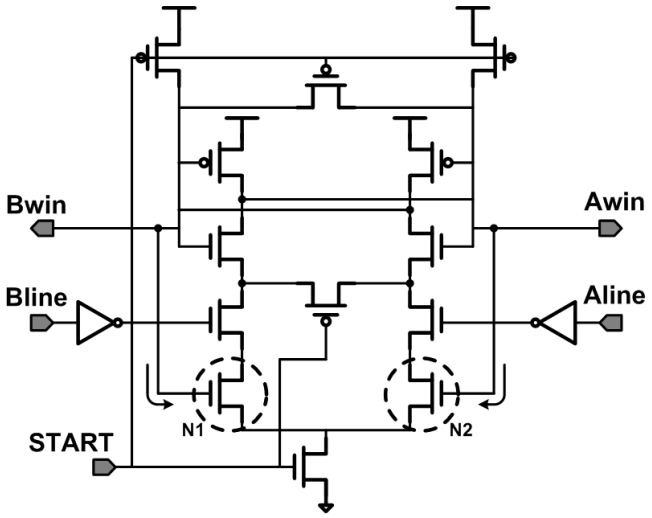

Fig. 4. Decision Logic

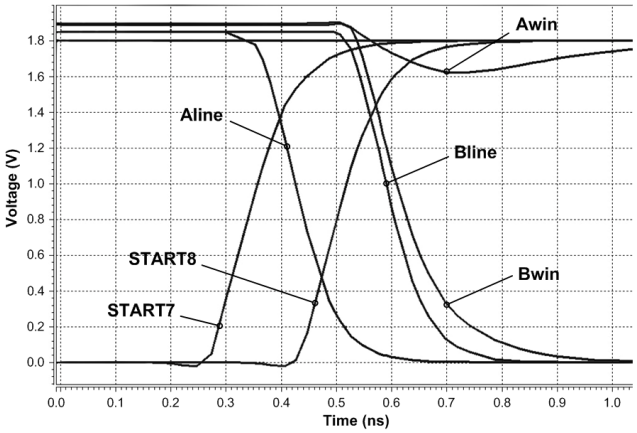

Fig. 5. Simulation waveforms in decision logic

respectively. The gray boxes show the signal transitions of a few important events in BCL operation. At box (1), all lines are precharged while the START signal is low. Triggering starts but both lines stay in VDD by the 7th start signal. At the 7th triggering of box (2), A line is dropped to GND because 7th bit of A is 1. The drop of A line forces decision logic to turn down B win of box (3). Finally, A win and B win, which represent the comparison results, are kept until the end of the cycle irrespective of B line voltage as shown in box (4). More detail

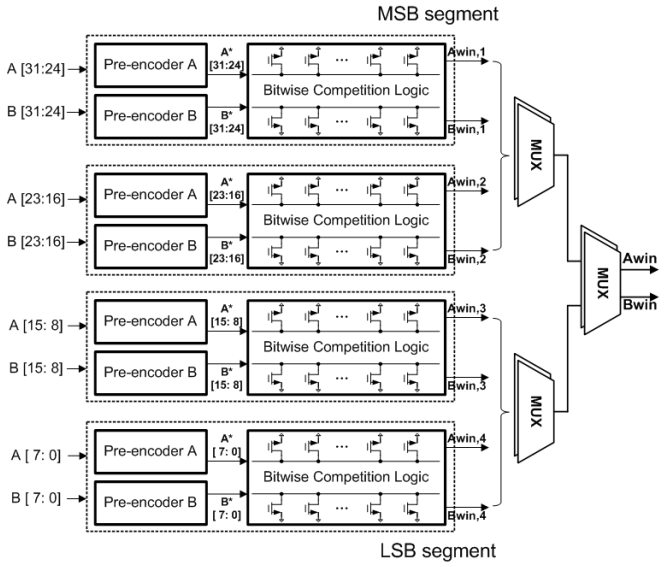

Fig. 6. Overall Block Diagram of BCL comparator

simulation waveforms are shown in Fig. 5. B line drops to GND after A line and decision logic forces B win signal to GND keeping A win stayed in VDD with a small fluctuation.

Over 8-bit implementation of BCL, it can be extended for long binary integer numbers such as 32-bit or 64-bit by just increasing the length of pre-encoded signals in two parallel lines. However, having lots of bits in one line pair is not proper because it takes too long time to generate triggering signals, and its execution time increases accordingly. Therefore, comparing all bits in one line pair is not a suitable way for long input numbers. As a solution of this, long input numbers can be divided into several segments and mapped into several short BCLs as shown in Fig. 6. It shows the overall diagram of 32-bit comparator using four 8-bit BCL segments with additional selection logic. Because each segment BCL operates in parallel, overall speed is degraded as slightly as the time taken by selection mux logic. Selection logic chooses the correct result among four intermediate results with the different priorities. Basically, the one who executes most significant bits has the highest priority. If the MSB segment is proved to be drawn, the final result will be made by the next segment. And if it draws again, the decision of final result can be made in lower segments. Because this process can be implemented in tree structure, two mux stages are required to select correct result.

Table II Performance Comparisons

	Transistor Count	Propagation Delay		Physical Area	
		Original (0.6)	Scaled (0.18)	Original (0.6)	Scaled (0.18)
C.-C Wang's CDT, 1998[4]	1,892	6.3ns	1.99ns	400μm x 380μm (=152,000 μm^2)	13945 μm^2
C.-H. Huang's JSSC, 2003[5]	1,640	5.4ns	1.70ns	322μm x 226μm (=72,772 μm^2)	6676 μm^2
S.-W. Cheng's ICECS, 2003[6]	1,556	4.2ns	1.33ns	576μm x 120μm (=69,120 μm^2)	6341 μm^2
Proposed	964	·	1.12ns	·	368μm x 12μm (=4416 μm^2)
Improvement	**38%**	**16%**		**30%**	

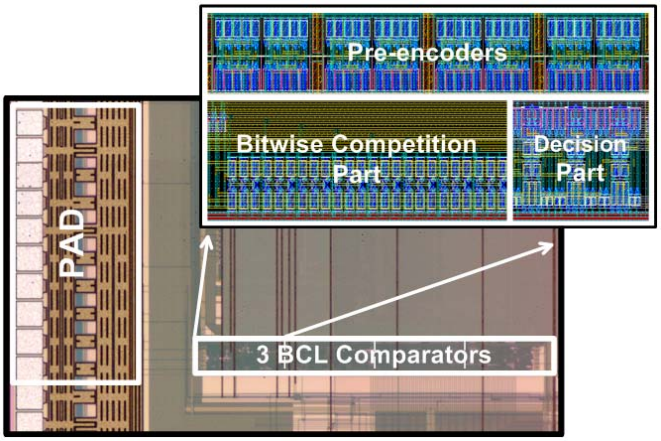

Fig. 7. Chip and Layout photograph

And using this, 64-bit comparator can be easily implemented with eight 8-bit BCL segments and 3-stage selection logic.

IV. Performance Comparision

In this chapter, the performance comparison between BCL comparator in 0.18μm process and conventional comparators will be shown. The results of BCL comparator are based on 64-bit inputs because conventional implementations were made for 64-bit inputs. Elaborate scaling down is done on the conventional results to compensate the process gap between 0.6μm and 0.18μm. Scaling factor for delay time is obtained as 3.15 based on the chart of ITRS 1997 [10]. And scaling factor for area is calculated as the square of process ratio, 10.9 [11]. As a result, BCL comparator shows 1.12ns delay, 964 transistor count, and 4416 mm^2 area which are 16% faster, 38% less transistor count, and 30% smaller than the best of conventional comparator. The comparison results are summarized in table II. Additionally, it consumes only 2.53mW in 1.8V when it operates every single cycle in 200MHz operation frequency.

V. Implementation Results

Fig. 7 shows the chip and layout photograph of fabricated BCL comparators in TSMC 0.18μm process. Three 32-bit comparators are embedded in SRAM to compare read data out of memory instantly. This memory is applied to object recognition system to accelerate local maximum search operation. The operation of BCL comparator is measured as shown in Fig. 8. It shows STRAT 1, A line, B line and B win signal in case that input A is 0x00000001 and input B is 0x00000000. It is one of the worst cases because the decision is made in the last triggering. The waveforms show that A line is pulled down to GND after triggering starts while B line remains at VDD. As a result, B win signal is pulled down to GND by decision logic. It takes 1.07ns from the start of triggering, START 1 signal, to the final result B win signal. The measure waveforms are well matched to the simulation waveforms and the measured delay time is almost the same as the simulated delay time with negligible error. It is caused due to parameter variation and jitter of waveforms. And the slow slope of each waveform is caused by loading of the measurement probe and parasitic ingredients of the chip board.

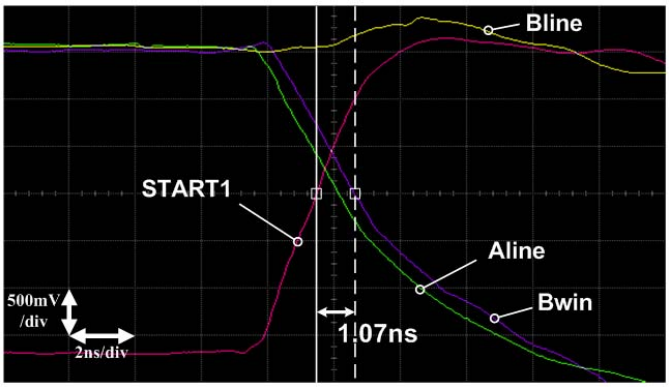

Fig. 8. Measurement Waveforms

VI. Conclusions

Bitwise Competition Logic (BCL) for high performance and area efficient digital comparator is proposed. It compares two numbers using the location of the first 1 from the MSB, different from arithmetic based comparators. Implemented BCL comparator reduces propagation delay, transistor count, and physical area by 16%, 38% and 30% compared to the best of reported conventional comparators. BCL comparator is fabricated in 0.18 m process as the embedded logic of memory and fully measured.

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