

Board Level Reliability of Flipchip Package

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Abstract

In the world of electronic materials, solder is a critical material that plays an important role in the first level (silicon to package substrate) and second level (package to printed circuit board) interconnection. As a joining material in electronic assemblies, solder provides electrical and mechanical connections. The increasing need for reliable electronic devices for harsh environment triggers the need for reliable solder joints. This study focuses on reliability of second level interconnections between package and printed circuit boards.

Board level temperature cycling and mechanical drop performance of a 15 mm x 15 mm FCBGA test vehicle were evaluated with different package construction (lidded vs non-lidded), and BGA solder alloys (SA1, SA2, and SA3). Daisy chain packages were assembled on 1.0 mm thick PCB. Mounted units were thermally cycled between from -40C to 125C. Additional samples were evaluated in mechanical drop test conditions following JEDEC standards. Results showed that packages with SA2, and SA3 BGA had significantly higher board-level thermal cycling life compared to SA1. The best drop performance was achieved with SA1 solder. The performance trend among different solder alloys was found to be similar between lidded vs non lidded package. However, lidded package showed improved board-level reliability performance compared to a non-lidded package.

Key words

Flip Chip Package, Solder Joint Reliability, Lead Free Solder Alloys, Board Level Temperature Cycling, Board Level Drop

I. Introduction

When an electronic assembly is subjected to temperature changes, the solder joints in the assembly remain under mechanical stress due to the mismatch in the coefficient of thermal expansion (CTE) of the printed circuit board (PCB) and the component. Hence the mechanical, and thermal properties of packaging materials, as well as package design/construction are critical to ensure reliability of the package in field application.

L. Yip, and A. Ng [1] studied the effect of underfill glass transition temperature (T_g), package size, and lid on package warpage, and board level temperature cycling (BL-TC) performance. They reported that units with low T_g underfill (UF-A) had lower coplanarity, and warpage compared to high T_g underfill (UF-B). Addition of lid resulted a change in warpage shape (from crying to smiling). It also helped to reduce warpage variation with respect to temperature. High T_g UF showed 42% less BL-

TC characteristic life compared to the low T_g UF. This is consistent with package warpage data as higher warpage will impose higher tensile stress on the BGAs resulting a lower life. Addition of a lid improved BL-TC performance by 27%. The dye and pry result confirmed that the cracked solder joints were located at the middle of the package, which is also consistent with package warpage profile. 19mm package showed better BL-TC performance compared to 23mm packages. The authors hypothesized that the smaller pitch in 19mm package resulted increased solder ball density which eventually helped to increase BL-TC life of the smaller package.

Based on BL-TC experimental results, A. Prasad et al. [2] concluded that molded FCCSP package has 25-45% higher solder joint fatigue reliability compared to a lidless package. The authors explained that the molding compound helped to improve package stiffness, which eventually helped to improve BL-TC life.

Wang et al. [3] conducted a parametric study, using mechanical modeling, to investigate the influences of different parameters on the thermo-mechanical reliability of the package. They concluded that a thinner and wider stiffer and a thicker adhesive can improve the solder fatigue life. In a separate study, D. He, and coworkers [4] evaluated the BL-TC and board level drop test (BL-Drop) reliability performance of a 23 x 23 mm FCBGA package. They reported that bare die FCBGA package with 40% reduction of die thickness showed a 30% reduction in BL-TC life due to the higher warpage in a thinner die package. On the other hand, during a BL-Drop test, the thinner die (and hence less stiff) showed a 5x more drop test lifetime compared to the full thick die.

Lid helped to reduce package warpage at room temperature and made the warpage profile more consistent across different measurement temperatures. Lid also helped to bring overall package CTE close to PCB. Combining all these factors resulted in a 20% increase in BL-TC characteristic life for lidded package compared to a bare die package. However, being a stiffer package, lidded package showed poor (80% decrease) performance in drop test compared to a bare die package. For all the packages, location of failing BGA joints were near the die corner (die shadow) for BL-TC, and package corner for BL-Drop tests.

Addition of fourth element in the SAC solder creates a doped SAC alloy. Dopants (micro alloy additions) play an important role to control microstructure and mechanical properties of the alloy. Dopants have been found to strongly influence the properties and behaviors of lead-free solders. For example, addition of Bismuth (Bi) as a dopant has been demonstrated to have several beneficial effects. Bi helps to reduce solidification temperature, increase strength by means of precipitation hardening, and helps to reduce IMC (Intermetallic Compound) layer thickness in lead free solder materials [5]. The effect of Bi on the mechanical properties of a SAC (Sn3.5Ag0.9Cu) alloy was investigated by Mutahir and coworkers [6]. They reported that the shear strength increased with increasing Bi addition up to 2 wt.%. Beyond that point, the shear strength decreased with increasing Bi%. Improved shear strength might attribute to the role of Bi on the morphology of microstructure and distribution of dominant IMC (Ag₃Sn). Reduction of strength at higher Bi content was due to the evolution of Bi rich phase and fragmentation of the IMC. Panther, et al. [7] also reported that addition of 2% Bi in SAC alloys improves wetting and alloy spreading.

Zhao, et al. [8] found that addition of 0.02% Ni to SAC105 increased the formation of NiCuSn IMC and reduced the localized grain size at solder/NiAu pad interface. Lee and coworkers [9] found that micro-alloying SAC alloys with

Ni and Bi improved thermal fatigue life and drop impact resistance. Yeung, et al. [10] studied a novel lead-free solder SACQ. Based on BL-Drop, BL-TC and finite element simulation, they concluded that the doped alloy has improved board level reliability when compared to SAC105. Additional literature publications on the positive effects of dopants in SAC solder have been studied in reference [11].

In this work, BL-TC and BL-Drop performance of a 15 x 15 mm FCBGA test vehicle were evaluated with different package construction (lidded vs. non-lidded), and lead free BGA solder alloys (SA1, SA2, and SA3). While SA-1 is a Tin-Silver (Sn-Ag) based solder, SA-2, and SA-3 have around 3% Bismuth (Bi), <1% Copper (Cu), and ppm level Nickel, in addition to Sn-Ag. All three solder alloys came from three different vendors.

II. Experimental

A. Design

Daisy-chain (DC) test vehicle were used in this study to continuously monitor the solder joint integrity during both BL-TC and BL-Drop testing. The DC components used an electrical pattern on the top layer metal (layer M1) and bottom layer metal (layer M6) between BGA pads. Therefore, the established daisy-chain nets included routing through the PCB, solder-joints, and substrate layers and vias. The DC did not include the package corner joints because they were redundant ground locations in the product.

The associated daisy-chain PCB was designed such that there was a total of two nets monitored on each part: inner and outer nets. The inner net covered the central and redundant power and ground locations, while the outer net covered the remaining BGAs towards the perimeter of the package. Both nets were monitored during BL-TC testing. Only the outer net was monitored during BL-Drop testing, since failures typically occur on corner joints.

B. PCB Construction

Combination BL-TC and BL-Drop test boards were used to support Board Level Reliability (BLR) testing for both test types. The combination test board, which was designed with High Tg FR-4 (glass-reinforced epoxy laminate) material, is shown in Fig 1. The surface finish used was OSP and the PCB pad size was a diameter of 0.254mm. The test boards were 4.5in x 7.73in length and width and were 1.0mm thick with 10-layers. The board design followed IPC/JEDEC specifications [12, 13].

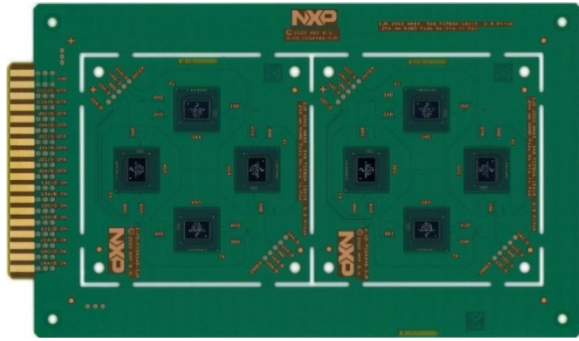


Fig 1: Eight units of daisy chain TV mounted on PCB

C. Stencil Design

A stainless-steel stencil with laser cut openings was used for the BL-TC and BL-Drop experimental analysis. The stencil apertures were 0.3 mm in diameter, and the stencil was 0.1 mm thick. The stencil utilized anti-adhesion advanced nanocoating for improved volume of paste release and uniformity shape of solder joints during SMT build.

D. Board Assembly

Solder paste was printed to boards using a no-clean, halide free, SAC305 ROL0 solder paste with Type IV (28 – 40 μm diameter) solder powder. Device placement onto the PCB was accomplished with a Nordson Dima automated pick and place. The fully populated PCB underwent reflow in a ten-heated zone and three-cooling zone convection belt furnace with a peak temperature at 240°C \pm 3°C. All assembled units were inspected with X-Ray prior to thermal cycling and JEDEC drop testing. A typical X-Ray post SMT is shown in Fig. 2.

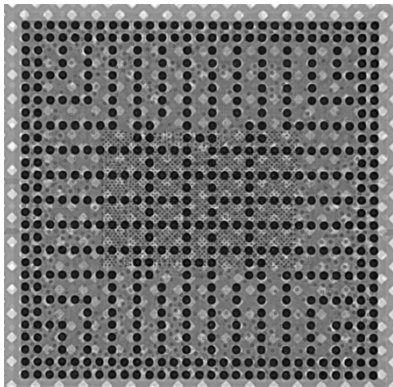


Fig. 2: A typical X-ray image of a package after SMT

E. Temperature Cycling

After assembly, the PCBs were placed into single chamber, 15-minute ramp and dwell, one hour total, -40 to 125°C thermal cycle. Representative profile is shown in Fig. 3.

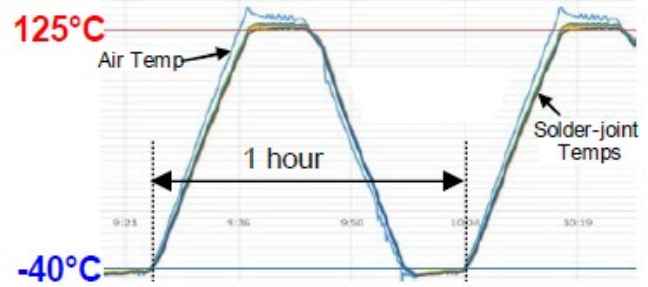


Fig. 3: Representative temperature profile of the temperature cycling chamber

Test nets were monitored in-situ during cycling using a 1.2mA current through each net. The Anatech STD256 event detector logged a failure when a net resistance exceeded 1000 ohms. The cycles to first electrical failure for each component were defined as the first cycle at which the daisy-chain resistance increases to 1000 Ω resistance or greater, followed by nine or more additional events per IPC-9701 [12]. The data was fit to two parameter Weibull distributions using MLE (maximum likelihood estimate). Comparisons were made based on first failure and characteristic life, η (Eta).

F. JEDEC BL-Drop Test

The drop testing requirements are outlined by the Joint Electronic Device Engineering Council (JEDEC) in the JESD22-B111A specification [13]. Eight JEDEC drop boards from each cell, for a total of 32 parts per cell, were subjected to JEDEC Condition B of 1500 G drop with a 0.5 ms duration, half-sine pulse. Testing was completed to 75% failure or to 1000 drops, whichever occurred first. All data was fit to two parameter Weibull distributions.

G. Failure Analysis Procedure

Failed unit was taken out of the test pool to perform flat-sectioning, and then failure isolation by manually measuring resistance of individual solder ball pairs. When the failed joint was identified, the unit was potted in epoxy and polished again to get the x-section. SEM (Scanning Electron Microscopy) was used to capture the image of a failed joint.

H. Test Matrix

DoE (design of experiment) legs evaluated are shown in Table 1. Both BL-TC, and BL-Drop tests were performed for all these DoE legs.

Table 1: DoE legs

DoE Leg	Lid Type	BGA Alloy
Leg 1	No Lid	SA-1
Leg 2	No Lid	SA-2
Leg 3	No Lid	SA-3
Leg 4	With Lid	SA-1
Leg 5	With Lid	SA-2
Leg 6	With Lid	SA-3

Example images of no lid, and lidded package are shown in Fig. 4 (a), and Fig 4 (b). BGA layout for both packages were same and showed in Fig 4 (c).

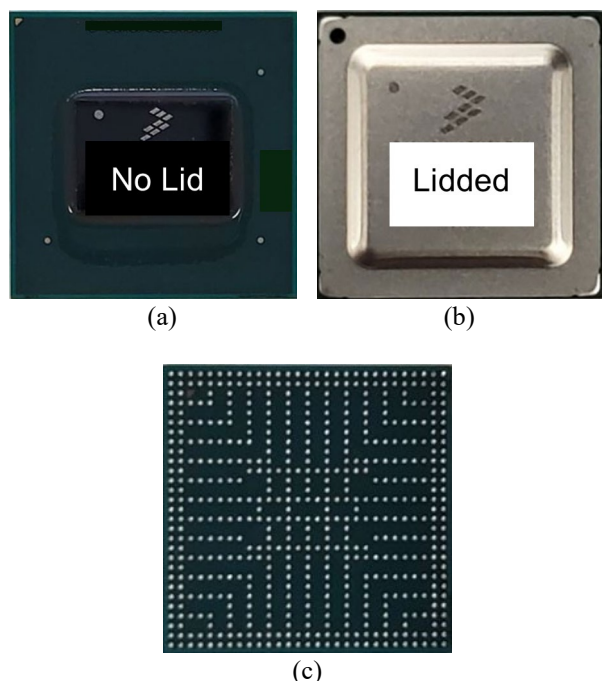
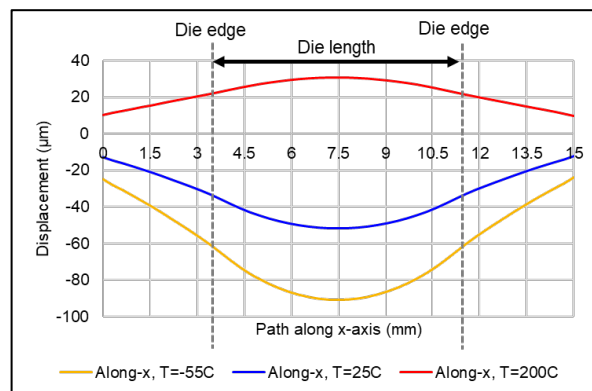


Fig 4: (a) Package without a lid, (b) Lidded package, and (c) BGA layout

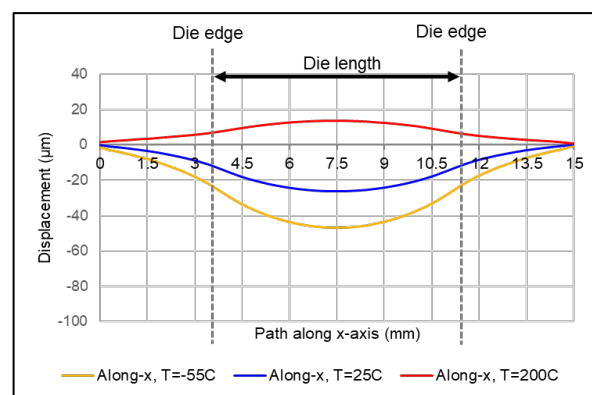
III. Results

A. Package Warpage

Fig. 5 shows package warpage modeling results for a) no lid and b) lidded package. In each graph, different color curve represents different test temperatures. Experimental results of Thermal Shadow Moire measurement of bare die package were used to calibrate the model, and then the model was extended to get the warpage data for the lidded package. It is evident from the figures that for all three test temperatures, lidded package has a significantly lower warpage compared to a bare die package. Lid helps to keep the package flat. A prior study [4] conducted by D. He et. al. on warpage comparison of bare die vs lidded package also reported the same conclusion.



(a)



(b)

Fig. 5: Simulated warpage profile for (a) no lid, and (b) lidded package

B. Board Level Temperature Cycling

The results of BL-TC test for all the DoE legs are shown in Table 2. For both bare die (no lid), and lidded package. SA-2, and SA-3, which are Bi added solder alloys, showed a more than 2x – 3x improvement in 1st fail, as well as characteristic life compared to SA-1. In a separate study conducted on Bi added lead-free solder [14], it was reported that addition of Bi and Ni helps to significantly improve mechanical strength, and elastic modulus of lead-free solder. Thus, we can conclude that for our study, Bi helped to increase strength of the solder alloy resulting a higher BL-TC life compared to SnAg solder.

For any solder alloy, lidded package showed more than 1.5x improvement in BL-TC performance compared to a bare die package. It is believed that a lid helps to keep the package flat, and hence reduce package warpage, which eventually helped to improve BL-TC life. Warpage data as shown in Fig 5 also confirms that a lidded package has less warpage compared to a bare die package. Weibull plot for all these six DoE legs is shown in Fig. 6.

Table 2: Board level temperature cycling results

Lid Type	BGA Alloy	First Fail (Cycles)	Characteristic Life, η (Cycles)
No Lid	SA-1	1589	2053
No Lid	SA-2	3206	4818
No Lid	SA-3	4568	6015
With Lid	SA-1	2632	3339
With Lid	SA-2	4825	7992
With Lid	SA-3	5495	7985

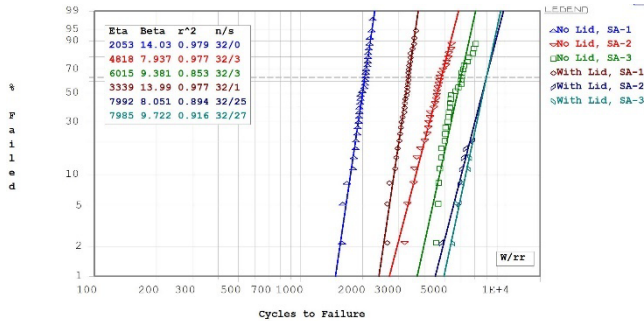


Fig. 6: Two parameter Weibull showing board level cycling results

C. BL-TC Failure Analysis

Failure location for all the failed units for each DoE legs was in the inner net. Failure analysis results, as shown in Fig. 7, tells that failure occurred in bulk solder and near IMC on the package side. It is believed that the combine effect of mostly shear stress coming from CTE mismatch between package, and PCB, as well as the mostly tensile stress coming from package warpage is maximum near the die shadow area causing this BGA failure. The presence of crack on the package side can be attributed to the solder mask defined (SMD) pad on the package side, compared to non-solder mask defined (NSMD) pad on the PCB side.

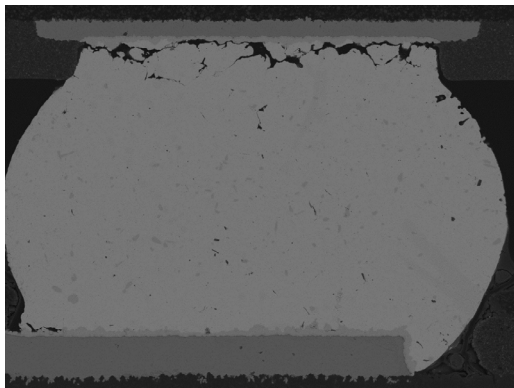


Fig. 7: Cross-section image of a solder joint failed during board level temperature cycling (No lid, SA-3)

D. Board Level Drop

Table 3 summarize the results of BL-Drop tests. It is evident that SA-1 solder, which do not have any Bi/Cu/Ni, showed superior BL-Drop performance compared to SA-2, and SA-3. It appears from this results that Bi reduces ductility of the solder joints and hence poor drop test performance of SAC-Bi solders compared to SnAg solder. As discussed earlier, a lid helps to increase package stiffness and hence lidded packages showed inferior drop test performance compared to a bare die package. Weibull plot of BL-Drop test is shown in Fig 8.

Table 3: Board level drop test results

Lid Type	BGA Alloy	First Fail (Drops)	Characteristic Life, η (Drops)
No Lid	SA-1	48	116
No Lid	SA-2	23	141
No Lid	SA-3	40	78
With Lid	SA-1	26	67
With Lid	SA-2	22	45
With Lid	SA-3	7	49

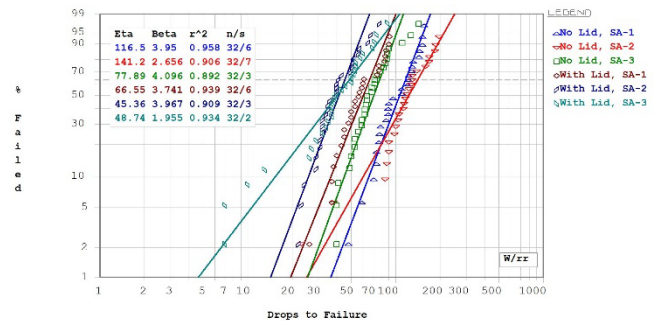


Fig. 8: Two parameter Weibull showing board level drop results

E. BL-Drop Failure analysis

Location of failing BGA was near the package corner. Cross-section of failing joint, and shown in Fig 9, tells that failure occurred on the package side along the IMC region.

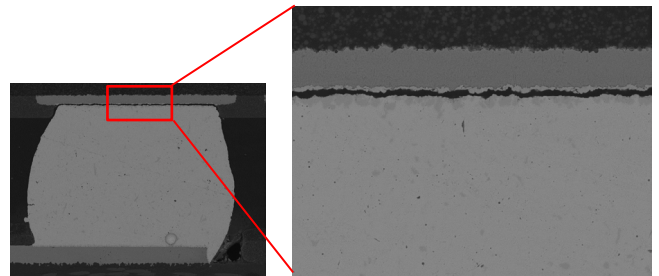


Fig 9: Cross-section image of a solder joint failed during board level drop test (No lid, SA-3)

IV. CONCLUSION

BL-TC, and BL-Drop performance of a flip chip BGA test vehicle with 15x15mm body was evaluated for two different package constructions (no lid vs. lidded). Mechanical modeling and experimental data showed that lid helps to reduce package warpage, which eventually helps to increase BL-TC life of the package. On the other hand, addition of a lid reduces BL-Drop life. This can be attributed to the increased package stiffness caused by the lid.

Bi, along with Cu, and Ni helps to significantly (2x-3x) improve BL-TC performance of FC-BGA package. However, Bi added lead-free solders (SA-2, SA-3) displayed inferior drop test performance compared to solder without any Bi content (SA-1).

Data presented in this paper can be useful in package design, and material selection based on target application, and reliability requirement.

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