Bonding constraint-induced defect formation at Si-dielectric interfaces and internal interfaces in dual-layer gate dielectrics

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As aggressive scaling of integrated circuits continues into the next century, insulators with dielectric constants higher than SiO_2 with different local bonding arrangements will be required to increase gate dielectric capacitance in field effect transistor devices. An important issue in semiconductor device physics is determining whether differences between the bonding at (i) $Si–SiO_2$ interfaces and (ii) interfaces between crystalline Si and alternative gate dielectric materials will result in increased densities of electrically active defects at the alternative dielectric interfaces, thereby limiting targeted levels of performance and reliability. In particular, it is important to understand from a chemical bonding perspective why $Si–SiO_2$ interfaces display both low defect densities and high reliability, while other interfaces such as $Si–Si_3N_4$ with similar bonding chemistry, display defect densities that are at least two orders of magnitude higher. Building on previously established criteria for formation of low defect density glasses and thin films, constraint theory is extended to crystalline Si-dielectric interfaces that go beyond $Si–SiO_2$ through development of a model that is based on the average bonding coordination at these interfaces. This approach identifies quantitative bonding criteria that distinguish between device-quality and highly defective interfaces. This extension of constraint theory is validated by its application to interfaces between Si and stacked silicon oxide/nitride dielectrics which demonstrates that as in bulk glasses and thin films an average coordination, $N_{av}>3$ yields increasingly defective interfaces. Finally, the universality of this application of constraint theory is demonstrated by showing that defect densities scale with overcoordination in the same way in thin films and at interfaces. © *1999 American Vacuum Society.*
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I. INTRODUCTION

As source-drain distances in field effect transistors (FETs) are scaled to <150 nm and ultimately to ~ 50 nm, the oxide equivalent thickness, $t_{ox\text{-}eq}$ of gate dielectrics must be reduced initially to <2 nm, and then to <1 mn. Values of $t_{ox\text{-}eq}$ are calculated from the experimentally determined gate capacitance in the accumulation region, C_{acc}, by assuming that the dielectric film or composite multilayer stack is equivalent to an SiO_2 film with a static dielectric constant, k_0, of 3.8, so that

$$t_{ox\text{-}eq}=k_0\epsilon_0 A/C_{acc}, \tag{1}$$

where ϵ_0 is the permittivity of free space, and A is the area of the capacitor. C_{acc} can be obtained directly from experimental $C–V$ data for *thicker* films, $t_{ox\text{-}eq}>2.5–3$ nm, at accumulation voltages $>\sim 3$ V, or from a fit to capacitance–voltage data for *ultrathin* dielectrics when $t_{ox\text{-}eq}<2.5$ nm.

At $t_{ox\text{-}eq}<1.5$ nm direct electron tunneling through SiO_2 films at ~ 1 V exceeds 1 A/cm^2, a value at which circuit performance and reliability are degraded. One approach to reduce direct tunneling current is to replace SiO_2 by physically thicker films with higher dielectric constants. The first step is this replacement process has been to substitute Si_3N_4 for SiO_2 so that the film thickness can increased by ~ 2, the ratio of the respective dielectric constants. Successful substitution requires (i) that the Si_3N_4 bulk films have fixed charge and trap densities that are comparable to SiO_2, i.e., $<1\times 10^{11}\,cm^{-2}$, (ii) that the interfaces between Si and Si_3N_4 have fixed charge and trap densities that are comparable to $Si–SiO_2$, i.e., $<5\times 10^{10}\,cm^{-2}$, and (iii) that changes in other material and interface properties, such as tunneling masses and barriers do not offset reductions in tunneling current anticipated from increased physical thickness. Recent experi-

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mental studies have demonstrated that reductions in electron tunneling masses in Si_3N_4 thin films, and in conduction band offset energies between Si_3N_4 and Si compensate almost exactly for increases in dielectric constant that allows the use of physically thicker SiO_2 films.[1] These aspects of Si_3N_4/SiO_2 substitutions are addressed in more detail elsewhere, and suggest that composite SiO_2/Si_3N_4 gate dielectric films may not satisfy many of the targeted goals for aggressive scaling required in advanced the most FET devices.[2]

With the exception of issues relating to tunneling currents, it has been demonstrated that bulk Si_3N_4 films prepared by remote plasma-enhanced chemical vapor deposition (RPECVD) at 300 °C, and annealed at 900 °C for at least 30 s in an inert, nonoxidizing ambient have bulk properties comparable to thermally grown SiO_2 when incorporated into capacitors with stacked oxide/nitride/oxide (ONO) dielectrics with $Si-SiO_2$ or nitrided $Si-SiO_2$ interfaces,[3,4] or in FETs with stacked oxide/nitride (ON) dielectrics with $Si-SiO_2$ or nitrided $Si-SiO_2$ interfaces.[5–7] In contrast to nitrides prepared by other techniques, such as rapid thermal CVD (RTCVD),[8] or jet vapor deposition (JVD),[9] which generally require an oxidizing anneal after film deposition to form oxynitride alloys with low bulk defect densities, the annealed RPECVD nitrides derive their low bulk defect densities from incorporation of ~10–15 at. % hydrogen.[4,7] The as-deposited RPECVD films have approximately 20–30 at. % bonded hydrogen, mostly in *near neighbor* in Si–H and SiN–H arrangements,[10–12] and after the 900 °C anneal, the remaining 10–15 at. % is bonded in *isolated* SiN–H arrangements. Detailed studies of the specific hydrogen bonding arrangements with nearest-neighbor Si–H and/or SiN–H groups, that readily evolve H_2 molecules upon annealing, are discussed in detail elsewhere.[11,12] This article focuses on issues relative to $Si-Si_3N_4$ interface bonding and defects.

It is shown that a direct substitution of Si_3N_4 for SiO_2 in FETs is limited by charged defects at the $Si-Si_3N_4$ interface that will be shown to result from constraints imposed by overcoordination in the spirit of Refs. 13–15. In particular, this article extends constraint theory, originally developed for bulk oxide and chalcogenide bulk glasses by Phillips[13,14] and thin films by Lucovsky and Phillips[15] and thereby provides a quantitative approach to explaining the significant differences in defect properties between $Si-SiO_2$ and $Si-Si_3N_4$ interfaces. Another paper at this conference by Misra and co-workers,[7] presents electrical measurements on both *p*-channel (hole conducting) and *n*-channel (electron conducting) FETs, and concludes that increases in the density of donor-like defects in the lower half of the gap *p*-channel FETs render these devices totally dysfunctional. This article presents complimentary studies of *p*-channel FETs and capacitors with $Si-Si_3N_4$ interfaces with essentially the same result. The results reported in this paper and in Ref. 7 further demonstrate that insertion of ~0.6 nm (or about two molecular layers) of SiO_2 between the Si substrate and the Si_3N_4 film deposited by RPECVD at 300 °C and annealed in an inert ambient for at least 30 s at 900 °C restores interface devices properties to essentially the same level as in devices with thermally grown $Si-SiO_2$ interfaces. This dramatic change in interfacial defect properties will also be explained in the context of the extension of constraint theory.

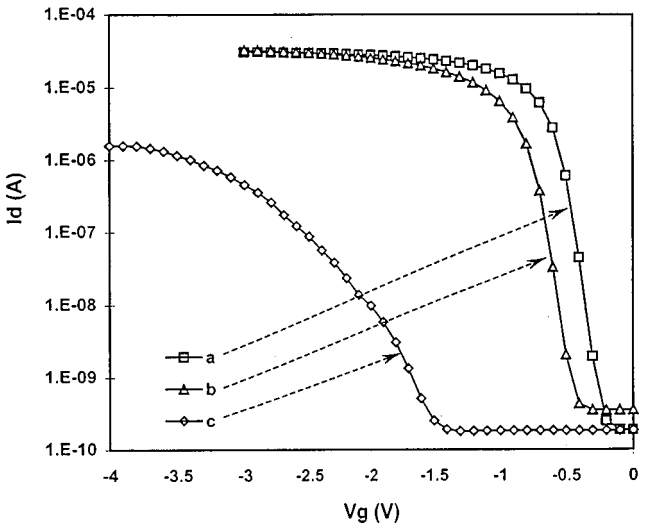

FIG. 1. Drive current–gate voltage (I_d-V_g) characteristics for PMOSFETs with $t_{ox\text{-}eq}\sim 2$ nm: (a) a 1.5 nm oxide separating a 1.0 nm nitride from the Si substrate, (b) a 0.6 nm oxide separating a 2.4 nm nitride from the Si substrate, and (c) a 4 nm nitride layer. The threshold voltage shift between (a) and (b) is due in part to substrate doping differences (0.16 V) and in part to positive charge at the oxide-nitride interface (0.04 eV).

Section II presents experimental results for $Si-Si_3N_4$ interfaces and Sec. III discusses constraint theory as proposed originally for bulk glasses[13,14] and thin films.[15] The application of constraint theory to thin films is used to develop quantitative relationships between departures from ideal average bonding coordination and defect concentrations, which serve as a basis for the development of a quantitative approach to defects semiconductor-dielectric interfaces and internal dielectric interfaces. Section IV extends constraint theory to interfaces and Sec. V applies this extended theory to the experimental results of Sec. II. The model is further generalized in Sec. V to interfaces between Si and the so-called *alternative high-K dielectrics* such as TiO_2 (Ref. 16) and Ta_2O_5 (Ref. 17) that are being considered as replacements for SiO_2 in aggressively scaled FET devices. In Sec. V, the theory is applied to internal interfaces in stacked dielectrics, such as the oxide/nitride interfaces of Refs. 1–6. Finally, in Sec. VI, the universality of quantitative defect scaling with overcoordination in thin films and at interfaces is demonstrated.

II. EXPERIMENTAL RESULTS FOR $Si-Si_3N_4$ INTERFACES

Figure 1 displays current–voltage, $I-V$, curves for *p*-channel FETs for different gate dielectrics with $t_{ox\text{-}eq}$ ~2 nm: (i) a 4 nm RPECVD nitride, (ii) a 0.6 nm plasma-oxide with a 2.4 nm RPECVD nitride, and (iii) a 1.5 nm thermal oxide with a 1.0 nm RPECVD nitride. The substrates are Si(100), doped to $5\times10^{17}\,cm^{-3}$ for (i) and (iii) 1.1

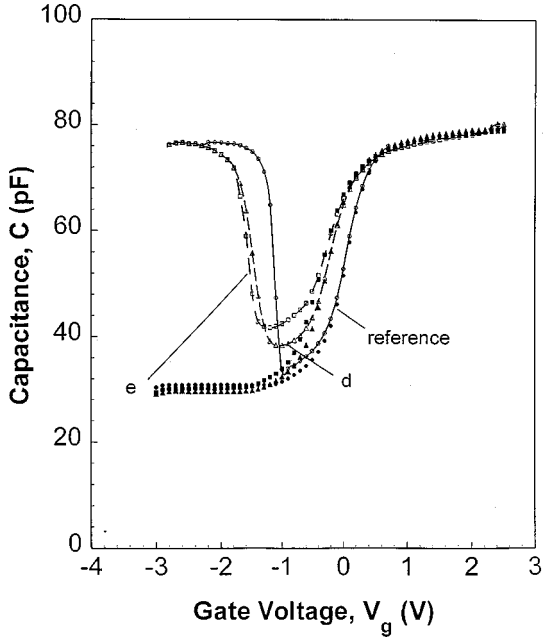

FIG. 2. $C-V$ characteristics demonstrate shift in flatband voltage due to positive charge, and increased separation between high frequency and quasi-static plots due to interface trapping accompanying direct deposition of thin nitride films onto Si. Each of these capacitors has $t_{ox\text{-}eq}\sim 2$ nm: (i) a reference oxide and (ii) two stacked NO structures with the nitride layer in contact with the Si substrate. The nitride layer thickness is 0.4 nm for (d), and 0.8 mn for (e).

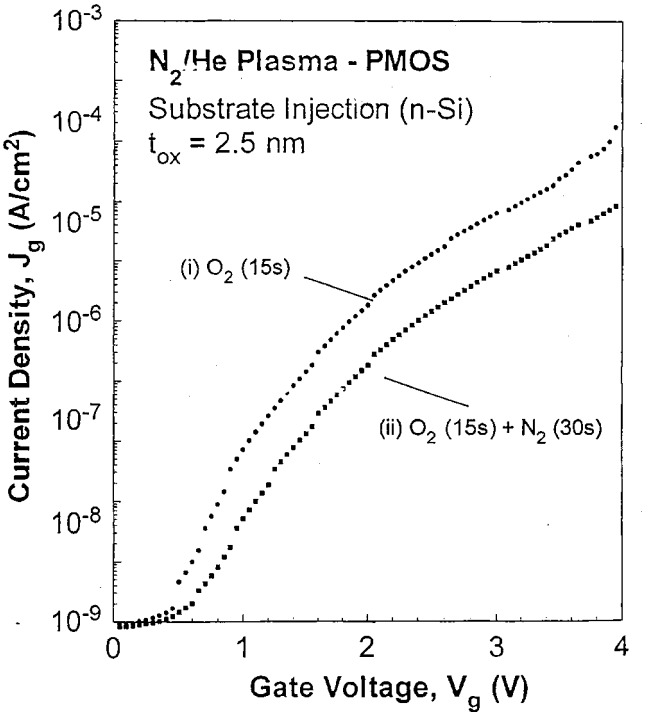

FIG. 3. $J-V$ characteristics for capacitors prepared on lightly doped n-type Si(100) with n^+ polycrystalline Si gate electrodes for $t_{ox\text{-}eq}\sim 2.5$ nm. The upper curve is for a device with an RPECVD SiO_2 layer and a non-nitrided $Si-SiO_2$ interface, and the lower curve is for a device with an RPECVD SiO_2 layer and a monolayer nitrided $Si-SiO_2$ interface.

$\times 10^{18}\,cm^{-3}$ for (ii). $I-V$ traces for (i) and (iii) display excellent turn-on behavior and the same current drive, with differences in threshold voltage between (ii) and (iii) derived primarily from differences in substrate doping noted above ($\sim$0.160 V out of the 0.200 V difference). In contrast, for the FET with the 4 nm nitride: (i) threshold voltage is shifted to negative voltages by >1 V, (ii) turn-on is soft, and (iii) channel drive current is reduced by ~ 50. Figure 2 displays capacitance–voltage, $C-V$, characteristics for p-type metal–oxide semiconductor (PMOS) devices with $t_{ox\text{-}eq}\sim 4.3$ nm: one with a plasma-oxide, and two with stacked dielectrics with RPECVD nitride interface layers of 0.4 and 0.8 nm, respectively. Shifts in threshold (and flatband) voltage relative to $Si-SiO_2$ indicate increased fixed charge for devices with nitride interfaces: $\Delta q_f = C_{ox}\Delta V_{th}(\text{or}\,\Delta V_{fb})$. Qualitatively similar results have been obtained for n-type metal–oxide–semiconductor (NMOS) devices with nitride layer interfaces.[7] Figure 3 displays current density–voltage, $J-V$, plots for a capacitor fabricated on lightly doped n-type substrates and n^+ polycrystalline Si gate electrodes for an oxide thickness of 2.5 nm as determined from analysis of $C-V$ data.[18] There are two types of devices shown in Fig. 3: (i) the device exhibiting the higher current was prepared by remote plasma processes that resulted in a non-nitrided interface, whereas (ii) the device exhibiting reduced tunneling current was prepared by remote plasma process that resulted in a monolayer nitrided interface.[18] The $C-V$ data establish that the flatband voltages are determined by the substrate and polycrystalline Si doping and not changed by interface nitridation. For this pair of devices with the same effective thickness, the tunneling current is reduced by the monolayer interface nitridation, indicating that insertion of a monolayer of nitride at the $Si-SiO_2$ interface is beneficial. This means that monolayer interface nitridation is *qualitatively different* from having one or more molecular layers of nitride present the interface with the crystalline Si substrate.

Summarizing the data in Figs. 1–3 and data presented in other papers,[19,20] the $I-V$ and $C-V$ data establish that: (i) that deposition of Si_3N_4 films by RPECVD at Si-dielectric interfaces degrades interface properties, (ii) that interface properties can be effectively restored by interposing an ultrathin ($\sim$0.6 nm) layer of plasma-grown SiO_2 between the Si substrate and the RPECVD Si_3N_4 film, and finally, (iii) monolayer interface nitridation either during remote plasma oxidation,[19] or after remote plasma oxidation[18] resulted in improvements in interface properties, rather than degradation.[7,20]

III. CONSTRAINT THEORY FOR BULK GLASSES AND THIN FILMS

Phillips showed that fully bonded, strain-free three-dimensional continuous random networks (CRNs) can be formed at compound and alloy chemical compositions by counting average bond constraints associated with applicable valence force fields, C_{av}, and then matching constraints to the dimensionality of the network structure.[13–15] For three-dimensional melt-quenched glasses these fields are simply

bond-stretching and bond-bending valence forces. The quantitative relationships between (i) local bonding coordination and geometry, and (ii) constraints are presented in the next paragraph. Under the condition of exactly matching constraints to network dimensionality, the average coordination number/atom, N_{av}, is 2.4, corresponding to the well-known glass-formers arsenic trisulfide and arsenic triselenide, As_2S_3 and As_2Se_3, respectively. Good glass formation has also been obtained in the Ge–S and Ge–Se systems, even at the compound compositions (GeS_2 and $GeSe_2$), where $N_{av}=2.67$, and $C_{av}=3.67$, exceeding the optimum value of 3. Recent studies have shown ideal-glass formation in Ge–S and Ge–Se alloy systems occurs at a chalcogenide-rich composition corresponding to $N_{av}\sim 2.45$ with a value of C_{av} close to 3.[21] For the SiO_x ($x\leqslant 2$) system, O-atom bond-bending forces are ineffective at fictive (or quench) temperatures above the effective viscoelastic relaxation temperature of $\sim$1000 °C, so that the applicable forces in bulk-quenched glasses are bond-stretching forces on both atoms, and bond bending forces only on the Si atoms. $N_{av}=2.67$ at the composition of SiO_2, and the number of constraints per atom, neglecting the O-atom bond-bending forces, is also $C_{av}=3$. This explains the ease of glass formation by quenching from melts exceeding the viscoelastic relaxation temperature.[13–15]

As indicated above, the calculation of C_{av} is based on counting constraints associated with valence forces. The number of bond-stretching constraints/atom is $m/2$, where m is the coordination number, and for three-dimensionally coordinated atoms, the number of bond-bending constraints is $2m$-3.[13] Applied to As_2S_3, the number of bond-stretching constraints is equals 6, and the number of bond-bending constraints is equals 9, so that the total number of constraints is 15, and $C_{av}=3$. Applied to SiO_2 glasses that are quenched from temperatures exceeding the viscoelastic relaxation temperature, the total number of bond-stretching constraints is 4, and the number of bond-bending constraints is associated with Si atoms is 5, so that $C_{av}=3$, as well.

The bonding of N in Si–N and Ge–N systems is planar or effectively two dimensional with the N atom bonded to three Si or Ge atoms in an NX_3 geometry, $X=$Si or Ge.[22] This bonding arrangement is stabilized by $p\pi$-$d\pi$ interactions in which the nonbonding pair of the N atom in p_z orbital perpendicular the Si(Ge–N) bonding x-y plane backdonates to unoccupied antibonding Si or Ge orbitals that have a d^3p symmetry. As a consequence of this planar bonding of N atoms in Si–N alloys, the number of N-atom bond-bending constraints is reduced to m-1, so that for Si_3N_4, $C_{av}=5.0$, and $N_{av}=3.43$. However, this value of C_{av} is significantly higher than the network dimensionality so that glass formation from the melt does not occur.

The optimum value of $C_{av}=3$ applies to ideal melt-quenched networks, and this criterion must be modified for vapor-deposited films prepared at temperatures well below the glass transition temperature. These films are generally not strain free, and contain voids as well.[14] For nonhydrogenated a-Si $N_{av}=4$ and $C_{av}=7$, and hydrogen-free a-Si films produced by sputtering generally contain high concentrations of dangling bonds, e.g., the concentration of Si dangling bonds detected by electron spin resonance is $\sim 10^{18}\,cm^{-3}$ after optimized thermal annealing.[23] The hydrogenated films also have internal voids which serve to reduce strain, thereby reducing the effective number of dangling bond defects below a value that is simply determined by C_{av}.[15] N_{av} and C_{av} can be reduced further by hydrogenation leading to significant reductions in the dangling bond density. For example, for an a-Si:H alloy with 10–15 at. % H, $N_{av}=3.5$, and $C_{av}=5.7$. These alloys display Si atom dangling bond densities of order $5\times 10^{16}\,cm^{-3}$, which is low enough for promoting good semiconductor properties as for example high substitutional doping efficiencies, thereby allowing the use of these doped a-Si:H films in photovolatic cells and thin film transistors (TFTs).[24]

TABLE I. Calculated values of N_{av} and N_{av} for melt-quenched and deposited dielectrics.

Material	Atomic coordination and (dimensionality) bulk-quenched glasses		N_{av}	C_{av}
$As_2S(Se)_3$	As: 3(3)	S(Se):2(3)	2.40	3.00
$GeS(Se)_2$	Ge: 4(3)	S(Se):2(3)	2.67	3.67
$GeS(Se)_{3.5}$	Ge: 4(3)	S(Se):2(3)	2.44	3.10
SiO_2	Si:4(2)O: 2[a]		2.67	3.00
	Plasma-deposited films			
SiO_2	Si: 4(3)O: 2(3)		2.67	3.67
Si_3N_4	Si: 4(3)N: 3(2)		3.43	5.00
a-Si:N:H[b]	Si: 4(3), N: 3(2), H: 1(1)		2.68	3.58
a-Si	Si: 4(3)		4.00	7.00
a-Si:H[c]	Si: 4(3)H: 1(1)		3.50	5.70

[a]Neglects bond-bending constraints for O atoms.
[b][N]=0.42, [Si]=0.28, and [H]=0.30.
[c][Si]=0.8, [H]=0.2.

Table I includes calculated values of N_{av} and C_{av} for ideal melt-quenched glasses, and for thin films. As shown in Fig. 4, increases in C_{av} correlate linearly with increases in N_{av} so that either descriptive can be applied to bulk-quenched glasses or plasma-deposited amorphous materials and as shall be demonstrated in the next section, to crystalline Si-dielectric interfaces and internal dielectric interfaces as well. In the remainder of this article, the N_{av} metric will be used in discussing scaling of defects.

As discussed above, if both bond-bending and stretching forces are present, the optimal average coordination number, N^*_{av}, which matches constraints to degrees of freedom is 2.4 as in $As_2S(Se)_3$, however, for SiO_2 bulk glasses, $N^*_{av}=2.67$ is optimal because bond-bending forces at O atoms are too weak to function as significant constraints at growth or annealing temperatures.[15] For overconstrained networks such as in thin film Si_3N_4 ($N_{av}=3.43$), Si-atom stretching constraints are stronger than bending constraints, so that strain energy accumulates along the bending constraints. The average Si–N–Si bond angle θ_{ij} is distorted from the ideal local value θ^*_{ij} by an amount

$$\delta\theta\propto\delta N^*_{av}=N_{av}-N^*_{av}. \quad (2)$$

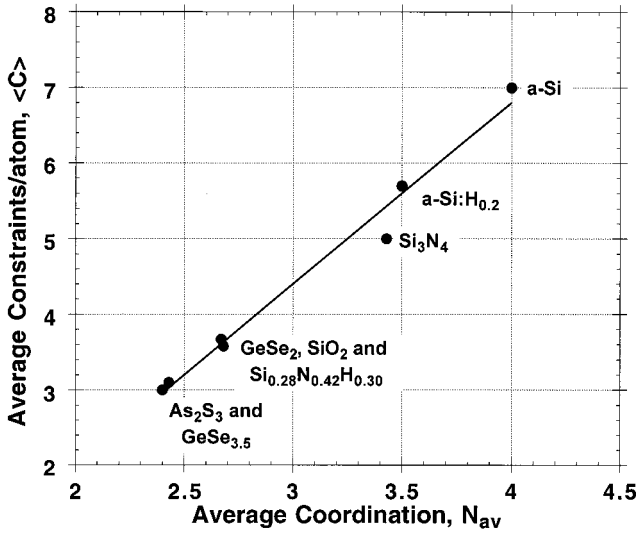

FIG. 4. Bonding constraints per atom, C_{av} vs average number of bonds per atom, N_{av}, for bulk-quenched glasses and deposited thin films (see Table I). The line in this figure is a least-squares fit the data points, excluding the value for bulk-quenched SiO_2.

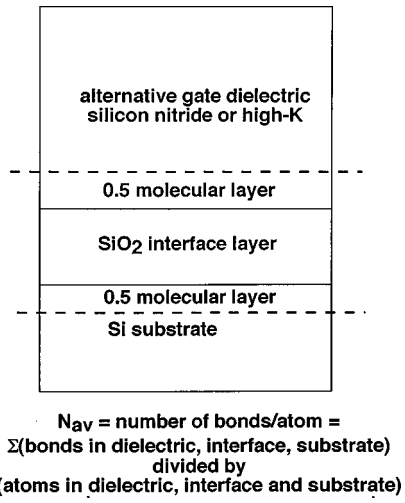

FIG. 5. Schematic representation of interface constituents used in the calculation of N_{av} for Si-dielectric interfaces.

Since total strain energy is proportional to $(\delta\theta)^2$,[25] it is then expected that defect creation, e.g., dangling Si or N bonds, will be proportional to $\{N_{av}-N_{av}^*\}^2$. Similar considerations apply to other thin film materials as well. Experiments have shown that $N_{av}\sim 3$ represents a reasonable demarcation criterion between low defect density ($\sim 10^{16}\,cm^{-3}$), and increasingly defective materials.[15] Equation (2) is also consistent with the structure of noncrystalline solids in which the statistical distribution of bond angles is much larger than the statistical spread in bond lengths, δr.

IV. EXTENSION OF CONSTRAINT THEORY TO Si-DIELECTRIC INTERFACES

Before applying constraint theory to Si-dielectric interfaces, it is important understand other factors than can play a role in interface bonding and the associated electronic structure. There are at least four factors related to bonding that can promote formation of interfacial defects; these are (i) differences between electronic charge required for bonding and for balancing the nuclear charge of the constituent atoms as first identified by Harrison and co-workers for group IV–group III–V heterojunctions such as Ge–GaAs (heterovalent as opposed to isovalent bonding),[26] (ii) interfacial dipoles produced by charge transfer between the Si substrate and the gate dielectric material,[27,28] (iii) molar volume differences between the Si substrate and gate dielectric that produce interfacial strain, and generally require interfacial dangling bond formation, and finally, (iv) overconstrained bonding due to differences between the average number of bonds per atom on each side of the interface.[29] Going down this list in order; (i) is not a consideration since both SiO_2 and Si_3N_4 can bond to a Si substrate by forming isovalent bonds between substrate Si atoms and either O or N atoms of the respective dielectrics. Second, it has been shown that interfacial charge transfer dipoles in (ii) result in relatively small differences in band offset energies at the $Si–SiO_2$ and $Si–Si_3N_4$ interfaces, and that charge transfer is smaller at the nitride interfaces that at oxide interfaces. Therefore it is not likely that these dipoles play a determinant role in defect or defect precursor formation since the defect densities at the $Si–Si_3N_4$ interfaces are larger than those at the $Si–SiO_2$ interfaces. Interfacial strain as in (iii) has been shown to be an important factor in interface quality. It has been shown that for thermally grown oxides on Si in a thickness range that extends to at least 100 nm, the residual density of interface traps, D_{it}, scales linearly with integrated strain in the oxide layer.[30] Since the molar volume mismatch between Si_3N_4 and Si is reduced with respect to that of SiO_2 to Si, residual interface strain cannot be the driver for the increased defect concentrations at $Si–Si_3N_4$ interfaces. The remainder of this section focus on the final interface consideration in (iv) dealing with bonding constraints.

The abruptness of $Si–SiO_2$ interfaces suggests that the defect density of thermally grown oxides and optimally annealed deposited oxides is a characteristic function of their bonding chemistry and structure. Experience with good glass-formers such as SiO_2 and As_2Se_3 has shown that as long as only single bonds are present charge transfer plays a minor part in determining structure. The major factor is the network stress which arises for a given space-filling bonding topology, and this factor is expected to extend to interfaces as well.

Extension of constraint theory to Si-dielectric-interfaces considers three interfacial contributions to N_{av}: (i) the Si substrate represented by one-half a Si atom, (ii) an ultrathin oxide or nitride interfacial layer (0.3–0.6 nm), and (iii) the bulk dielectric by one-half a molecular layer (see Fig. 5). Table II includes calculations of N_{av} for representative Si-dielectric interfaces. When a demarcation level $N_{av}\sim 3$ is applied between device-quality and highly defective interfaces, these calculations are in excellent agreement with experiment (see Figs. 1 and 2). For example, the model con-

TABLE II. Average bonding coordination at Si-dielectric interfaces.

Material system	Average coordination (N_{av})	Electrical quality
Si–SiO_2 (1.5 molecular layers)	2.8	excellent
Si–Si_3N_4 (1.5 molecular layers)	3.5	very poor (Fig. 1)
Si–{SiO_2}(t)–Si_3N_4	t=0.5 nm: 3.1	excellent (Fig. 1)
t=oxide layer thickness	t=1.5 nm: 2.9	excellent (Fig. 1)
Si–{Si_3N_4}(t)–SiO_2	t=0.4 nm: 3.3	poor (Fig. 2)
t=oxide layer thickness	t=0.8 nm: 3.4	poor (Fig. 2)
Si–N–SiO_2 {1 monolayer}	2.8	excellent (Ref. 18)
Si–$(SiO_2)_{0.9}\{Si_3N_4)_{0.1}$	10 at. % N: 2.9	very good (Ref. 31)
Si–$(SiO_2)_{0.7}\{Si_3N_4)_{0.3}$	26 at. % N: 3.1	poor (Ref. 31)
Si–TiO_2}[a] (1.5 molecular layers)	4.0	unreported
Si–Ta_2O_5}[b] (1.5 molecular layers)	3.5	unreported
Si–Al_2O_3}[c] (1.5 molecular layers)	3.6	unreported

[a]Average coordination: [Ti]=6, [O]=3.0 (rutile/anatase bonding).
[b]Average coordination: [Ta]=6, [O]=2.4 (Ref. 32).
[c]Average coordination: Al=[4.5], [O]=3.0 (3:1 ratio of tetrahedral to octahedral sites, see Ref. 33).

firms that Si–SiO_2 interfaces are expected to display excellent interface properties ($N_{av}\sim 2.8$), whereas Si–Si_3N_4 interfaces are not ($N_{av}\sim 3.5$). Equally important, the calculations demonstrate that interposition of ultrathin SiO_2 layers between Si and Si_3N_4 results in values of $N_{av}\sim 3$ consistent with very good electrical properties as in Fig. 1, whereas interposition of ultra thin Si_3N_4 layers between Si and SiO_2 results in $N_{av}>3$ and degraded electrical performance as in Fig. 2 Figure 6 is based on the data of Figs. 1 and 2, and demonstrates that defect scaling for bulk films, Eq. (1), also holds at interfaces. The defect densities, in this case increases fixed positive charge, Δq_f,

$$\Delta q_f = C_{ox}\Delta V_{th}(\text{or } \Delta V_{fb}), \tag{3}$$

scale with shifts of the flatband or threshold voltages (ΔV_{fb} or ΔV_{th}), from values anticipated from considerations of the substrate doping and gate electrode material; is the oxide capacitance, $C_{ox}\sim C_{acc}$.

The model can also been applied to interfaces between Si and (i) silicon oxynitride alloys and (ii) alternative high-K dielectrics. For oxynitride alloys a maximum interfacial N incorporation for low defects of ~15 at. % as indicated by the value of N_{av} in Table II; is consistent with results of Vogel *et al.*[31] The model calculations for Ta_2O_5, TiO_2, and Al_2O_3 explain the necessity for ultrathin SiO_2 layers between the Si substrate and these high-K oxides (see, for example, Ref. 17). The model thereby establishes important limitations for extension for gate dielectric interfaces other than Si–SiO_2. Specifically: (i) Si_3N_4 cannot be substituted for SiO_2 at Si substrates; and (ii) substitution of more highly coordinated high-K dielectrics such as Ta_2O_5, etc., requires SiO_2, or monolayer nitrided SiO_2 interfaces, thus establishing a limitation on the extent to which $t_{ox\text{-}eq}$ can be reduced below 1 nm.

V. EXTENSION OF CONSTRAINT THEORY TO INTERNAL DIELECTRIC INTERFACES

As noted above, the integration of high-K alternative gate dielectrics into aggressively scaled devices for ultrahigh density integrated circuits will require compliant interface layers to bridge reduce bond constraint interfacial defects. It is

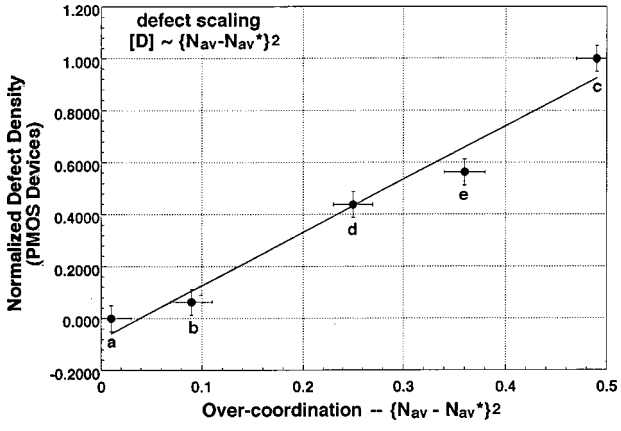

FIG. 6. Plot of normalized defect density as a function of $\{N_{av}-N^*_{av}\}^2$, where N^*_{av} is the value for an ideal Si–SiO_2 interface. Data points a, b, and c are from Fig. 1, and d and e from Fig. 2, and the solid line is a linear regression analysis of the data points.

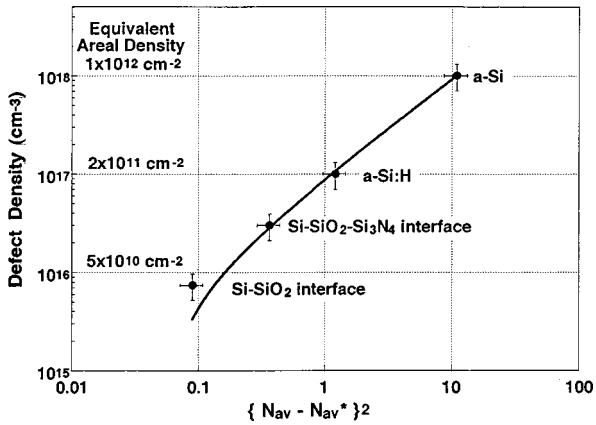

FIG. 7. Log-log plot of volume defect density vs $\{N_{av}-N^*_{av}\}^2$, where $N^*_{av}=2.4$ for ideal three-dimensional network structures. The solid line is a linear regression analysis of the data points.

therefore necessary to consider bond-constraint induced defects at the internal dielectric layer and the high-K materials. This has been studied in ONO stacks, where the density of positively charged defects at ON interfaces, well separated from the Si–SiO_2 interface ($\sim$5 nm), was found to be $\sim 3 \times 10^{11}\,cm^{-2}$ for stacked dielectrics deposited by RPECVD at 300 °C, and annealed in inert ambients at 900 °C.[2] Similar defect densities have been reported[20] for internal ON interfaces even when the SiO_2 layer thickness is reduced to <1 nm.

A two component model similar to the one developed earlier in this article for the Si-dielectric interface structure has been used as a basis for this calculation. In this model, N_{av} is simply the average of the N_{av} values of the interface constituents, so for SiO_2–Si_3N_4 internal interfaces, $N_{av} \sim 3$, consistent with the interfacial defect concentrations in the low $10^{11}\,cm^{-2}$ regime. Since N_{av} values are also $\sim$3.5 for other candidate high-K materials such as Al_2O_3 and Ta_2O_5, similar interfacial defect densities are anticipated. This in agreement with experimental results reported for stacked SiO_2–Ta_2O_5 dielectrics.[17] The effect of these interfacial defects on performance and reliability has yet to be fully evaluated, but it is expected to a factor due to the large change in the longitudinal electric field at internal dielectric interfaces between SiO_2 and alternative high-K dielectric materials. The electric field in the SiO_2 will be the same as that calculated for a homogeneous oxide with a thickness equal to $t_{ox\text{-}eq}$, whereas the field in the high-K dielectric is reduced by the dielectric constant ratio.

VI. SUMMARY

It has been shown how constraint theory originally developed for bulk glasses[13,14] and thin films,[15] can be extended to (i) interfaces between crystalline Si and noncrystalline gate dielectric materials such as SiO_2, Si_3N_4, etc., and (ii) internal interfaces in stacked gate dielectrics such as SiO_2–Si_3N_4, SiO_2–Ta_2O_5. For the thin film materials, and the two interfacial materials systems, $N_{av} \sim 3$ represents a demarcation between device-quality and increasingly defective materials and interfaces. This is illustrated in Fig. 7, which is a log-log plot of defect density versus $\{N_{av} - N^*_{av}\}^2$. The data in this plot include different thin film materials and dielectric interfaces. By including both thin film a-Si and a-Si:H, the general trend in Fig. 7 establishes the universality of the approach to interfacial bonding constraints developed in this article.

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