Boosted Readout for CMOS APS Pixels

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***Abstract*—In order to reduce power consumption and improve low-voltage operation capability of standard three transistor (3T) CMOS active pixel sensor (APS), new pixel readout is proposed utilizing supply boosting technique (SBT). Pixel supply voltage as well as reset and select signals for APS pixel are boosted to achieve wider and extended linear operating range in a standard CMOS process with high-Vt transistors. Reset and supply boosting was used for extending dynamic range of the pixel source follower (PSF) amplifier, while the select signal boosting was utilized for linearizing transfer characteristics of the PSF. Extension of PSF dynamic range using reset, select, and supply boosting (RSSB) resulted in operation of 3T APS pixel at 1.2V supply with 150mV dynamic range even though the threshold of the NMOS device was 0.8V. Proposed method does not degrade the device reliability margins and use single supply input.**

Keywords- CMOS APS, image sensors, supply boosting, low-voltage, low-power

I. INTRODUCTION

CMOS active pixel sensor (APS) imagers become the mainstream technology for consumer applications such as cell phones, camcorders, personal assistances, and game consoles. They continue to advance their penetration in high end applications for which charged-coupled devices (CCD) are still used. Resolution, image quality, and power consumption are the main driving specifications for the mid- and high-end applications. Low to medium resolution camera systems on the other end of application spectrum, especially the ones that are battery operated such as implantable biomedical devices, image sensor networks, and toys necessitate very low-power and low voltage operation. They also require low leakage or standby current to extend the battery life. Low leakage current and wafer cost are not the main strengths of sub-100nm CMOS processes considering the low-end and low-volume imaging applications. Thus, mature, low-leakage, sub-micron CMOS processes (L_{min}>180nm) are typically considered. However, these processes provide high-Vt devices that are optimized for higher process supply voltages. High threshold voltages in all these processes limit minimum usable supply voltage due to the reduced overdrive voltages on analog signal paths. Thus, new pixel readout electronics and techniques are required for low-voltage applications.

Pinned photo diode (PPD) type CMOS APS pixels are well suited for mid- to high-end applications due to their high sensitivity and low noise. However, they are not suitable for low voltage applications due to incomplete charge transfer and difficulty of full depletion in the pinned photodiode structure. Thus, the standard tree transistor (3T) CMOS APS pixels are typically favored in low-voltage applications. Any new low-voltage operation techniques for 3T APS, however, should not increase the complexity, device count, and scaling capability of the APS pixel. This is not the case for the published work in literature for low-voltage CMOS APS pixels [1-9].

Recently, a mixed-signal design technique, called supply boosting (SBT), was demonstrated for sub-1V analog to digital converters achieving low-voltage and low-power operations in high-Vt CMOS processes [10,11]. It was foreseen that the SBT is well suited for analog signal chains of CMOS APS imagers achieving low-power and wider operating ranges for pixel source followers (PSF), especially when the supply voltage is reduced way below the process supply voltage in the orders of the threshold voltages of MOSFETs. Detailed analysis of dynamic range improvement for PSF and analog readout by utilizing the reset, select, and supply boosting (RSSB) is presented in this paper.

This paper is organized as follows. Previously published low-voltage and wide dynamic range pixel readout circuit techniques proposed for CMOS APS imagers are presented in section II. Proposed operation mode of the pixel readout electronics utilizing reset, select, and supply boosting (RSSB) is discussed in section III. Supporting electronics including row drivers, clock and supply boosters, and global readout channel are discussed in section III. Section IV was dedicated for simulation results. Finally conclusion is presented in section V.

II. LOW VOLTAGE CMOS APS PIXEL READOUTS

Few methods have been proposed to improve dynamic range of CMOS APS readout electronics [1-9]. Proposed techniques mainly address characteristics of pixel source follower (PSF) which deteriorates as a result of technology scaling and reduced supply voltages. One commonly used method to extend the dynamic range of conventional 3T CMOS APS readout electronic is to bootstrap pixel reset signal beyond the supply voltage [1,2]. However bootstrapping technique may result in hot-carrier reliability issues if the system supply voltage (V_{AA}) is close to the process supply voltage (V_{AAP}). Another widely used approach is to use PMOS type reset transistor that increase photodiode signal swing with the expense of reduced fill factor, and increased pixel size, [3,4]. These methods address the signal swing issue at the input of the PSF for low supply voltages. However output swing and gain linearity is still limited by the threshold voltage and linear operating range of the amplifying and pixel select transistors of the PSF. Output swing limitations was addressed by using complementary readout electronics with the expenses of

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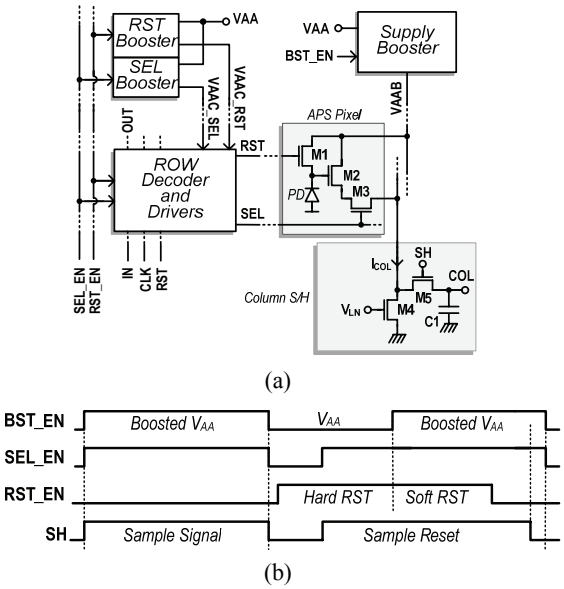


Figure 1. Schematic (a) and timing (b) diagram of signal and supply boosted CMOS APS imager and its analog signal chain.

increased transistor count per pixel, reduced fill factor, and diminished scaling prospect [5,6]. These techniques and circuits are based on voltage mode readout of the pixel photodiode signals. There were also current mode readout techniques proposed for low-voltage operation of CMOS APS pixels [7,8]. Current mode readouts, on the other hand, initially suffered from high fixed pattern noise (FPN), nonlinear transfer characteristics, and significantly higher current consumption then that of their voltage mode counterparts. Their nonlinear output characteristics diminish the effective use of offset-cancellation method to eliminate FPN. Despite, recently their FPN performance improved close to 0.4% FPN [8] as oppose to voltage mode FPN levels of 0.01% [9].

In all the methods mentioned, scaling of the APS pixel is inhibited and fill factor is reduced. In this work, however, we used standard 3T CMOS APS pixel without changing any properties of the transistors or routing. We also assumed that the sensor supply voltage (V_{AA}) is much smaller than that of the process supply voltage (V_{AAP}) (i.e. 1.5V for V_{AA} versus 3.3-5V of V_{AAP}), and single supply voltage (V_{AA}) for pixel array, digital, I/O, and analog parts of the imager is used by the user. Reset boosting was utilized for extended PSF input range while select boosting was proposed for linearization of PSF transfer curve. Input and output range further improved by utilizing supply boosting technique, [10,11].

III. Boosted Readout For CMOS APS Pixel

Proposed reset, select and supply boosted (RSSB) CMOS APS readout and supporting electronics are shown in Fig.1. Pixel composes of standard CMOS APS transistors (M1-M3) and a photodiode (PD). Pixel reset (RST) and select (SEL) signals are generated by row decoder. Both are globally boosted by two single-shot booster circuits. Pixel supply voltage (V_{AAB}) is also boosted by a similar booster circuit. Proper control of supply booster low-noise, hard-to-soft pixel reset operation is possible as shown in Fig.1(b). Low voltage compact column sample and hold circuit was adopted.

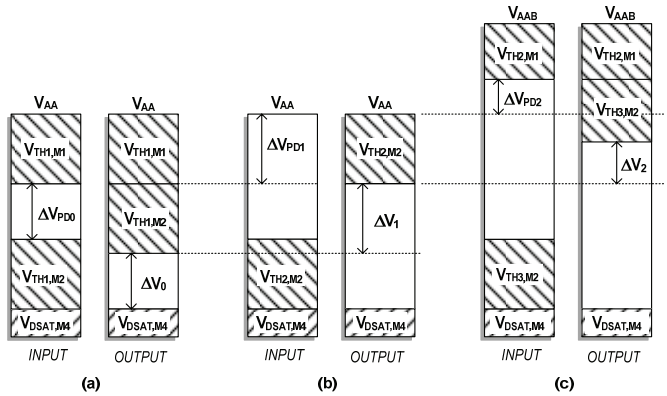


Figure 2. Dynamic range of 3T CMOS APS pixel for (a) standard, (b) reset boosted, (c) supply and reset boosted readout.

A. Reset Boosting

Nonzero backgate bias voltage ($V_{SB}>0$) results in increased threshold voltage for pixel transistors M1-M3. This increase could be as large as 50% of the zero threshold voltage for these devices [12] effecting linear input output characteristics of the PSF. Increased threshold voltage for example reduces the PD reset level one threshold (V_{TH} of M1) below the V_{AA} at the high end of the PSF input range. Lower input boundary is set by the PSF transistors M2 and M4. It equals to the addition of the V_{DSAT} of M4 and the V_{TH} of M2 as shown in Fig.2(a). Assuming small signal gain (A_v) is unity for PSF, the input range (ΔV_{PD0}) is level shifted and linearly buffered by the PSF between $V_{DSAT,M4}$ and $2V_{TH}$ below the V_{AA}. Thus, signal dependent threshold voltage variations effects and severely limits both input and output ranges of the PSF.

Boosting RST pulse at least one threshold above the V_{AA} improves input range (ΔV_{PD1}) by one V_{TH} and output range (ΔV_1) by $A_v*V_{TH,M1}$ as shown in Fig.2(b) allowing low-voltage operation of the 3T APS pixels [2].

B. Supply Boosting

The pixel supply voltage could also be boosted beyond V_{AA} during pixel readout further extending the dynamic range of PSF as shown in Fig.2(c). Here RST signal is also boosted allowing soft reset of the PD node to one threshold below boosted supply level (V_{AAB}). Note that the threshold voltage of M1 in boosted supply case ($V_{TH2,M1}$) is larger than that of non boosted case ($V_{TH1,M1}$) due to the increased back gate bias voltage. This is true for the threshold voltage of M2. As a result of boosted supply resetting, photodiode node is discharged from initial level beyond the supply voltage. Buffering this high reset level by the N-type PSF during reset sampling does not degrade linearity and operating range of the 3T APS rather improves the input range (ΔV_{PD2}) by $[(\beta-1)V_{AA}-V_{TH,M1}]$. Here β is the boosting factor which is between 1 and 2. In this case output range is also improved by $A_v*\Delta V_{PD2}$ as shown in Fig.2(c). As a result of reset and supply boosting, input range of the PSF could be improved by $(\beta-1)V_{AA}$ volt while the output range could be improved A_v times of this amount.

C. Select Boosting for PSF Linearization

As threshold voltage of PSF transistors, small signal voltage gain (A_V) also changes depending on the PD voltage as shown in Fig.3(a). Pixel select transistor (M3) works in linear

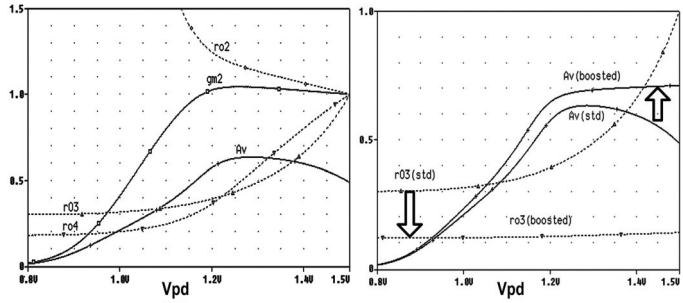


Figure 3. Small signal parameters and gain of PSF for a) standard select (V_{SEL}=V_{AA}=1.5V), b) boosted select (V_{SEL}=2V_{AA})

region around the lower input range of the PSF. For high inputs (i.e. PD reset level), it works in saturation possessing higher output impedance (r_{o3}). On both end of the PSF input range, PSF load transistor M4 works in saturation yet its output impedance increases for increased PD voltage. Variation of these small signal parameters result in very nonlinear small signal voltage gain as it is given with (1).

$$Av = \frac{V_{col}}{V_{pd}} = \frac{+ g_{m2} r_{o2} r_{o4}}{r_{o2} + (r_{o4} + r_{o3})(1 + g_{m2} r_{o2})} \quad (1)$$

Equation (1) shows that sensitivity of the gain to r_{o3} is much higher than that of the other output impedances (r_{o2} and r_{o4}) and transconductance of M2 (g_{m2}). Thus, increased r_{o3} at higher input ranges reduces the gain while introducing nonlinearity as seen in Fig.3(a). In Fig3(a), all small signal parameters are normalized with their nominal values attained when V_{PD}=V_{AA}=1.5V to show their trends.

Small signal voltage gain of PSF can be linearized at higher input range by boosting the SEL signal above the supply voltage. Boosting SEL to 2V_{AA}, for example, causes overdrive voltage of the M3 to be larger than its V_{DS} voltage and force M3 to work in linear region throughout the input range with small output impedance variation. Increased overdrive voltage also reduces the output impedance of M3 in linear region. As a result, boosting SEL reduces r_{o3}, improves small signal voltage gain of PSF, and flattens the gain for higher PD voltages as seen in Fig.3(b).

D. Compact Booster and Driver Circuits

Single clock boosting circuit from [13] as shown in Fig.4(a) was adopted for boosting SEL, RST and supply signals in our design. It is called supply and clock booster (SCB) [10,11]. SCB composes of two inverters, three transistors and a booster capacitor (C). Bulk nodes of the PMOS transistors (M2, M3) are connected to boosted supply (V_{AAB}). Second inverter has to be designed stronger than the first one to derive large parasitic load. It is because the bottom plate of boosting capacitor, C, is connected on inverter side to achieve better boosting efficiency. Node voltages of the SCB for low and high inputs are shown in Fig.4(a). Boosted supply level is given with (2).

$$V_{AAB} = \frac{2C + C_L}{C + C_L} \cdot V_{AA} - \frac{N \cdot I_{COL} \cdot \Delta T_{on}}{C + C_L} \quad (2)$$

Here, C_L is the total load capacitance, N is the number of columns, I_{COL} is the column bias current, and ΔT_{on} is the time that clock input us high. In case of driving all capacitive loads

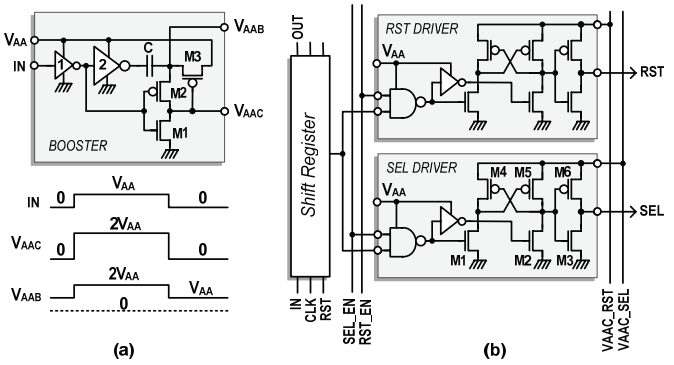


Figure 4. Schematic diagrams of (a) supply and clock booster and its timing diagram, and (b) row drivers.

(i.e. RST and SEL) the second term in (2) can be ignored. The second (discharge) term could also be ignored if the nominator (N, ΔT_{on}, or the load current) is very small.

IV. Simulation Results and Discussion

A standard 0.5μm, 2P3M CMOS process with high-V_{TH} transistors (+0.8V and -0.9V) was used for simulation. PSPICE simulation result of the entire signal chain from pixel PD node to column output is shown in Fig.5 for 1.8V supply. Icol was set to 35nA. PD signal level was set to 1.378V which is 0.70V below the boosted pixel reset level of 2.078V. PSF gain was close to 0.74. Boosted supply voltage was clamped to 3.175V and discharged to 2.715V by the 54 column currents. Thus, the boosting factor (β) for supply booster was 1.76, while it was 1.95 for the RST and SEL boosters.

Simulation of boosted CMOS APS readout for different supply voltages and operation modes were also performed. Fig.6 shows the simulation results for supply voltage between 1.2V and 2.8V. For these supply voltages, four different operation modes are reported. First one is the standard readout without any boosting. The second one is with only RST boosting (RB), next is with RST and SEL boosting (RSB), and the last one is with RST, SEL and supply boosting (RSSB).

For all the supply voltages, standard readout without RST and SEL boosting produce no PSF output below 1.8V. Thus, simulation shows that RST and SEL boosting increases the PSF

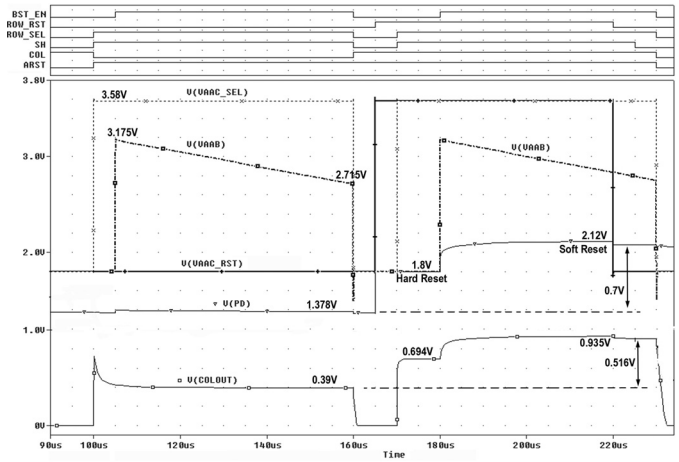
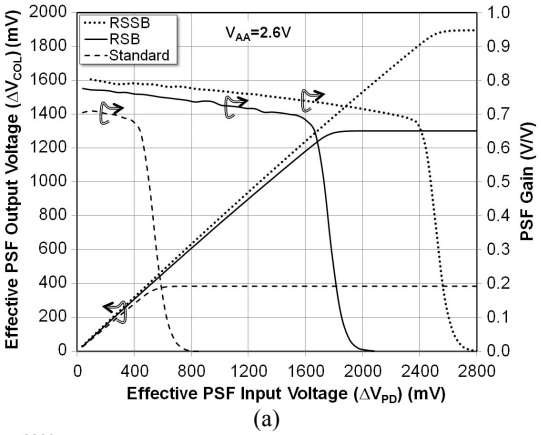
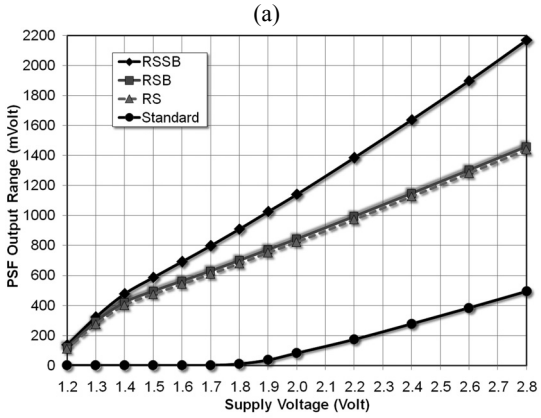


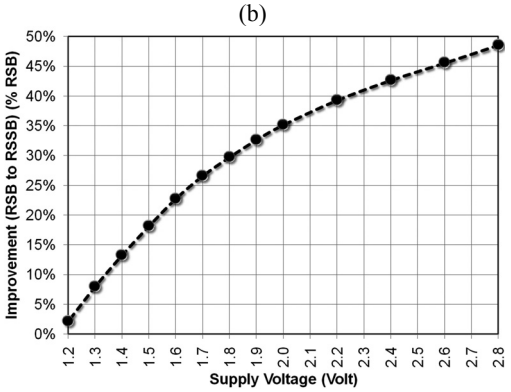
Figure 5. Simulation of boosted CMOS APS imager from PD to analog chip output at 1.8V supply.



(a)



(b)



(c)

Figure 6. Simulation results of PSF for different supply and operation modes. (a) Gain and I/O characteristics of PSF at V_{AA}=2.6V, (b) PSF output range versus supply voltage at four operation modes, (c) improvement of the PSF output range by using supply boosting along with reset and select boosting.

dynamic range drastically allowing very low voltage operations down to 1.2V supply with 150mV PSF dynamic range. In combination with RST and SEL boosting, supply boosting further improves the PSF range up to 50% comparing with the RST and SEL boosting for higher supply voltages. For example, RSB improves PSF dynamic range at 2.6V from 0.39V to 1.3V (a 3.3x improvement) and RSSB improve the range further to 1.9V (a 4.9x improvement over standard and 46% improvement over RSB operation modes). Proposed RSSB improves dynamic range more at higher end of the supply voltages as shown in Fig.6(c) comparing with RSB.

V. CONCLUSION

Dynamic range improvement of pixel source follower (PSF) in 3T CMOS APS pixels without degrading scaling prospect of the pixel technology was investigated. A supply boosting method was proposed along with reset and select signal boosting (RSSB) to improve dynamic range, small signal voltage gain, and gain linearity of the PSF. The RSSB method improves the dynamic range of standard 3T readout architecture dramatically while reducing minimum operating supply voltage below 1.2V in designs that a CMOS process with low-leakage, and high-Vt transistors is used. Only concern with the proposed method is the device reliability that can easily be mitigated if system supply voltage is set half of the process supply voltage or lower.

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