mater.scichina.com link.springer.com Published online 1 April 2021 | https://doi.org/10.1007/s40843-020-1617-x
Sci China Mater 2021, 64(9): 2118–2126

Boosting the efficiency of GeSe solar cells by low-temperature treatment of p-n junction

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ABSTRACT **Germanium monoselenide (GeSe) is an emerging promising photovoltaic absorber material due to its attractive optoelectronic properties as well as non-toxic and earth-abundant constitutes. However, all previously reported GeSe solar cells rely on a superstrate configuration coupled with a CdS buffer layer, and suffer from unsatisfactory performance. Here we demonstrate that this low efficiency arises from the inevitable high-temperature treatment of p-n junction in superstrate configuration. This results in the diffusion of Cd atoms from CdS layer into GeSe film that introduces detrimental deep trap states inside the bandgap of GeSe (~0.34 eV below conduction band minimum). We adopt therefore a substrate configuration that enables the deposition of CdS atop pre-deposited polycrystalline GeSe film at room temperature, avoiding the Cd diffusion. By optimizing the annealing temperature of complete devices *via* a high-throughput screening method, the resulting substrate solar cells annealed at 150°C achieve an efficiency of 3.1%, two times that of the best previously reported superstrate GeSe results.**

Keywords: germanium monoselenide, heterojunction, photovoltaic, thin film

INTRODUCTION

Germanium monoselenide (GeSe) has recently emerged as a promising photovoltaic absorber material in view of its attractive optoelectronic properties such as suitable bandgap (about 1.14 eV) for single junction solar cells [1,2], high absorption coefficient (greater than 10^5 cm^{-1}) at wavelength close to the absorption onset [3,4], high carrier mobility (about 128.6 cm^2 V^{-1} s^{-1}) [5,6], and decent carrier lifetime (about 9.9 ns, measured using transient absorption spectroscopy) [7,8]. GeSe also possesses earth-abundant and non-toxic constituents as well as fixed orthorhombic phase at room temperature [9–12]. Its sublimation characteristic offers the simultaneous combination of film deposition and *in situ* purification of the raw material—leaving impurities in sublimation source during film deposition. The congruent sublimation feature further prevents the formation of detrimental Ge and Se interstitials [1,8]. These attributes make GeSe attractive as an absorber material for photovoltaic application [13–18].

The first GeSe thin-film solar cell was reported by our group in 2017 [1]. We fabricated CdS-based GeSe solar cells (indium tin oxide (ITO)/CdS/GeSe/Au) with an efficiency of 1.48% using self-regulated rapid thermal sublimation (RTS) technique. In 2018, Chen *et al.* [19] demonstrated magnetron sputtering deposition of GeSe films on CdS layer and fabricated fluorine doped tin oxide (FTO)/CdS/GeSe/C-Ag solar cells with an efficiency of 0.05%. Very recently, Zi *et al.* [20] fabricated GeSe films using thermal evaporation and constructed FTO/CdS/GeSe/Au devices that achieved an efficiency of 0.65%. All GeSe solar cells reported to date have relied on superstrate configuration [21,22] that requires the illumination into solar cell through the substrate (Fig. 1a).

However, despite the intensive efforts to fabricate GeSe solar cells, their performance is still inferior, considering its Shockley-Queisser efficiency limit as high as ~30% [23–25]. We reasoned that this could arise from the superstrate device configuration. In such configuration, the absorber layer is directly deposited on the buffer layer such as widely-used CdS layer. For most of the reported

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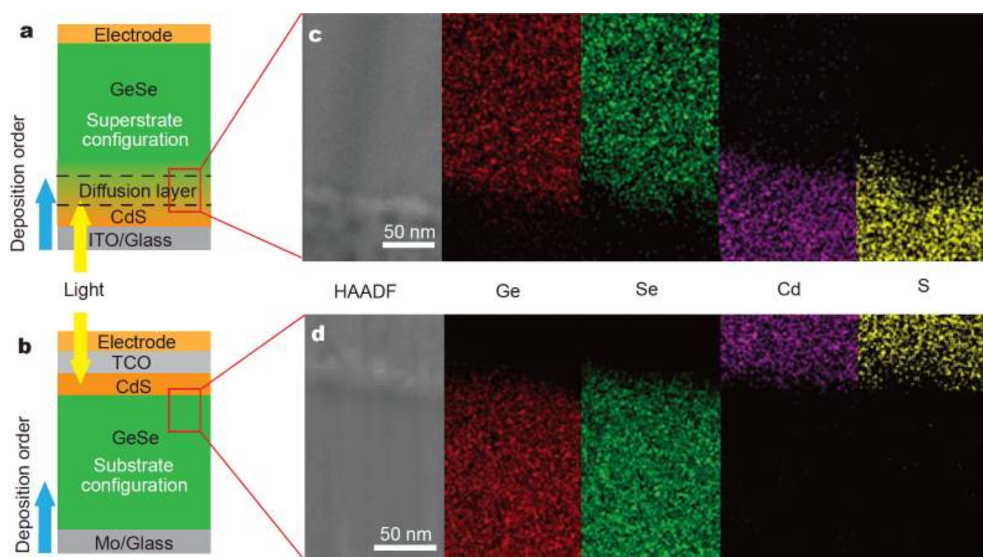

Figure 1 Schematic configurations of (a) superstrate and (b) substrate GeSe solar cells (TCO: transparent conductive oxide). HAADF cross-sectional images and energy-dispersive spectroscopy elemental mapping of the GeSe/CdS junction interface in (c) superstrate and (d) substrate GeSe solar cells. The yellow arrow represents the direction of illumination.

absorber materials, the deposition process usually requires high temperature for high-quality films, such as 550 and 500°C for $Cu(In,Ga)Se_2$ and $Cu_2ZnSn(S,Se)_4$ [26–28]. This thereby leads to the inevitable high-temperature annealing of p-n junction, which may result in severe interface diffusion.

By contrast, in substrate configuration (light enters the device through the front contact shown in Fig. 1b), the absorber film is deposited before the deposition of CdS layer that is usually prepared using low-temperature methods such as chemical bath deposition and magnetron sputtering [29]. Therefore, the p-n junction does not undergo high-temperature treatment in this configuration.

Considering the crystallization temperature of GeSe over 300°C [30], the deposition temperature of GeSe is usually as high as 350°C for high-quality polycrystalline film [1,8]. Whether this high-temperature process in superstrate configuration damages the GeSe/CdS interface or not, and, ultimately, is responsible for the low device efficiency, remains unclear.

Here we explore the origin of low efficiency in widely-reported superstrate GeSe solar cells. We find that the high-temperature treatment of p-n junction leads to the Cd atom diffusion from CdS into GeSe; this introduces a deep defect state inside the bandgap of GeSe (~0.34 eV below conduction band minimum (CBM)). We adopt therefore a substrate configuration, where CdS layer is deposited on pre-deposited polycrystalline GeSe film at room temperature. This low-temperature process of p-n junction avoids the Cd diffusion. By optimizing the annealing temperature of devices for the crystallization of CdS, the resulting substrate solar cells annealed at 150°C achieve an efficiency of 3.1%, two times that of the best previously reported superstrate GeSe results.

EXPERIMENTAL SECTION

Solar cell fabrication

Substrate GeSe solar cells: the bilayer Mo back contacts were prepared by a two-step direct current (DC) magnetron sputtering process, which consisted of low-power (80 W, 7 mTorr) and high-power (170 W, 3 mTorr) process. A Mo selenization process was carried out at 600°C for 25 min by using rapid thermal processing to reduce back contact barrier and improve the quality of heterojunction. The GeSe absorber layers were grown on selenized Mo-coated glass by RTS method as in a previous report [1]: the deposition process was to first preheat the GeSe powder and substrate at 350°C for 20 min, then quickly increase the source temperature to 420°C within 3 s, maintain this temperature for 15 s, and finally turn off the heating. CdS layers were deposited by a radio frequency (RF) magnetron sputtering process. Window layers of i-ZnO and ITO were sputtered from pure ZnO and ITO targets by RF. Finally, Ag electrodes of the solar cells were formed by thermal evaporation. The active area was defined by mechanical scribing.

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Superstrate GeSe solar cells: CdS buffer layer was deposited on ITO glass by RF magnetron sputtering process. GeSe layers were then deposited by RTS method on CdS. Finally, Au electrode was deposited by thermal evaporation through a shadow mask (active area: 0.09 cm^2) on the top of devices.

Material and device characterizations

Scanning electron microscopy (SEM) images were obtained using Hitachi S-4800. Samples for energy-dispersive microscopy (EDS) analyses were prepared by ablating the devices using Helios Nanolab G3 CX (FEI). EDS measurements were taken using JEOL JEM-2100F. For temperature-dependent conductivity, the test sample was loaded in a cryostat (Janis Research Co., Inc.) in conjunction with a temperature controller (LakeShore, 325 Temperature Controller), and the current-voltage (*I-V*) curves were measured by Keithley 4200. Current density-voltage (*J-V*) curves for device performance were measured with a solar simulator (450 W Model 94023A, Newport) with an AM 1.5 solar spectrum filter and a Keithley 2420 source meter. NREL certified Si solar was used to adjust light intensity. The external quantum efficiency (EQE) was measured by an Enlitech QER3011 system equipped with a 150-W xenon light source. Capacitance-voltage (*C-V*) tests were carried out using a Solartron 1260A frequency response analyzer in the dark with 30-mV alternating current (AC) amplitude at 10^4 Hz.

Calculation

All first-principles calculations were carried out using the Vienna *ab initio* simulation package (VASP) with a planewave basis set. We chose the Perdew-Burke-Ernzerhofer (PBE) formula with general gradient approximation (GGA) to treat the exchange-correlation atomic interactions. The ultrasoft pseudopotential was used to describe the exchange-correlation effects and electron-ion interactions. An energy cutoff of 600 eV was set for the planewave basis, and the Brillouin-Zone (BZ) integral was sampled by a 6 × 6 × 1 Monkhorst-Pack *k*-points set. For the lattice relaxations, the maximum force criterion and perpendicular force were all set as 0.01 eV $Å^{-1}$. After full lattice relaxations of GeSe (111) and CdS (100) surfaces with 20-Å vacuum regions, the p-n junction was constructed. The interface was then obtained after full relaxation. Employing method of transition state search, the diffusion energy of Cd atoms from CdS to GeSe interlayers was calculated based on the above relaxed structure. Finally, the hybrid functional approximation of Heyd–Scuseria–Ernzerhof (HSE06) was applied to obtain accurate bandgap in these cases, respectively.

RESULTS AND DISCUSSION

Comparison of superstrate and substrate GeSe solar cells

We fabricated GeSe solar cells in two structures: superstrate (Glass/ITO/CdS/GeSe/Au) and substrate (Glass/Mo/GeSe/CdS/iZO/ITO/Ag) configurations (Figs S1 and S2). To investigate the GeSe/CdS interface in these two configurations, we applied high-angle annular dark-field scanning transmission electron microscope (HAADF-STEM) equipped with EDS to characterize the Ge, Se, Cd and S element distributions at the GeSe/CdS interface. In the superstrate configuration, the obviously overlapped edges of Ge/Se and Cd/S in their spatial distribution maps indicate the diffusions of Cd and S from CdS layer into the GeSe film (Fig. 1c). In contrast, the substrate configuration exhibits sharp edges of Ge/Se and Cd/S, showing the negligible interfacial diffusion at the GeSe/CdS heterojunction (Fig. 1d). EDS line scanning analysis further confirms the above elemental mapping results (Fig. S3).

To investigate the impact of interfacial diffusion on the photovoltaic performance of GeSe solar cells, we compared the *J-V* curves of GeSe devices in superstrate and substrate configurations (Fig. 2a). Typical performance of superstrate devices measured under AM1.5G illumination showed a power conversion efficiency (PCE) of 1.4%, with an open-circuit voltage (V_{OC}) of 0.23 V, a short-circuit current (J_{SC}) of 15.5 mA cm^{-2}, and a filled factor (FF) of 39.2%, similar to previous reports [1,8]. In contrast, the devices in substrate configuration exhibited an improved PCE of 2.7% through the combination of V_{OC} of 0.33 V, J_{SC} of 19.8 mA cm^{-2}, and FF of 41.3%. The corresponding performance parameters are summarized in Table 1.

We fabricated 30 GeSe solar cells in each superstrate and substrate configuration to obtain statistical results, where GeSe layers were deposited by identical conditions. Fig. 2b shows the statistical photovoltaic performance of GeSe devices in these two different architectures. Compared with the superstrate devices with average PCEs of 1%, the substrate devices exhibited higher average PCEs of 2.3%. Notably, the largest relatively improved performance parameter in substrate devices is the V_{OC}—about 1.5 times that of the superstrate devices (Fig. 2c)—compared with the J_{SC} and FF (Fig. 2d, e). These findings indicate that the interfacial diffusion induced by the high-temperature treatment of GeSe/CdS junction results in

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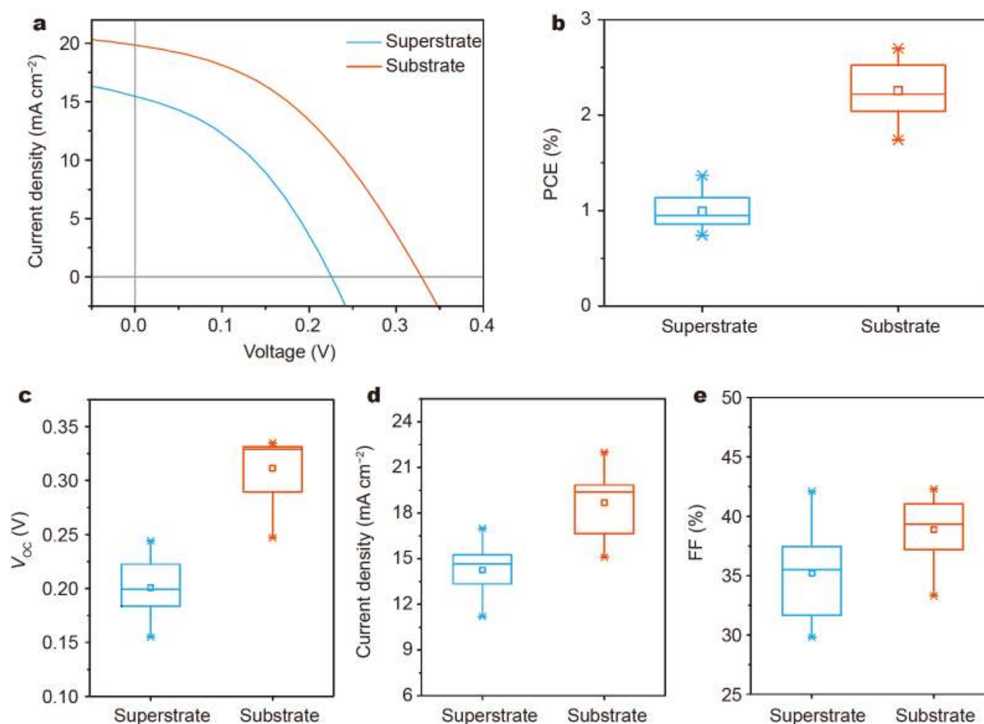

Figure 2 (a) *J-V* curves of superstrate and substrate GeSe solar cells under AM 1.5G illumination. Performance statistics of 30 GeSe solar cells in each superstrate and substrate configuration: (b) PCE; (c) V_{OC}; (d) J_{SC}; and (e) FF. The boxes indicate the 25th and 75th percentiles. The whiskers indicate the 5th and 95th percentiles. The cross symbols correspond to the maximum and minimum values. The median and mean are represented by the line dividing the boxes and the open square symbols, respectively.

Table 1 Photovoltaic parameters of GeSe solar cells

Device	V_{OC} (V)	J_{SC} (mA cm^{-2})	FF (%)	PCE (%)
Superstrate	0.23	15.5	39.2	1.4
Substrate (pristine)	0.33	19.8	41.3	2.7
Substrate (annealed at 150°C)	0.33	20.1	47.1	3.1

the inferior performance of superstrate GeSe solar cells, especially the low V_{OC}.

Investigation of the detrimental effect of Cd diffusion on device performance

We then sought to investigate the underlying reason for the interfacial diffusion-induced inferior performance of superstrate GeSe solar cells. Here we mainly focused on the diffusion of Cd into GeSe layer considering that S and Se belong to the same group, and the S diffusion may have little impact on the device performance [31]. We first used density functional theory (DFT) to calculate the diffusion energy of Cd from CdS to GeSe, which directly reflects the difficult degree of Cd diffusion. The low energy of 0.57 eV indicates that Cd atoms in CdS are prone to diffusing into GeSe along the layers (Fig. 3a). This may be attributed to the relatively low bond energy of Cd–S (~201 kJ mol^{-1}) [32] and the 2D layered crystal structure of GeSe that enables the Cd atoms to preferentially diffuse along the interlayer direction with a relatively large space, rather than Ge substitution. Once Cd atoms diffuse into GeSe, we further calculated the electronic band structure of Cd-doped GeSe. The addition of Cd introduces a deep defect state inside the bandgap that is below the CBM about 0.34 eV (Fig. 3b). This may act as a recombination center, resulting in severe carrier recombination loss and thus low device efficiency.

To directly evaluate the Cd-related defect depth in GeSe from experiment, we measured temperature-dependent conductivity (σ) of pure and Cd-doped GeSe films. Fig. 3c shows the conductivities derived from the *I-V* curves recorded at temperatures ranging from 180 to 320 K at a step of 10 K (Fig. S4). The linear dependence of lnσ as a function of reciprocal temperature indicates the conductivity follows the Arrhenius relation [31]:

$\sigma = \sigma_0 \exp(-E_a/k_B T)$,

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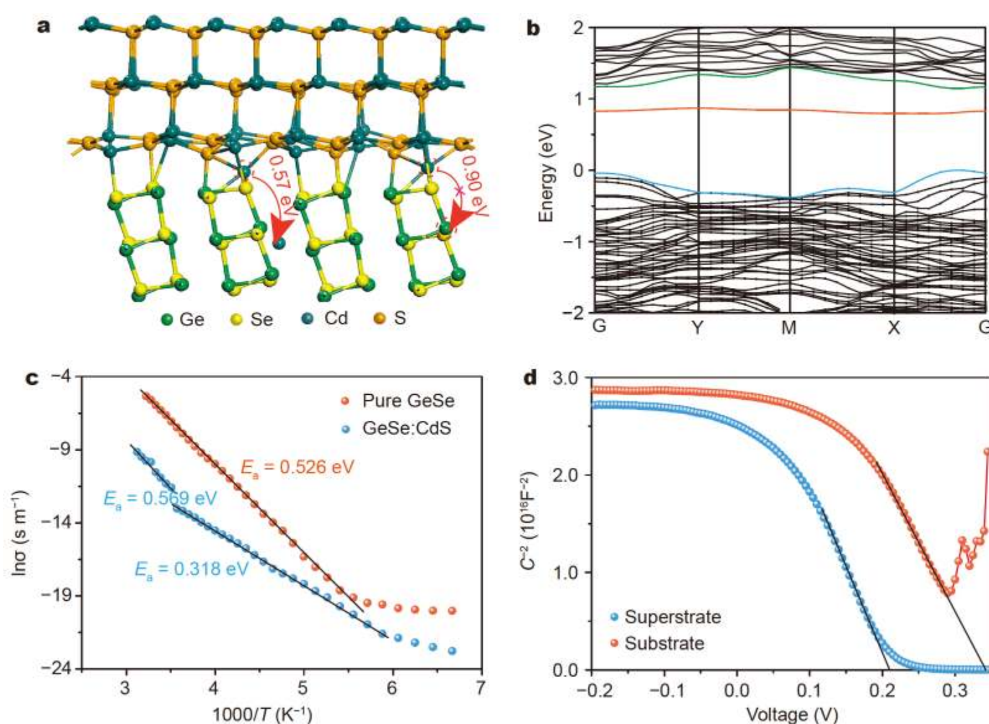

Figure 3 (a) Calculated diffusion energy of Cd in GeSe. (b) Calculated band structure of Cd-doped GeSe. The green line represents the CBM. The blue line represents the valence band maximum (VBM). The red line represents the Cd-induced energy level inside the bandgap of GeSe. (c) Temperature-dependent conductivity and corresponding Arrhenius fitting of pure and Cd-doped GeSe films. (d) C^{-2}-V plots of superstrate and substrate GeSe solar cells.

where σ is the conductivity at absolute temperature T, σ_0 is the pre-exponential factor that is nearly a constant, k_B is the Boltzmann constant, and E_a is the activation energy that represents the energy required for a carrier to escape from defects to the conduction/valence band. By fitting the linear regions in the plot of lnσ against 1000/T, the extracted slope can be used to estimate the dopant activation energy according to the above Arrhenius relation. E_a extracted for pure GeSe film is 0.526 eV that is nearly half of the bandgap of GeSe, indicating that intrinsic thermal excitation dominates the σ throughout the whole testing temperature range. In contrast, besides the E_a of 0.569 eV for the intrinsic thermal activation in Cd-doped GeSe, another E_a of 0.318 eV can be attributed to the formation of new defect level generated by Cd doping, agreeing well with our calculated results.

We further performed C-V measurements on superstrate and substrate GeSe solar cells to investigate the influence of Cd diffusion-induced trap states on device performance. Fig. 3d shows the difference in the C^{-2}-V curves of devices in two configurations. The built-in potential (V_{bi}) is fitted by the following equation [33]: $1/C^2 = 2(V_{bi} - V)/(A^2 e\varepsilon_0\varepsilon_r N_A)$,

where V is the applied voltage, A is the device area, N_A is the carrier concentration, ε_0 is the vacuum permittivity, and ε_r is the relative dielectric constant. The V_{bi} of substrate device was estimated to be 0.34 V, higher than that of superstrate device (0.21 V). This lower V_{bi} in superstrate device can be attributed to Cd doping-induced deep defect states, thereby lowering the V_{OC} of GeSe solar cells. The above combined theoretical and experimental results confirm that Cd atoms in CdS layer are prone to diffusing into GeSe films under high-temperature annealing; diffused Cd atoms then introduce deep defect states inside the bandgap of GeSe, and finally undermine the device performance.

Fabrication of high-performance GeSe solar cells

To explore the critical temperature of Cd diffusion from CdS into GeSe under heat treatment condition for further optimization of device performance, we developed a high-throughput experimental method to speed up the device optimization process. Gradient temperature field was obtained by connecting 30 and 350°C hotplates with a graphite block of 6 cm × 11 cm area (Fig. 4a). The actual temperature distribution of graphite block measured

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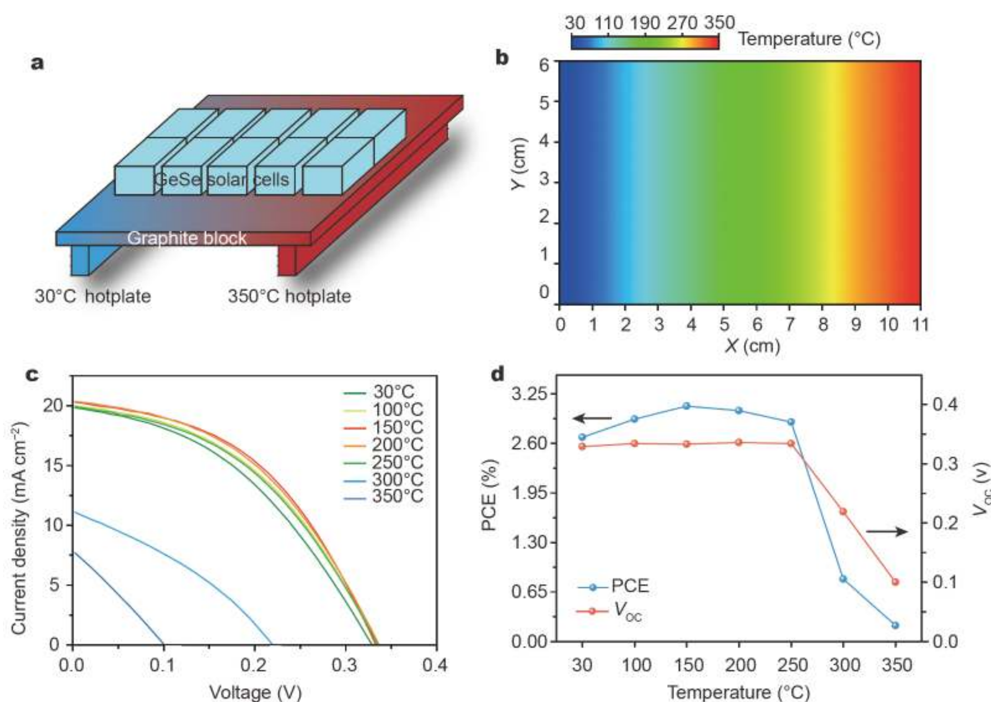

Figure 4 (a) Schematic diagram of high-throughput annealing method for GeSe solar cells. (b) Measured temperature distribution of graphite block. (c) Annealing temperature-dependent *J-V* curves of substrate GeSe solar cells. (d) Annealing temperature-dependent PCE and V_{OC} of substrate GeSe solar cells.

through thermocouple is shown in Fig. 4b. Five pieces of complete substrate GeSe solar cells with an area of 2 cm × 4 cm were placed on the surface of graphite block for 15 min and then measured the PCEs of these annealed GeSe substrate solar cells under AM 1.5G illumination.

Fig. 4c shows the annealing temperature-dependent *J-V* curves of substrate GeSe solar cells. We found that when annealing the device at temperatures over 300°C, the V_{OC} dramatically reduced from the initial 0.33 to 0.21 V, similar to that of GeSe solar cells in superstrate configuration, where the corresponding PCE decreased drastically (Fig. 4d). This indicates that the critical temperature of Cd diffusion from CdS to GeSe is about 300°C (Fig. S5). Note that this temperature is lower than the crystallization temperature of GeSe (330°C) [30]. This finding explains the intrinsic low V_{OC} of widely reported superstrate GeSe solar cells. In the superstrate configuration, the deposition of polycrystalline GeSe film atop CdS layer inevitably requires high temperature above 330°C for the crystallization of GeSe; this high-temperature process of GeSe/CdS junction therefore leads to the detrimental Cd diffusion. Previously reported CdS-based superstrate GeSe solar cells also verify this result, where the highest V_{OC} is 0.24 V (Table S1), significantly lower than the V_{OC} (0.33 V) in the substrate configuration.

Besides the identification of critical temperature of Cd diffusion, we also found that controlled annealing of complete substrate GeSe solar cells leads to an improvement of device efficiency, despite the observation that high-temperature annealing decreases the device performance. Fig. 4c shows that the optimum annealing temperature is 150°C, leading to a peak PCE in the entire annealing temperature range from 30 to 350°C. Compared with the pristine device before annealing, the efficiency gain after annealing at 150°C mainly comes from the increased FF, where V_{OC} and J_{SC} remain nearly unchanged (Table S2). This may be attributed to the increased crystallinity of room-temperature-sputtered CdS layer (Fig. S6) [34]. The improved efficiency further confirms the acceleration effect of our developed high-throughput method for the optimization of device performance.

Fig. 5a shows the *J-V* curve of the best-performing substrate GeSe solar cell. The champion device—obtained by annealing the pristine substrate solar cell at 150°C—exhibits a PCE of 3.1% (V_{OC} = 0.33 V, J_{SC}= 20.1 mA cm^{-2}, and FF = 47.1%). This is the highest PCE reported for GeSe solar cells, two times that of the best previously-

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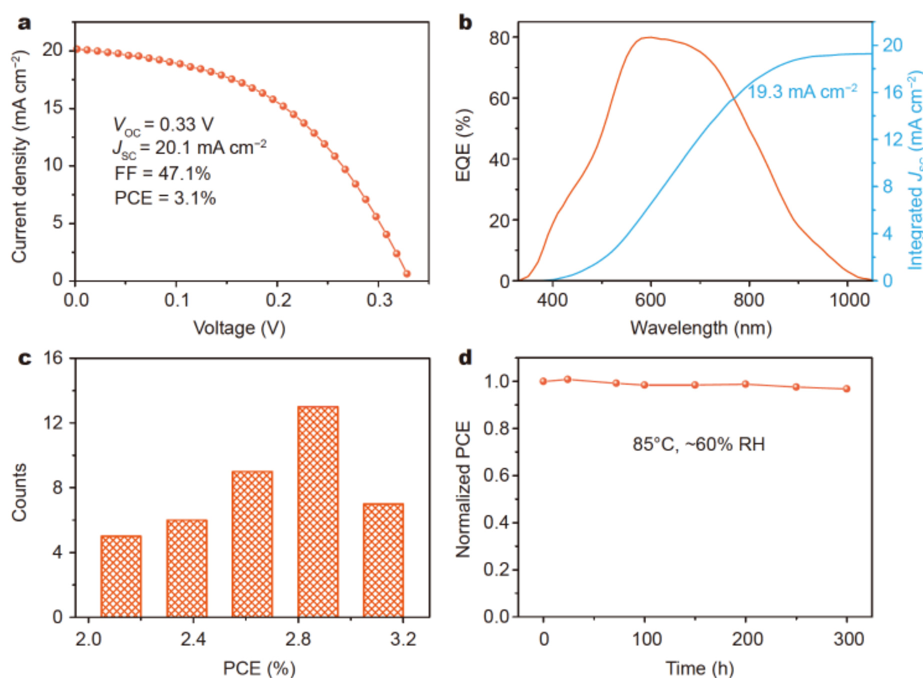

Figure 5 (a) *J-V* curve of the best-performing substrate GeSe solar cell that was obtained by annealing the pristine device at 150°C. (b) EQE spectrum and integrated current density of the device. (c) Histograms of PCE values for 30 devices of substrate GeSe solar cells. (d) Evolution of normalized PCEs of substrate GeSe solar cells kept at 85°C in an ambient atmosphere.

reported superstrate GeSe devices. No hysteresis between forward and reverse scans is observed in our device (Fig. S7). The integrated photocurrent density from the EQE spectrum is 19.3 mA cm^{-2} (Fig. 5b), consistent with the J_{SC} value measured from *J-V* characterization (within 5% deviation).

The fabricated substrate GeSe solar cells show a narrow PCE distribution (Fig. 5c), demonstrating the reproducibility of the performance enhancement associated with the controlled annealing of pristine substrate GeSe solar cells. We further investigated the thermal stability of substrate GeSe solar cells with no encapsulation. We heated these devices to 85°C and maintained at this temperature for 300 h in an ambient atmosphere and a relative humidity of ~50%. They showed no loss of efficiency after 300 h of heating at 85°C (Fig. 5d), demonstrating the good stability of GeSe solar cells in the substrate configuration.

CONCLUSIONS

In summary, we have found the origin of the low performance of widely reported superstrate GeSe solar cells. The low critical temperature of Cd diffusion (300°C) and high crystallization temperature of GeSe (330°C) result in the inevitable Cd diffusion into GeSe during the high-temperature process of GeSe deposition atop CdS in this configuration. The diffused Cd atoms introduce deep trap states inside the bandgap of GeSe, resulting in severe carrier recombination loss and thus low device efficiency. These findings guide us to adopt substrate device configuration, where no high-temperature treatment of p-n junction is processed, thereby avoiding the Cd diffusion. By optimizing the annealing temperature of complete devices *via* a self-developed high-throughput method, we achieved a record PCE of 3.1% with high thermal stability. This work introduces a way to design high-performance GeSe solar cells.

Received 21 December 2020; accepted 13 January 2021; published online 1 April 2021

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Acknowledgements This work was supported by the National Natural Science Foundation of China (21922512 and 21875264), and the Youth Innovation Promotion Association CAS (2017050). The authors thank Dr. Xiang Li (ICCAS) for the preparation of TEM samples.

Author contributions Xue DJ and Liu SC conceived the idea and designed the experiments. Liu SC prepared the films, fabricated the devices and characterized them. Zhang X carried out the TEM characterization. Li Z performed the DFT calculations and analyzed the results. Wu J and Feng M assisted in the device fabrication. Xue DJ and Liu SC wrote the paper. Xue DJ and Hu JS supervised the project.

Conflict of interest The authors declare that they have no conflict of interest.

Supplementary information Experimental details and supporting data are available in the online version of the paper.

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通过p-n结低温退火处理提升GeSe太阳能电池效率

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摘要 GeSe作为一种新兴光伏吸收层材料，具有良好的光电性能，且原料无毒、储量丰富. 然而，以往报道的GeSe太阳能电池都采用顶衬结构，并使用CdS缓冲层，性能不理想. 本文发现顶衬结构GeSe太阳能电池效率低下的原因是不可避免的p-n结高温热处理. 这导致Cd原子从CdS层扩散到GeSe薄膜中，并在GeSe的禁带内引入有害的深缺陷态(位于导带底~0.34 eV的位置). 因此，我们首次制备了底衬结构GeSe太阳能电池. 该结构可实现CdS层在多晶GeSe薄膜上的室温沉积，从而避免了有害的Cd扩散. 通过进一步采用高通量的筛选方法来优化器件的退火温度，当退火温度在150°C时，器件效率达到最高的3.1%，为以前报道最佳结果的2倍.

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