Bottom-up approach for carbon nanotube interconnects

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We report a bottom-up approach to integrate multiwalled carbon nanotubes (MWNTs) into multilevel interconnects in silicon integrated-circuit manufacturing. MWNTs are grown vertically from patterned catalyst spots using plasma-enhanced chemical vapor deposition. We demonstrate the capability to grow aligned structures ranging from a single tube to forest-like arrays at desired locations. SiO_2 is deposited to encapsulate each nanotube and the substrate, followed by a mechanical polishing process for planarization. MWNTs retain their integrity and demonstrate electrical properties consistent with their original structure. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1566791]

The interconnect in an integrated circuit (IC) distributes clock and other signals as well as provides power or ground to various circuits on a chip. The *International Technology Roadmap for Semiconductors* (ITRS)[1] emphasizes the high-speed transmission needs of the chip as the driver for future interconnect development. Interconnect requirements for the near and long term for both high performance microprocessors (MPs) and dynamic random access memory (DRAM) are outlined in ITRS. MP needs involve solutions to local, intermediate and global wiring. In general, the challenges in interconnect technology arise from both material requirements and difficulties in processing. The susceptibility of common interconnect metals to electromigration at high current densities ($>10^6$ A/cm^2) is a problem. The copper interconnect, introduced in 1998, is now routinely used with minimum feature sizes down to 130 nm.[2,3] However the electrical resistivity of Cu increases with a decrease in dimensions due to electron surface scattering and grain-boundary scattering.[4,5] Such size effects arise from interface roughness and small grain size, which are hard to overcome.[5] On the processing side, current technology relies on three steps: dry etching to create the trenches/vias, deposition to fill metal plugs, and planarization. The aspect ratio of contact holes for DRAM stacked capacitors now is 12:1 and is expected to increase to 23:1 by 2016.[1] Creating such high aspect ratio contacts with straight walls is an extremely difficult task. HBr etching of SiO_2 for a 9:1 contact hole reported in Ref. 6 yields a diameter of 135 nm at the top but only 70 nm at the bottom. Aspect ratio dependent etching becomes a serious problem with each new IC generation. Plasma damage and cleaning of high aspect ratio features also pose concerns. Void-free filling of high aspect ratio features is an equally difficult task.

Innovative material and process solutions are critical to sustain the growth curve according to ITRS. In this regard, the potential of carbon nanotubes (CNTs) as an interconnect material has been recognized.[7] For a discussion on the structure and properties of CNTs, the reader is referred to Refs. 8 and 9. The extraordinary electrical, mechanical, and thermal properties of CNTs may provide near-term solutions for problems in interconnects, chip cooling, etc. in silicon IC technology. For example, Wei *et al.*[10] showed that the current carrying capacity of multiwalled CNTs (MWNTs) did not degrade after 350 h at current densities of 10^{10} A/cm^2 at 250 °C. The thermal conductivity of CNTs[11,12] is about 1700–3000 W/m K. The mechanical properties of CNTs are also superior to those of traditional materials used in the IC industry.

Kreupl *et al.*[13] recently deposited MWNTs inside 400 nm vias and 5×5 μm^2 contact holes (1.25 μm depth). Although their estimated resistance per nanotube of 600 kΩ was high, this value will certainly decrease as CNT growth matures and the quality of the CNT–metal contacts improves. But this approach does not offer a viable solution to interconnect problems. It is well known that CNTs, as deposited on substrates and inside trenches, appear as ''noodles.'' The anticipated ballistic transport is unlikely to happen in entangled nanotubes. Although the reported fill factor is low and can be improved in the future, planarization by chemical mechanical polishing (CMP) is likely to unravel the noodles. This approach simply replaces Cu or Al with CNTs and relies on the traditional etch-deposition-planarization path; thus all the problems of high aspect ratio etching of vias and holes remain. Seeding the bottom of a deep trench with the catalyst for CNT growth may also become an issue. We offer an alternative solution in which MWNTs are first grown at prespecified locations, then gap filled with SiO_2, and finally planarized. This bottom-up approach eliminates the etching step, already provides an aspect ratio of 20 or more uniform diameter interconnects, eliminates void-related problems since the SiO_2 is gap filled rather than CNTs and provides a SiO_2-CNT structure that is smooth, mechanically stable, and withstands the aggressiveness of CMP.

Figure 1 shows a schematic of our process sequence. A Si (100) wafer covered with 500 nm thermal oxide and 200 nm Cr (or Ta) lines is used to deposit 20 nm thick Ni as a catalyst. Ion beam sputtering is used to deposit Ni on patterned spots for local wiring or contact hole applications; for global wiring, Ni can be deposited as a 20 nm thick micron-

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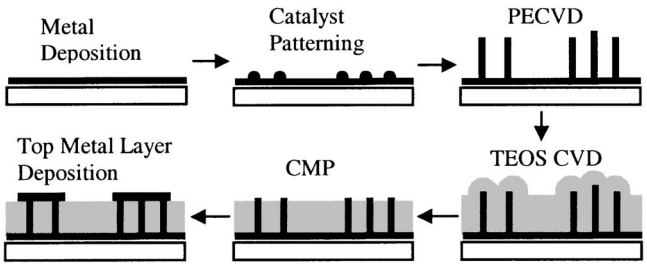

FIG. 1. Schematic of the process sequence.

scale film. Then plasma enhanced chemical vapor deposition (PECVD) is used to grow a low density MWNT array by an inductively coupled plasma process or dc plasma-assisted hot filament CVD as reported previously.[14–16] Each CNT is vertically aligned and freestanding on the surface (see Fig. 2). Such CNT structures are not possible by thermal CVD but are produced by PECVD due to the electric field normal to the substrate.[14] Next, the free space between the individual CNTs is filled with SiO_2 by CVD using tetraethylorthosilicate (TEOS).[16] This is followed by CMP to produce a CNT array embedded in SiO_2 with only the ends exposed over the planarized solid surface.[16] The top metal line may also be deposited although it is omitted here.

Figure 2 shows scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images of some CNT arrays at various stages of processing. Well-separated, vertically aligned MWNTs are grown on ~100 nm diam catalyst spots [Fig. 2(a)] and 2 μm spots [Fig. 2(b)] defined by e-beam and UV lithography, respectively. The 2 μm spots each have approximately 10 nanotubes. The nanotubes have an aspect ratio of up to 100:1 and lengths varying from 2 to 10 μm (depending on the growth time and conditions) and diameters of between 30 to 200 nm (depending on the diameter of the patterned spot and the catalyst thickness).

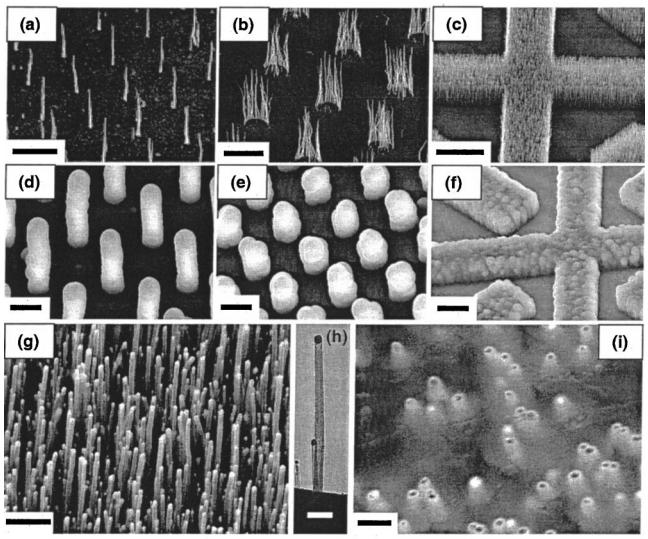

FIG. 2. SEM images of as-grown MWNTs on (a) 100 nm diam catalyst spots and (b) 2 μm diam catalyst spots, and (c) a catalyst film deposited at alignment markers over 10 μm in size; (d)–(f) images corresponding to those in (a)–(c), respectively, after being encapsulated with SiO_2; (g) high magnification SEM image of a MWNT array; (h) TEM image of a single MWNT from the array; (i) SEM image of the top surface of an embedded CNT array after CMP. The perspective of all SEM images is 45°. The scale bars are 5, 3, 10, 2, 5, 10, 1, 0.2, and 0.2 μm, respectively.

Figure 2(c) shows MWNTs on a catalyst film deposited at alignment markers over 10 μm in size. In all cases, we have successfully grown uniform MWNT arrays with uniform diameters along the axis from the base to the top [Figs. 2(g) and 2(h)]. Attachment of the nanotubes to the substrate is very strong and they cannot be removed easily.

SiO_2 deposition is found to be conformal around each nanotube as well as on the substrate. When the SiO_2 film grows thicker, it starts to break down to about 2–3 μm size grains. For catalyst spots smaller than 2 μm, we found that the CNTs are normally embedded within a single SiO_2 grain whereas multiple grains form for larger spot sizes [Figs. 2(d)–2(f)]. The Cr surface is also covered with a uniform SiO_2 film about 3 μm in thickness (not shown). There are some voids ($\leqslant$100 nm in size) inside the SiO_2 film as a result of the grain boundaries. This can be avoided for catalyst spot sizes less than 2 μm. Although not optimized, TEOS CVD has shown the formation of a conformal SiO_2 layer around CNTs and good gap-filling properties. The CMP process removes the excess SiO_2 and breaks the CNTs resulting in a planarized SiO_2 surface with only the very ends of the CNTs exposed. As shown in Fig. 2(i), the CNTs extend about 30–50 nm above the SiO_2 surface, likely due to their better mechanical resilience. Bright contrast indicates conformal SiO_2 wrapping around each individual CNT even in the portion that protrudes.

The planarized SiO_2-CNT structure without the top metal line is amenable to current–voltage ($I-V$) measurements using atomic force microscopy (AFM) modified with a current sensing AFM (CSAFM) module. This technique can be used to measure electrical properties of individual CNTs. The Si_3N_4 cantilever was coated with a Pt film so that voltage bias can be applied. Figure 3 shows images of the topography, deflection, and current of an embedded CNT sample [grown on a macro-sized continuous catalyst film like in Fig. 2(i)] and corresponding profiles along the line on the surface as highlighted. The topography clearly indicates that CNTs protrude out of the SiO_2 matrix, consistent with the SEM image in Fig. 2(i). The black spots in Fig. 3(c) correlate well with the protruding CNTs, indicating that CNTs have higher conductance than the SiO_2 matrix. Clearly, the CNTs are well separated in the SiO_2 matrix.

Corresponding to the CSAFM image in Fig. 3(c), the AFM tip can be easily positioned over different conducting spots to generate $I-V$ curves of individual CNTs quickly. Figure 3(d) shows typical $I-V$ curves of a single MWNT and a compact bundle ($\sim 250\times 500\ \mathrm{nm}^2$) in the embedded array. The $I-V$ curve of the single MWNT is a straight line within the instrumental limits of $\pm$10 nA. The resistance of the single MWNT is about 300 kΩ but that of the bundle is much lower than the 2 kΩ instrumental limit. The $I-V$ curve of the insulating SiO_2 shows a flat line at zero with 1 pA root mean square (rms) noise. Further measurements using a four-probe station linked to a semiconductor parameter analyzer were carried out to inspect the bundles in the $\pm$5.0 V range. As shown in the inset of Fig. 3(d), a perfect linear curve is observed that has resistance of 5.2 kΩ, corresponding to about 60 MWNTs in parallel contact with the 25 μm diam probe, consistent with the CNT density seen in Fig. 3(c). In these experiments, repeatedly applying $\sim 1\times 10^6$ A/cm^2 cur-

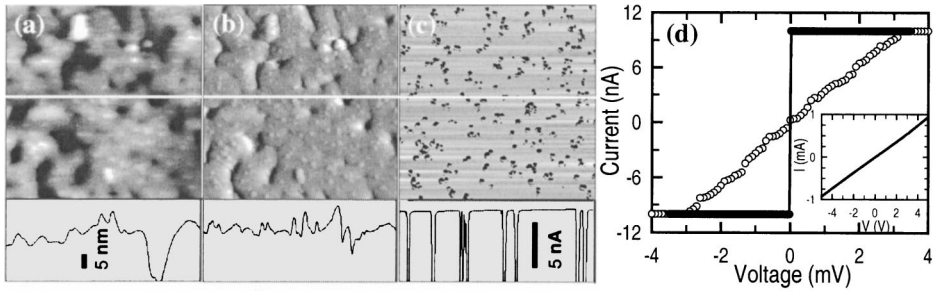

FIG. 3. Images of the (a) topography, (b) deflection, and (c) current sensing (at -5 mV) of a $5\times5\ \mu m^2$ planarized CNT array embedded in a SiO_2 matrix with profiles along the line marked. The scale bars for the profiles are as noted except for deflection (arbitrary). (d) $I-V$ curve of a single CNT (open circles) and a $250\times500\ nm^2$ compact bundle (closed circles) in the embedded array, both measured with CSAFM. Inset: $I-V$ curve of a parallel contacted CNT array measured with a four-probe station linked to a semiconductor analyzer.

rent density for many hours did not show any damage according to the $I-V$ measurements. It was already reported[10] there was no degradation even at 10^{10} A/cm^2 with only loose thermal contacts. So, it is expected that CNTs embedded in a SiO_2 matrix would withstand current densities far higher than that desired by the ITRS.[1]

Ballistic transport in MWNTs with quantized conductance corresponds to resistance of 12.9 kΩ.[8] The resistance measured here of a single MWNT is more than an order of magnitude higher than the theoretical value. Nevertheless, the use of a compact bundle or increasing the number of MWNTs in contact may already be sufficient for global wiring. There are several reasons for the observed resistance and possible ways to reduce it. First, the contacts to nanotubes to date are not perfect. Typically,[13] metal contact has always been to the sidewall of CNTs. In the case of MWNTs, contact then is only to the outermost shell. In our approach, contact is made to all the shells which is favorable for interconnect applications. Theoretical studies[17,18] show that the length of contact between the metal and the nanotube is critical for low resistance. The conductance drops dramatically when the contact length is less than 10 nm. For the point contact geometry of CSAFM used here, this may be a valid issue and along with the AFM tip/CNT contact may contribute to the observed resistance. In practice, a catalyst metal such as Fe, Co, or Ni may be deposited on top of the MWNTs before deposition of the top metal line. Thermal annealing in the presence of the transition metal can improve the electrical contact between CNTs and metal lines.[19] On the bottom side, MWNTs are grown directly from the substrate and show strong attachment to the metal film on the substrate, so good electrical contact may be possible.

Finally, the quality of the material itself contributes to the resistance observed. It is known[14–16] that most plasma-grown structures are somewhat defective, and are characterized by periodic bamboo-like or ice cream cone-like closed shells along the axis, as confirmed by TEM images. Whereas an ideal MWNT will have all walls parallel to the center axis ($\theta=0$), most plasma-grown structures exhibit small θ values and hence they are sometimes referred to as multiwalled carbon nanofibers.[14] In any case, the electrons have to cross the graphitic layers in such structures in order to be transported from one end to the other. This gives much larger resistance, similar to what one would get perpendicular to the basal plane of graphite. True ballistic behavior is possible with ideal MWNTs. We are currently investigating postgrowth annealing as well as higher temperature growth to reduce the resistance. The conductance may also be increased by introducing intercalation species such as I or Br to improve electron transport across graphitic layers.[20]

In summary, we have demonstrated a material and processing solution to integrate carbon nanotubes into multilevel interconnects to meet future silicon IC needs. The process sequence, which involves plasma deposition of CNTs, dielectric gap filling, planarization, annealing, etc., is compatible with current IC manufacturing practice.

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