Bottom-up organic integrated circuits

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Published in:
Nature

DOI:
10.1038/nature07320

Publication date:
2008

SUPPLEMENTARY INFORMATION

Contents

1. Summary

This Supplementary Information presents the details on preparation and characterisation of discrete SAMFETs and integrated circuits. The methods are presented in the experimental part, section 2. The rationale behind the design of the semiconducting self-assembling molecules is presented is section 3. We concentrated on chloro[11-(5""-ethyl-2,2':5',2":5",2"':5"',2""-quinquethien-5-yl)undecyl]dimethyl-silane. The synthesis is described and the full data set of investigated related molecules is presented.

The SAM formation and characterisation is presented in section 4. The layer thickness was first derived from XPS measurements. The thickness obtained corresponds to the calculated length of the active molecule. The presence of a single monolayer was confirmed by AFM measurements on fully and partially covered monolayers, as well as by X-Ray reflectivity measurements. Braggs rods were observed in grazing incidence diffraction measurements. The occurrence is due to the absence of periodicity perpendicular to the ordered SAM layer. This unambiguously showed that the SAM layer is a dense smooth monolayer. To analyse the electrical transport through the molecules, we focussed on partially covered SAMFETs. With scanning Kelvin probe microscopy (SKPM) measurements we show that electrical conduction only occurs in those parts of the SAM that are electrically connected to the source or drain electrode.

Device fabrication is addressed in section 5. The SAM layer is only 3.5 nm thick. The necessary use of electrode adhesion layers therefore can inhibit injection. We show with TEM images on cross sections obtained with focussed ion beam milling that the gold electrodes are under-etched. The titanium adhesion layer at the edge of the electrode is dissolved. The electrode is collapsed and the gold makes intimate contact with the SiO_2. Hence, despite the use of the Ti adhesion layer, the charge injection occurs through the Au contact. This is confirmed by fabrication of functional SAMFETs without Ti adhesion layer exhibiting comparable mobilities.

Section 6 addresses the electrical transport measurements on discrete SAMFETs. Statistical data on key device parameters as mobility, threshold voltage and subthreshold slope are presented. Scaling of the mobility with channel length is discussed and the contact resistance is estimated by TLM analysis. We show that partially covered SAMFETs show inverse scaling. Finally the reliability under prolonged gate bias can be described by a stretched-exponential time dependence. The parameters are comparable to that of regular organic field-effect transistors.

Fabrication of integrated circuits is discussed in section 7. The surface roughness of polysilicon gates overgrown with SiO_2 is addressed. We show that the mobility of the SAMFET is remarkably insensitive to the interface roughness. This unexpected result is rationalized with additional TFT measurements using amorphous bulk semiconductors. Finally a section on design, modeling and circuit lay-out is included, and measures to minimize parasitic currents are presented.

2. Experimental

Discrete SAMFETs were fabricated starting with heavily doped arsenic (n^{++}) Czochralski silicon wafers (0.001-0.005 Ω/cm) from Siltronic AG. The wafers were thermally oxidized at 1000 ºC in an oven until a 200 nm thermal oxide layer was grown. The layer thickness was confirmed by ellipsometry measurements. The substrate acts as a common gate. The capacitance per unit area amounts to 17 nF/cm^2. As source and drain electrode a 50 nm to 100 nm gold layer was applied. A 5 nm to 10 nm Ti film was used as adhesion layer. Metal electrodes were applied by sputtering using a CVC Connexion 800 sputter unit. The electrodes were defined by standard photolithography and wet etching.

Integrated devices require a patterned gate and vertical interconnects. A monitor wafer was used as support. To prevent parasitic leakages, a 1.5 μm thick oxide layer was thermally grown. On this support, 250 nm of phosphor doped polysilicon was applied via low-pressure chemical vapour deposition. The polysilicon layer was structured by photolithography and Reactive Ion Etching (RIE) to define the gate electrodes and the first layer of interconnects, The polysilicon was subsequently thermally oxidized to yield a 130 nm gate oxide (26.5 nF/cm^2). The vertical interconnects were defined in the gate oxide by photolithography and RIE etching. Finally for the source and drain electrodes and second layer of interconnects, a gold layer (150 nm) with a thin titanium adhesion layer (5 nm) was sputtered and patterned via standard photolithography and wet etching.

The SAM layers were fabricated as follows. First the substrate containing the MIM stacks were rinsed with ethanol and iso-propanol. The surface was cleaned with a 600 W O_2 plasma for 2 minutes at 25 ºC. Next, the substrates were activated by dipping for 30 seconds in a strong acid, rinsed thoroughly with water and blow dried with nitrogen. The substrates were transferred to the N_2 flow box. The solution with the active molecule was made by dissolving 10 mg of the compound in 10 ml dry toluene during an hour in a N_2 flow box. The solution was filtered through a 0.2 μm PVDF filter (Whatman). Then the substrates were submerged in this solution for an incubation time between 15 minutes and 6 days at room temperature. Fully covered SAMFETs are formed after 2 days. The procedure has not been optimised for throughput however. The samples were transferred to a bottle containing clean toluene, taken out of the flow box, thoroughly rinsed with toluene, and blow dried.

The SAMFETs were characterised with various analytical techniques. X-ray Photoelectron Spectroscopy (XPS) measurements were carried out in a Quantera from PHI (Q1). Measurements were done at a take-off angles Θ of 60°. A monochromatic AlKα-radiation in High Power mode (100 Watt, measuring spot 100 μm, scanned over 1400 x 500 μm^2) was used. By means of wide-scan measurements the elements present at the surface have been identified. The chemical state and the atomic concentrations of the elements present are determined from accurate narrow-scan measurements. Atomic Force Microscopy (AFM) measurements were performed with a Veeco Dimension 3100 atomic force microscope equipped with a Nanoscope IV control unit. The profile measurements were performed in non-contact tapping mode. Scanning Kelvin probe microscopy measurements were performed with the AFM operated in ambient atmosphere or in a nitrogen environment. First, the height profile was recorded in tapping mode. Then the potential profiles were measured in non-

contact lift mode at a distance of 25 nm from the surface. The internal voltage sources of the AFM were used to apply the biases to the electrodes. Ellipsometry measurements were performed on a J.A. Woollam Co., Inc Spectroscopic Ellipsometer, VB-400. Cross sections of molecular junctions were made by focused ion beam milling using a FIB200. Subsequent transmission electron microscopic (TEM) studies of the milled slabs were performed using a TECNAI F30ST TEM operated at 300 kV. The chemical composition was obtained using energy selective filters.

Specular X-ray reflectivity measurements were performed using a Bruker D8 DISCOVER diffractometer with a copper sealed tube and secondary graphite monochromator. The diffractometer was configured in a Bragg-Brentano geometry with divergence slits of 0.05 mm and a receiving slit of 0.1 mm. The measurements were performed with a step width of 0.004 deg. and integration times of 5 seconds. The experimental data were fitted using WINGIXA by introducing a four layer structure including silicon, silicon oxide, alkyl chains and thiophene units with different mean electron densities. The data were compared with the molecular dimensions as obtained from MM2 force field calculations using ChemDraw3D version 8.

Grazing Incidence Diffraction was performed on the beam line ID10B at the European Synchrotron Radiation Facility in Grenoble using a radiation of 7.996 keV. A 2+2 goniometer with a horizontal sample stage was used. The primary beam was set 0.18 degrees relative to the horizontal goniometer plane. The incident angle of the primary beam relative to the sample was optimised at an angle of 0.18 degree to get maximum scattering intensity of the SAM. The scattered intensity was measured with a one-dimensional position sensitive detector equipped with a Soller slit mounted in z-direction covering an angular range of 10 degrees. The angular step width in lateral direction was between 0.02 and 0.1 degrees and the intensity was integrated over a time interval between 15 and 60 seconds.

Discrete SAMFETs were measured as function of bias and ambient using an Agilent 4155C semiconductor parameter analyzer. For electrical characterisation of integrated circuits Delta power supplies were used. A Tektronix TDS 714 L oscilloscope connected over a resistor was used to measure the output signal.

3. Molecular design

The molecular structure is schematically depicted in Fig. S1. The molecule consists of an anchoring group, an aliphatic spacer, a semiconducting core and an end-capping group. An anchoring group is crucial. Without such a group we could not form monolayers. All attempts to fabricate transistors with molecules without anchoring groups failed. Current in devices could not be measured. Chemical structures investigated are presented in Fig. S1. The measured electrical transport properties are summarised in Table S1.

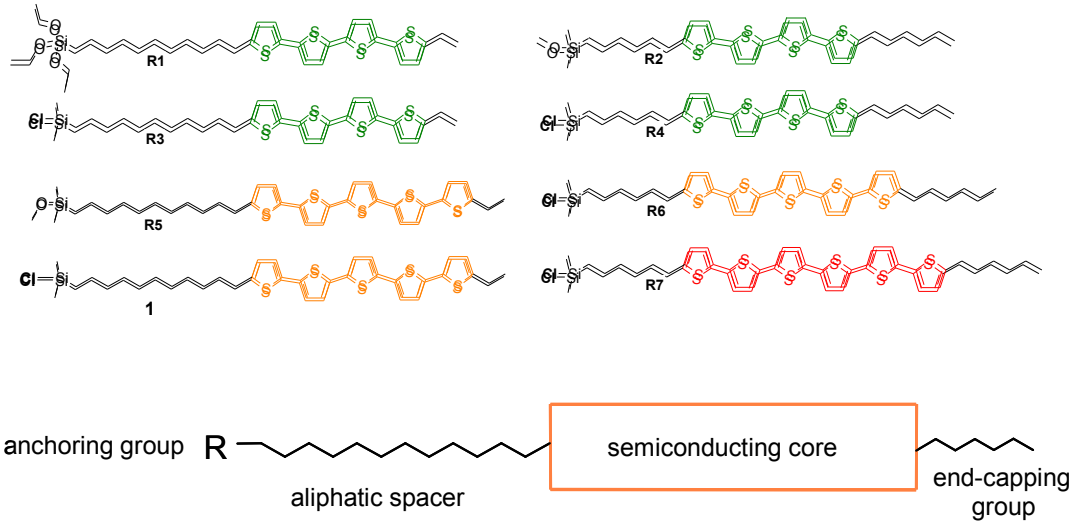

Fig. S1. Schematic representation of the molecular structure of SAMFET molecules. All molecules consist of an anchoring group, an aliphatic spacer, a semiconducting core and an end-capping group. Structural formulas of synthesised molecules,

The original idea was to construct a molecule that could form a self-assembled monolayer and that should combine both dielectric and semiconducting moieties. For the dielectric part we focussed therefore on a rather long undecylenic spacer between the semiconducting core and the anchoring functional organosilicon group. Quarterthiohene (4T) was chosen as a semiconducting core for its high solubility in common organic solvents and for high mobility values reported for quarterthiophene based thin film transistors. We started with molecule **R1** using a trifunctional, triethoxysilyl anchor group. However, in spite of numerous modifications of the gate dielectric, yielding static contact angles between 15º and 80º, no field-effect could be measured. These results were rationalised by the formation of an ultrathin amorphous dielectric film due to uncontrolled condensation reactions of the trifunctional triethoxysilyl groups not only with the surface bound Si-OH groups, but also between the molecules themselves.

Therefore, we changed strategy. To prevent uncontrolled polymerisation reactions we focussed on monofunctional anchor groups. A methoxysilyl group, yielding molecule **R2,** was preferred over an ethoxysilyl anchor group due to its higher reactivity. However, we could not form a monolayer. Apparently the reactivity of the methoxysilyl group was too low. Only when switching to highly reactive monochlorosilyl anchor groups, molecules **R3** and **R4**, self-assembled monolayers could be formed and the electrical transport properties could be determined. The mobility did hardly depend on the length of the spacer, C6 and C11, and amounted to 10^{-3} cm^2/Vs. To increase the mobility we replaced the quaterthiophene core (T4) by a quinquethiophene core (5T), yielding molecules **1**, **R5** and **R6**. Here again we found that molecule **R5**, with a methoxysilyl end group, does not form a monolayer. Functional SAMFETs could be only obtained with molecules **1** and **R6**, both using a reactive monochlorosilyl end group. We note that by replacing the T4 core by a T5 core the mobility increased by about one order of magnitude. Hence we attempted an

even larger core, T6, molecule **R7**. However, functional SAMFETs could not be obtained, presumably due to too low solubility. Therefore we focussed on molecule **1**. Details on the other molecules, **R1** through **R7**, such as the complicated synthesis, chemical analysis and electrical transport properties will be published in a journal dedicated to specialists.

Sample ID	anchoring group R	aliphatic spacer	semicon-ducting core	End-capping group	Electrical properties	
					Mobility, cm^2/Vs	On/Off ratio
R1	$(C_2H_5O)_3Si$-	-$C_{11}H_{22}$-	4T	-C_2H_5	Disordered dielectric insulator	
R2	CH_3O-$Si(CH_3)_2$-	-C_6H_{12}-	4T	-C_6H_{13}	No SAM, reactivity too low	
R3	Cl-$Si(CH_3)_2$-	-$C_{11}H_{22}$-	4T	-C_2H_5	3.E-03	1.E+06
R4	Cl-$Si(CH_3)_2$-	-C_6H_{12}-	4T	-C_6H_{13}	1.E-03	1.E+05
R5	CH_3O-$Si(CH_3)_2$-	-$C_{11}H_{22}$-	5T	-C_2H_5	No Sam Reactivity too low	
1	**Cl-$Si(CH_3)_2$-**	**-$C_{11}H_{22}$-**	**5T**	**-C_2H_5**	**4.E-02**	**1.E+08**
R6	Cl-$Si(CH_3)_2$-	-C_6H_{12}-	5T	-C_6H_{13}	2.E-02	1.E+07
R7	Cl-$Si(CH_3)_2$-	-C_6H_{12}-	6T	-C_6H_{13}	No SAM Solubility too low	

Table S1. Chemical structure of the compounds investigated. The molecules consist of an anchoring group, an aliphatic spacer, a semiconducting core and an end-capping group. The last entry presents the electrical transport properties of SAMFETs and reasons for failure.

The active molecule **1,** chloro[11-(5""-ethyl-2,2':5',2":5",2"':5"',2""-quinquethien-5-yl)undecyl]dimethylsilane, was synthesized by hydrosilylation of 5-ethyl-5""-undec-10-en-1-yl-2,2':5',2":5",2"':5"',2""-quinquethiophene[1] (compound **2**) with dimethylchlorosilane as depicted in Fig. S2. The reaction was carried out in a 1% solution of the reagent in dry toluene under argon atmosphere at 85 °C in a closed vessel. To accelerate the reaction and suppress side-reactions a 20 times mole excess of dimethylchlorosilane was used. The completion of the reaction was followed by ^1H NMR analysis by looking at the disappearance of the multiplets at 5.0 and 5.8 ppm coming from the terminal double bond of the initial reagent (compound **2**) and the appearance of a singlet at 0.4 ppm from the dimethylchlorosilyl group (Fig. S3). The product was isolated by distilling the toluene and the excess of dimethylchlorosilane under argon atmosphere, followed by drying in vacuum., According to the integral intensities of Si-CH_3 and thiophene protons in ^1H NMR spectra, the product contained ca. 50% of the active surfactant (compound **1**) together with ca. 50% of a by-product 5-ethyl-5""-undec-9-en-1-yl-2,2':5',2":5",2"':5"',2""-quinquethiophene (compound **3**) with inactive migrated double bond. It was not possible to separate compounds **1** and **3** by any conventional methods. Nevertheless, compound **3** is a non-functional impurity *i.e.* it cannot bind to Si-OH surface. Hence, we used the mixed product for preparation of the self-assembled monolayers. In a similar way various organic semiconducting molecules can be functionalised for self-assembly. Additionally different anchoring groups could be used.

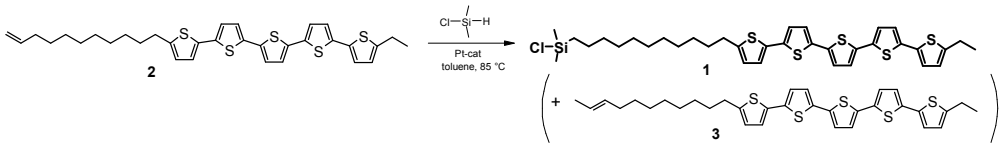

*Fig. S2. Synthesis of the molecule **1**. The compound is obtained by a hydrosilylation reaction of compound **2**. As an impurity compound **3** is produced, which was not removed as it cannot adhere to Si-OH groups.*

The hydrosilylation reaction was performed under argon with compound **2 (**0.69 g, 1.2 mmol), dimethylchlorosilane (2.5 ml, 23 mmol), 70 ml of dry toluene and 25 ml of Carsted's catalyst mixed in a closed vessel at 85 ºC during 10 hours. After completion of the reaction, a distillation apparatus was attached to the reaction vessel and a mixture of toluene and the excess of dimethylchlorosilane were distilled at 120 °C. Then, the vessel was dried at the same temperature under vacuum (10^{-2} mbar) during 4 hours. Finally, the vessel was cooled to room temperature and filled with argon. The characteristics of the MS spectra are DCI MS (gas reagent isobutane), 70 eV, DCI MS (gas reagent isobutane), 70 eV**:** m/z = 686/688 (3.6/2.5, M^+), 651 (2.1, M^+ – Cl), 593 (22, M^+ – Cl-Si$(CH_3)_2$-). The NMR spectrum is presented in Fig. S3.

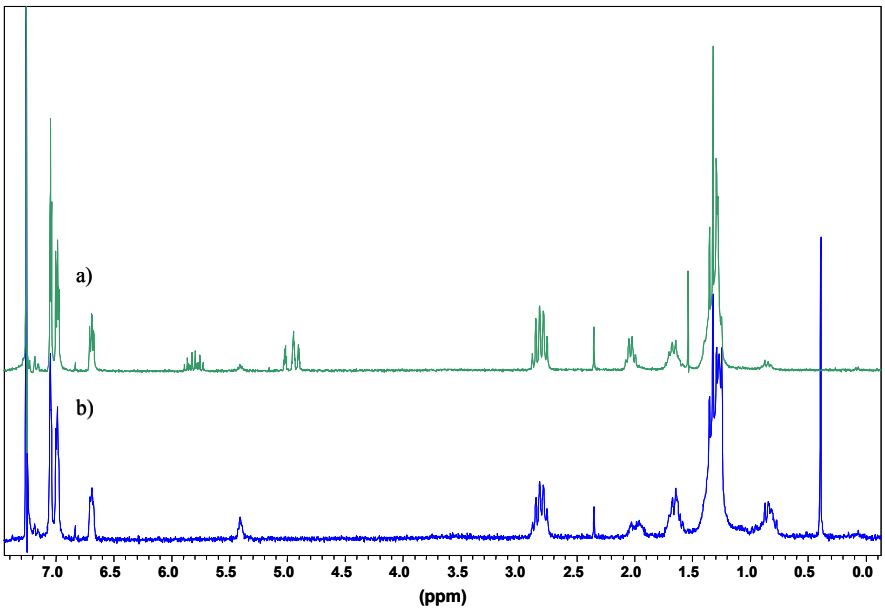

*Fig. S3. ^1H NMR spectra of a) the starting compound **2**; and b) the end-product being a 1:1 mixture of compound **1** and **3**.*

4. Monolayer fabrication and characterisation

The SAM fabrication is schematically depicted in Fig. S4. First the silicon dioxide substrates were rinsed with ethanol and iso-propanol. The surface was cleaned with a 600 W O_2 plasma for 2 minutes at 25 ºC. Next, the substrates were activated by dipping for 30 seconds in a strong acid, rinsed thoroughly with water and blow dried with nitrogen. The substrates were transferred to the N_2 flow box. The solution with the compound **1** was made as follows: 10 mg of the mixture of compound **1** and **3** was

dissolved in 10 ml dry toluene during an hour in a N_2 flow box. The solution was filtered through a 0.2 μm PVDF filter (Whatman). Then the substrates were added to this solution for an incubation time between 15 minutes and 6 days at room temperature. Fully covered SAMFETs are formed after 2 days. The procedure has not been optimised for throughput however. The samples were transferred to a bottle containing clean toluene, taken out of the flow box, thoroughly rinsed with toluene, and blow dried.

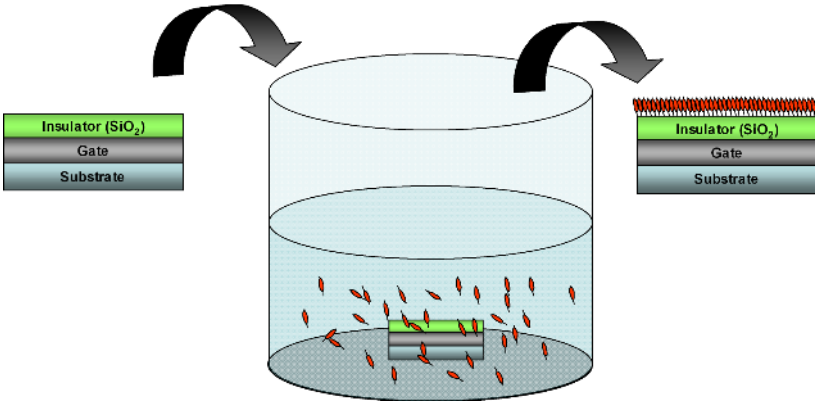

Fig. S4. Schematic overview of the self-assembly. 1) A clean and activated substrate is submerged in a solution containing the active molecules. 2) The molecules self-assemble on the SiO_2. 3) The substrate is removed from the solution and rinsed to remove any residues from the surface.

We note that active molecule **1** can covalently bind to the hydrolysed SiO_2 surface as schematically depicted in Fig. S5. The by-product compound **3** is not functionalised and, in theory, this inactive compound cannot bind to the surface. Co-crystallization is unlikely but cannot yet be excluded by chemical analysis. An artist impression of a possible microstructure is presented in Fig. S6.

The non-functionalised compound **3** has no anchor group to bind to the SiO_2 surface. However a driving force for co-crystallisation could be π–π stacking of the oligo-thiophene cores. To verify that the SAM is dominantly composed of the functional molecule **1**, we thoroughly washed the SAMFETs by submerging the substrate ultrasonically in toluene at 80 ^{0}C. Toluene is a good solvent for the by-product, molecule **3**. Hence upon heating and exposure to ultrasound, a reduction of its content in the SAM is expected. Experimentally, we find minor changes in charge transport of the SAMFETs after this treatment. These measurements strongly suggest, but do not prove, that co-crystallisation is unlikely.

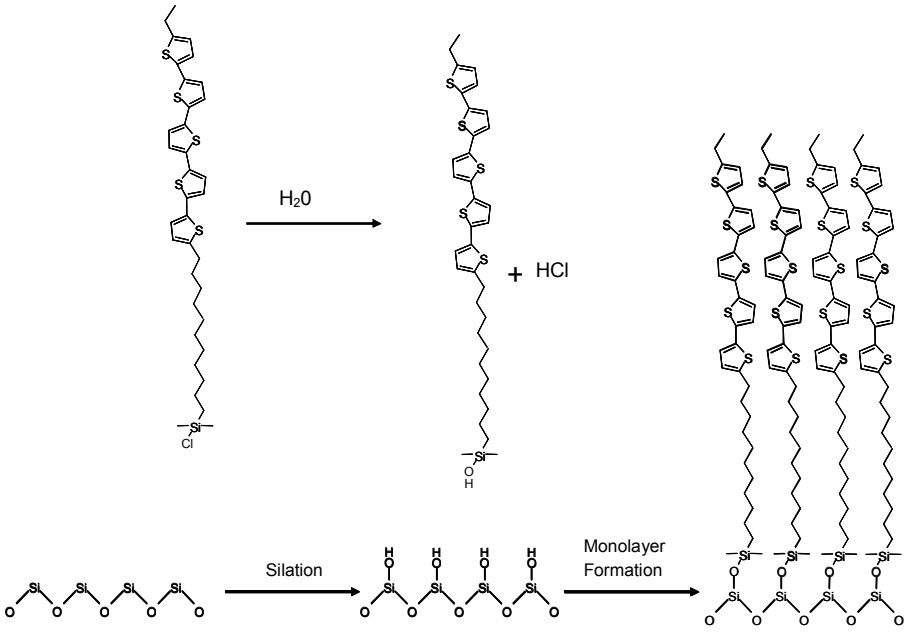

Fig. S5. Schematic for the formation of a self-assembled monolayer on SiO_2.

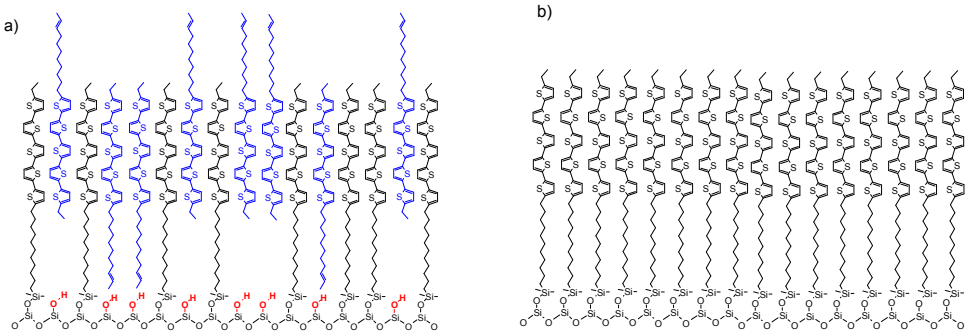

Fig.e S6. Possible structures of the self-assembled monolayers: a) formed by co-crystallization of the mixture of active and non-active molecules and b) formed only by the active molecules.

Quantifying the content of compound **3** in the SAM turned out to be extremely difficult. Various techniques were tried. The sensitivity of Raman spectroscopy is too low. Monolayer sensitivity can be obtained with attenuated total reflectance IR spectroscopy using a grazing incidence geometry and evanescent wave mode detection. However, molecules **1** and **3** have no contrast difference and therefore cannot be distinguished. LCMS (liquid chromatography with mass spectrometry detection) requires complete dissolution of the SAM which is hard to accomplish and which yields too low concentrations. With XPS we tried to detect the presence of C=C and Si-OH groups. However, the difference between saturated and unsaturated carbon is only 0.25 eV, which is too small with respect to the measured line width. Furthermore the Si 2p peak in Si-OH coincides with that of $Si-CH_x$ and the O 1s peak

is swamped in that of SiO_2. X-Ray reflectivity measurements turned out to be no option either.

Although we could not determine the exact chemical composition of the SAM, a significant degree of co-crystallisation is unlikely. When this mechanism is operative, then there is no reason to exclude similar co-crystallisation of the functional molecules upside down, *i.e.* Si-Cl up. This would lead to formation of a second layer by hydrolysis of the upper Si-Cl bond followed by self-condensation with the excess functional molecules in the solution. The X-Ray reflectivity measurements, AFM measurements, and grazing incidence synchrotron measurements as presented in the letter, unambiguously demonstrate the presence of a fully ordered monolayer. We have no indications for layer-by-layer growth.

SAM characterisation

The overall chemical composition and layer thickness was estimated from XPS measurements. The chemical state and the atomic concentrations of the elements present were determined from accurate narrow-scan measurements. The relative concentrations of the elements per unit area are presented in the Table S2. Standard sensitivity factors were used to convert peak areas to atomic concentrations.[2] From a 3 layer model, *i.e.* SiO_2 / $Si-CH_3$ / hydrocarbons, a thickness of about 2.9 nm is estimated for the monolayer.

Sample	C1s				O 1s	S2p		Si2p	
	284.8 eV	+1.6	+2.8	+4.1		165.2 eV	163.8 eV	101.9 eV	103.8 eV
	C-H	C-O	C=O	O-C=O		R'-S=O	thiophene	Si-C	SiO_2
1	46.9	2.2	1.5	0.5	26.2	0.1	5.6	1.5	15.5
2	47.4	2.2	1.3	0.5	25.8	0.1	5.7	1.3	15.6

Sample	Organic layer									SiO_2	
	d_{org}	N_Si-C	C1s	O1s	S 2p	S 2p	Si 2p	S/C	Si/C	O1s	Si 2p
	(nm)	at/cm^2		-org	-high	-low	-Si-C			-inorg	-ox
1	2.9	1.9E+14	81	7.9	0.1	9.1	1.5	0.113	0.019	66	34
2	2.9	1.8E+14	81	8.0	0.2	9.1	1.4	0.114	0.017	65	35

Table S2. Top panel shows the relative peak intensities. Bottom panel shows the apparent concentrations of the elements in the self-assembled monolayer, calculated with the 3 layer model as described in the text. The determined thickness is denoted with d_{org}, the calculated density with N_Si-C.

Grazing Incidence X-Ray Diffraction

The in-plane order in the SAM was determined from grazing incidence diffraction measurements. The diffracted intensity as a function of the in-plane scattering vector, q_{xy}, is presented in Fig 1b of the letter and reproduced here as Fig. S7. The inset showed the diffracted intensity perpendicular to the substrate, q_z, as a function of in-plane scattering vector, q_{xy}. The horizontal line at small q_z is due to diffuse scattering from the sample surface at the critical angle as first described by Yoneda.[3] The

vertical lines are the so-called Bragg rods[4] showing in-plane order in the SAM layer. The rods are observed at scattering vectors that are indexed as the (1.1), (0.2) and (1.2) reflections of a rectangular unit cell with lattice constants 5.49 Å and 7.69 Å. The peak indices and unit cell dimensions are in agreement with a unit cell that contains two molecules packed in a herringbone motive as commonly observed for oligothiophenes.[5] The molecular packing is depicted in Fig. S8. The occurrence of Bragg rods is due to the absence of periodicity perpendicular to the ordered layer. This indicates that our SAM layer is a dense smooth monolayer.

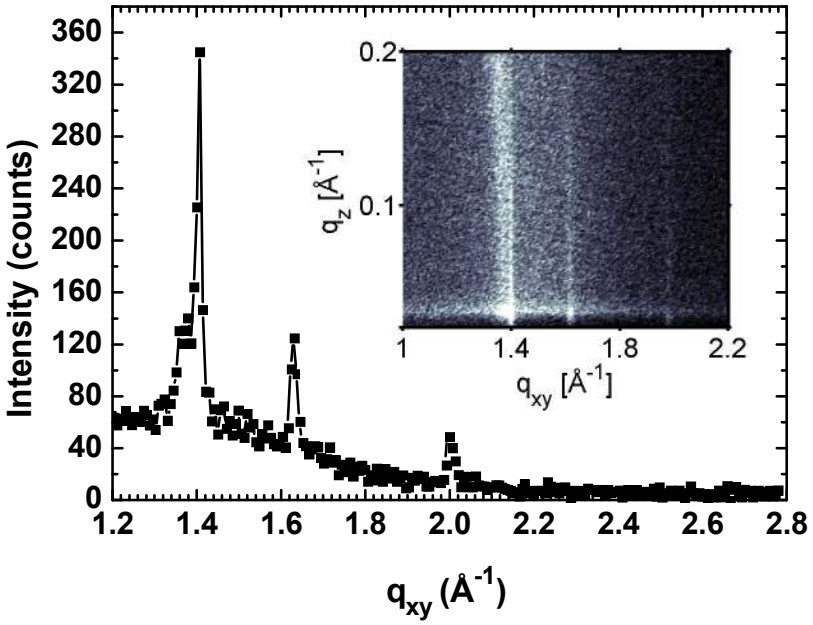

Fig. S7. Synchrotron grazing incidence diffraction measurements showing the diffracted intensity as a function of in-plane scattering vector, q_{xy}. The inset shows the presence of Bragg rods at in-plane scattering vectors of 1.407 Å^{-1}, 1.635 Å^{-1} and 1.997 Å^{-1} indicative for two-dimensional crystalline in-plane order in the self assembled monolayer.

Additional zoom in of the Bragg rods at in-plane scattering vectors of 1.635 Å^{-1} and 1.997 Å^{-1} are given in Fig. S9.

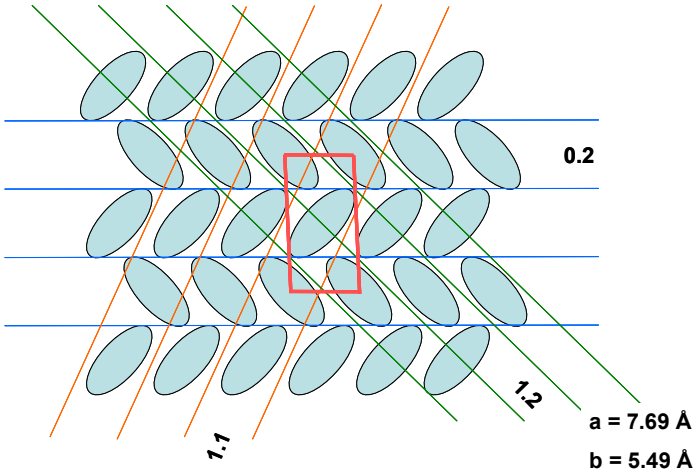

Fig. S8. Representation of the crystal lattice of the molecules in a herringbone structure. The (1.1), (1.2) and (0.2) planes are indicated as well as the lattice constants a= 7.69 Å and b = 5.49 Å.

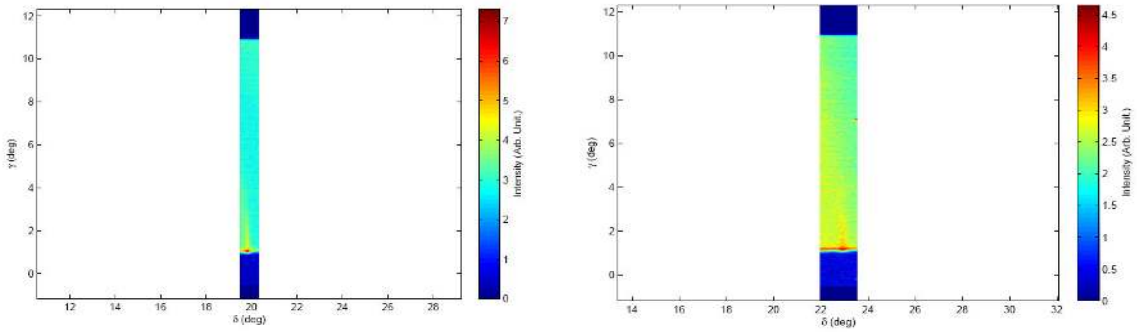

Fig. S9. Zoom in of the Bragg rods observed at scatter angles of about 20 and 23 degrees corresponding to in-plane scattering vectors of 1.635 $Å^{-1}$ and 1.997 $Å^{-1}$

Monolayer morphology

The morphology was investigated with AFM measurements. The height topography of a 5 μm by 5 μm surface area is presented in Fig. S10. The image shows a smooth layer. There are some defects, presumably absorbed aggregates formed in the solution. The top right of the image shows a void in the monolayer which allows to determine the SAM thickness. A cross section reveals a thickness of 3.5 nm corresponding to the calculated length of the molecule.

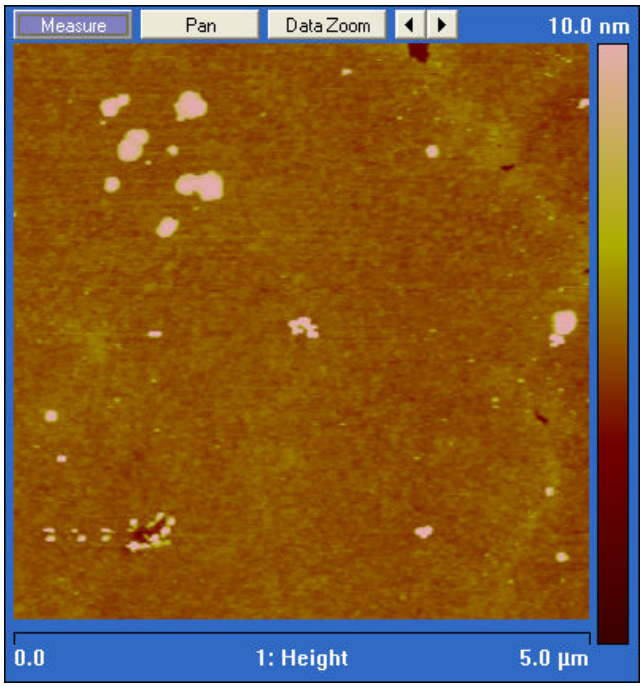

Fig. S10. AFM topography of the SAM measured on a 5µm by 5 µm surface area.

Connectivity of molecules

In order to demonstrate that we are dealing with a monolayer and that electrical conductivity only occurs through connected molecules, we focussed on partially covered SAMFETs. Partially covered SAMFETs were formed both by reducing the concentration of active molecules in the solution from 1mM to 0.05 mM and by varying reducing the incubation time between 15 minutes and 2 days.

AFM and scanning Kelvin probe microscopy (SKPM) measurements of the partially covered SAMFET are presented in Fig. S11. The AFM height image (Fig. S11a) shows on the left and the right side in dark brown, the source and drain electrode. The channel length is 5 µm. Islands of the self-assembled molecules are clearly visible in the channel as the light blue spots. Because of the partial coverage, height profiles can be obtained from cross sections. A typical example, shown in Fig. S11c, shows a height of approximately 3.5 nm in good agreement with the calculated length of the molecule. We note that the AFM image shows that the height of all island are identical. Furthermore we don't observe any anomalies at the contacts.

In order to obtain information on the local charge transport, SKPM measurements were performed on the same SAMFET. In accordance with literature procedures[6] first the height profile was recorded with tapping mode AFM. In a second pass the potential profile was measured at a fixed lift height above the surface of 25 nm. During this second pass source and drain electrodes were grounded and on the gate a bias of -3V was applied. The resulting potential map is shown in Fig. S11b. The islands which are intimately connected to one of the contacts have the same potential as the source drain electrode, *viz.* 0 V. Mobile holes accumulate in those islands thereby shielding the gate field. Holes cannot accumulate in islands that are not electrically connected with one of the electrodes. The gate bias then is not

compensated and the measured potential is due to the non-shielded applied gate potential.

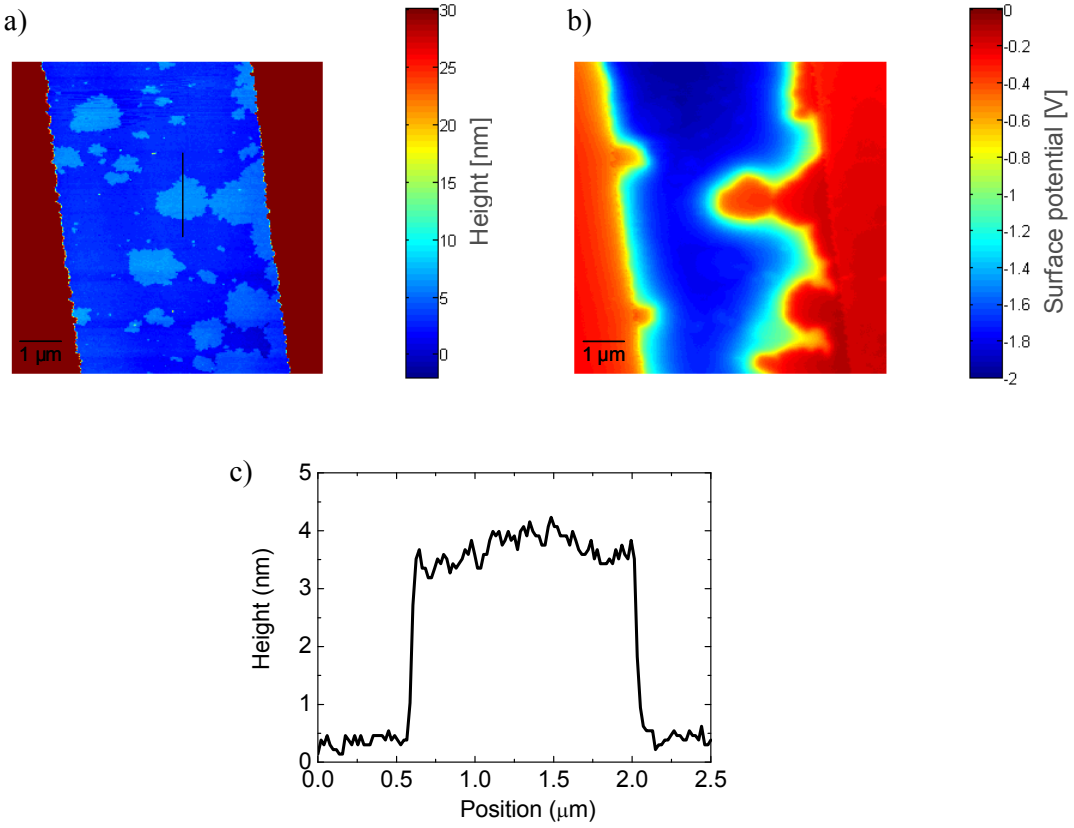

Fig. S11. a) The topography of a partially covered SAMFET measured with AFM. b) The simultaneously measured surface potential map using SKPM. The gate bias was set at -3V and the source and drain electrodes were grounded. c) Cross-section of the topography along the black line marked in panel a. The cross section shows a uniform height of about 3.5 nm that coincides with the calculated length of the molecule.

5. Device fabrication

Heavily doped arsenic (n^{++}) Czochralski silicon wafers (0.001-0.005 Ω/cm) were used as substates. The wafers were thermally oxidized at 1000 ºC in an oven until a 200 nm thermal oxide layer was grown. The layer thickness was confirmed by ellipsometry measurements. The wafer is used for fabricating discrete transistors. The substrate acts as common gate. The capacitance per unit area amounts to 17 nF/cm^2. As source and drain electrode a 50 nm to 100 nm gold layer was sputtered. A 5 nm to 10 nm Ti film was used as adhesion layer. The electrodes were defined by standard photolithography and wet etching. The MIM stack is used to assemble discrete SAMFETs.

Electrical contacts

The SAM layer is only 3.5 nm thick. The necessary use of adhesion layers therefore can inhibit injection. We show below with TEM images on cross sections obtained with focussed ion beam milling (FIB) that the gold electrodes are under-etched. The titanium at the edge of the electrode is dissolved. The electrode is collapsed and the gold makes intimate contact with the SiO_2. Hence, despite the use of the Ti adhesion layer, the charge injection occurs through the Au contact. This is confirmed by fabrication of functional SAMFETs without Ti adhesion layer exhibiting comparable mobilities.

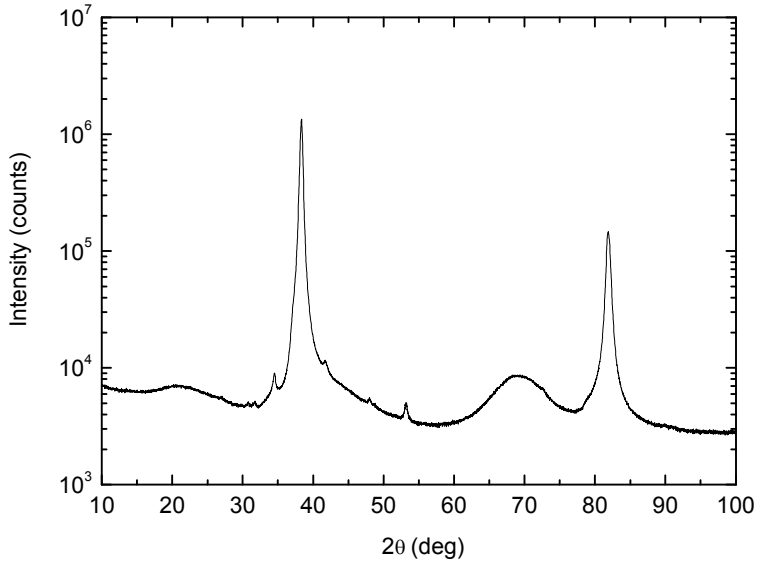

Fig. S12. X-ray diffractogram of a 50 nm Au film on SiO_2 using a 5 nm Ti adhesion layer. The diffraction peaks at 2Θ values of 38.3^0 and 81.8^0 are due to preferentially <111> oriented gold.

The source and drain contacts are made from gold. Titanium is used as an adhesion layer. The contacts are characterised with XRD, X-ray reflectivity measurements and FIB-TEM measurements. The diffracted intensity as a function of 2Θ measured on a wafer with 5 nm Ti and 50 nm Au is presented on a semi-logarithmic scale in Fig. S12. The peaks at 38.3^0 and 81.8^0 are due to <111> oriented gold. This preferential orientation is typical for metals with an fcc crystal structure. The other minor diffraction peaks are due to spectral impurities of the X-ray beam, *e.g.* Cu Kβ, W Lα. None of the diffraction features can be attributed to the Ti film. The presence of the Ti adhesion layer however can be inferred from X-ray reflectivity measurements. The reflected X-ray intensity is presented in Fig. S13 as a function of angle of incidence. The experimental data are represented in blue. The red line is the calculated reflectivity curve. A good agreement is obtained. The high frequency oscillations are interference patterns due to the 50 nm gold layer. The longer wave oscillations originate from the 5 nm titanium adhesion layer. This implies that when the electrode

contains an adhesion layer of *exposed* titanium, poor injection from the electrode into the SAM is expected.

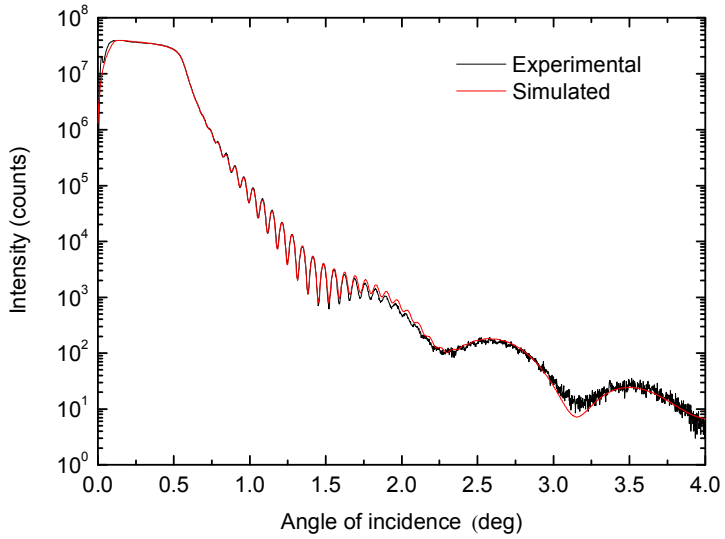

Fig. S13. X-ray reflectivity measurements on a 50 nm Au film on SiO_2 using a 5 nm Ti adhesion layer. The measured reflected intensity as a function of incidence angle is presented in blue. The calculated reflectivity curve is presented in red.

However, we will show that the titanium is not exposed. A cross section of the electrodes was made by focussed ion beam milling (FIB) followed by TEM imaging. A layer of aluminium followed by a layer of platinum is deposited over the electrode in order to protect the sample during focussed ion beam milling. Using 30 keV Ga-ions a hole is milled twice in the surface with one steep edge oriented perpendicular to the sample surface, and a step like construction at the opposite side. The thin slab between the steep edges is lifted, further milled to electron transparency, and investigated separately with TEM. The spatially resolved transmitted electron density is presented in Fig. S14. The electron density reveals the chemical composition. Fig S14 shows from bottom to top the doped Si gate, the SiO_2 gate dielectric, a thin partially covered Ti layer, followed by a Au, Al and Pt film, respectively.

The Au is clearly under-etched by about half a micron. The Ti layer at the edge of the contact is dissolved. The Au collapses on the SiO_2. The arrow in Fig. S14 shows that exactly at the edge of the Ti layer a void is formed. The collapsed Au makes intimate contact with the SiO_2. Hence, despite the use of the Ti adhesion layer, the charge injection occurs through the Au contact.

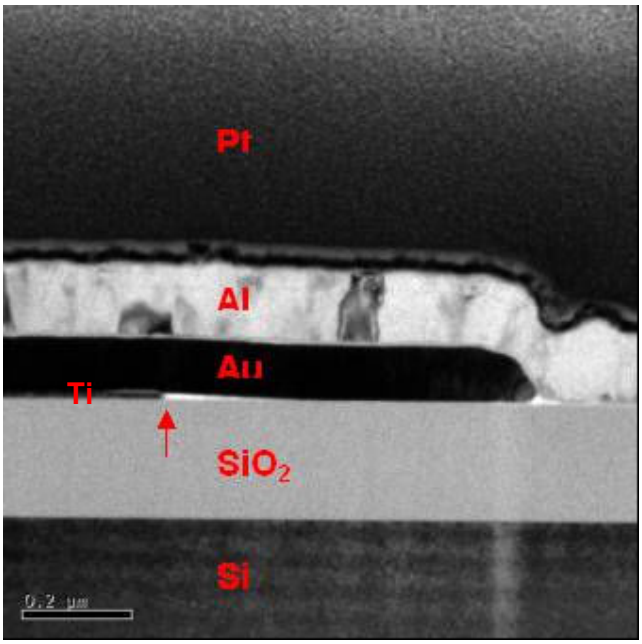

Fig. S14. Bright field TEM image of the edge of an electrode. The chemical composition of the layers is indicated. The gold is under-etched by about half a micron. The arrow points to the end of the titanium adhesion layer.

This last statement is confirmed by fabrication of SAMFETs without Ti adhesion layer. The limited adhesion of Au on bare SiO_2 prevents wet processing. Instead of wet etching of the gold, dry etching with Ar ions was used to define source and drain electrodes. Similarly the SiO_2 cannot be activated using a wet acid dip. Instead only an oxygen plasma was used. The SAMFETs were then prepared following the standard procedure of submerging the samples in a solution containing the active molecules. The electrical transport measurements show non-zero pinch off voltages presumably due to fixed ions at the SiO_2 interface. However, in all cases functional SAMFETs were obtained with comparable mobility.

6. Electrical transport in discrete SAMFETs

All measurements were performed in dynamic vacuum of 10^{-6} mbar. The devices were first annealed at 120 °C to remove any contaminants of water and solvent. Typical linear and saturated transfer curves as measured in vacuum and ambient air are presented in Fig. S15. The mobility was determined in the linear (V_d = -2 V) and saturated (V_d = -20 V) regime by $\mu_{lin,FET} = -LV_d / WC \cdot dI_{ds} / dV_g$ and $\mu_{sat,FET} = -L / WC \cdot d(dI_{ds} / V_g) / dV_g$ respectively. Fig. S15 shows that there is no hysteresis in vacuum. In air the SAMFETs function properly despite a slight hysteresis. The linear mobility is comparable to the saturated mobility and amount to about 0.03 cm^2/Vs, both in air and vacuum.

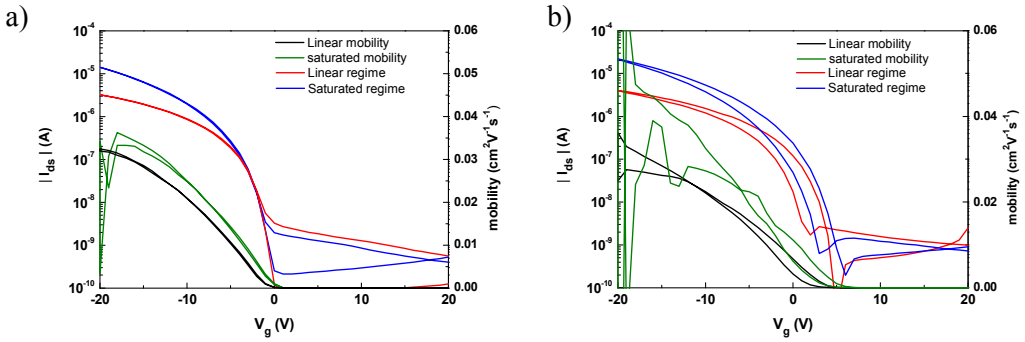

Fig. S15. Transfer characteristics of a SAMFET measured in a) vacuum and b) air.

The activation energy of the mobility was measured using a ring transistor with a channel length of 40 μm and a width of 1000 μm. The mobility as a function of temperature is presented in Fig. S16. The mobility is thermally activated. The activation energy as obtained from $\mu_{FET}=\mu_0 \exp(-E_a/kT)$ amounted to 80 meV.

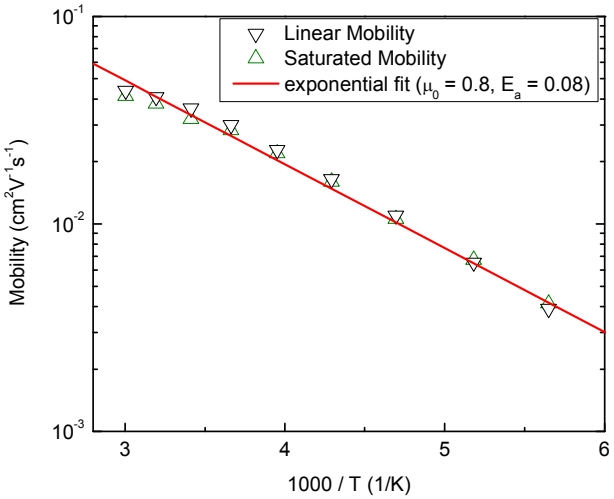

Fig. S16. The mobility of a SAMFET as a function of temperature.

For disordered semiconductors the activation energy scales with the absolute value of the mobility[7]. The same relation holds for polycrystalline and single crystalline semiconductors[8]. The value found for the activation energy of 80 meV therefore could indicate transport by hopping in a disordered semiconductor or could be due grain boundaries, *i.e.* the transport could be trap limited.

Parameter extraction and statistics

We have extracted the key device parameters for 60 so-called interdigitated finger transistors and 24 ring transistors, *viz.* the linear mobility, the saturated mobility, the threshold voltage, switch-on voltage, On/Off current ratio and subthreshold slope. The

transistors vary in channel length and channel width. We note that the mobility is a function of channel length. Fig. S17 shows the parameter spread. The scaling of the mobility with channel length will be addressed in detail below.

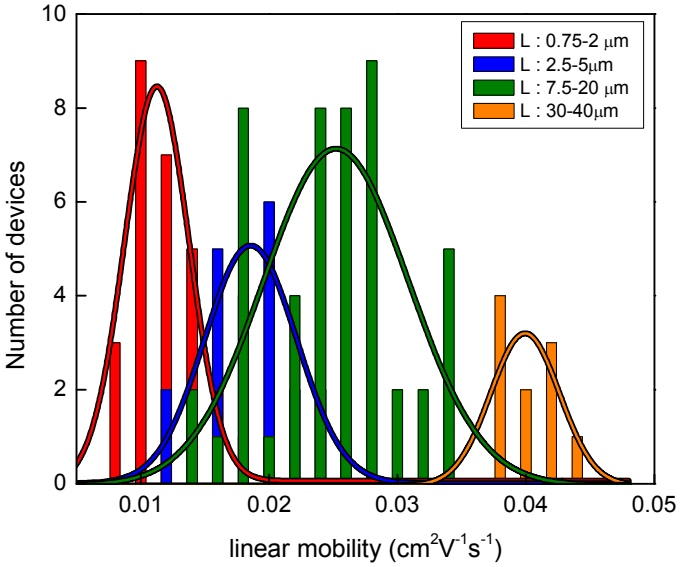

Fig. S17. The linear mobility for SAMFETs with varying channel width and length is plotted. By using a Gaussian fit the following values were obtained for L = 0.75-2, center = 0.011 $cm^2V^{-1}s^{-1}$ width = 0.005, L = 2.5-5, center = 0.019 $cm^2V^{-1}s^{-1}$ width = 0.007, L=7.5-20, center = 0.025 $cm^2V^{-1}s^{-1}$ width = 0.01, L= 30-40, center = 0.040 $cm^2V^{-1}s^{-1}$ width = 0.005.

For the statistical analysis the variation of mobility with lateral dimensions is ignored. This implies the presented standard deviations are upper limits. Table S3 summarises the linear mobility, the saturated mobility, the threshold voltage, switch-on voltage, On/Off current ratio and subthreshold slope.

Finger transistor (60 devices)	Lin mob (cm^2/Vs)	Sat mob (cm^2/Vs)	V_t (V)	V_{so} (V)	On/Off	S (V/dec)
Value	0.024	0.024	0.77	4.8	$2\ 10^6$	0.87
σ	0.008	0.007	0.26	1.2	$3\ 10^6$	0.16

Ring transistors (24 devices)	Lin mob (cm^2/Vs)	Sat mob (cm^2/Vs)	V_t (V)	V_{so} (V)	On/Off	S (V/dec)
Value	0.016	0.017	-3	0.14	$3\ 10^8$	0.55
σ	0.009	0.007	0.4	0.31	$3\ 10^8$	0.1

Table S3. Summary of extracted key SAMFET parameters

The threshold voltage is obtained as intercept from a square root extrapolation of drain current versus gate bias. The switch-on voltage is arbitrarily taken as the gate bias where the drain current in the linear regime is 10 nA. The On/Off ratio is taken as the current

ratio in the saturated regime at gate biases of -20 V and +20 V. The subthreshold slope is obtained at the minimum derivate of the gate bias over the logarithm of the drain current.

The standard deviations are benchmarked with organic TFTs previously used to fabricate 32-stage shift registers.[9] These integrated circuits combined 1888 transistors. The standard deviations in mobility and threshold voltage of the SAMFETs as presented in Table S3 are comparable to the reported values.[9] The reason for the different mobility in ring and finger transistors is not yet fully understood. It could originate from stray fields. In the ring transistors the circular drain is enclosed in the source electrode. This eliminates parasitic currents originating from an unpatterned semiconductor and gate. Hence the On/Off current ratio of the ring transistors exceeds that of the interdigitated finger transistors.

Scaling of mobility with channel length

We have investigated the scaling of the mobility with lateral dimensions. The nominal channel length was varied between 0.75 μm and 40 μm. Typical linear and saturated mobility for fully covered SAMFETs are presented in Fig. S18 as a function of channel length. Fig. S18 shows that there is no difference between linear and saturated mobility, and that the mobility decreases with decreasing channel length.

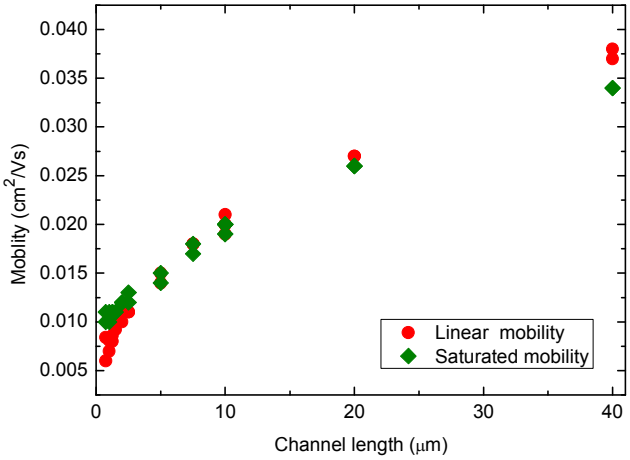

Fig. S18. The linear and saturated mobility of SAMFETs as a function of channel length. The nominal channel length was varied between 0.75μm and 40 μm.

The scaling behaviour is due to a contact resistance. In first order the total device resistance, R_{on}, is given by: [10]

$$R_{ON}(L) = \left.\frac{\partial V_{sd}}{\partial I_{sd}}\right|_{V_{sd}\to 0} = R_{ch}(L) + R_p \qquad (1)$$

where the parasitic contact resistance, $Rp = Rs + Rd$, at the source and drain contacts is assumed to be independent of the channel length. The device resistance is presented as a function of channel length in Fig. S19. The gate bias is varied in steps of 2.5 V

from – 2.5 V (black symbols) to – 20 V (brown symbols). A fair agreement with Eq. (1) is obtained. From the slope of the fit we find the channel resistance, R_{ch}, the inverse of which, $[\Delta R_{on}/\Delta L]^{-1}$, is the channel conductivity. From the derivative of the channel conductivity, the field-effect mobility corrected for the contact resistance can be obtained:

$$\frac{\partial\left(\left[\frac{\Delta R_{ON}}{\Delta L}\right]^{-1}\right)}{\partial V_g} = \mu_{FE}(V_g)WC_i \qquad (2)$$

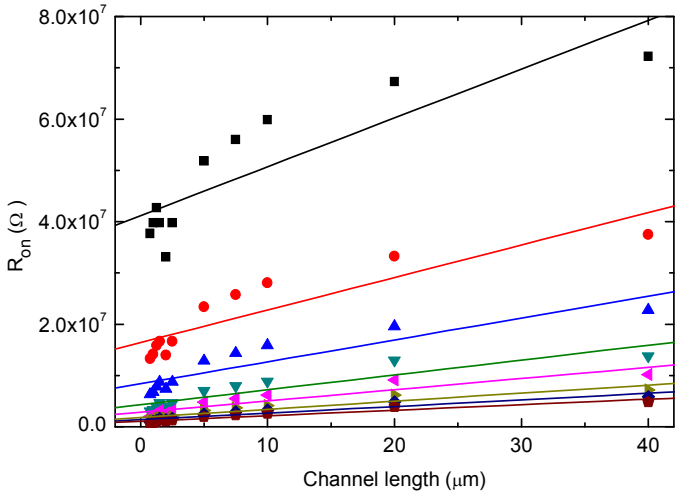

Fig. S19. The total device resistance of SAMFETs as a function of channel length between 0.75 μm and 40 μm. The drain bias was kept at –2 V. The gate bias is varied in steps of -2.5 V from -2.5 V (black symbols) to -20 V (brown symbols).

The calculated corrected mobilities are presented as a function of gate bias in Fig. S20 as the black squares. The measured mobilities for the various channel lengths are included as well. Fig. S20 indicates that according to this analysis the contact resistance cannot be observed for channel lengths larger than 40 μm. In first order approximation the SAMFET does not behave differently than regular organic field-effect transistors.

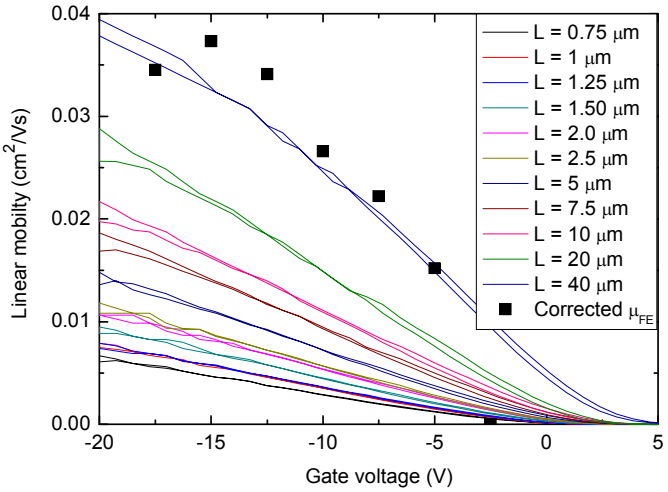

Fig. S20. The linear mobility of a SAMFET as a function of gate bias. The solid lines are the measured mobilities for channel lengths between 0.75 μm and 40 μm. The solid squares are the linear mobilities corrected for contact resistances.

Partially covered SAMFETs

For a monolayer transistor it is expected that the mobility is a function of coverage. Therefore we investigated the electrical transport of partially covered SAMFETs. Partially covered SAMFETs were formed both by reducing the concentration of active molecules in the solution from 1 mM to 0.05 mM and by varying reducing the incubation time between 15 minutes and 2 days. The coverage was determined from AFM pictures, similar to Fig. S11, and averaged over 4 different positions. The mobility for a transistor with a channel length of 7.5 μm as a function of coverage is presented in Fig. S21. At 5% coverage the mobility cannot reliably be measured. The value presented is an upper limit. Fig. S21 shows that the mobility increases with coverage. A coverage of almost 100 % is needed to obtain the maximum mobility.

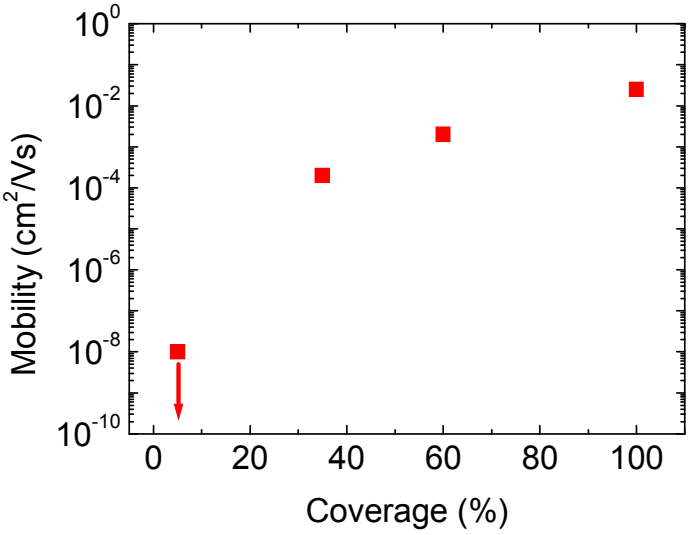

Fig. S21. Field-effect mobility of SAMFETs as a function of surface coverage. The mobility was measured for transistors with a channel length of 7.5 μm. The surface coverage was obtained from AFM measurements.

The data of Fig. S21 was obtained using a channel length of 7.5 μm. The mobility depends on the channel length as well. We take a partially covered SAMFET. In the limiting case that the channel length goes to infinity there is no percolating path. The mobility then goes to zero. As an example the transfer curves for a partially covered SAMFET are presented in Fig. S22 as a function of channel length. For fully covered SAMFETs we have shown that the contact resistance becomes more prominent for small channels. Consequently with increasing channel length the mobility increases. However, partially covered SAMFETs show inverse scaling. With increasing channel length the extracted device mobility decreases.

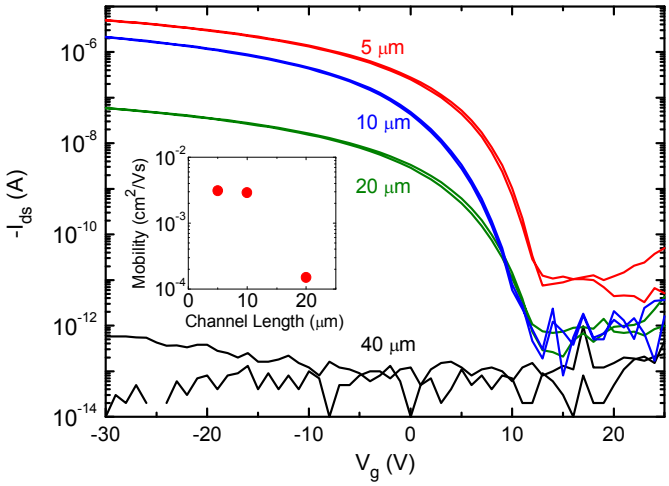

Fig. S22. Transfer characteristics of a partially covered SAMFET as a function of channel length. No current is observed for a transistor with a channel length of 40

μm. The inset shows inverse scaling, with increasing channel length the mobility decreases.

Reliability under prolonged gate bias

We fabricate our SAM onto a hydrophilic SiO_2 substrate containing a large density of OH groups. The presence of OH[11,12] and water[13,14] is known to have a detrimental effect on device reliability. Because we cannot rule out the presence of residual OH groups at the SiO_2 SAM interface by chemical analysis, we measured the reliability of the SAMFET under gate bias stress and benchmarked the stability. As a typical example, transfer curves are presented as a function of stress time in Fig. S23a. The applied gate bias during stress was -20 V and the temperature 60 °C. Transfer curves were measured at a drain bias of -2 V by sweeping the gate bias from + 20 to -35 V. The transfer curve shifts with stress time in the direction of the gate bias; in Fig. S23a to the left. Threshold voltage shifts were extracted from the transfer characteristics and plotted as a function of time in Fig. S23b. The time dependence of the threshold voltage shift (ΔV_{th}) is best described using a stretched exponential time relaxation:

$$\Delta V_{th} = V_0\left(1-\exp\left(-\frac{t}{\tau}\right)^{\beta}\right) \qquad (3)$$

in which V_0 equals the applied bias during stress minus the initial threshold voltage. The characteristic time scale for the process is denoted with τ. This empirical relation allows for comparing different transistors with different organic semiconductors. The values of τ and β deduced from the fit in Fig. S13b are $6.5 \cdot 10^4$ s and 0.4 respectively. The values obtained for τ and β are in the same range as for other organic semiconductors on HMDS passivated silicon dioxide gate dielectrics such polytriarylamine and PTV.[13] Hence, the reliability of the SAMFET is comparable to that of other organic transistors. The reliability is implicitly supported by circuit measurements. These large integrated circuits combining over 300 transistors only function when there is a small parameter spread and when there is no hysteresis in the discrete SAMFETs.

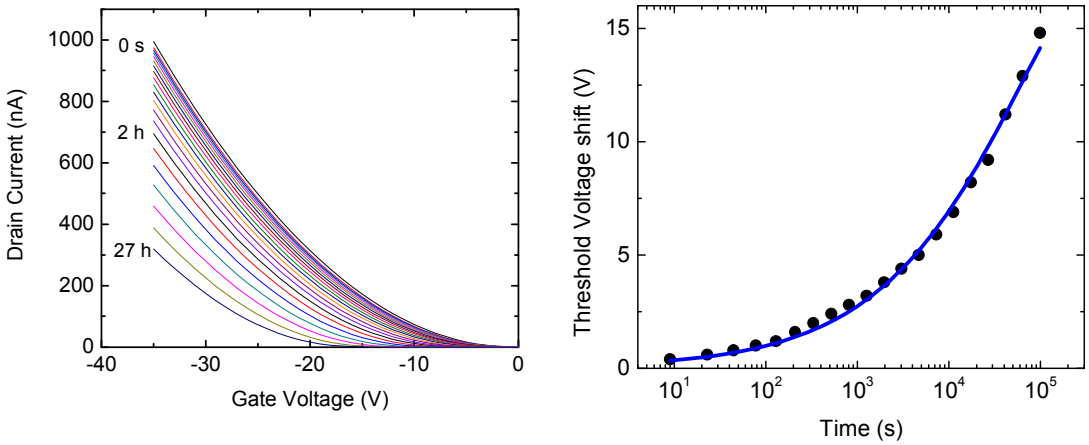

Fig. S23. a) Transfer curves in the linear region of a SAMFET as a function of time under applied gate bias of -20 V. The temperature was 60 °C. b) The threshold

voltages obtained from Fig. 3a presented as a function of time on a semi-logarithmic scale. The fully drawn curve is fit with a stretched exponential time dependence.

7. Integrated circuits

Integrated devices require a patterned gate and vertical interconnects. A monitor wafer was used as support. To prevent parasitic leakages, a 1.5 µm thick oxide layer was thermally grown. On this support, 250 nm of phosphor doped polysilicon was applied via low-pressure chemical vapour deposition. The polysilicon layer was structured by photolithography and Reactive Ion Etching (RIE) to define the gate electrodes and the first layer of interconnects. The polysilicon was subsequently thermally oxidized to yield a 130 nm gate oxide (26.5 nF/cm^2). The vertical interconnects were defined in the gate oxide by photolithography and RIE etching. Finally for the second layer of interconnects and source and drain electrodes, a gold layer (150 nm) with a thin titanium adhesion layer (5 nm) was sputtered and patterned via photolithography and wet etching.

SAMFETs made with polysilicon gates overgrown with SiO_2

A typical linear and saturated transfer curve for a SAMFET using a patterned polysilicon gate and a channel length of 10 µm is presented in Fig. S24. The inset shows the scaling of the mobility with channel length. Fig. S24 shows that the electrical transport in SAMFETs using thermally grown oxide on single crystalline Si and on patterned polysilicon is similar. This is remarkable taking into account the higher roughness of the polysilicon gates overgrown with thermal oxide.

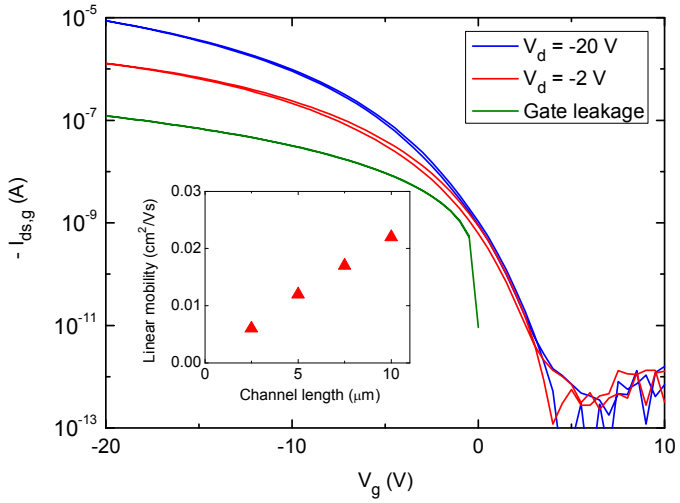

Fig. S24. Linear and saturated transfer characteristics as well as the gate current measured of an integrated SAMFET with a channel length of 2.5 µm and a channel width of 1000 µm, using drain biases of -2 and -20 V, respectively. The inset shows the linear and saturated mobility as a function of channel length.

The gate current is presented as the green curve. The gate current is an order of magnitude lower than the drain current. The magnitude of the gate current does not depend on the drain bias or on the lateral dimensions of the channel. The gate current is a parasitic current between source and gate, due to the use of an unpatterned semiconductor. In actual integrated circuits the gate current is minimised by design measures as explained separately below.

Polysilicon surfaces are notoriously rough. The field-effect mobility of organic transistors is reported to decrease exponentially with increasing surface roughness. [15-18] For polycrystalline pentacene thin film transistors a reduction in mobility of one order of magnitude has been reported for a surface roughness of 2 nm[15] as well as for a surface roughness of 4 nm.[16] A reduction in mobility with surface roughness has also been reported for semi-crystalline semi-conducting polymers.[17,18] For poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophene (pBTTT) a factor of four hundred for a surface roughness was reported for a surface roughness of 3 nm.[17] For pBTTT substituted with hexadecyl side chains the reduction was much smaller, only a factor of 10 for the same roughness of 3 nm.[18] In summary, we had expected a significant decrease in charge transport properties of the SAMFETs using polysilicon gates. Fortunately, that turned out to be not the case. The mobility of the SAMFET appears to be remarkably insensitive to the interface roughness.

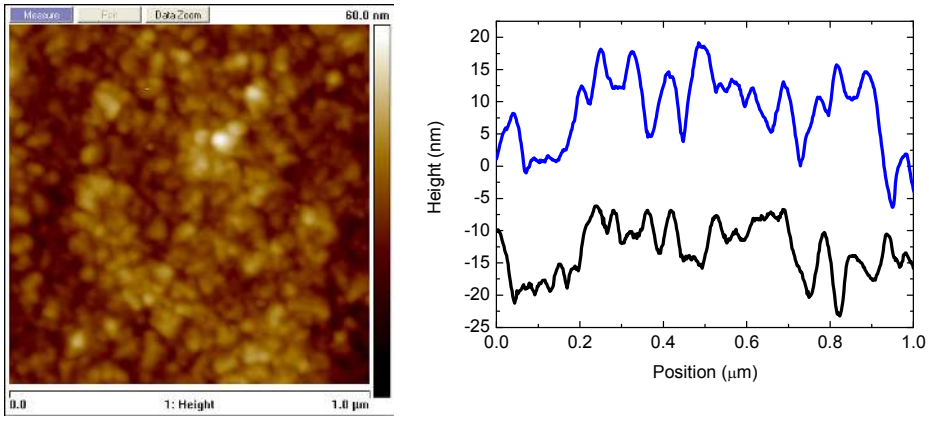

Fig. S25. AFM height profile of a polysilicon gate overgrown with thermal oxide and two representative cross sections. The profiles are shifted for clarity. The rms roughness of the dielectric interface amounts to 4 nm.

To elucidate the influence of topography on mobility we measured the surface roughness with AFM. The height image of a polysilicon gate overgrown with thermal oxide is presented in Fig. S25. The rms surface roughness is typically 4 nm. Despite the surface roughness, the mobility of the SAMFET is comparable to those made on atomically smooth SiO_2. The decrease in mobility is at most a factor of two. This unexpected result could be due to the conformal growth of the SAM on the SiO_2. The growth mechanism is then completely different from that of pentacene where upon changing the surface roughness large changes in morphology are reported.[15,16] This hypothesis was confirmed by fabricating transistors with amorphous polytriarylamine (PTAA) as the semiconductor. The transfer curves using atomically smooth SiO_2 as gate dielectric and using polysilicon gates overgrown with thermal oxide are presented in Fig. S26. Despite the difference in surface roughness the transfer curves

are similar. The field-effect mobility amounts to $2 \cdot 10^{-3}$ cm2/Vs in good agreement with literature data.[19]

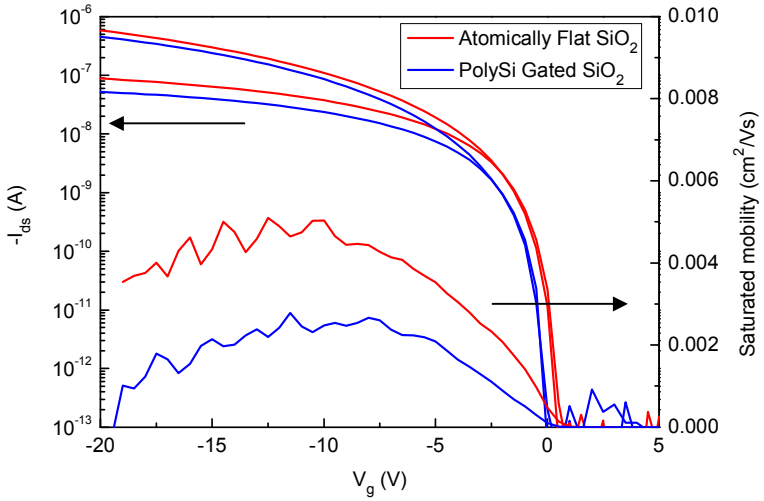

Figure S26. Linear and saturated transfer curves of transistors using polytriarylamine as a semiconductor. The red curve corresponds to the transistor using atomically flat, thermally grown SiO_2 as a gate dielectric. The blue curve corresponds to the transistor using a polysilicon gate overgrown with thermal oxide. The saturated field-effect mobilites are 0.004 and 0.002 cm^2/Vs respectively. Despite the difference in surface roughness the change in mobility is only a factor of about two.

Design, lay-out and circuit modelling

Circuit simulations have been performed using a proprietary circuit solver and a model based on nine technology parameters. Details on the underlying physics and the equations used in this model are given in ref. 20.

Ring oscillators

Integrated inverters based on $V_{gs=0}$ logic were used. The load to driver ratio was 6 and the channel length of was 2.5 µm. Inverters were combined into 7-stage ring oscillators. A buffer stage was added to determine the switching frequency. An optical photograph of a ring transistor is presented in Fig. S27. The channel length is 7.5 µm. The circular drain is enclosed into the source electrode to minimise parasitic currents The top right panel shows an optical photograph of an inverter. The bottom panel shows an optical photograph of a seven stage ring oscillator using V_{gs} is zero logic.

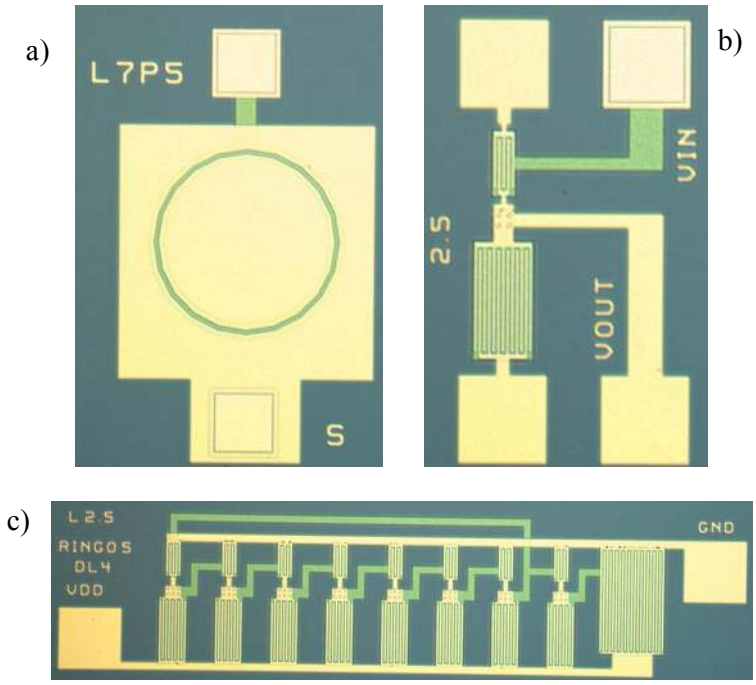

Fig. S27. a) Optical photograph of a ring transistor. The channel length is 7.5 μm. The circular drain is enclosed into the source electrode to minimise parasitic currents. b) Optical photograph of an inverter. The channel length of driver and load transistor is 2.5 μm. (c) Optical photograph of a seven stage ring oscillator using V_{gs} is zero logic. The channel length is 2.5 μm. The ratio between the widths of driver and load is 4.

The ring oscillators were measured at a supply voltage of -10 V over a resistor with an oscilloscope as demonstrated in the left panel of Fig. S28. An oscillation frequency of about 5 kHz was obtained as shown in the right panel of Fig. S28.

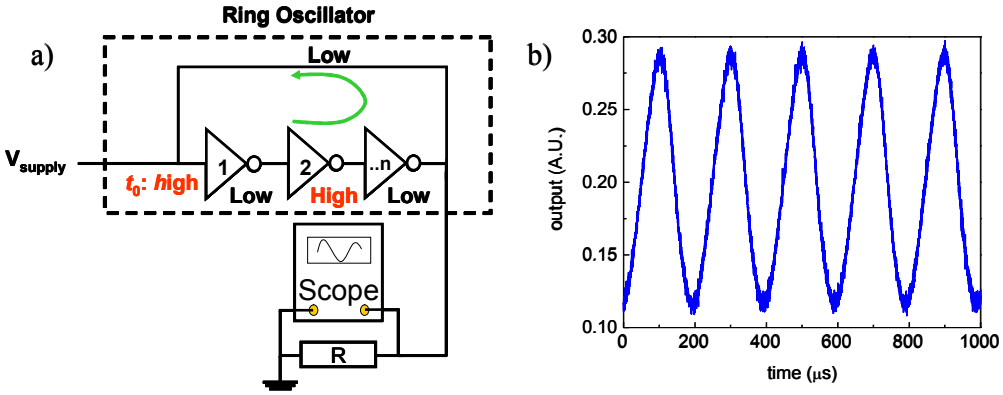

Fig. S28. a) Schematic overview of the measurement set-up for the ring oscillators. b) A SAMFET based integrated ring oscillator oscillating at a frequency of 5 kHz with a supply voltage of -10 V.

Reduction of parasitic currents

The technology used to integrate SAMFETs in circuits does not include, at the moment, a patterning step for the semiconductor. As a consequence, a semiconductor monolayer covers the entire wafer surface, both the oxidized monitor wafer used as substrate and the oxidized poly lines used as gate and first interconnect electrode layer. This results in two kinds of potential leakage structures within a circuit layout. We can analyze them with the help of layout diagrams (Fig. S29) where the red areas denote gate/first interconnect layer poly, blue areas denote source/drain and second interconnect layer metal and black is used for vias between interconnect levels one and two.

a) Semiconductor layer between two metal contacts without underlying gate (highlighted in green in Fig. S29a). In adjacent transistors the external contacts (marked D_1 and D_2 in the picture) are always connected to the same potential (normally one of the bias voltages: V_{dd} or Ground) so that no current can flow between them.[21] This measure minimizes the leakage current flowing through this kind of resistive structures.

b) Semiconductor layer between two metal contacts with an underlying gate. This kind of structure actually forms parasitic transistors. One example of such parasitic is shown in Fig. S29b, where the channel is highlighted in green and source and drain are marked with the letters S and D. Special effort has been put during layout to make these parasitic transistors as long as possible (see picture), to minimize the current flowing through them.

Using the layout techniques here described it was possible to keep leakage under control, as witnessed by the functional circuits.

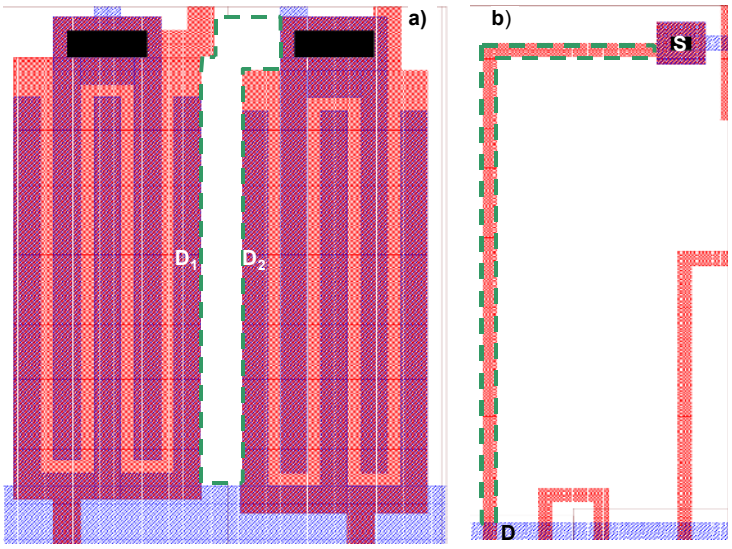

Fig. S29. Parasitic structures present in the circuit layout

Design and lay-out of a 15-bit code generator

A detailed block diagram of the 15-bit code generator circuit is shown in Fig. S30. An integrated ring oscillator generates a square wave that clocks a 4-bit counter. The counter output is transformed by a decoder in 15 enable signals, of which only one at a time is active. These signals enable each memory bit one after the other, while a 15-input OR combines the memory outputs on a single line, where the programmed code appears as a serial sequence of one and zeros (Fig. 4 in the letter). This serial line is connected to the gate of a load modulator, i.e. a transistor connected between the power supply voltages, which can be used to change the antenna impedance and hence send back the generated code in RFID applications.[22]

The different circuit blocks are designed using fully-standard digital design procedures using exclusively inverters, NAND and flip-flops based on the $V_{gs=0}$ logic. A detailed report on the schematic used and on the design issues encountered in these elementary building blocks is given in ref. 22.

The device geometry is shown in Fig. S29. Source and drain are interdigitated to allow a layout containing a large *W*/*L* transistor with a compact footprint. The geometry of the transistor is described in the simulation model using as parameters *L* (transistor length), *W* (transistor width), *mult* (number of parallel channels) f_w (finger width) and g_e (extension of the gate past the inner drain edge (see Fig. S29)). The gate-source and gate-drain overlap capacitances are evaluated for each transistor by the circuit solver employing the parallel-plate capacitor formula (C_{ox}= 26 nF/cm). The overlapping areas are calculated using the geometry parameters. The total channel capacitance is attributed half to the source and half to the drain contact under all bias conditions. Although this is a rough approximation, it turns out to be sufficient to approximate the dynamic behaviour of our slow circuits. The geometry parameters of the transistor used in most inverters and NANDs are summarized in Table S4.

Circuit		*W* [μm]	*L* [μm]	*mult*	f_w [μm]	g_e [μm]
V_{gs}=0 inverter	Drive transistor	50	2.5	2	5	5
	Load transistor	300	2.5	4	5	5
V_{gs}=0 NAND	Drive transistor	50	2.5	2	5	5
	Load transistor	400	2.5	4	5	5

Table S4: Geometry parameters of the transistors used in the inverters and NAND gates

An optical photograph the functional 15-bit SAMFET code generator is presented in Fig. S31. The circuit combines over 300 SAMFETs

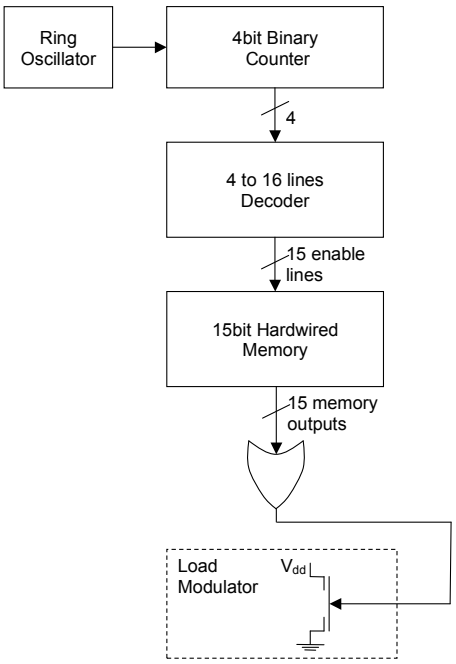

Fig. S30. Block diagram of the 15-bit code generator.

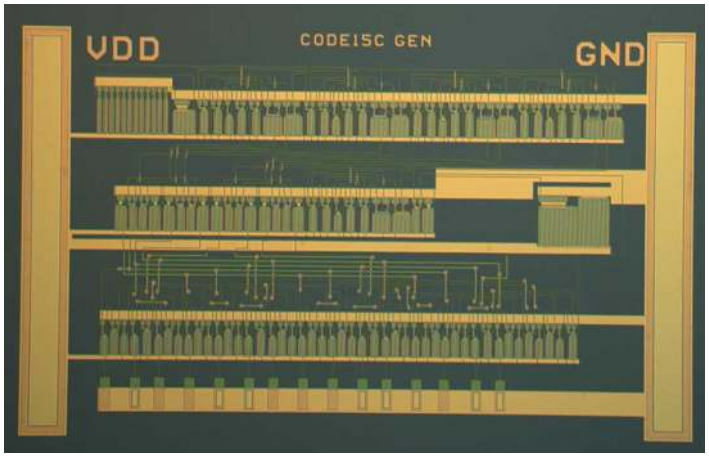

Fig. S31. Optical photograph of a functional 15-bit SAMFET code generator. The circuit combines over 300 SAMFETs.

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