BPSK to ASK Signal Conversion Using Injection-Locked Oscillators–Part II: Experiment

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***Abstract*—This paper demonstrates the feasibility of a new circuit for the conversion of binary phase-shift keying signals into amplitude-shift keying signals. In its simplest form, the converter circuit is composed by a power divider, a couple of second harmonic injection-locked oscillators, and a power combiner. The operation of the converter circuit relies on the frequency synchronization of both oscillators and the generation of an interference pattern by combining their outputs, which reproduces the original phase modulation. Two prototypes of the converter have been implemented. The first one is a hybrid version working in the 400–530-MHz frequency range. The second one has been implemented using multichip-module technology, and is intended to work in the 1.8–2.2-GHz frequency range.**

***Index Terms*—Amplitude-shift keying (ASK), CMOS analog integrated circuits, converters, injection-locked oscillators (ILOs), multichip modules (MCMs), phase shift keying.**

I. Introduction

In PART I of this paper [1], a new method to convert binary phase-shift keying (BPSK) signals into amplitude-shift keying (ASK) signals based on the use of second harmonic injection-locked oscillators (ILOs) has been presented. The dynamic behavior of injected oscillators as a response to phase changes of the input signal has been analyzed in detail. The conversion mechanism, based on frequency and phase synchronization and interference phenomena, has been studied exhaustively and, finally, the limitations of the conversion process related to the characteristics of the BPSK signal have been considered as well. This second part is devoted to the discussion of practical issues related to the implementation of the new converter circuit.

To demonstrate the feasibility and performance of the conversion method, two prototypes of the converter have been implemented. The first one is a hybrid version working in the range of 400–530 MHz. The second one is a multichip module (MCM) version operating between 1.8–2.2 GHz. Fig. 1 shows a block diagram of the circuit. In both hybrid and MCM versions, the converter circuit is composed by a power divider, two second harmonic ILOs, and a power combiner. The use of this circuit topology allows much simpler implementation of BPSK demodulators than using synchronization loops. Hence, coherent demodulation of BPSK signals can be accomplished just cascading a simple envelope detector with the BPSK to ASK converter circuit.

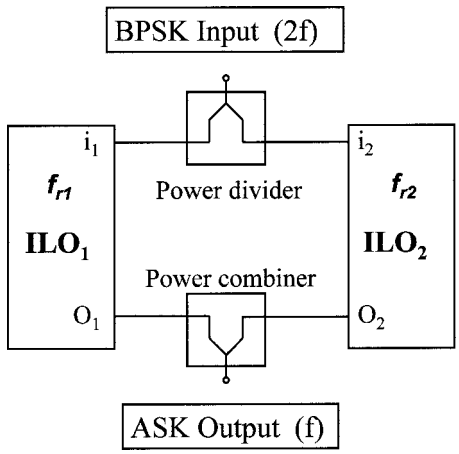

Fig. 1. Circuit block diagram of the proposed BPSK to ASK converter.

II. Design Methodology and Fabrication Technologies

Both prototypes of the converter circuit have been designed and implemented using a system-in-package (SiP) approach [2], [3]. In contrast with the system-on-chip (SoC) approach, SiP design methodology combines different technologies, processes, and packaging techniques to get a compact RF system. The key of success is to use the best available technology to realize each part of the system, in this way getting the best performance at the lowest price in the smaller package. The SiP approach applied to the design of compact RF systems requires: 1) *a technological platform*: i.e., the set of available fabrication processes and mounting/packaging techniques and 2) *technology partitioning rules*: for a given technological platform, partitioning rules have to be defined in order to implement each part of the circuit using the best available technology according to performance and/or cost criteria.

In our case, the technological platform used to implement the hybrid version of the converter circuit is a standard printed circuit board (PCB) process, which combines lumped surface mount device (SMD) active and passive components and printed passives on an FR4 standard substrate. For the design and implementation of the MCM version, a substrate carrier fabricated on 100-mm-diameter glass wafers (Pyrex 7740) has been used. Two metal levels (Al/0.5%Cu/0.75%Si) with

Manuscript received January 31, 2005; revised July 8, 2005. This work was supported by the Spanish Science and Technology Commission under Project TIC2001-2947-C02-01.

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Digital Object Identifier 10.1109/TMTT.2005.860335

a thickness of 1.5 μm are available as interconnects and to perform the required embedded passives. Intermetal dielectric and passivation layer material is Polyamide with a thickness of 4.5 μm. RF integrated circuit (RFIC) dies including the active part of the circuit have been fabricated using 0.35-μm CMOS technology. These dies have been mounted by flip-chip on the carrier substrate using Pb/Sn solder bumps over pads with a previous Ti/Ni/Au metallization.

Common technology partitioning rules have been established in both hybrid and MCM implementations. They can be summarized in the following three main rules.

1) Keep as simple as possible the fabrication process of the carrier substrate. Obviously, the carrier substrate is the most area consuming element. Thus, a complete fabrication process to allow all kinds of embedded passives (i.e., resistors, capacitors, inductors, and transformers) could be noncompetitive in terms of cost. It could be a better solution to integrate some passives together with the active devices, or use miniature SMD passive components directly attached to the carrier substrate.
2) Think about tunability and reusability when designing the active parts. RF modules have a certain degree of tunability in between the monolithic and hybrid extremes. By redesigning and replacing some parts, it could be possible to achieve the expected performance of the whole RF module. Moreover, a shrewd design of the active parts allows them to be reused in different modules.
3) Use embedded transformers as much as possible. Embedded transformers are very easy to implement on the carrier substrate. They are more effective than inductors for harmonic and noise suppression in resonant tanks. Moreover, they can replace inductors chokes and coupling capacitors between stages, facilitating biasing.

III. Converter Circuit Design and Implementation

A. Power Divider/Combiner Design

Key components in the design of the BPSK to ASK converter circuit are the power divider and power combiner. On one hand, the function of the power divider is to split the incoming BPSK signal in two ways, minimizing as much as possible the power loss, and the amplitude and phase mismatches. Moreover, the power divider must assure a good isolation between its outputs to prevent mutual locking of both ILOs at the second harmonic. On the other hand, the power combiner should pass input signals to the output with equal amplitude and phase changes. Moreover, good isolation between inputs is required to prevent mutual locking of both ILOs at the fundamental frequency.

The above isolation requirements allow us to discard broad-band resistive power dividers/combiners [4]. Good isolation can be achieved using a narrow-band Wilkinson power divider/combiner [5]. However, at frequencies in the range or below 1–2 GHz, this circuit is no more a compact small size implementation. Broad-band active dividers and combiners can be a good alternative, mainly in the case of a monolithic integration. However, increased noise, harmonic distortion, and power consumption are important drawbacks of this solution.

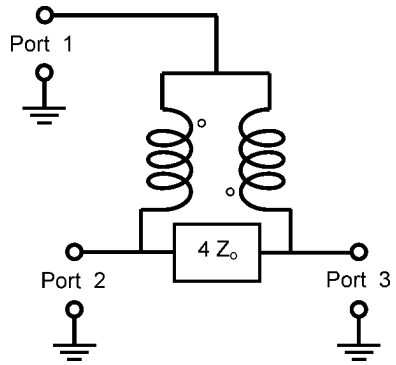

Fig. 2. Schematic circuit diagram of the broad-band power divider/combiner.

In the context of a SiP approach, the best alternative to implement the power divider/combiner consists of taking advantage of technology partitioning. The carrier substrate used to mount on active dies and SMD components can also be used to embed high-quality passives. Carrier substrates (ceramic, glass, etc.) are usually much less expensive than standard Si substrates; therefore, the required area to implement embedded inductors and transformers is not a big concern. Moreover, carrier substrates are better insulating materials than Si substrates. Consequently, the quality of embedded passives is much higher compared with that of their integrated counterparts. For all this, we finally decided to choose a broad-band passive divider/combiner based on the use of embedded or printed transformers. Fig. 2 shows the schematic diagram of the circuit [6]. The key component of the divider/combiner is the inverter transformer. Assuming that all ports are loaded by Z_o impedances and considering ideal conditions for the transformer (i.e., transformation ratio $r = 1$, coupling factor $k = 1$, and equivalent inductance $L \to \infty$), let us consider in detail the inverter transformer behavior as follows.

1) *Common-mode excitation*. Under common-mode excitation, the inverter transformer ideally acts as a short circuit. Hence, voltages at all three ports are equal, $V_1 = V_2 = V_3 = V_{\rm CM}$. Currents verify that $I_1 = -(I_2 + I_3)$ and $I_2 = I_3 = I_{\rm CM} = V_{\rm CM}/2Z_o$.
2) *Differential-mode excitation*. Under differential-mode excitation, the inverter transformer ideally acts as an open circuit. Voltages verify that $V_1 = 0$ and $V_2 = -V_3 = V_{\rm DM}$ and currents $I_1 = 0$ and $I_2 = -I_3 = I_{\rm DM} = V_{\rm DM}/2Z_o$.
3) *Single-port excitation*. When the excited port is port 1, equal fractions of the injected power (ideally 4/9) are derived to ports 2 and 3. Moreover, no phase shift or propagation delay is expected. Finally, input impedance measured at port 1 will be $Z_o/2$.

   If the excited port is ports 2 or 3, the analysis is a little more complex. The input signal should be considered as the superposition of a common mode part and a differential mode part. If the impedance connecting ports 2 and 3 is equal to $4Z_o$, common-mode voltage and current are equals to differential-mode voltage and current, respectively. Assuming that the input port is port 2, this implies that $V_3 = V_{\rm CM} - V_{\rm DM} = 0$ and $I_3 = I_{\rm DM} - I_{\rm CM} = 0$. Consequently, there is an ideally perfect isolation between

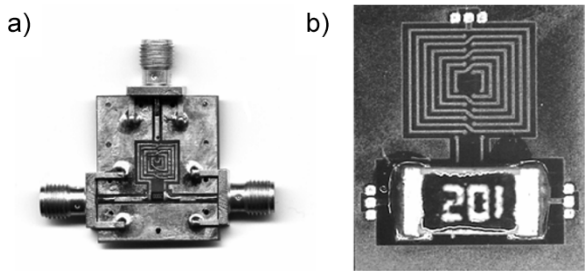

Fig. 3. View photographs of the power-divider/combiner prototypes. (a) Hybrid implementation. (b) MCM implementation.

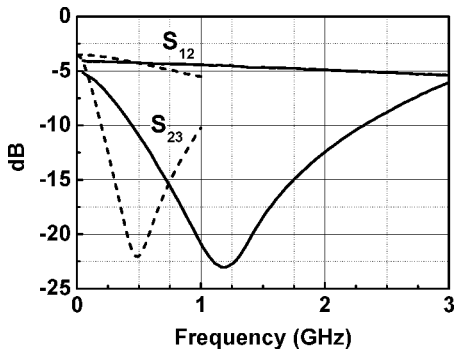

Fig. 4. Measured S-parameters of the power-divider/combiner prototypes of Fig. 3. The continuous line corresponds to the MCM version and the dashed line corresponds to the hybrid version.

ports 2 and 3. Finally, the input impedance is in this case $2Z_o$ and the fraction of the power derived from ports 2 to 1 is equal to 4/9 (-3.5 dB).

In practice, the finite inductance of the transformer, reduced coupling factor (i.e., $k < 1$), and capacitive coupling between the transformer turns will disturb the previously described behavior. As a consequence, good isolation between ports 2 and 3 will be found only in a certain frequency range.

Fig. 3 shows the photographs of two power combiner/dividers. The first one corresponds to a hybrid implementation intended to work around 500 MHz. The second one is an MCM version working around 1.2 GHz. The measured S-parameters for both power combiner/dividers are shown on Fig. 4. The hybrid implementation shows a maximum isolation of 22 dB at 490 MHz. The isolation bandwidth limits (defined as the frequencies at which isolation is equal to the maximum -3 dB) are 385 and 610 MHz. Inside this frequency range, insertion losses are between 4.0–4.5 dB, which correspond to an increase in 0.5–1 dB with respect to the ideal value of 3.5 dB. For the MCM implementation, the maximum isolation is 23 dB at 1.18 GHz and the isolation bandwidth is limited from 965 MHz to 1.41 GHz. For this frequency range, insertion loss ranges from 4.4 to 4.7 dB, which exceeds approximately 0.9–1.2 dB the ideal value.

B. ILO Design

Fig. 5 shows the schematic of the second harmonic ILO. From top to bottom, it is composed of a double transformer, couple of varactor diodes, transistors cross pair, and current source. The double transformer acts as the inductive part of the resonant tank and as a coupling element for sensing the oscillator output. Varactor diodes also play a double role: first, as the capacitive part of the resonant tank, and second, as the nonlinear element responsible for locking. The cross pair is the gain element and, finally, the current source sets the right bias conditions.

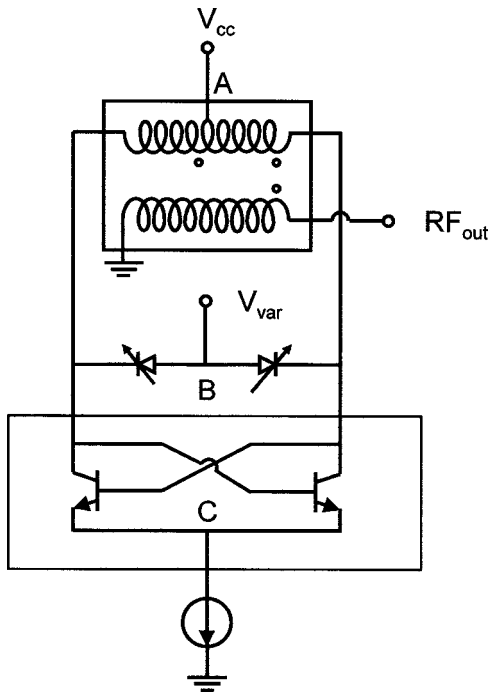

Fig. 5. Circuit schematic of a second harmonic ILO.

Labels A–C indicate common-mode nodes. In these nodes, only the presence of even harmonics of the fundamental oscillation frequency is expected. Reciprocally, common-mode nodes are the best locations to inject even harmonics (i.e., second harmonic) to assure an efficient locking. Injection at the current source level (i.e., node C) has been already used to mutually lock a couple of CMOS oscillators and generate direct quadrature outputs [7]. Due to the high impedance of node C, nodes A and B are equivalents from the point-of-view of the injection of even harmonics.

Below, each part of the general schematic in Fig. 5 will be discussed in detail, whatever concerns its functionality or its practical design and implementation.

1) *Double transformer*. As mentioned previously, the function of the double transformer is to provide a coupling output of the oscillator signal and to implement the inductive element of the oscillator resonant tank. The former functionality is accomplished by the secondary winding of the transformer, whereas the later is accomplished by the primary. Moreover, the primary is constructed by connecting both windings of an inverter transformer, as described in the power-divider/combiner design (Section III-A).

As an example, Fig. 6 shows the footprint of the double transformer used in the hybrid version of the ILO. The design has been optimized to work at a fundamental frequency around 217 MHz (i.e., half the frequency of the European 433.92-MHz industrial–scientific–medical

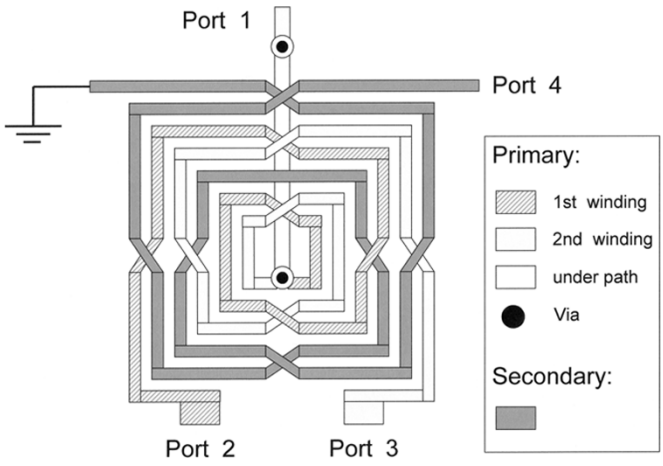

Fig. 6. Footprint of the double transformer used in the hybrid prototype of the ILO.

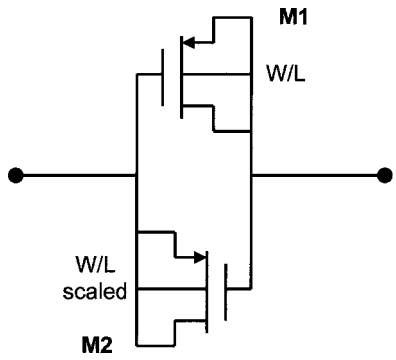

Fig. 7. Varactors configuration for the MCM prototype of the ILO.

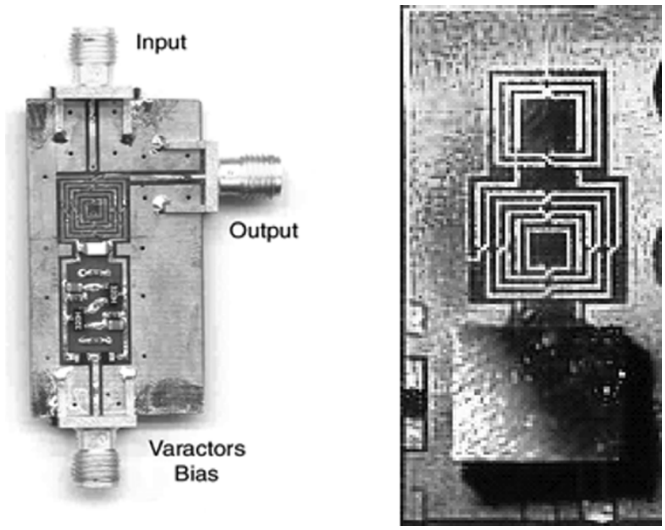

Fig. 8. View photographs of both prototypes of ILO circuits. (*left*) Hybrid version. (*right*) MCM version.

(ISM) frequency band). At the fundamental frequency, when ports 2 and 3 are excited differentially, the primary of the transformer is equivalent to an inductance of 65.5 nH. Moreover, the power transfer ratios are -30 dB to port 1 and -7 dB to port 4. Consequently, good isolation between differential (ports 2 and 3) and common nodes (port 1) is accomplished. Note that the low-power transfer to port 4 allows the use of 50-Ω loads without disturbing or even canceling the oscillator signal. In addition, the power transfer ratio at the fundamental frequency between ports 1 and 4 is equal to -18.9 dB. When port 1 is excited in the common mode at twice the fundamental frequency, the primary of the double transformer is equivalent to an inductance of 12 nH, which is 25% lower than the obtained if, instead of coupled inductors, two single noncoupled inductors were used to form the primary. Finally, the power transfer ratio at twice the fundamental frequency between ports 1 and 4 is -20.2 dB. This figure reduces the coupling of common mode signals at port 1 to the output at port 4.

Apart from the inductance values, which are scaled according to the different operating frequency, similar performances are obtained for the double transformer included in the MCM version of the ILO circuit.

2) *Varactor diodes*. For implementing the hybrid version of the ILO circuit, a couple of discrete BB 833 varactor diodes have been used. The high-capacitance ratio of these devices (i.e., more than 10 from 1- to 10-V reverse bias) allows to change the free-running frequency of the hybrid version from 200 up to 265 MHz, which means input frequencies from 400 up to 530 MHz. For the design and implementation of the MCM version, the varactor diodes are included in the RFICs dies fabricated using 0.35-μm CMOS technology. They are based on two pMOS transistors placed as shown in Fig. 7. The size scaling ratio between transistors M1 and M2 is approximately 0.2. This value has been found by optimizing the linear behavior of the capacitance versus the control voltage. Output frequency can be tuned from 900 MHz to 1.1 GHz, which means injected frequencies from 1.8 up to 2.2 GHz.
3) *Transistor cross pair*. For the hybrid version, the cross pair has been implemented using a couple of discrete AT-32033 npn silicon bipolar transistors from Agilent Technologies Inc., Palo Alto, CA. For the MCM version, the implementation of the transistor cross pair is the main part of the RFIC dies fabricated using 0.35-μm CMOS technology. In order to minimize mismatch problems, two arrays of ten equal nMOS transistors have been used instead of two single transistors.
4) *Current source*. This part of the circuit has been implemented as a single bias resistor in the hybrid version of the ILO. In the case of the MCM version, a temperature-compensated current mirror has been implemented.

Fig. 8 shows two view photographs of the final ILO circuits. An example, in the frequency domain, the locking behavior of the hybrid version is shown in Fig. 9. The initial free-running oscillation frequency of 255.5 MHz is shifted to 253 MHz when a -6-dBm 506-MHz signal is injected at common node A (Fig. 5). In this example, bias voltage V_{cc} and varactor bias $V_{\rm var}$ are 3 and 0 V, respectively. The time-domain locking behavior is shown in Fig. 10. Both the injected signal at frequency $2f_{\rm lock}$ and the oscillator output signal at frequency $f_{\rm lock}$ are

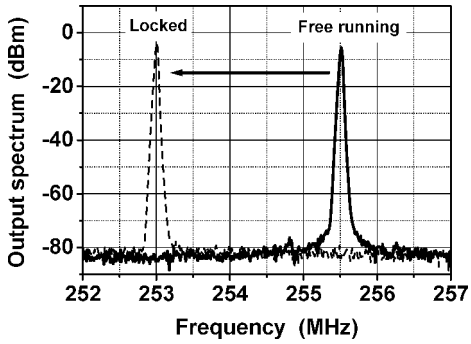

Fig. 9. Examples of the measured output spectra of the hybrid version of second harmonic ILO.

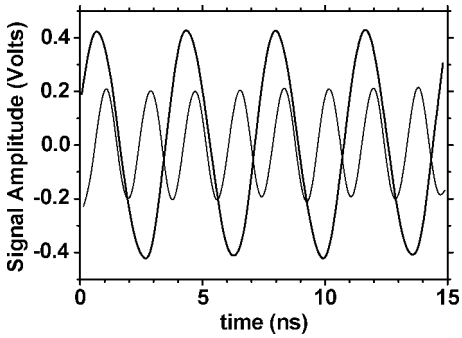

Fig. 10. Time-domain waveform of the injected signal (thin line) and the ILO output (thick line) in the locking state.

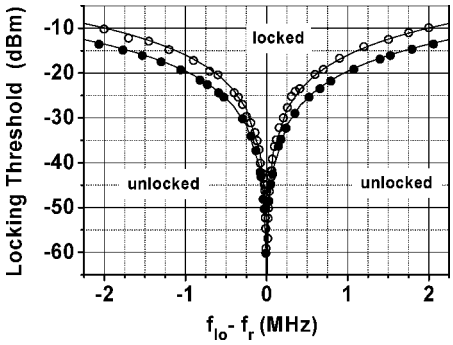

Fig. 11. Locking sensitivity (in dBm) as a function of the frequency shift from the free-running frequency. (•) Measured data for the hybrid version. (∘) Measured data for the MCM prototype. (—) Quadratic law fitting.

plotted on the same graph. The phase relationship between the input and output signals, which is characteristic of the locking state, should be noted. Fig. 11 shows the locking threshold or locking sensitivity (i.e., minimum input power required for locking the oscillator) as a function of the frequency shift from the free-running frequency f_r to the final locking frequency $f_{\rm lock}$. Filled circles correspond to measured data for the hybrid version. The frequency shift reference (i.e., the free-running frequency) is equal to 255.5 MHz. Outlined circles correspond to the experimental measurements for the MCM version. In this case, the frequency shift reference is equal to 1160.8 MHz. Both sets of data points have been fitted according to the expected quadratic law [1]—*Locking Threshold proportional to frequency shift squared*—showing good agreement.

It should be noted that ideally the locking threshold or locking sensitivity trends to zero when the locking frequency approaches the free-running frequency, i.e., power is required to frequency lock the oscillator, but not to phase-lock it. In practice, there are several factors that worsen the locking sensitivity. Among them are: 1) frequency drifts due to temperature or bias variations; 2) ILOs phase noise; or 3) in-band additive white Gaussian noise (AWGN). As an example, Fig. 12 shows a simulation example of the hybrid converter sensitivity degradation due to AWGN. The locking thresholds is plotted as a function of the absolute value of the frequency shift for two noise conditions: (■) correspond to the noiseless injection and (●) correspond to the injection of a signal composed by the carrier at $2f_{\rm lock}$ and AWGN in a 1-MHz bandwidth around $2f_{\rm lock}$, being the total noise power of -53.5 dBm. Note that the smaller the frequency shifts, the more important the sensitivity worsening is. Consequently, the main effect of noise is to set a minimum sensitivity value.

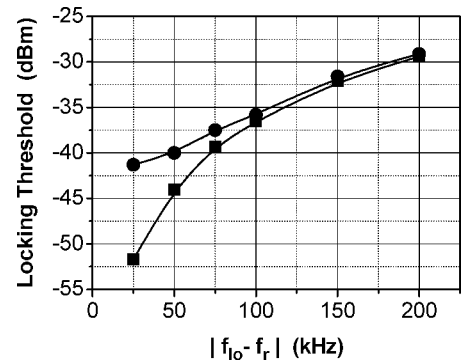

Fig. 12. Locking threshold (in dBm) as a function of the frequency shift from the free-running frequency: (■) simulated data for the hybrid version corresponding to noiseless injection, (•) simulated data corresponding to noisy injection (AWGN over a 1-MHz bandwidth around $2f_{\rm lo}$, -53.5-dBm total noise power).

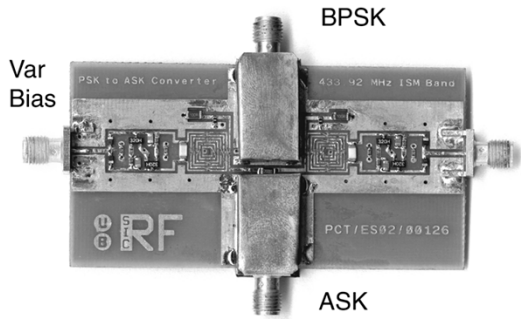

Fig. 13. View photograph of the hybrid prototype of the BPSK to ASK converter circuit.

C. Converter Circuit

View photographs of the hybrid prototype and MCM prototype of the BPSK to ASK converter circuit are shown in Figs. 13 and 14, respectively. The hybrid implementation in Fig. 13 shows shielding covers to prevent coupling of external signals. Input and output connectors are located on the top and bottom of the circuit board. Left and right are the connectors for biasing the varactor diodes of both ILOs. In the MCM version photograph of Fig. 14, a couple of SMD resistors and a couple of RFIC dies flip-chipped on the Pyrex substrate can be seen. Input and output RF pads are located centered on the top and

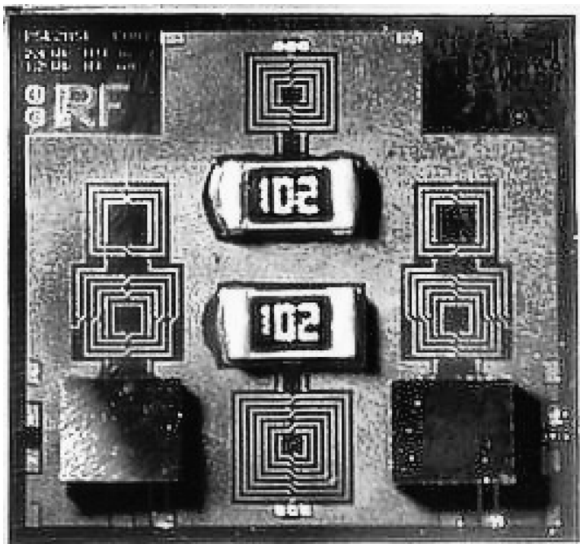

Fig. 14. View photograph of the MCM prototype of the BPSK to ASK converter circuit.

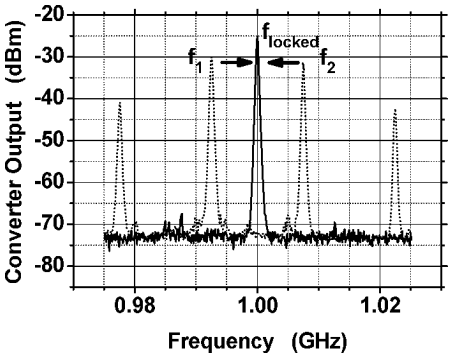

Fig. 15. Output spectra of the MCM prototype of BPSK to ASK converter. Dashed line corresponds to the free-running behavior. Continuous line corresponds to the locked behavior after the injection of a 2-GHz input signal.

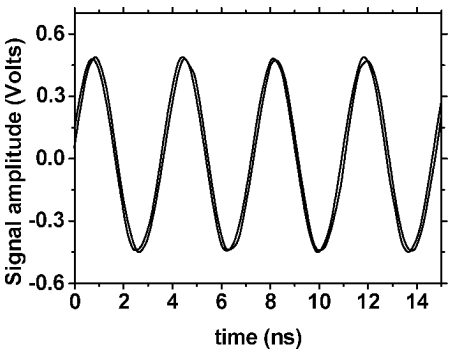

Fig. 16. Output waveforms of both ILOs of the hybrid converter in the "in-phase" state.

bottom of the circuit, respectively. Located on the lower left and right corners, there are the dc pads for varactor and RFIC dies biasing.

- *Steady-state behavior*. Figs. 15–17 show the steady-state behavior of the proposed converter circuits. The output spectrum of the free-running MCM converter is shown in Fig. 15. This figure also shows the converter's output spectrum when it is injected with a 2-GHz input signal. Arrows

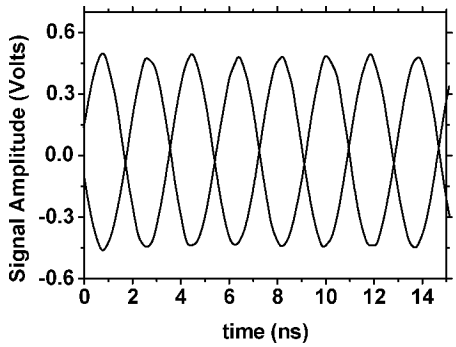

Fig. 17. Output waveforms of both ILOs of the hybrid converter in the "counter-phase" state.

in this figure indicate the frequency shift of both oscillators from the free-running state to the locked state. Note the presence of intermodulation products at both sides of the main peaks f_1 and f_2 due to the finite isolation of the power divider and combiner and electromagnetic coupling. It is important to remark that the interval $[f_2, f_1]$ defines the conversion channel. BPSK signals, of which carriers are outside this frequency range, will not be converted because both ILOs will increase or decrease their phases simultaneously and no interference pattern will be produced at the converter's output [1]. Moreover, according to the results of Fig. 11, it is straightforward that the wider the conversion channel, the higher the injected power required to lock the converter will be. Thus, there appears to be a tradeoff between bandwidth and sensitivity of the converter.

Once the converter is locked, its output can be in either of two possible states, depending on the relative phases of both ILOs. Fig. 16 shows the output waveforms of both ILOs of the hybrid prototype when they are in the "in-phase" state. Obviously, the interference of these two waveforms through the power combiner will lead to a maximum amplitude output. On the contrary, Fig. 17 shows the ILOs' outputs in the "counter-phase" state. In this case, it is clear that the interference through the power combiner will lead to the minimum amplitude output. It should be noted that both "in-phase" and "counter-phase" states are stable and equally probable.

- *Dynamic response*. Let us now consider that the injected signal is a BPSK signal. According to our previous theoretical analysis [1], provided the locking frequency is in between the free-running frequencies of both ILOs, every phase shift at the BPSK input will cause a phase change in $\pi/2$ at the output of one of the ILOs and $-\pi/2$ at the output of the other one. Thus, if the converter was in the "in-phase" state, it will evolve toward the "counter-phase" state and vice versa. Examples of this dynamic process can be seen in Figs. 18 and 19. Fig. 18 shows the ASK output of the hybrid converter at 272 MHz. The injected power of the input BPSK signal at 544 MHz is -12 dBm and its phase changes in 180° every 500 ns (i.e., 2 Mbits/s). The free-running frequencies of both ILOs are 271 and 273 MHz, respectively. Fig. 19 shows the output of the MCM version of the converter at $f_{\rm lock} = 1$ GHz. In this

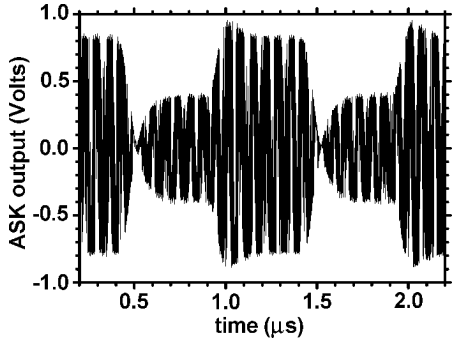

Fig. 18. ASK output waveform of the hybrid converter when injected with a BPSK input signal which phase changes every 500 ns (i.e., 2 Mbits/s).

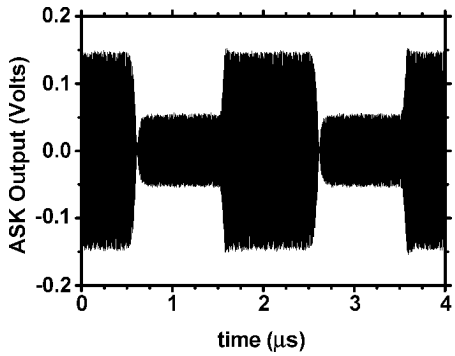

Fig. 19. ASK output waveform of the MCM converter when injected with a BPSK input signal, which phase changes every 1000 ns (i.e., 1 Mbits/s).

case, the injected power at 2 GHz is 3 dBm, the phase-change period is 1 μs (i.e., 1 Mbit/s), and the free-running frequencies of both ILOs are $f_{\rm lock} + 7.5$ MHz and $f_{\rm lock} - 7.5$ MHz, respectively.

IV. Performance Test of the BPSK to ASK Conversion

In order to verify the predictions of our previous theoretical analysis of the BPSK to ASK converter performance [1], two main dependences have been studied: first, the dependence of the BPSK to ASK conversion on the injected power and, second, the dependence of the conversion process on the transit time (i.e., maximum fall and/or rise time of the BPSK phase change). Due to the easy of measuring of the hybrid converter, both studies have been carried out using this implementation. It should be noted that, at the exception of a scaling factor, the same results are expected for the MCM version of the converter.

A. Dependence on the Injected Power

For the analysis of the BPSK to ASK converter performance as a function of the injected power, six different injection conditions have been considered. In all the cases, the conversion channel width (i.e., $f_1 - f_2$) has been kept constant and equal to 3 MHz and the frequency of the injected signal has been fixed to 522 MHz so that the converter's locking frequency $f_{\rm lock} = 261$ MHz was centered in the conversion channel (i.e., $f_1 - f_{\rm lock} = f_{\rm lock} - f_2$). The carrier at 522 MHz has been modulated using a double-balanced mixer. The modulating signal was a trapezoidal wave varying from -1 to $+1$ V, being the fall and rise times equal to 10 ns. Finally, the power at the

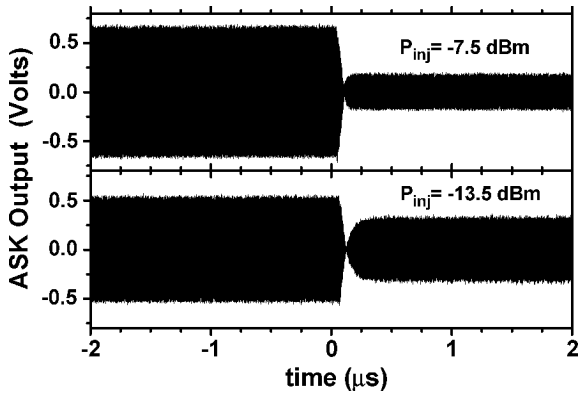

Fig. 20. Examples of BPSK to ASK conversion for two different values of the injected power.

modulator output, which directly injected the converted, ranged from -15 to -7.5 dBm with a step of 1.5 dB. The first power level (-15 dBm) is below the locking threshold, therefore, no BPSK to ASK conversion is observed. The rest of injected power levels correspond to different locking conditions. Fig. 20 shows two representative examples. Note that the conversion efficiency, measured in terms of the amplitude difference between the in-phase and counter-phase states, increases as the injected power increases. In order to quantify this observation, we can define the conversion efficiency η as follows:

$$\eta = \frac{\Sigma - \sigma}{\Sigma + \sigma} = \frac{1 - r}{1 + r} \tag{1}$$

where Σ and σ are the maximum and minimum ASK output amplitudes, respectively, and r is the ratio between them ($r = \sigma/\Sigma$).

According to the previous theoretical analysis [1], maximum and minimum interference amplitudes are given by

$$\Sigma = A_1\sqrt{2}\sqrt{1 + \cos\left(\frac{(\theta_{s1} - \theta_{s2})}{2}\right)}$$
$$\sigma = A_1\sqrt{2}\sqrt{1 - \cos\left(\frac{(\theta_{s1} - \theta_{s2})}{2}\right)} \tag{2}$$

where A_1 is the amplitude of the ILO oscillators and

$$\theta_{si} = \arcsin\left(\frac{4C_o}{\alpha A_2}\frac{f_i - f_{\rm lock}}{f_i}\right), \qquad i = 1, 2 \tag{3}$$

where C_o and α are the varactors capacitance and its voltage derivative at the bias point and A_2 is the amplitude of the injected BPSK signal.

By combining (1)–(3), a theoretical expression of the efficiency η as a function of the injected amplitude (power) can be obtained. Fig. 21 shows the comparison of this theoretical expression with the measured values of the efficiency as a function of the injected power. It should be noted that the only fitting parameter is the locking threshold, which is equal to -14.2 dBm in the example shown in this figure. This value is in good agreement with experimental measurements of the locking threshold.

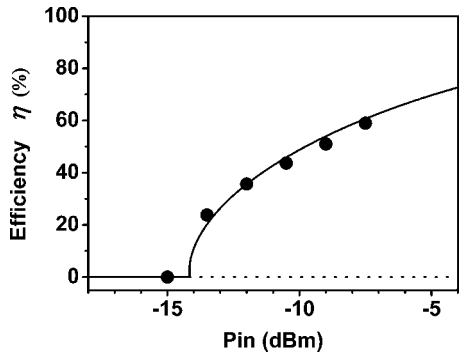

Fig. 21. Converter's efficiency versus injected power. (•) Measured data. (—) Theory.

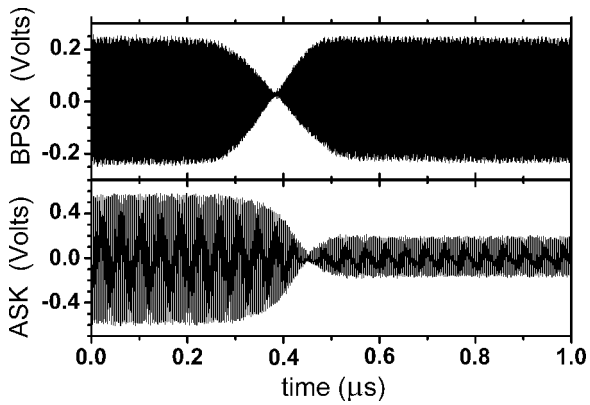

Fig. 22. Example of: (*top*) BPSK input and (*bottom*) ASK output waveforms of the hybrid converter for a transit time of 200 ns.

As shown in Fig. 11, the measured value for the hybrid version of the converter is approximately −15 dBm at 1.5 MHz of frequency shift from the 255.5-MHz locking frequency.

B. Dependence on the Transit Time

The analysis of the BPSK to ASK conversion performance versus transit time has been carried out simultaneously increasing the fall and rise times of the trapezoidal signal used to generate the BPSK input from their minimum value (10 ns) up to the time at which the converter fails. According to the previous theoretical analysis [1], this time corresponds to the bifurcation time.

Fig. 22 shows an example of the signal waveforms used in this study; on top, the generated BPSK signal when the transit time is equal to 200 ns, on the bottom, the corresponding output ASK signal. In this example, the injected power is equal to −7.5 dBm and the conversion channel width and locking frequency are, once again, 3 and 261 MHz, respectively. To conclude, Fig. 23 shows the change of the converter behavior when the transit time increases beyond the bifurcation time. On top, the normal behavior of the conversion process is observed for a transit time of 830 ns. On the bottom, a wrong BPSK to ASK conversion is observed, just increasing the transit time up to 840 ns. This

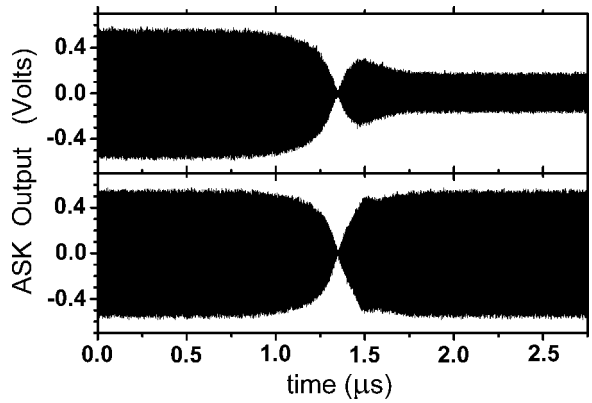

Fig. 23. ASK output waveforms of the hybrid converter for transit times of: (*top*) 830 ns and (*bottom*) 840 ns. Note the sudden change from the normal behavior at 830-ns transit time to a wrong BPSK to ASK conversion at 840 ns.

sudden change is a consequence of the chaotic dynamics of the injection process.

V. Conclusion

The feasibility of a new circuit to convert BPSK signals into ASK signals, based on the use of second harmonic ILOs and interference phenomena, has been demonstrated.

Two prototypes of the converter circuit have been designed using a SiP approach. First, a hybrid prototype has been fabricated using a standard PCB process, which combines lumped SMD active and passive components and printed passives on an FR4 standard substrate. Second, an MCM version has been implemented using a glass carrier substrate, including two interconnect metal levels, and RFIC flip-chip dies fabricated using a standard 0.35-μm CMOS process.

Both static and dynamic performance of the converter prototypes has been analyzed as a function of the injected power. Moreover, the dynamic behavior has also been analyzed as a function of the phase transit time of the BPSK injected signal. The obtained results for the locking threshold, conversion efficiency, and phase transit time dependence are in perfect agreement with the theoretical predictions.

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