

Brain–Silicon Interface for High-Resolution *in vitro* Neural Recording

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Invited Paper

Abstract—A 256-channel integrated interface for simultaneous recording of distributed neural activity from acute brain slices is presented. An array of 16×16 Au recording electrodes are fabricated directly on the die. Each channel implements differential voltage acquisition, amplification and band-pass filtering. In-channel analog memory stores an electronic image of neural activity. A $3 \text{ mm} \times 4.5 \text{ mm}$ integrated prototype fabricated in a $0.35\text{-}\mu\text{m}$ CMOS technology is experimentally validated in single-channel extracellular *in vitro* recordings from the hippocampus of mice and in multichannel simultaneous recordings in a controlled environment.

Index Terms—Acute brain slices, integrated neural interfaces, neural amplifier, on-chip microelectrodes.

I. INTRODUCTION

THE electrophysiology of the human brain governs a complex array of neurological functions. The human brain is a large-scale interconnected network with common behavioral properties extending across large spatial areas. To gain full understanding of how biological neural networks encode and process information, it is necessary to simultaneously record signals from many neighboring neurons.

Significant insights have been gained into ways of neural information coding through the use of microelectrodes that record the activity of single neurons and neural populations in the brain. Recording of neural activity has been traditionally performed using bench-top biomedical instrumentation equipment. These instruments are generally stationary, bulky, limited to one or

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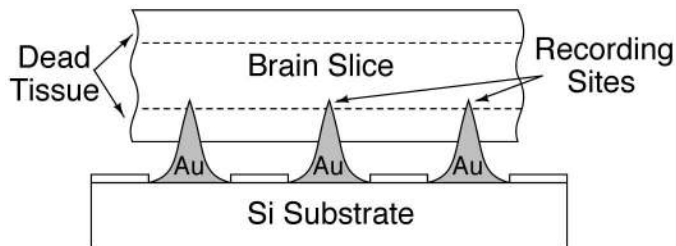
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(a)



(b)

Fig. 1. (a) Cross section of the proposed microsystem for recording from acute brain slices. (b) Mouse hippocampal-entorhinal cortex slice in a recording chamber.

a few acquisition channels, and prone to excessive noise due to wiring. Integrated neural interfaces, fabricated on a single miniature physical substrate, lack these drawbacks. They offer a small, low-power, low-noise, and cost effective chronically implantable alternative to commercial bench-top instruments. Integrated neural interfaces perform signal acquisition, amplification, filtering, and, in some instances, quantization and neural stimulation [1]–[7]. They may also provide wireless data interface on the same chip [8].

Recording microsystems with 3-D electrode arrays of various configurations have been reported such as with electrodes co-planar with the die [9]. Implementations with 3-D electrode arrays bonded directly to the surface of the chip have been proposed [6], [10]. Previously reported neural interfaces integrated with on-chip 3-D microelectrodes have been typically limited to 100 channels [10]. Implementations with higher number of

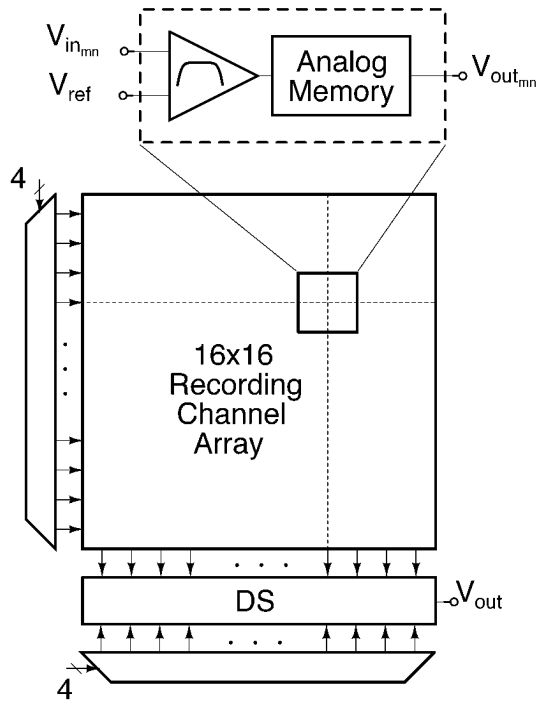


Fig. 2. Top-level architecture of the brain-silicon interface.

channels have been reported without electrodes and at the cost of increased circuit noise [11].

We present a CMOS brain-silicon interface for high-resolution *in vitro* recording from acute brain slices. Neurophysiological studies of acute brain slices such as those of hippocampus are critical in investigating therapies for such debilitating neurological disorders as epilepsy and Alzheimer's disease. A region of interest in the brain is extracted from an animal and sliced. The thickness of a slice is typically in the order of several hundreds of microns. As a result of slicing, acute brain slices have an outer layer of dead tissue which needs to be penetrated by recording electrodes. Its thickness can be in the order of tens of microns. For this purpose, golden 3-D electrodes are post-fabricated on the surface of the die of the proposed integrated neural recording interface. The cross section of the proposed microsystem is depicted in Fig. 1(a). Au electrodes are individually bonded directly onto the surface of the chip employing conventional die bonding equipment. This fabrication method yields low manufacturing costs, high yield, and flexibility in electrode location and shape. The size and geometry of the electrodes are chosen specifically for recording from acute brain slices of mice such as the hippocampal-entorhinal cortex slice shown in Fig. 1(b). The slice is inserted onto the recording electrodes and is placed into a fluidic chamber. The slice rests on the bases of the electrodes and is held in place by a slice anchor (or harp). This allows the tissue slice to be perfused from both above and below in order to maintain its vitality.

Each channel of the integrated neural interface contains a low-noise amplifier with up to 74 dB of programmable gain, a tunable antialiasing low-pass filter (LPF), and a high-pass filter (HPF) that removes a dc voltage offset present at the electrode-tissue interface. The brain-chip interface records action

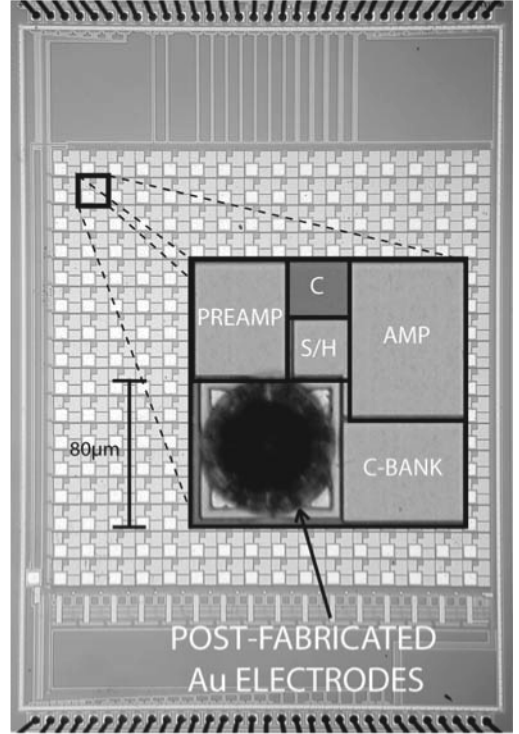


Fig. 3. Micrograph of the 256-channel integrated neural interface. The 3×4.5 mm² die was fabricated in a 0.35- μ m CMOS technology. Electrode pitch is 170 μ m.

potentials in the range of tens of microvolts to hundreds of millivolts in the tunable 0.1–10 kHz frequency band in order to capture relevant neural activity, as required for analysis and treatment of neurological disorders [12]. Each channel also has a sample-and-hold circuit with analog memory, allowing for truly simultaneous signal acquisition across all channels, with subsequent multiplexed array readout and off-chip serial analog-to-digital conversion. A column-parallel double-sampling circuit removes fixed pattern noise.

The rest of this paper is organized as follows. Section II presents the architecture of the integrated prototype and describes the electrode manufacturing process. Section II-C provides details of VLSI implementation of the recording channel. The low-noise transconductance amplifier is presented in Section II-D. The recording frame buffer implementation is described in Section II-E. All presented results are experimentally recorded from the integrated prototype.

II. ARCHITECTURE AND VLSI IMPLEMENTATION

A. Architecture

Most of the frequency content of extracellular neural activity in the brain is concentrated between 0.1 Hz and 10 kHz. Signal amplitudes range from a few microvolts to hundreds of millivolts. For low-noise distributed neural potential field recording, a multichannel integrated neural interface has been designed and prototyped.

The presented neural interface simultaneously acquires voltages on 256 independent channels organized in a 16×16 array as shown in Fig. 2. Each channel contains a band-pass filter

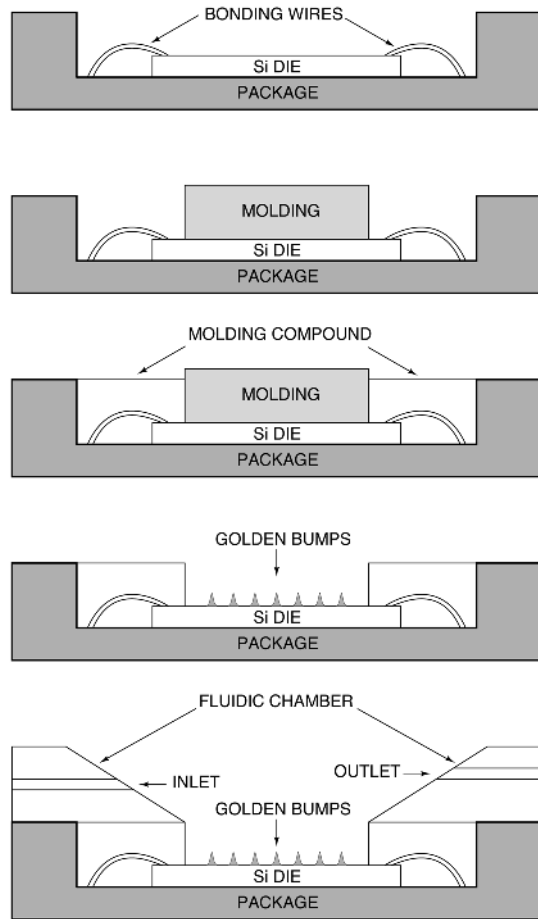


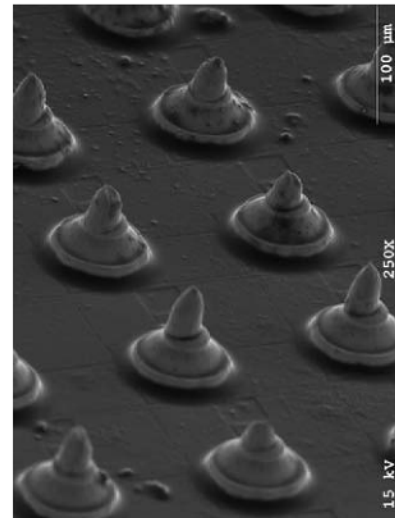
Fig. 4. Fabrication steps in the the brain-silicon interface hybrid integration procedure.

with a nominal amplification gain. Each channel also contains a sample-and-hold (S/H) cell. A bank of double sampling (DS) circuits sample the analog memories one row at a time to remove offsets resulting from device mismatches. Array readout is implemented in a serial fashion as controlled by row and column address decoders.

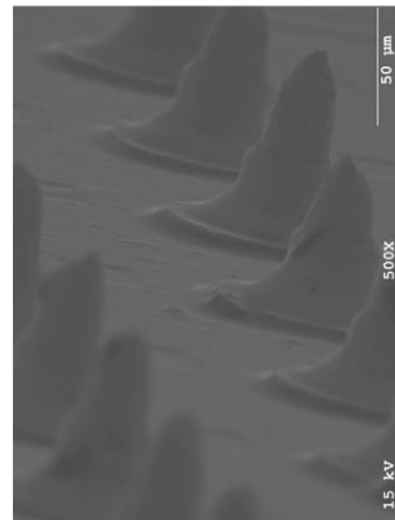
The 256-channel integrated neural interface was fabricated in a $0.35\text{-}\mu\text{m}$ double-poly standard CMOS technology. The $3\text{ mm} \times 4.5\text{ mm}$ die micrograph is shown in Fig. 3. Each channel is connected to one on-chip data recording site and a reference recording site, for low-noise differential recording. Each recording site is comprised of a stack of several aluminum layers with the topmost layer left unpassivated similarly to a conventional bonding pad. One on-chip reference recording pad is shared by all recording channels. An off-chip reference voltage can also be supplied from an external recording electrode.

B. Microsystem Integration

In vitro neural recording procedure requires preserving the vitality of a brain slice by its continuous perfusion. The perfusion fluid such as as artificial cerebrospinal fluid (ACSF) is electrically conductive. The close proximity of bonding wires to the recording array necessitates their electrical insulation. To



(a)



(b)



(c)

Fig. 5. SEM photographs of golden electrodes fabricated on the surface of the chip. (a) Midangle view. (b) Low-angle view. (c) Partial array view.

simplify the process of electrical insulation of bonding wires all wire-bonded pads are located on the two opposite sides of

TABLE I
TRANSISTOR SIZES AND OPERATING POINTS

Transistor	W/L (μm)	I_D (nA)	g_m ($\mu\text{A}/\text{V}$)	g_m/I_D (V^{-1})
$M_{1,2}$	400/15	125	3.14	25.17
M_{3-6}	10/400	125	0.83	6.64
$M_{7,8}$	10/200	125	0.65	5.2
M_9	45/45	250	3.79	15.16
$M_{\text{casc}N}$	18/8	125	3.1	24.8
$M_{\text{casc}P}$	25/8	125	2.65	21.2

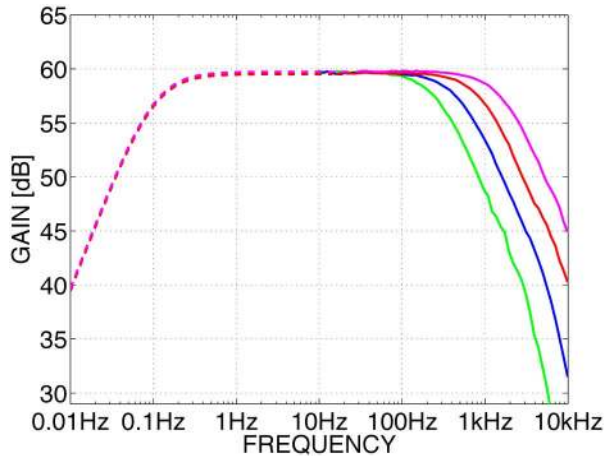


Fig. 8. Experimentally measured frequency response of a single recording channel. Bandwidth can be varied by adjusting the bias current.

performance given a small power budget. Fig. 7 shows the circuit diagram of the OTA employed in each stage of the channel.

The input pair is chosen to be a p-channel MOS with a large gate area to minimize the flicker noise contribution. According to the circuit noise analysis presented in [5] and [14], the thermal noise component of the OTA can be reduced by biasing the input pair ($M_{1,2}$) in weak inversion and the mirroring transistors (M_{3-8}) in strong inversion. Thus, the thermal noise contribution is optimized for a given current value. The thermal noise level can be further decreased by increasing the biasing current and thus the power consumption. Table I summarizes the size and the dc operating point for each transistor.

Fig. 8 depicts the experimentally measured frequency response of a single channel configured for a nominal gain of 1000 (60 dB). The solid line represents the measurements done with a spectrum analyzer. Due to limitations of the available measurement equipment, the high-pass corner frequency is estimated by applying a step signal at the amplifier input and observing the amplifier transient response time constant.

Fig. 9 shows the experimentally measured input referred noise of one channel. The measurement is obtained by recording the noise spectrum at the output of the amplifier and referring it back to the input. The total rms noise is $13 \mu\text{V}$ over the 10 Hz–10 kHz bandwidth.

For experimental recordings the neural recording interface prototype is placed in a custom-manufactured fluidic chamber. The fluidic chamber is positioned on the surface of the chip package and attached to the top of a protective plexiglass box to

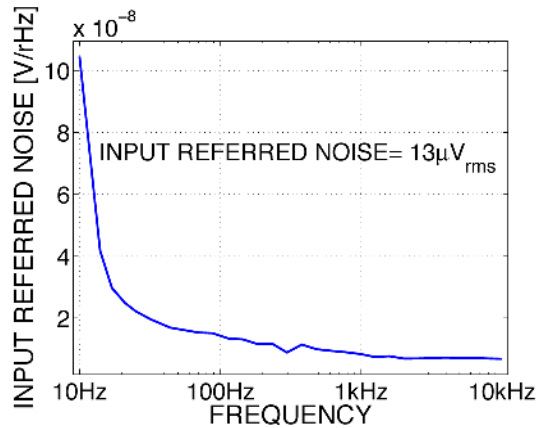


Fig. 9. Experimentally measured input-referred noise of a single recording channel.

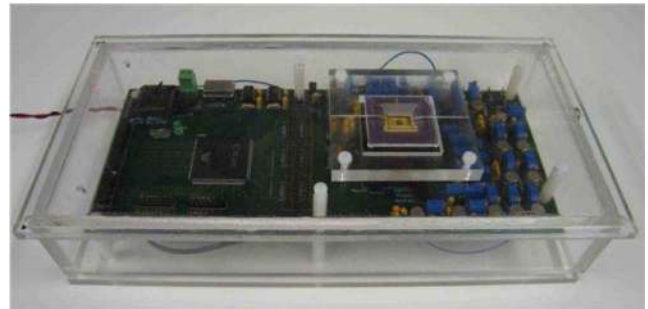


Fig. 10. Fluidic chamber attached to the top of the testing printed circuit board.

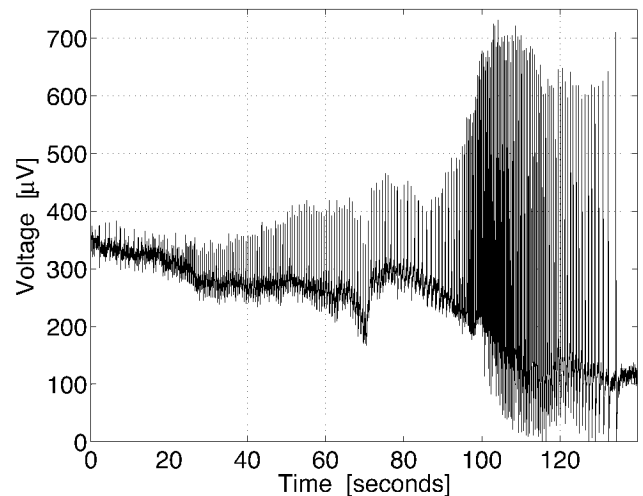


Fig. 11. Epileptic seizure in a mouse hippocampus experimentally recorded on one channel of the integrated neural interface.

form a hydraulic seal as shown in Fig. 10. The testing printed circuit board generates necessary analog and digital signals, quantizes recorded neural data and sends the data to a personal computer through a high-speed digital interface. The recorded data are buffered and displayed in Matlab.

Fig. 11 depicts an extracellular neural activity recording from a mouse hippocampus performed on one channel of the integrated neural interface prototype. Hippocampus was obtained

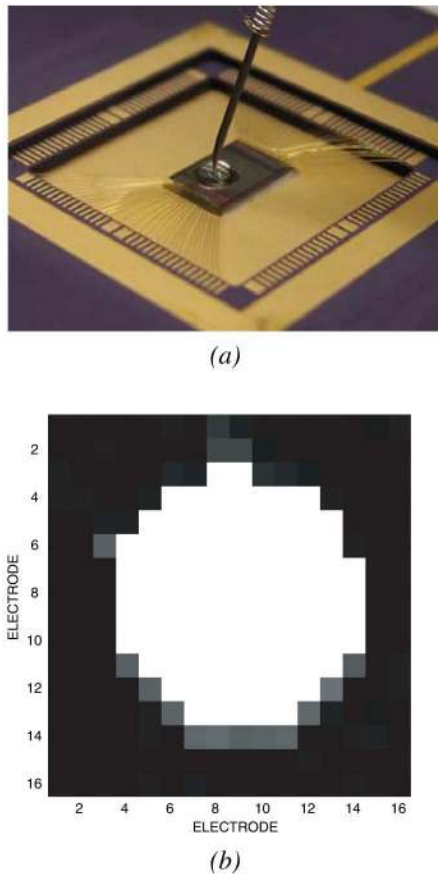


Fig. 12. (a) Water drop placed on the surface of the die. (b) 2-D experimental recording of a water drop driven by a sinusoidal signal.

from male Wistar rats (5–25 days old). Animals were anesthetized with halothane and decapitated in accordance with the Canadian Animal Care Guidelines. The brains were dissected and maintained in oxygenated ice-cold ACSF. The recording represents an epileptic seizure-like activity induced *in vitro* in the presence of low Mg^{2+} ACSF.

E. Frame Buffer

Accurate distributed multisite sensing requires maintaining a high degree of correlation in time between all channels. Multisite recording time-multiplexed architectures do not preserve cross-channel correlation unless the sampling frequency is much higher than the neural signal bandwidth. This necessitates a memory buffer in each recording cell to store the sampled signal. Frames of samples across the whole array are captured simultaneously. This eliminates the rolling delay during serial read-out. The local memory cell also allows for delaying high-noise on-chip digital switching until after a recording has been completed. Low-noise signal acquisition is time-multiplexed with high-noise peripheral switch capacitor signal processing and read-out. This ensures no high-amplitude switching activity during the signal acquisition phase and thus prevents substrate noise from coupling into the low-amplitude signal being acquired.

TABLE II
EXPERIMENTALLY MEASURED CHARACTERISTICS

Channels	256
Max Sampling Rate	40kHz
Programmable Gain	200, 1000, 2500, 5000
Input-Referred RMS Voltage Noise	$13\mu V$ over 10kHz
Output Voltage Range	1.5V
DC Offset Compensation	Double Sampling
LPF cut-off Frequency	1kHz-10kHz
HPF cut-off Frequency	<0.1 Hz
Supply Voltage	3.3V
Core Power Dissipation	6mW
Technology	$0.35\mu m$, mixed-signal CMOS, double poly
Electrode Type	On-chip, Au; $100\mu m$
Cell Pitch	$170\mu m$
Die Size	$3 \times 4.5 mm^2$

In order to validate the 2-D recording functionality of the array the following experiment was conducted. A drop of distilled water was placed on the surface of the 16×16 electrode array similarly to the one shown in Fig. 12(a) and driven by a 2-mV peak-to-peak sinusoidal voltage. The stimulus signal was recorded at 5-kHz sampling rate and displayed in real time as an “electronic video” stream. Fig. 12(b) shows a two dimensional intensity map of a recording frame corresponding to a particular instantaneous value of the input sinusoid.

The experimentally measured characteristics are summarized in Table II. The measured core power dissipation of 6 mW on the $3 \times 4.5 mm^2$ die area falls within the limits of power density considered safe for brain tissue [15], [16].

III. CONCLUSION

We have presented the architecture and VLSI implementation of an integrated neural interface for simultaneous recording of distributed neural activity. A $3 mm \times 4.5 mm$ integrated prototype was fabricated in a $0.35\text{-}\mu m$ CMOS technology. Two hundred fifty-six (256) $100\text{-}\mu m$ low-cost Au electrodes were fabricated directly on the surface of the chip for high-resolution electronic imaging of neural activity in acute brain slices. The microsystem was validated in extracellular *in vitro* recordings from a mouse hippocampus.

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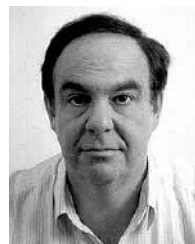
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