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Bridgeless PFC Topology Simplification and Design for Performance Benchmarking

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***Abstract*—Compared with conventional power factor correction (PFC) topologies, although dual-converter cell-based bridgeless topologies usually have higher efficiency, most of them suffer from high component counts. Thus, this paper proposes general topology simplification methods for these topologies. Besides, several selected converter cells are exemplified to show the specific topology simplification processes and the performance of the resultant simplified topologies is reviewed. Meanwhile, based on the same design specifications, in order to provide an unbiased quantitative topology comparison in terms of power loss, cost, and volume, this paper introduces a consistent component database-based design procedure with electrical, thermal, and cost models. As case studies, the conventional and two selected bridgeless buck-boost type topologies are compared by following the design procedure. The comparison results are analyzed to provide a reference for topology selection. Three prototypes are built and tested to verify the theoretical analysis.**

***Index Terms*—PFC, bridgeless converters, topology simplification, consistent design, comparison, buck-boost converter.**

I. Introduction

BRIDGELESS power factor correction (PFC) topologies without diode bridges are gaining popularity in recent years due to the efficiency improvement by the removal of conducting diodes [1]–[7]. Their applications range from relatively high power industry to hundred watts household electronic products, e.g., a bridgeless interleaved boost topology for a 3.4-kW electric vehicle battery charger [4], an interleave totem-pole bridgeless boost topology with a triangular current mode control in telecom applications [5], a bridgeless buck-boost topology with the variable DC-link voltage control for a 250-W (rated power) adjustable speed motor drive [6], an 100-W bridgeless without electrolytic capacitors as a light-emitting diode (LED) driver [7], etc.

Seen from the topology view, the conventional PFC topology requires at least one diode bridge to transfer AC to DC and then a cascaded DC-DC converter to shape the input current into sinusoidal, i.e., reduce the total harmonic distortions (THD) and obtain a high power factor (PF). Thus, as shown in Fig. 1, to eliminate the diode bridge, one straight way is to use two converter cells arranged in input-parallel output-series (IPOS) and input-parallel output-parallel (IPOP) configurations to handle each polarity of the AC input. This topology derivation method has been systematically presented in [8], which allows most of the converter cells to form their corresponding bridgeless topologies and most of the state-of-the-art bridgeless topologies can be identified and categorized into dual cell-based IPOP and IPOS bridgeless topologies [6], [9]–[18]. However, the obtained topologies, by using this derivation method, suffer from an increased component count compared with their conventional topology counterparts due to the dual-converter structure.

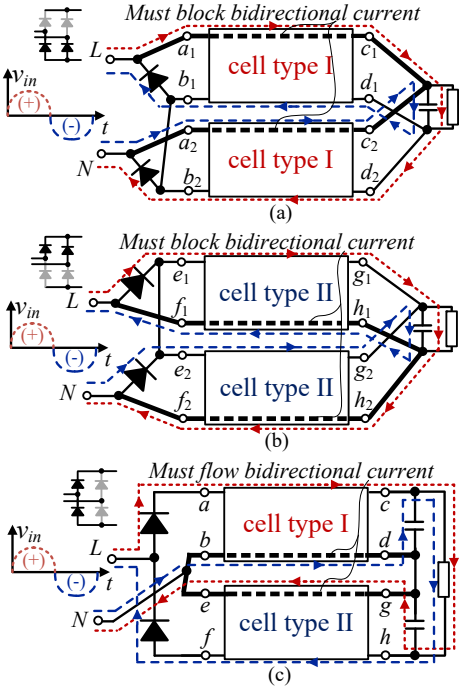

Fig. 1. Bridgeless topology derivation with dual converter cells in IPOP and IPOS configurations [8]: (a) IPOP-I with eliminated diodes in the high legs of a diode bridge, (b) IPOP-II with eliminated diodes in the low legs of a diode bridge, and (c) IPOS with eliminated diodes in one leg of a diode bridge.

Thus, as an extension study of [8], this paper proposes general topology simplification methods to reduce the component count. Although other existing topology-related articles [9]–[13], [19], [20] have proposed different versions of same converter cell type bridgeless topologies, e.g., several SEPIC/Cuk type bridgeless [9]–[12], buck-boost type bridgeless family

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[13], boost type bridgeless group [19], [20], questions on how the same converter cell bridgeless topologies can have various topology versions, why some of them have simpler structures, and what the performance differences are between them, require further exploration. The proposed topology simplification guidelines can help to find the answers by simplifying the dual cell-based bridgeless topology in systematical ways. Meanwhile, more bridgeless topologies may be derived and simplified from those existing converter cells of interest by following the proposed methods. For clarity, several selected converter cells are exemplified in this paper and the performance differences between these simplified topologies as well as some special concerns about the simplified topologies are reviewed.

Furthermore, for the dual cell-based IPOP and IPOS bridgeless topologies, on one hand, the dual components imply increased component counts. On the other hand, they have better heat dissipation abilities and the increased converter efficiency also contributes to smaller heatsinks. Thus, it is still an open question on the power density and cost of bridgeless topologies compared to the conventional ones, and between IPOP and IPOS types [21]. Besides, the simplified bridgeless topologies are not guaranteed to have better efficiency than their original ones, even though the simplified ones have fewer components. Hence, it is of meaningfulness to benchmark different topologies under the same design criteria.

Most bridgeless topology evaluations do not offer quantitative comparisons in terms of efficiency, cost, and volume, which are also strongly related to component parameters [3], [22]–[24]. For example, in [3], [22], [23], the boost bridgeless topologies are evaluated based on their operation modes and topology features. In [24], several boost type PFC converters are explored and compared under different power levels. Although specific efficiency comparison is presented, the quantitative cost and size assessments are not included due to the lack of component data and models. In contrast, by considering component parameters in optimization algorithms, [25] and [26] investigate different topologies in inverter applications, leading to a more convincing topology selection result. Similarly, for a fair topology comparison, [27] uses the same semiconductor design criterion to optimize the volumes of the compared three-phase multi-level topologies. Besides, other boost PFC optimization designs also take the component parameters into consideration [28]–[30]. However, if the goal is to compare topologies, adopting many components from different manufacturers increases the complexity to build the design procedure and intrigues the question that whether the topology performance differences are caused by the component manufacturing techniques [31], rather than the topologies.

Hence, in light of the aforementioned issue, this paper proposes a consistent PFC design procedure, which is based on identical design specifications to search the requirement-fulfilled components from the same series of the manufacturer. Moreover, electrical, thermal, cost models for each component are built in the database to support a fair topology comparison. Although this design principle has already been used in the previous work [8] to compare boost type bridgeless topologies, the procedure was not generalized for other type topology comparison. Besides, an inductor core winding turn calculation loop is added in the design procedure in this paper. Unlike other PFC designs [21], [28]–[30], the calculated junction temperatures are obtained by the electro-thermal iteration loop, which means that the thermal models will update thermal-dependent parameters (derived by curve fitting equations) in each loop iteration. Regarding the cost models, they are rarely covered in most topology comparative study or design procedures [3], [22]–[25], [27], [29], which are built based on the component physical properties, referring to [32]. In addition, to make this design procedure more user-friendly, the procedure is programmed in Microsoft® Excel with the built component database (shared in the corresponding web).

Although the boost topology is most widely used in the PFC applications due to its topology simplicity and control maturity, it can only operate in the boost mode, which means its output voltage must be higher than the input voltage and with a limited output voltage range. However, in some specific applications, e.g., air condition system, a variable output voltage of the PFC converter is preferred as the pre-regulator, since it allows the post-stage inverter to use a simple and low switching frequency pulse amplitude modulation (PAM) to drive the motor. Thus, the buck-boost type topology, capable of a variable output voltage, is preferred in this scenario [6], [33]. Moreover, in LED applications, where strict PF and low input current THD are demanding, the buck-boost type PFC converter with a low output voltage and high PF is a promising candidate [34], [35]. This is also why it is meaningful to explore other types of bridgeless topologies. For case studies, this paper adopts conventional and two selected bridgeless buck-boost type topologies to compare their performance by following the proposed consistent design procedure.

In summary, there are two major contributions of this paper.

- General simplification guidelines on bridgeless topology classifications and derivations based on systematical simplifications of dual-converter cell-based topologies are proposed to obtain different bridgeless topology families.
- A consistent design procedure, based on identical design specifications, with the built component electric, thermal, and cost models in the component database, is proposed to benchmark the same type bridgeless topologies in terms of power loss, cost, and volume.

The rest of this paper is arranged as follows. In Section II, the bridgeless topology simplification guidelines are presented and applied to the selected converter cells to obtain the simplified IPOS and IPOP bridgeless topologies. Moreover, the simplified topologies are reviewed. Section III introduces the design procedure with the conventional, IPOS, and IPOP (seen as a simplified IPOP) buck-boost as targets for the comparative study in power loss, volume, and cost aspects. Section IV gives the topology comparison results and the corresponding analysis. Experimental validations are presented in Section V and conclusions are drawn in Section VI.

II. Topology Simplifications

A. General Configuration Restriction

Fig. 1 shows the IPOP and IPOS bridgeless topology derivation methods using dual converter cells. To simplify

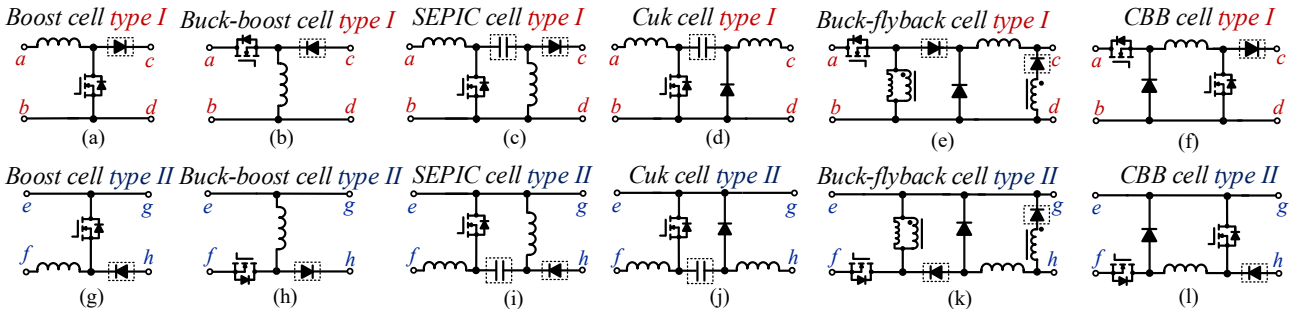

Fig. 2. Selected examples of converter cells to form their bridgeless topologies with identified critical components in rectangular blocks.

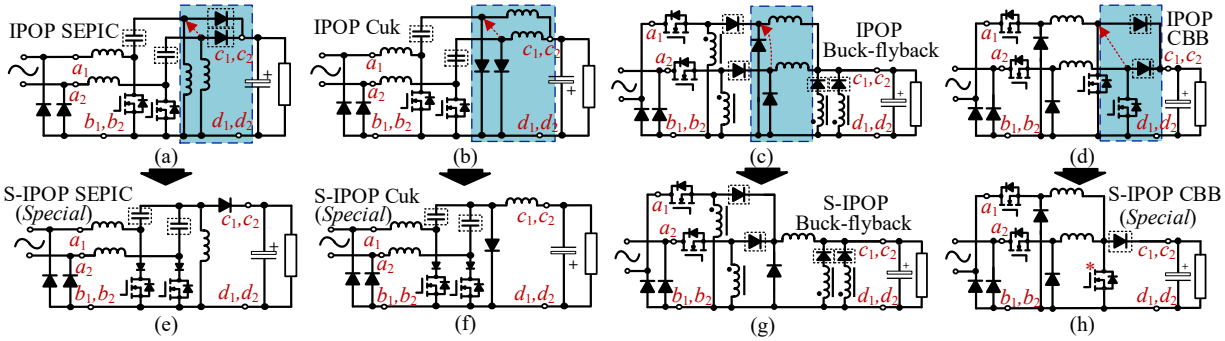

Fig. 3. Simplification method for IPOP topologies: (a) IPOP SEPIC, (b) IPOP Cuk [10], (c) IPOP buck-flyback [36], (d) IPOP CBB, (e) S-IPOP SEPIC [11], (f) S-IPOP Cuk [11], (g) S-IPOP buck-flyback, and (h) S-IPOP CBB. Note that the diodes in series with MOSFETs are mandatory in (e) and (f) for operation.

these topologies, the basic principle is to integrate the components in parallel. However, before topology simplifications, the fundamental restriction for each configuration should be clarified and followed to prevent possible malfunctions of the simplified topologies. In fact, to guarantee the functionality, all the simplified topologies in this paper have been verified by simulations under the discontinuous conduction mode (DCM) operation.

For the IPOP-I and IPOP-II topologies in Fig. 1(a) and (b), the current path without rectifier diodes must be a unidirectional to avoid the short-circuit of the AC input (dashed lines in Fig. 1(a) and (b)). As for the IPOS topology, the requirement for the converter cell is to have the bidirectional current flow ability in the converter cell type I and type II (dashed lines in Fig. 1(c)). Since there are different requirements for the IPOP and IPOS topologies, the corresponding simplification methods also differ.

To present the topology simplification clearly, Fig. 2 shows the selected example converter cell type I and type II with the critical components in rectangular blocks, which enable these converter cells to meet the aforementioned cell requirements. Note that like diodes, the small capacitors (e.g., in the Cuk and SEPIC cells) in "a-c" and "f-h" terminals are also seen as the critical components, which can block the bidirectional AC input current of the fundamental frequency (50-60 Hz). Meanwhile, since the topology simplification is relatively important for the complex converter cells, the buck-flyback and cascaded buck-boost (CBB) converter cells are selected as examples, which have been introduced in [36], [37] and [33], [38], respectively.

B. IPOP Topology Simplification

Since IPOP-I and IPOP-II topologies are similar, only the IPOP-I (IPOP for short in the following) topology simplification is given. As mentioned above, the critical components are key to avoid the short-circuit of the AC input current in the IPOP topologies, which is originally fulfilled by the diode bridge in the conventional PFC converters. Hence, the IPOP topology simplification has to keep the critical components and only integrate the components located behind the critical components (from the input side view). For example, in Fig. 3(a), the output diodes and secondary inductors are behind the middle capacitors and thus they are integrated.

According to this rule, Fig. 3(a)∼(d) illustrate the cell-based derived bridgeless topologies and Fig. 3(e)∼(h) show their simplified IPOP (S-IPOP) topologies. Besides, for the boost and buck-boost converter cells in Fig. 2, there is no component behind critical components, which means that the IPOP boost and IPOP buck-boost are already simplified. Note that in Fig. 3(e) and (f), the stray currents, flowing through the anti-parallel diodes of the MOSFETs, will cause the current surge due to the rapid voltage changes of the middle capacitors. Consequently, the diodes in series with the MOSFETs are required to avoid the stray currents. These special concerns about the simplified topologies are reviewed in Part D.

C. IPOS Topology Simplification

Given the aforementioned IPOS configuration restriction, there are two general simplification methods, as shown in Figs. 4 and 5. In Fig. 4(a), the S-I-IPOS type topology uses the converter cell inner current path branches to complete the AC current flow, rather than the split output capacitors (cf., Fig.

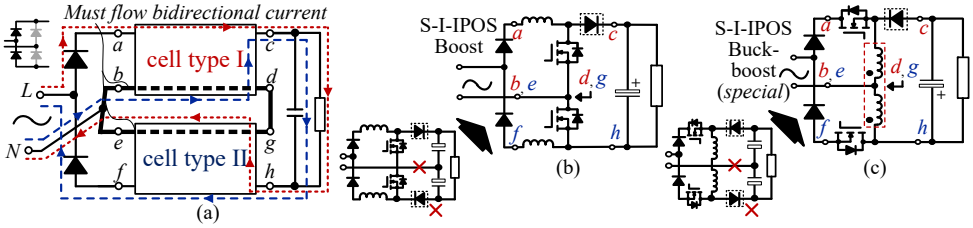

Fig. 4. Simplification method I for IPOS topologies: (a) general configuration, (b) S-I-IPOS boost, and (c) S-I-IPOS buck-boost with a tapped inductor [13]. Note that totem-pole boost can be seen as the output diode-free version of the S-I-IPOS boost.

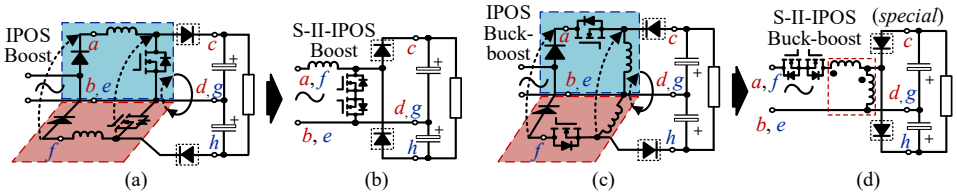

Fig. 5. Simplification method II for IPOS topologies: (a) IPOS boost [19], (b) S-II-IPOS boost [20], (c) IPOS buck-boost [18], and (d) S-II-IPOS buck-boost with a tapped inductor [13].

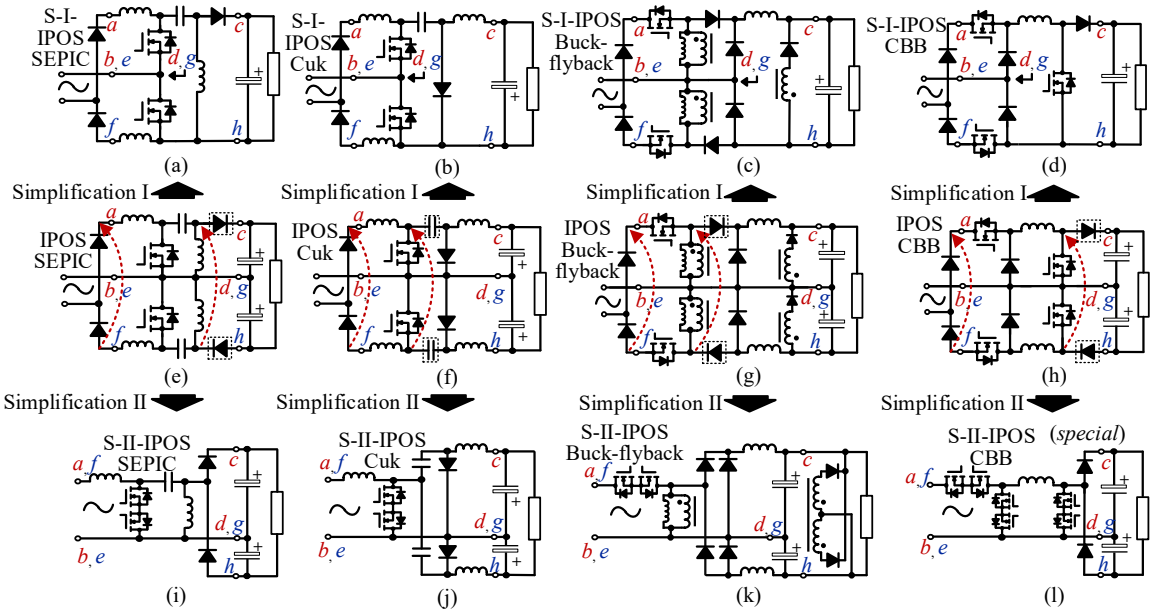

Fig. 6. Derived topologies by using the simplification method I and II: (a)∼(d) simplified type I IPOS (S-I-IPOS) topologies, (e)∼(h) original IPOS topologies, and (i)∼(l) simplified type II IPOS (S-II-IPOS) topologies. Among the simplified topologies, (a), (b), and (j) have been proposed [10], [39], [40] and others (c), (d), (i), (k), and (l) are not seen in the available literature.

1(c)). This configuration can be seen as another way to form the IPOS type topology without two split output capacitors.

On the other hand, in order to integrate the parallel components in the input side in the IPOS topologies (cf., Fig. 5), it also requires to identify the critical components in each IPOS topology and keep them in the S-II-IPOS topologies. The reason is that the original input rectifier didoes in IPOS topologies are eliminated in the S-II-IPOS topologies and their bidirectional current blockage tasks are now fulfilled by these critical components. This simplification is exemplified on the IPOS boost and IPOS buck-boost, as shown in Fig. 5(a) and (c). Fig. 6 presents other selected converter cell-based bridgeless topologies and their simplified versions.

D. Simplified Topology Reviews

Although this paper proposes the general bridgeless topology simplification methods as presented in the above, some special cases are of interest, i.e., the simplified bridgeless topologies in Fig. 7. In addition, integrating magnetic inductors in these simplified bridgeless topologies is also important to improve power density, as investigated in DC-DC converters or inverters [41], [42]. These simplified topologies are further discussed as follows.

S-IPOP. In general, the S-IPOP type topology performances are similar to their IPOP and conventional counterparts, since the basic operation circuits are still two DC-DC converter cells. It means the similar control strategy, semiconductor voltage stress, and electromagnetic interference (EMI) performance

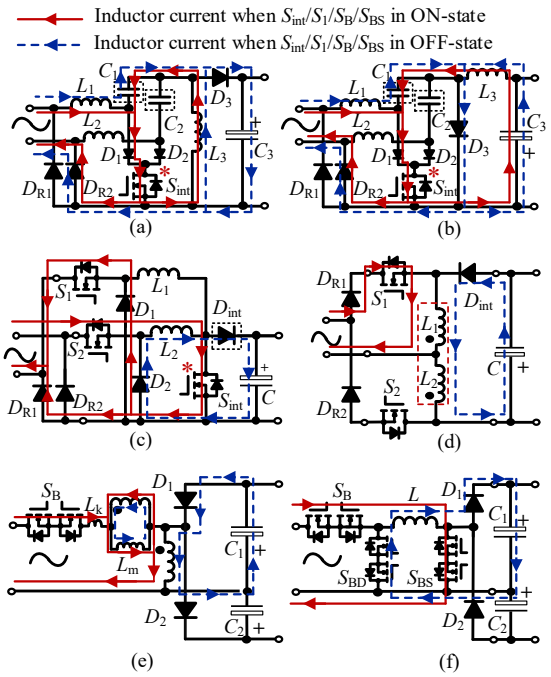

Fig. 7. Special modified topologies when applying the simplification methods: (a) switch integrated S-IPOP SEPIC, (b) switch integrated S-IPOP Cuk, (c) S-IPOP CBB, (d) S-I-IPOS buck-boost, (e) S-II-IPOS buck-boost, and (f) S-II-IPOS CBB. Note that in (a) and (b), the inductor currents in the OFF-state are only one operation mode and more details can be found in [11], [12].

[3], [8], [11]. The S-IPOP SEPIC and S-IPOP Cuk in Fig. 3 have been proposed and analyzed in [11] and the parallel switches can be further integrated into one, as shown in Fig. 7(a) and (b). A similar switch-integrated S-IPOP-II Cuk (Fig. 7(b) shows the S-IPOP-I Cuk) with a positive output voltage has been proposed in [12] and a low-cost non-floating switch driver can be used. Besides, among them, capacitors C_1 and C_2 should be carefully determined to avoid the low-frequency oscillations in the L_1-L_2-C_1-C_2 loop [12]. As for the S-IPOP Buck-flyback and S-IPOP CBB, they are newly found by this simplification method. Specially, as shown in Fig. 7(c), the S-IPOP CBB topology can even integrate the critical component into one and without the AC input short-circuit concern by the S_2-L_2-S_1-L_1 loop, as the S_2-L_2-$S_{\rm int}$-$D_{\rm R1}$ (part of current also flows through D_1-S_1) current path has a lower impedance than the path S_2-L_2-L_1-S_1.

S-I-IPOS. The S-I-IPOS type topology spares one of the bulky split output capacitors and the power density improvement is foreseeable, whereas the semiconductor voltage stress is typically higher than the IPOS topologies. Additionally, these topologies usually require more complex control strategies compared to the S-IPOP or S-II-IPOS topologies, since the AC current flow in the inner converter cell branch has to be controlled. For example, in Fig. 6(c) and (d), the switch signal can not be the same and they should be associated with the input voltage polarity; otherwise, the stray current will cause additional power losses in the undesired current loop associated with rectifier diodes and switches. Back to the simplified IPOS topologies in Figs. 4∼6, most of them have been proposed [10], [13], [20], [39], [40]. Notably, the S-I-

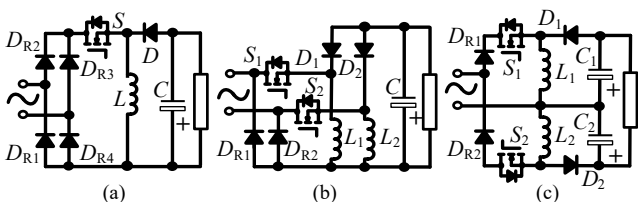

Fig. 8. Topologies for comparison: (a) Conventional buck-boost, (b) IPOP buck-boost (same to the S-IPOP buck-boost), (c) IPOS buck-boost. Note that other buck-boost is not selected for the requirements of the tapped inductors.

IPOS buck-boost has to employ the tapped inductor to avoid the sudden inductor current change in L_2 when the switch is turned off, as shown in Fig. 7(d). This means that the S-I-IPOS buck-boost has to suffer from additional power losses in L_2 to achieve the topology simplification.

S-II-IPOS. The S-II-IPOS type topology can still employ the same control strategy as that in its IPOP or conventional counterparts and the identical switch driving signals from one single switch driver can be used for the bidirectional switch [9], [10], [13], [17]. Meanwhile, a lower voltage stress across the switch compared to its other counterparts is another advantage [9], [10]. Besides, since one AC input terminal is always connected to the output capacitor in the S-II-IPOS (similar to IPOS) topologies, their common-mode (CM) EMI performances are similar to their conventional ones [10], [43].

For the exemplified S-II-IPOS topologies, the S-II-IPOS SEPIC in Fig. 6(i) has fewer components than another version of the S-II-IPOS SEPIC in [10], which is the version derived by considering the middle capacitors as the critical components instead of output diodes (cf., Fig. 2, two critical components identified in the SEPIC cell). Note that similar to [9], the inductors of the S-II-IPOS SEPIC can be coupled into a single magnetic core to make the topologies more practical. Additionally, as shown in Fig. 7(e) and (f), the S-II-IPOS buck-boost has to add a tapped inductor located in the input path to avoid the current flowing through D_2-C_2 directly and the S-II-IPOS CBB needs a bidirectional switch $S_{\rm BD}$ to replace the eliminated diodes in the inner converter branch. However, in the S-II-IPOS buck-boost, the leakage inductance in the tapped inductor will cause voltage spikes across semiconductors and extra power losses, which leads to the use of a snubber circuit and relatively high voltage rating MOSFETs [13].

III. Proposed Design Procedure

As introduced in the above, the buck-boost type PFC is focused on in this paper as case studies. Given the aforementioned power loss penalty of using tapped inductors in the S-I-IPOS and S-II-IPOS buck-boost, the comparison between the conventional buck-boost, IPOS buck-boot, and IPOP buck-boost is considered, as shown in Fig. 8. Note that the IPOP buck-boost can represent the S-IPOP buck-boost, as discussed in Section II-B. The details of the compared converter operation modes can be found in [6], [16] and the considered design specifications are shown in Table I.

Fig. 9 shows the proposed design procedure, which includes four major parts, i.e., consistent component database, cost, electrical, and thermal models. Firstly, a general description

TABLE I. DESIGN SPECIFICATIONS OF COMPARED CONVERTERS

Symbols	Parameters	Quantities*
f_S / T_S	Switching frequency / cycle	50 kHz / 20 μs
f_L	Line frequency cycle	50 Hz
V_{in}	RMS input voltage	90 to 135 Vac
V_o	Output voltage	160 V
P_o	Output power	100 W
$v_{o,rip}$	Output voltage ripple	⩽2 V @ 100 W
$i_{L,pk}$ ($i_{L,rip}$)	Inductor peak current (ripple)	⩽10 A @ 100 W
T_a	Ambient temperature	-10°C to 65°C

* Note: quantities are fixed in the Excel-based program for simplifications, although some can be seen as variables for optimization.

of the design procedure is given in this section and then how to build these four major parts is introduced in detail.

A. Limitations of Design Procedure

Since the PFC topology comparison involves many factors, limitations are made for simplifications and make this design procedure easier to be followed and built. 1) The component database only includes the same series components to exclude the manufacturing technique impacts, unless there are other reasons (explained in Section III-C). 2) This design procedure is mainly served as a topology benchmarking tool considering the same design specifications, e.g., Table I. Note that each compared converter is not optimized. 3) Topologies are mainly concerned in this paper and the EMI filter design is not involved in the design procedure, since it involves modeling [43], the filter stage number selection [44], impedance measurement [45], etc. 4) The PF and THD$_i$ comparisons are mainly compared by the experiment data and are considered separately from the design procedure since they are more related to the converter types and the control strategies.

Moreover, suggestions are given to build the design procedure. 1) The compared topologies are suggested to be the same type; otherwise, based on the same design specifications, the comparison results may be biased. 2) If the design procedure is used to optimize one converter based on one parameter (e.g., switch frequency), the limited consistent component database is recommended to include more other components and the concerned parameter in the design specifications needs to update after each running of the component selection program.

B. General Description of Design Procedure

For the given design specifications, the inductor current operation modes are decided firstly. Then, the inductance and capacitance calculations and voltage stress analysis for the main components are performed to determine the component series, which will be further used to build the component database. The component database is built by the extracted critical component parameters from datasheets to support each component's cost, electrical, and thermal models. Afterward, based on each component's models, the design procedure lists the stored (requirement-fulfilled) components for users and two selection criteria are used.

Criterion 1): for semiconductors and capacitors, their stable junction/hot-spot temperatures are used as the selection

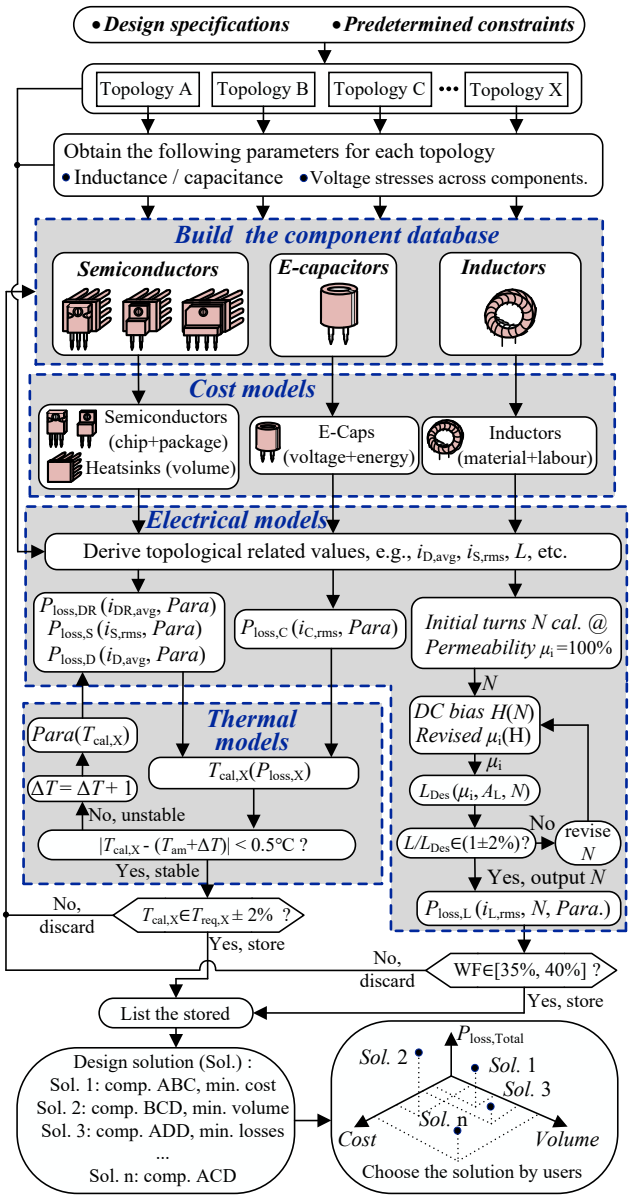

Fig. 9. Design procedure for the topology benchmarking. Initially, the procedure calculates the stable junction/hot-spot temperature of each component and the winding factor of each core in the component database by the electro-thermal loop and the permeability-related turn calculation loop (details in Section III-F). Then, it lists the stored (requirement-fulfilled) components or component combinations (including heatsinks) with cost, volume, and power loss for users to select them based on their design priorities.

considerations and obtained by an electro-thermal loop with a temperature feedback loop to update the electrical parameters in each iteration loop, which differs from most PFC designs [21], [28]–[30], [46], [47]. Criterion 2): for a toroidal core, the winding factor (WF) is considered as the selection criterion instead of the core temperature due to its good heat dissipation ability. The inductor core is stored if its WF is within the typical range of 35% to 40% [48]. Specific details about the inductor electrical model are given in Part F of this section.

Finally, once the stored components are listed, users can adopt these components based on their design purposes, e.g., minimum cost, power loss, volume, and even multiple design

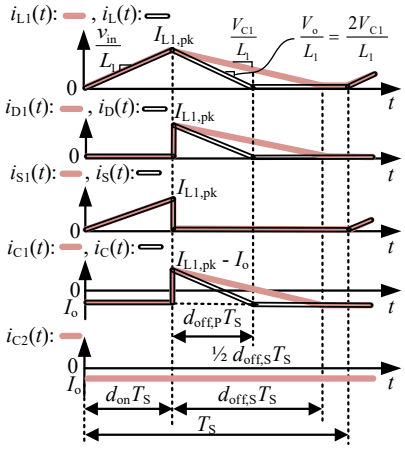

Fig. 10. Key waveforms of the conventional (same to IPOP) and IPOS buck-boost, where i_L and i_{L1} are the inductor currents, i_D and i_{D1} the output diode currents, i_S and i_{S1} the switch currents, I_o the output current, $d_{off,P}$ and $d_{off,S}$ the discharging duty cycle of inductors in the conventional and IPOS buck-boost. Besides, i_C are the conventional buck-boost output capacitor current, i_{C1} and i_{C2} the IPOS buck-boost output capacitor currents, $i_{L,pk}$ the peak inductor current in both converters, T_{on} and d_{on} the switch on-state period and the on-state duty cycle.

priority with weighting factors in each aspect.

For the design cases, based on Table I, the compared converters are designed to operate in the DCM, since the output power is low and the DCM operation nullifies the reverse recovery losses in the output diodes. Fig. 10 shows the converter key waveforms. The voltage stress and capacitance analyses of the compared topologies can refer to [6], [16].

Given the output ripple requirement and the derating factor (0.8, same in [14]) of the capacitor voltage rating, the capacitor is determined as 1500 μF/200 V for the conventional and IPOP buck-boost and 3300 μF/100 V for the IPOS buck-boost. The maximum inductor peak current expressions between the compared converters are identical [16] and given the same inductor peak current (= inductor ripple current, also kept as the same in [8]) between the compared converters, it has

$$i_{L1,pk}(t) = i_{L,pk}(t) = 2\sin(\omega t)\sqrt{\frac{P_o}{L_1 f_S \eta_e}} \leqslant 10(\mathrm{A}) \quad (1)$$

where ω is the grid angular frequency and η_e is the estimated efficiency with η_e=0.9. Based on (1), it indicates that the same inductor peak current with the power level and switching frequency given in Table I leads to the identical inductance between the compared converters. Besides, As shown in Fig. 10, compared to others, the IPOS buck-boost is easier to become the continuous conduction mode (CCM) operation. Thus, the designed inductance should ensure the DCM operation of the IPOS buck-boost. The maximum inductance is obtained by considering d_{on} + $d_{off,S} < 1$ (cf., Fig. 10), as

$$L_1 = L_2 < \frac{{V_{C1}}^2 {V_{in}}^2 T_S}{\left(V_{C1} + \sqrt{2}V_{in}\left|\sin\omega t\right|\right)^2 P_o} \quad (2)$$

where V_{C1} (= ½V_o) is the voltage across one of the output split capacitors. According to (1), (2), and Table I, the calculated maximum and minimum inductance are 115.7 and 88.9 μH, respectively. Then, the inductance is set to 110 μH to ensure the DCM operation with certain margins.

Additionally, PF expressions of the compared topologies can be derived when they are operating in the DCM and they all have a theoretical unity PF if ignoring the phase shift between the input voltage and current caused by the EMI filter [16]. Besides, the EMI filters for the benchmarked topologies are designed by referring to [6], [49].

C. Component Database

Although this design procedure requires the same type components only from the same series, there are some exceptions, e.g., MOSFETs or heatsinks in the same series only cover a limited range of rated voltages or thermal resistances. Specifically, in the case studies, the maximum theoretical voltage stresses are 351 V in the conventional and IPOP buck-boost, 271 V in the IPOS one. Given the MOSFET voltage stress margin factor (1.75, typical 1.5-1.65 in the boost PFC [47] or even up to 2.4-2.5 in some bridgeless [13], [15]), the MOSFETs of the CoolMOS$^{\mathrm{TM}}$ C7 series with 650-V rated voltage and CP series with 500-V are included in the database, since C7 or CP series only cover limited rated voltages [31].

The built component database (also cf., Table II), in this case, includes output diodes from Infineon CoolSiC$^{\mathrm{TM}}$ G5 with the TO-220 package [50], MOSFETs from Infineon CoolMOS$^{\mathrm{TM}}$ C7 and CP with the TO-247 package [31], heatsinks from Aavid with straight and unequal type extruded channel fin [51] and Ohmite *P* series [52], toroidal cores from Magnetics Kool Mμ with the outside diameter (OD) sizes between 2.7 and 4.7 cm [48], and output capacitors from Nichicon LLS series. For the input rectifier diodes, the bridgeless type converters only need two discrete diodes. However, the conventional converter needs four diodes. Thus, Infineon CoolSiC$^{\mathrm{TM}}$ G5 diodes, along with Vishay New isoCink+$^{\mathrm{TM}}$ diode bridges (a single four-terminal bridge rectifier) [53], are both considered as the rectifier diode solutions. Although the diode bridge solution is not cost-effective for the bridgeless topologies, the design procedure will judge the feasibility on its own and list the stored solutions.

D. Cost Models

To avoid components' price fluctuations due to distributors price strategies, material marketing behaviors, policy impacts, and etc., cost models are built based on the component physical properties (cf., Fig. 9, "cost models").

For semiconductors, their cost models consist of two parts, the chip area and the package. Due to the lack of information in the corresponding datasheets [31], the rated on-state drain current $I_{don,rated}$ or forward current $I_{F,rated}$ are taken into account in the cost models since they can reflect the chip areas inside the devices. On the other hand, the package cost in the manufacturing processing is fixed for the devices of the same series. Hence, the estimated cost models are given as

$$C_{MOS}(I_{on,rated}) = a_{Mos,chip} \cdot I_{don,rated} + b_{Mos,pack} \quad (3)$$
$$C_{D/DR}(I_{F,rated}) = a_{D/DR,chip} \cdot I_{F,rated} + b_{D/DR,pack} \quad (4)$$

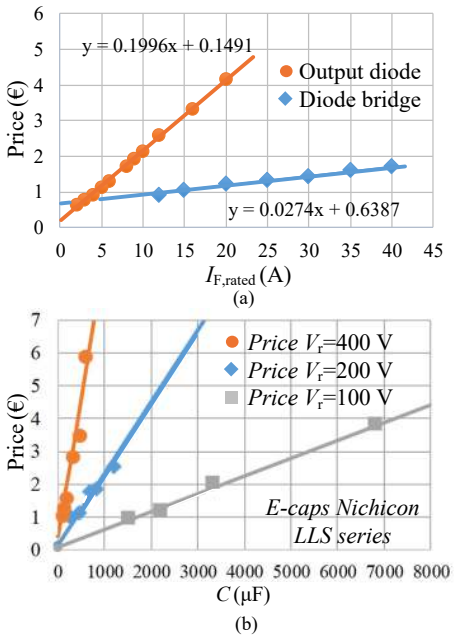

Fig. 11. Component prices from Mouser and the curve fitting-based cost models: (a) CoolSiC^{TM} G5 series diodes and New isoCink+^{TM} series diode bridges and (b) the LLS series electrolytic capacitors.

TABLE II. COEFFICIENTS IN COST MODELS

Components	a_x	b_x	c_x
Inductors (Kool Mμ core)	0.140	0.00146	3.28
Diodes (CoolSiC^{TM} G5)	0.200	0.149	-
Bridges (New isoCink+^{TM})	0.027	0.639	-
Capacitors (Nichicon LLS)	8.13×10^{-3}	7.21×10^{-8}	-
MOSFETs (CoolMOS^{TM} CP)	0.110	0.210	-
MOSFETs (CoolMOS^{TM} C7)	0.404	0.811	-
Heatsinks (straight / unequal channel)	0.0244 / 0.0875	0.450 / 0.616	-
Heatsinks (Ohmite *P* series)	0.092	1.044	-

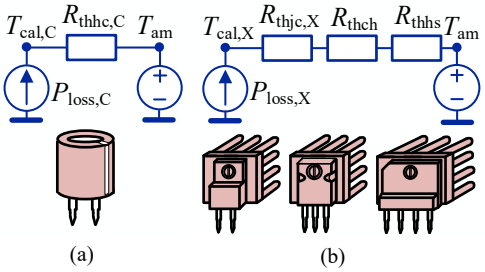

Fig. 12. Considered power loss-based thermal resistance networks for the components: (a) capacitors and (b) semiconductors with heatsinks.

where $a_{\mathrm{Mos,chip}}$ and $a_{\mathrm{D/DR,chip}}$ are the chip area related coefficients for MOSFETs and diodes, $b_{\mathrm{Mos,pack}}$ and $b_{\mathrm{D/DR,pack}}$ are the package-related coefficients.

For the inductor, the considered cost model includes the volume-based core, winding wire, and labor (winding the core + fixed core producing) costs, expressed as

$$C_{\mathrm{ind}}(Vol, N) = a_{\mathrm{core}} \cdot Vol_{\mathrm{core}} + b_{\mathrm{wire}} \cdot N \cdot \mathrm{MLT} + c_{\mathrm{labor}} \quad (5)$$

in which a_{core}, b_{wire}, and c_{labor} are the cost related coefficients and MLT is the mean length per turn for winding a core.

The cost models of heatsinks and electrolytic capacitors are the same as given in [32]. The capacitor cost model is

$$C_{\mathrm{cap}}(V_{\mathrm{r}}, C) = a_{\mathrm{cap}} \cdot V_{\mathrm{r}} + b_{\mathrm{cap}} \cdot (C \cdot V_{\mathrm{r}}^2) \quad (6)$$

where V_{r} and C represent the rated voltage and the capacitance, a_{cap} and b_{cap} are the rated voltage and energy related coefficients, respectively. The heatsink cost model is

$$C_{\mathrm{HS}}(Vol) = a_{\mathrm{vol}} \cdot Vol_{\mathrm{HS}} + b_{\mathrm{fix}} \quad (7)$$

with Vol_{HS} being the heatsink volume, a_{vol} and b_{fix} being the volume and manufacturing related fixed coefficients.

Fig. 11 shows the component prices from Mouser and the cost model-based fitting curves for the diodes, diode bridges, and capacitors. As observed in Fig. 11, the cost models almost fit the prices offered by the distributor. Table II shows all the coefficients in the cost models.

E. Thermal Models

In each iteration of the electro-thermal loop, the thermal models receive the power losses $P_{\mathrm{loss,X}}$ of the component X from the electrical models and output the calculated junction/hot-spot temperature $T_{\mathrm{cal,X}}$. If the temperature is not stable yet ($T_{\mathrm{cal,X}}$ – assumed temperature $\geq$ 0.5 °C), then the thermal models update new junction/hot-spot temperature-dependent parameters *Para* for the electrical models to re-calculate $P_{\mathrm{loss,X}}$. Thus, the thermal models consist of two parts: the junction/hot-spot temperature-based models for calculating the thermal-dependent parameters *Para* and the power loss-based thermal networks for computing the junction/hot-spot temperatures $T_{\mathrm{cal,X}}$.

For simplicity, certain assumptions are made: 1) All the thermal capacitances and the cross-coupling between components are not considered. 2) Due to the insignificant change of equivalent-series-resistance (ESR) with the temperature for the capacitors of interest, the ESR of the analyzed electrolytic capacitors is assumed thermal-independent. 3) MOSFET on-state resistance $R_{\mathrm{on,S}}$, output diode forward voltage $V_{\mathrm{F,D}}$, and input rectifier diode forward voltage $V_{\mathrm{F,DR}}$ are considered as the thermal-dependent parameters. 4) The case-to-heatsink thermal resistance R_{thch} in Fig. 12 is caused by the thermal grease and is assumed to be 1 °C/W [46].

To calculate $T_{\mathrm{cal,X}}$, the component thermal resistance networks are determined, as shown in Fig. 12. The junction-to-case ($R_{\mathrm{thjc,X}}$) and heatsink-to-ambient ($R_{\mathrm{thhs,X}}$) thermal resistances can be extracted from datasheets [54], except for the capacitor hot-spot-to-case thermal resistance $R_{\mathrm{thhc,C}}$, which is extracted from [55]. Note that if the heatsink is not employed for a semiconductor, the junction-to-ambient thermal resistance R_{thja} will be used instead of R_{thjc}+R_{thch}+R_{thhs}, which are also included in datasheets. Assuming that R_{th} is the sum of the thermal resistance in the thermal path, the junction temperature of the component X can be calculated as

$$T_{\mathrm{cal,X}} = T_{\mathrm{am}} + P_{\mathrm{loss,X}} \cdot \sum R_{\mathrm{th}}. \quad (8)$$

To obtain *Para*, the critical data are extracted from

datasheets and fitting curves are employed. Fig. 13 exemplifies the corresponding fitting curves of $R_{\mathrm{on,S}}$ for the MOSFETs and $V_{\mathrm{F,DR}}$ for the diode bridges. Here, $R_{\mathrm{on,S}}$ is related to the on-state drain current I_{don} and $T_{\mathrm{cal,S}}$. Similarly, for $V_{\mathrm{F,DR}}$, the forward current $I_{\mathrm{F,DR}}$ and $T_{\mathrm{cal,DR}}$ are taken into account in the fitting curves. The following gives the general fitting equations for $R_{\mathrm{on,S}}$ and $V_{\mathrm{F,DR}}$ as

$$R_{\mathrm{on,S}} = \frac{a_{\mathrm{th,S}} \cdot e^{b_{\mathrm{th,S}} \cdot I_{\mathrm{don}}}}{a_{\mathrm{th,S}} \cdot e^{b_{\mathrm{th,S}} \cdot I_{\mathrm{don,rated}}}} \cdot c_{\mathrm{th,S}} \cdot e^{d_{\mathrm{th,S}} \cdot T_{\mathrm{j,cal,S}}} \tag{9}$$

$$V_{\mathrm{F,DR}} = a_{\mathrm{th,DR}} \cdot T_{\mathrm{j,cal,DR}}^{b_{\mathrm{th,DR}}} \cdot c_{\mathrm{th,DR}} \cdot I_{\mathrm{F,DR}}^{d_{\mathrm{th,DR}}} \tag{10}$$

where $a_{\mathrm{th,X}}$, $b_{\mathrm{th,X}}$, $c_{\mathrm{th,X}}$, and $d_{\mathrm{th,X}}$ are determined by the data from each component datasheet. Note that since the Infineon depicts $R_{\mathrm{on,S}}$ by referring to the rated on-state current in the datasheets, the above fitting models for the MOSFETs and diode bridges (from Vishay) are different.

As for the output diodes, the threshold voltage $V_{\mathrm{th,D}}$ and on-state resistance R_{DIFF} are considered. Meanwhile, the datasheets already offer the thermal-dependent fitting equations and the corresponding coefficients $a_{\mathrm{th,D}}$, $b_{\mathrm{th,D}}$, and $c_{\mathrm{th,D}}$ for each component [54], as

$$\begin{cases} V_{\mathrm{th,D}} = -0.001 \cdot T_{\mathrm{j,cal,D}} + 1.04 \\ R_{\mathrm{DIFF}} = a_{\mathrm{th,D}} \cdot T_{\mathrm{j,cal,D}}^2 + b_{\mathrm{th,D}} \cdot T_{\mathrm{j,cal,D}} + c_{\mathrm{th,D}} \end{cases} \tag{11}$$

in which, constants –0.001 and 1.04 are the same coefficients for each component (TO-220 real 2-pin package) in the CoolSiC$^{\mathrm{TM}}$ G5 series while $a_{\mathrm{th,D}}$, $b_{\mathrm{th,D}}$, and $c_{\mathrm{th,D}}$ differ between components (e.g., IDH06G65C5 and IDH08G65C5). The obtained parameters from (9)-(11) are used to calculate the power losses under the different junction temperatures. It is suggested to include these coefficients in the component database along with other parameters extracted from datasheets, which is easier to implement the entire procedure.

F. Electrical Models

This part mainly relates to the parameters extracted from datasheets and the compared topologies. For simplicity, assumptions are made: 1) The switching frequency f_{S} is much higher than the line frequency f_{L}. 2) The AC input voltage $v_{\mathrm{in}}(t)$ is seen as a constant during one switching cycle T_{S}. 3) Since the New isoCink+$^{\mathrm{TM}}$ series diode bridges do not offer the switching loss-related parameters (i.e., the capacitive charge Q_{c}) in the datasheets [53], the switching losses in the input rectifier diodes are neglected in all the compared converters. 4) Energy losses caused by the resistor-capacitor-diode (RCD) snubber circuits are ignored. 5) The skin effect and eddy current in the inductor are not considered.

This part focuses on the key component expressions in the IPOS buck-boost only, since similar derivations can be obtained for the conventional and IPOP buck-boost by referring to [6], [16]. In one switching cycle, the RMS currents of the switch S_1, output diode D_1, inductor L_1, and capacitors C_1 and C_2 are derived as

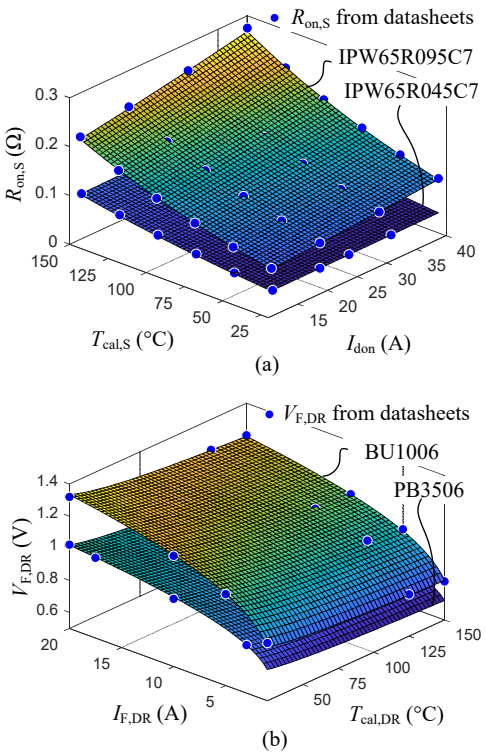

Fig. 13. Four fitting curve examples of total 28 built junction temperature-based thermal models: (a) $R_{\mathrm{on,S}}$ in the MOSFETs with the junction temperature $T_{\mathrm{cal,S}}$ and on-state drain current I_{don} as variables, (b) $V_{\mathrm{F,DR}}$ in the diode bridge with the junction temperature $T_{\mathrm{cal,DR}}$ and forward current $I_{\mathrm{F,DR}}$ as variables. Note that in the case studies, I_{don} and $I_{\mathrm{F,DR}}$ are assumed as the switch RMS current and the output diode average current in a half line cycle, as given in the electrical models.

$$i_{\mathrm{S1,RMS}}^2 = \frac{1}{T_{\mathrm{S}}} \int_0^{T_{\mathrm{S}}} [i_{\mathrm{S1}}(t)]^2 d(t) = \frac{T_{\mathrm{S}}^2 v_{\mathrm{in}}^2 d_{\mathrm{on}}^3}{3L_1^2} \tag{12}$$

$$i_{\mathrm{L1,RMS}}^2 = \frac{1}{T_{\mathrm{S}}} \int_0^{T_{\mathrm{S}}} [i_{\mathrm{L1}}(t)]^2 d(t) = \frac{T_{\mathrm{S}}^2 d_{\mathrm{on}}^3 v_{\mathrm{in}}^2 (V_{\mathrm{C1}} + v_{\mathrm{in}})}{3V_{\mathrm{C1}} L_1^2} \tag{13}$$

$$i_{\mathrm{D1,RMS}}^2 = \frac{1}{T_{\mathrm{S}}} \int_0^{T_{\mathrm{S}}} [i_{\mathrm{D1}}(t)]^2 d(t) = \frac{{T_{\mathrm{S}}}^2 d_{\mathrm{on}}^3 v_{\mathrm{in}}^3}{3V_{\mathrm{C1}} {L_1}^2} \tag{14}$$

$$i_{\mathrm{C1,RMS}}^2 = \frac{T_{\mathrm{S}}^2 d_{\mathrm{on}}^3 v_{\mathrm{in}}^3 - 3d_{\mathrm{on}}^2 I_{\mathrm{o}} T_{\mathrm{S}} L_1 v_{\mathrm{in}}^2 + 3I_{\mathrm{o}}^2 V_{\mathrm{C1}} L_1^2}{3V_{\mathrm{C1}} L_1^2} \tag{15}$$

$$i_{\mathrm{C2,RMS}} = I_{\mathrm{o}}. \tag{16}$$

The average currents of the diode bridge D_{R} and output diode D_1 are

$$i_{\mathrm{DR,avg}}(t) = i_{\mathrm{S1,avg}}(t) = \frac{2P_{\mathrm{in}} |\sin(\omega t)|}{V_{\mathrm{M}}} \tag{17}$$

$$i_{\mathrm{D1,avg}}(t) = \frac{2|\sin \omega t|^2 P_{\mathrm{o}}}{V_{\mathrm{C1}}} = 4I_{\mathrm{o}} |\sin \omega t|^2 \tag{18}$$

where P_{in} is the input power, and V_{M} is the AC input peak voltage. The above RMS and average currents in (12)-(18) are

the expressions in one switching cycle. In the half line cycle, they are re-calculated as

$$i^2_{\mathrm{X,RMS,L}} = \frac{1}{1/2T_\mathrm{L}} \int_0^{1/2T_\mathrm{L}} i^2_{\mathrm{X,RMS}}(t)dt, \mathrm{X} \in \{L, S, C\} \quad (19)$$

$$i_{\mathrm{Y,avg,L}} = \frac{1}{1/2T_\mathrm{L}} \int_0^{1/2T_\mathrm{L}} i_{\mathrm{Y,avg}}(t)dt, \mathrm{Y} \in \{D, DR\}. \quad (20)$$

The derived topology-related values are further used to calculate the power losses. For semiconductors, the power losses mainly include switching losses $P_{\mathrm{X,sw,L}}$ and conduction losses $P_{\mathrm{X,cond,L}}$, as

$$P_{\mathrm{loss,DR}} = \overbrace{V_{\mathrm{F,DR}} \cdot i_{\mathrm{DR,avg,L}}}^{P_{\mathrm{DR,cond,L}}} \quad (21)$$

$$P_{\mathrm{loss,D}} = \overbrace{V_{\mathrm{th,D}} \cdot i_{\mathrm{D,avg,L}} + R_{\mathrm{DIFF}} \cdot i^2_{\mathrm{D,RMS,L}}}^{P_{\mathrm{D,cond,L}}} + \overbrace{Q_\mathrm{c} \cdot V_{\mathrm{re,D}} \cdot f_\mathrm{S}}^{P_{\mathrm{D,sw,L}}} \quad (22)$$

$$P_{\mathrm{loss,S}} = \overbrace{R_{\mathrm{on,S}} \cdot i^2_{\mathrm{S,rms,L}}}^{P_{\mathrm{S,cond,L}}} + \overbrace{E_{\mathrm{oss}} \cdot f_\mathrm{S} + \frac{2}{T_\mathrm{L}} \sum^{f_\mathrm{S}/(2f_\mathrm{L})} E_{\mathrm{sw}}}^{P_{\mathrm{S,sw,L}}} \quad (23)$$

in which E_{sw} indicates hard switching energy losses in each switching cycle, E_{oss} is the energy stored in the output capacitance C_{oss} that needs to turn off the switch [46], Q_c is the capacitive charge that is required to turn off the diode, and $V_{\mathrm{re,D}}$ is the reversed voltage across the output diode.

In (22), the output diode switching losses are ignored since the converters are in the DCM. In (23), E_{sw} can be calculated by summing up the turning-on power losses $E_{\mathrm{sw,on}}$ and turning-off power losses $E_{\mathrm{sw,off}}$ in one switching cycle T_S. Besides, E_{oss} is a nonlinear value relating to V_{DS} and Fig. 14 shows the fitting curve for E_{oss} with V_{DS}∈[50, 400] (V) of the CoolMOS$^{\mathrm{TM}}$ C7 series. Here, E_{sw} is obtained as

$$\begin{aligned} E_{\mathrm{sw}} &= E_{\mathrm{sw,on}} + E_{\mathrm{sw,off}} \\ &= \frac{V_{\mathrm{DS}} i_{\mathrm{S,on}}(t_2 - t_1 + t_3)}{2} + \frac{V_{\mathrm{DS}} i_{\mathrm{S,off}}(t_5 + t_6)}{2} \end{aligned} \quad (24)$$

in which t_1∼t_6 are calculated by referring to [56], $i_{\mathrm{S,on}}$ and $i_{\mathrm{S,off}}$ are the drain currents during device turning-on and turning-off transitions. Due to the short period of t_3, t_4, and t_5, $i_{\mathrm{S,on}}$, $i_{\mathrm{S,off}}$, and V_{DS} are evaluated by

$$i_{\mathrm{S,on}} = V_\mathrm{M} |\sin(\omega t)|_{t=\mathrm{j}\cdot T_\mathrm{S}} \cdot (t_3 + t_2 - t_1)/L_1 \quad (25)$$

$$i_{\mathrm{S,off}} = I_{\mathrm{L1,pk}} \quad (26)$$

$$V_{\mathrm{DS}} = V_\mathrm{M} |\sin(\omega t)|_{t=\mathrm{j}\cdot \mathrm{T_S} + T_{\mathrm{on}}} + V_\mathrm{o}/2. \quad (27)$$

where j indicates the jth switching cycle in the half line cycle and the maximum value of j is $f_\mathrm{S}/(2f_\mathrm{L})$. In fact, $i_{\mathrm{S,on}}$ is very close to zero due to the small value of t_3+t_2-t_1.

As for capacitors, the calculated losses are

$$P_{\mathrm{loss,C}} = ESR \cdot i^2_{\mathrm{C,rms,L}}. \quad (28)$$

Note that some manufacturers only offer the dissipation factor in datasheets. Then, ESR can be calculated by the equation introduced in [57] or directly measured.

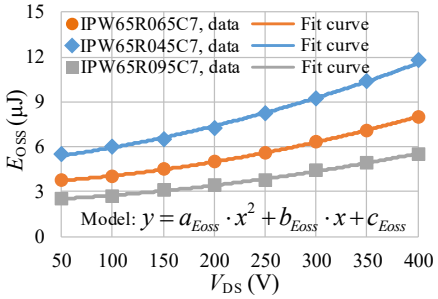

Fig. 14. Three examples of total 12 built curve fitting models for drain to source voltage V_{DS} related E_{oss} in CoolMOS$^{\mathrm{TM}}$ C7 series. The models are 2nd polynomial functions with a_{Eoss} = 2^{-5}, 1^{-5}, 2^{-5}, b_{Eoss} = 0.0077, 0.0027, 0.0036, and c_{Eoss} = 4.96, 2.34, 3.51 in IPW65R045C7, IPW65R065C7, and IPW65R095C7, respectively.

Regarding inductors, copper losses and core losses are taken into account. Be careful about the parameter units in the magnetic datasheet, e.g., Oersted and Gauss [58]. The corresponding power loss equation is

$$P_{\mathrm{loss,ind}} = \overbrace{R_{\mathrm{Cu}} \cdot i^2_{\mathrm{L1,rms,L}}}^{P_{\mathrm{ind,copper,L}}} + \overbrace{l_\mathrm{e} \cdot A_\mathrm{e} \cdot N_\mathrm{c} \cdot P_{\mathrm{core,v}}}^{P_{\mathrm{ind,core,L}}} \quad (29)$$

in which R_{Cu} is the winding wire resistance, l_e the core effective path length, A_e the effective cross section of the inductor core, N_c the inductor core number, and $P_{\mathrm{core,v}}$ the time-average core loss per unit volume.

To compute the copper losses $P_{\mathrm{ind,copper,L}}$, the core winding turn N needs to be determined firstly by the turn calculation loop, as shown in Fig. 9. Initially, when the inductance is determined, N can be obtained as [48]

$$N = \sqrt{\frac{L}{A_\mathrm{L}}} \quad (30)$$

where L is the desired inductance and A_L is the inductance factor (nominal inductance). Afterward, the magnetizing force (DC bias) $H(N)$ is expressed as

$$H(N) = 0.4\pi N \cdot i_\mathrm{L}(t)/l_\mathrm{e}. \quad (31)$$

Then, the obtained $H(N)_{\mathrm{max}}$ (let $i_\mathrm{L}(t) = i_{\mathrm{L,pk}}$ in (31)) is used to compute the corresponding permeability μ_i, based on the "permeability vs. DC bias" curve fitting equations offered by the manufacturer [58]. Subsequently, the calculated μ_i is used to revise the actual designed inductance L_{Des} as

$$L_{\mathrm{Des}} = N^2 \cdot \mu_\mathrm{i} \cdot A_\mathrm{L} \cdot 10^{-3}/l_\mathrm{e}. \quad (32)$$

Afterward, L is compared with L_{Des} to check if N can fulfill the required inductance. If not, N is increased if $L_{\mathrm{Des}} < L$ and decreased if $L_{\mathrm{Des}} > L$. The revised N is used again to re-calculate new L_{Des} by (31) and (32). This loop for calculating N aborts until $L/L_{\mathrm{Des}} \in (1 \pm 2\%)$. Finally, R_{Cu} in (29) is

$$R_{\mathrm{Cu}} = \rho_{\mathrm{Cu}} \cdot l_{\mathrm{Cu}}/A_{\mathrm{Cu}} = \rho_{\mathrm{Cu}} \cdot N \cdot \mathrm{MLT}/A_{\mathrm{Cu}} \quad (33)$$

where ρ_{Cu}, l_{Cu}, and A_{Cu} are the electrical resistivity (= 1.68×10^{-8} $\Omega \cdot$ m), winding wire length, and cross section of wire, respectively. In the design cases, wire AWG 17 is used and thus A_{Cu}=1.04 mm^2.

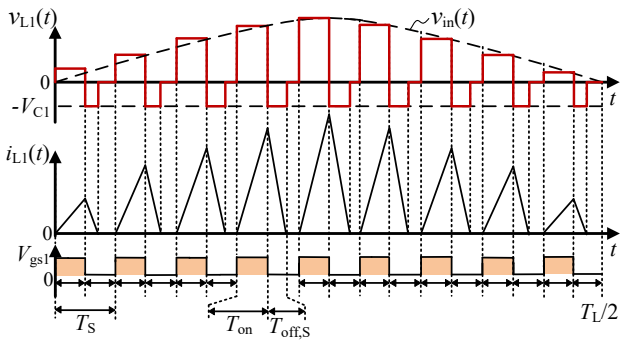

Fig. 15. Applied voltages across the inductor in the IPOS buck-boost in each half line cycle. Notably, the switching cycle period shown here is expanded for brevity and according to the derived d_{on} expression [16], T_{on} is almost fixed while $T_{off,S}$ is related to the input voltage $v_{in}(t)$.

To determine core losses $P_{ind,core,L}$, $P_{core,v}$ should be calculated firstly, which can be done by the Steinmetz equation with material parameters α, β, and k, as

$$P_{core,v} = k \cdot {f_S}^{\alpha} \cdot \Delta B^{\beta} \tag{34}$$

where ΔB is the peak-peak flux density [48]. However, the accuracy of (34) is limited and the improved generalized Steinmetz equation (iGSE) is proposed with more accuracy even for non-sinusoidal excitation [59]. Besides, a simplified loss calculation is provided and only requires ΔB in each flux repeating cycle T_B, which is

$$\begin{cases} k_i = k/\left\{2^{\beta+1}\pi^{\alpha-1}\left[0.2761 + 1.706/(\alpha+1.354)\right]\right\} \\ P_{Core,v} = \frac{k_i(\Delta B)^{\beta-\alpha}}{T_B}\sum_i\left(\left|\frac{V_i}{NA_e}\right|^{\alpha}\cdot\Delta T_i\right) \end{cases} \tag{35}$$

Here, k_i is a constant determined by each core material parameters and V_i is the applied voltage across the inductor during the i^{th} time period ΔT_i. Note that the sum of each ΔT_i should be equal to the cycle T_B. If T_B is seen as one switching cycle T_S, then ΔB is the peak-peak flux density within T_S.

However, in PFC applications, as shown in Fig. 15, the variety in the ac input voltage will cause the differences of ΔB in every switching cycle. Thus, in order to apply the core loss calculation expression, ΔB needs to be updated within every switching cycle. A similar method is also used in [57] to estimate the boost type PFC inductor core loss.

In this design, $i_{L1,pk,j}$ in the j^{th} switching cycle is used to calculate $H_{max,j}$ by (31) and $H_{min,j}$ is considered as zero. Then, the H-B curve fitting equation provided in [58] is used to compute ΔB_j. Finally, $P_{core,v}$ is estimated by

$$\begin{cases} k_i = k/\left\{2^{\beta+1}\pi^{\alpha-1}\left[0.2761 + 1.706/(\alpha+1.354)\right]\right\} \\ P_{Core,v,j} = \frac{k_i}{T_S}(\Delta B_j)^{\beta-\alpha}\left[\left(\frac{v_{in,j}}{NA_e}\right)^{\alpha}T_{on} + \left(\frac{V_{C1}}{NA_e}\right)^{\alpha}T_{off,S}\right] \\ P_{core,v} = \frac{1}{T_L/2}\sum_{j=1}^{f_S/(2f_L)}\left(P_{core,v,j}\cdot T_S\right) \end{cases} \tag{36}$$

where T_{on} can be derived by referring to [16] and $T_{off,S}$ can be expressed by T_{on} through the inductor volt-second balance.

TABLE III. STORED MOSFETS IN CONVENTIONAL BUCK-BOOST AT 90-VAC INPUT, 100-W RATED POWER

No.	MOSFETs	Heatsinks	$T_{j,cal}$ ($90 \pm 2°C$)	P_{loss} (W)	Cost (€)	Vol. (cm^3)
1	IPW65R045C7	7.0 °C/W	92	3.18	8.10	29.36
2	IPW65R045C7	6.8 °C/W	91	3.18	7.51	30.72
3	IPW65R065C7	8.8 °C/W	91	2.45	5.96	23.66
4	IPW65R095C7	10.2 °C/W	90	2.09	4.34	18.40
5*	IPW65R125C7	11.4 °CW	92	1.97	3.23	12.71
6*	IPW65R125C7	10.2 °C/W	89	1.95	3.73	18.40
7*	IPW65R190C7	10.2 °C/W	92	2.10	3.08	18.40
8	IPW65R190C7	8.8 °C/W	89	2.07	3.54	23.66

* Note: No. 5 has the minimal volume, No. 6 the min. power losses, and No. 7 the min. cost.

IV. BENCHMARKING RESULTS

A. Stored Component Selection

The proposed design procedure generates the stored component/combination lists and users select the final solutions based on their design priorities. For example, Table III lists the stored MOSFETs with heatsinks in the conventional buck-boost. Comparing the power losses in Table III, it indicates that MOSFETs with lower $R_{on,S}$ (e.g., IPW65R045C7 $R_{on,S}$ = 45 mΩ) do not ensure the lower power losses since the power losses include switching losses and conduction losses and a good selection of the specific MOSFET should be based on the balancing between the losses at a target load condition [46]. That is also one of the reasons why this consistent design procedure is needed to implement the same design specifications and then give a fair performance assessment for each compared topology.

In this design case, the cost is the most concerned design target since the buck-boost PFC converter is usually adopted in cost-sensitive applications [6], [34]. Thus, the combination (MOSFET + Heatsink) of No. 7 in Table III is finally selected. Similarly, if the design target is the minimal power loss, No. 6 should be chosen; if the design target is the minimal volume, No. 5 is preferred.

Table IV shows the final selected components for converters, based on the minimal cost design target at the 90-Vac input, 100-W output condition (max. current stress condition). Moreover, the minimal cost, minimal power loss, and minimal volume design target-based comparison results are also given in Figs. 16-18. Note that in Fig. 18, when using the minimal volume as the first design target, the component selection has multiple-options and the second design target is required to finally select one component. This is because some stored components may have the same volume although they have different performance, e.g., cores 0077930A7 and 0077934A7 with the same OD size are stored for users and another selection rule is needed from users to finally determine one.

Thus, in Fig. 18, apart from the minimal volume design target, the minimal cost design target is taken as the second design priority to further size the stored components. Then, for the IPOS and IPOP buck-boost PFC converters, their final total volumes under the minimal volume design are actually the same as that under the minimal cost design, which means that the converters achieve minimal cost and volume simultaneously. This can be explained by that for the main components of determining the converter volume, e.g.,

TABLE IV. MINIMAL COST DESIGN BASED COMPONENT SELECTION AT 90-VAC INPUT, 100-W RATED POWER

Buck-boost converters	Ind.* (WF$\in$ 35% $\sim$ 40%)	S + Hs * ($T_{j,cal} \in 90 \pm 2$ °C)	Cap * ($T_{j,cal} \in 70 \pm 2$ °C)	D + Hs * ($T_{j,cal} \in 95 \pm 2$ °C)	D_R + Hs * ($T_{j,cal} \in 100 \pm 2$ °C)
Conv. buck-boost	0077930A7×1 (110 μH)	IPW65R190C7×1 (650 V) SW38-2G×1 (10.2 °C/W)	LLS2D152MELC×1 (200 V / 1500 μF)	IDH06G65C5×1 (650 V) 507302B00000G×1 (24.5 °C/W)	BU1006×1 (600 V) None
IPOS buck-boost	0077930A7×2 (110 μH each)	IPW50R250C7×2 (500 V) 507302B00000G×2 (24.5 °C/W)	LLS2A332MELA×2 (100 V / 3300 μF)	IDH06G65C5×2 (650 V) 507302B00000G×2 (24.5 °C/W)	IDH06G65C5×2 (650 V) None
IPOP buck-boost	0077930A7×2 (110 μH each)	IPW65R190C7×2 (650 V) 507302B00000G×2 (24.5 °C/W)	LLS2D152MELC×1 (200 V / 1500 μF)	IDH06G65C5×2 (650 V) None	IDH06G65C5×2 (650 V) None

* Note: "Ind." represents the inductor, "S" the switch, "Hs" the heatsink, "Cap" the capacitor, "D" the diode, and "D_R" the diode rectifier.

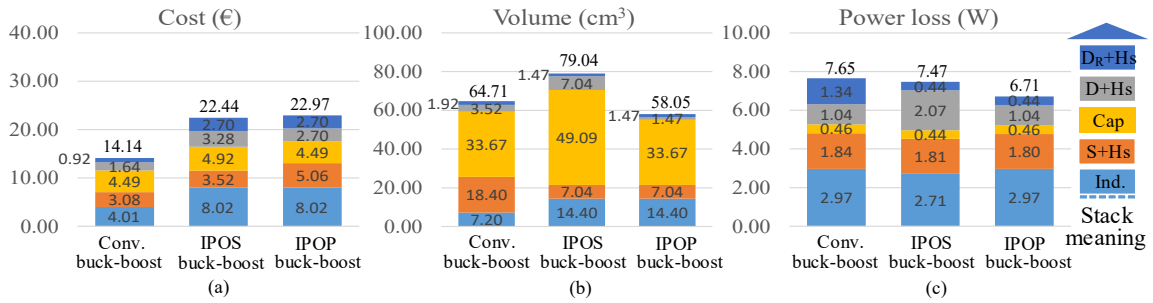

Fig. 16. Minimal cost design target-based comparison results in terms of (a) cost, (b) volume, and (c) power loss at the 110-Vac, 100-W rated power.

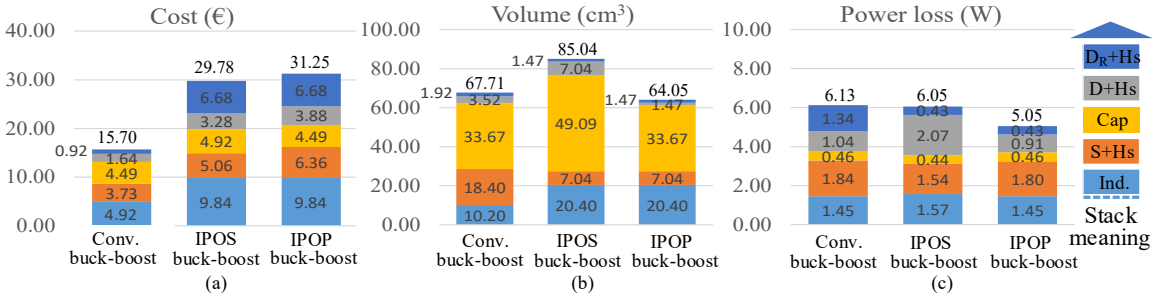

Fig. 17. Minimal power loss design target-based comparison results in terms of (a) cost, (b) volume, and (c) power loss at the 110-Vac, 100-W rated power.

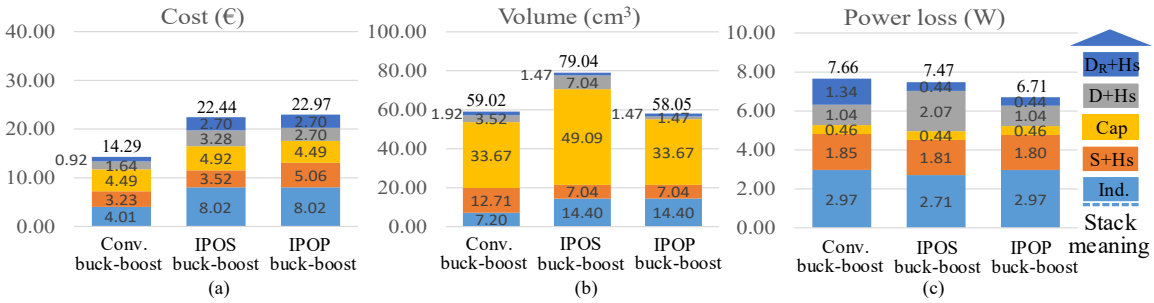

Fig. 18. Minimal volume design target-based comparison results in terms of (a) cost, (b) volume, and (c) power loss at the 110-Vac, 100-W rated power.

heatsinks and inductor cores, their volumes correlate the costs positively (cf., (6) and (7)). Then, the minimal volume design may also lead to the minimal cost.

B. Consistent Design Results (min. cost design)

Cost comparison: As shown in Fig. 16(a), the conventional buck-boost has the lowest material cost, only around 63% of the compared IPOP and IPOS buck-boost.On the other hand, seeing the "S + Hs" column in Table IV, due to the adoption of a lower voltage rating (500 V) MOSFET, the IPOS buck-boost has a 2.3% lower cost than the IPOP buck-boost.

Volume comparison: Regarding the volume in Fig. 16(b), the IPOS buck-boost has the largest volume among the compared converters. Meanwhile, in the conventional and IPOP buck-boost, although the same MOSFET IPW65R190C7 is selected (cf., "S + Hs" in Table IV), a larger and more expensive heatsink is required in the conventional buck-boost since the dual-component sets in the bridgeless topology have a better heat dissipation ability. Thus, the IPOP buck-boost has a 10.3% less volume than the conventional buck-boost. These results imply that the dual component-based bridgeless type topologies may have a smaller volume than their conventional

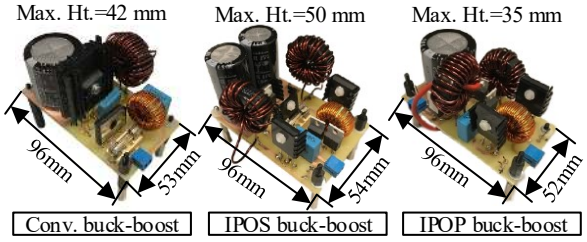

Fig. 19. Experimental prototypes based on the minimal cost design target. The IPOP buck-boost PFC converter has the minimal volume among the three compared converters.

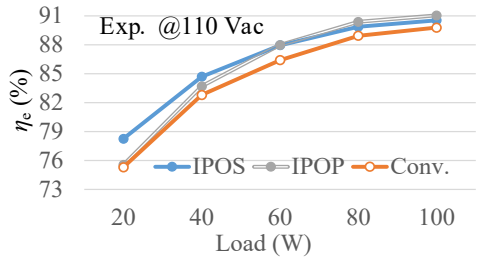

Fig. 20. Measured efficiency curves of the conventional buck-boost, IPOS buck-boost, and IPOP buck-boost PFC converters over different loads.

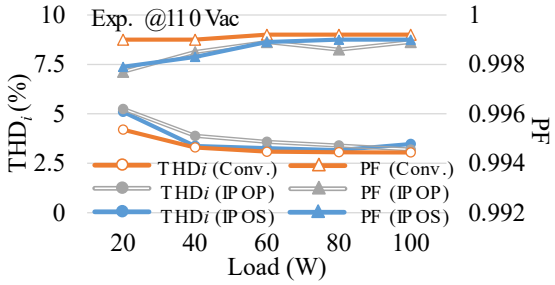

Fig. 21. Measured PF and THD$_i$ curves of the conventional buck-boost, IPOS buck-boost, and IPOP buck-boost PFC converters over different loads.

counterparts under a consistent design.

Power loss comparison: As shown in Fig. 16(c), the IPOP buck-boost has the minimum power loss among the compared converters. Besides, referring to "D + Hs" in Fig. 16(c), the IPOS buck-boost has twice larger conduction losses in the output diodes compared to the other converters, which agrees with the waveforms of $i_{\rm D1}$ and $i_{\rm D}$ in Fig. 10. The high power losses in the output diodes of the IPOS buck-boost leads to poor efficiency in heavy load conditions and the use of heatsinks, which is not employed in the IPOP buck-boost (cf., "D + Hs" in Table IV).

In addition, comparing the three converters in Figs. 16-18, although different quantitative comparison results are revealed, a similar comparative conclusion can be drawn. It indicates that within the same design target, the IPOP buck-boost shows the lowest power loss and volume among the compared converters. Meanwhile, the conventional buck-boost has the lowest cost among the compared converters. As for the IPOS buck-boost, it has a slightly lower cost than its IPOP counterpart but with the disadvantage of higher volume and power losses, which can be seen only as a compromising solution between the conventional and IPOP buck-boost.

In summary, by implementing this consistent design procedure, users can choose the most-suitable topology based on the quantitative comparison results. On the other hand, if other topology comparisons are required, users mainly need to analyze compared topologies, build a consistent database, and replace the key component expressions in the electrical models. Notably, some details (e.g., the change of thermal resistance network when none heatsink is employed, the voltage change across inductor core in each switching cycle, etc.) still need extra attentions as introduced in this section.

V. Experimental Results

Based on Table IV, the conventional buck-boost, IPOS buck-boost, and IPOP buck-boost PFC converters, shown in Fig. 8, are designed under the minimal cost target. The three converters adopt the same single loop control with the same proportional-integral (PI) parameters, implemented in a digital signal processor (DSP) TMS320F28335. Fig. 19 shows the photos of the three prototypes and their volume comparison results match the aforementioned theoretical analysis. Figs. 20 and 21 show the measured efficiency $\eta_{\rm e}$, PF, and THD$_i$ curves, respectively. Figs. 22-24 present the experimental waveforms of the converters in the 100-W output condition.

In Fig. 20, the IPOP buck-boost has the highest efficiency (91.1%) in the 100-W output condition and the IPOS buck-boost ranks the second (90.6%), followed by the conventional one (89.7%). According to the measured efficiency, the IPOP buck-boost, IPOS buck-boost, and conventional buck-boost have total power losses, as 9.7 W, 10.4 W, and 11.4 W, respectively, which are different from the results in Fig. 16 This is mainly due to the RCD snubber circuits across the switches for voltage spike absorption, calculation errors of ΔB for core losses, the neglect of the switching losses in the input rectifier diodes (key parameters not available in datasheets).

As observed in Figs. 21, 22(a), 23(a), and 24(a), the compared converters have almost the same PF (close to unity) and THD$_i$. Meanwhile, their output voltage ripples $v_{\rm o,rip}$ are also similar and within the design target. Besides, compared to the conventional and IPOP buck-boost, the IPOS buck-boost has lower voltage stresses across semiconductors, which reduce the switching losses. The specific peak $V_{\rm DS}$ in the conventional, IPOS, and IPOP converters are 325 V, 255 V, and 330 V, close to the theoretical values, 316 V, 236 V, and 316 V, respectively. Errors may come from measurements and the non-ideal switching due to parasitics. As shown in Fig. 20, the lower switching losses in the semiconductors allow the IPOS buck-boost to have a higher efficiency than the other two converters in relatively light load conditions, where switching losses dominate the total power losses.

Furthermore, the zoom-in experimental waveforms are shown in Figs. 22(c), 23(c), and 24(c). The discharging period of the inductor in the IPOS buck-boost (12 μs) is twice larger than that of the IPOP and conventional buck-boost (6 μs), which verifies the power loss analysis about the output diodes (cf., Section IV-B). The higher conduction losses of the output diodes in the IPOS buck-boost lead to the lower efficiency in

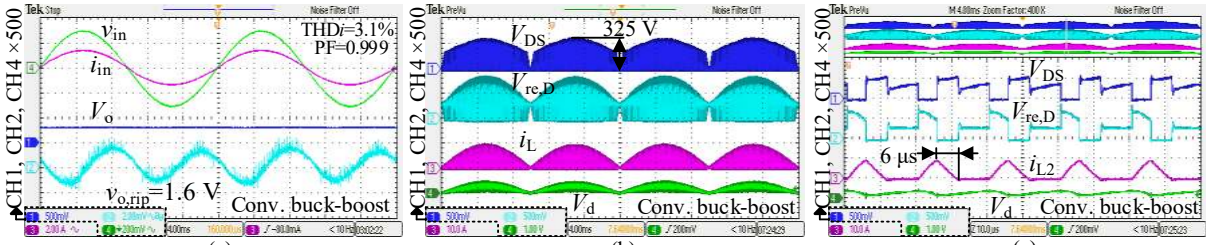

Fig. 22. Experimental waveforms of the conventional buck-boost at the 110-Vac input voltage: (a) input voltage $v_{\rm in}$ [100 V/div], input current $i_{\rm in}$ [2 A/div], output voltage $V_{\rm o}$ [250 V/div], output voltage ripple $v_{\rm o,rip}$ [1 V/div], and time [4 ms/div], (b) reverse voltages $V_{\rm DS}$, $V_{\rm re,D}$ [250 V/div], input voltage after diode bridge $V_{\rm d}$ [500 V/div], inductor currents $i_{\rm L}$ [10 A/div], and time [4 ms/div], and (c) zoom-in of (b), time [10 μs/div].

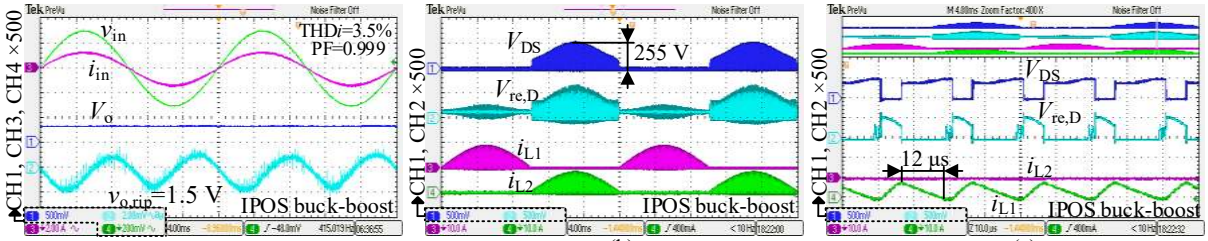

Fig. 23. Experimental waveforms of the IPOS buck-boost at the 110-Vac input voltage: (a) input voltage $v_{\rm in}$ [100 V/div], input current $i_{\rm in}$ [2 A/div], output voltage $V_{\rm o}$ [250 V/div], output voltage ripple $v_{\rm o,rip}$ [1 V/div], and time [4 ms/div], (b) reverse voltages $V_{\rm DS}$, $V_{\rm re,D}$ [250 V/div], inductor currents $i_{\rm L1}$, $i_{\rm L2}$ [10 A/div], and time [4 ms/div], and (c) zoom-in of (b), time [10 μs/div].

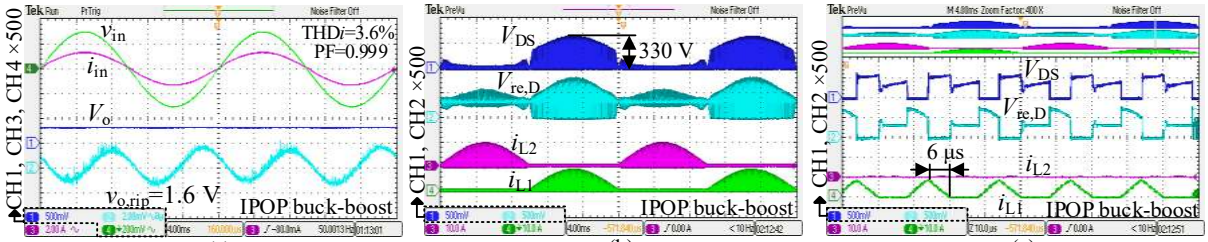

Fig. 24. Experimental waveforms of the IPOP buck-boost at the 110-Vac input voltage: (a) input voltage $v_{\rm in}$ [100 V/div], input current $i_{\rm in}$ [2 A/div], output voltage $V_{\rm o}$ [250 V/div], output voltage ripple $v_{\rm o,rip}$ [1 V/div], and time [4 ms/div], (b) reverse voltages $V_{\rm DS}$, $V_{\rm re,D}$ [250 V/div], inductor currents $i_{\rm L1}$, $i_{\rm L2}$ [10 A/div], and time [4 ms/div], and (c) zoom-in of (b), time [10 μs/div].

heavy load conditions (cf., Fig. 20).

Besides, the dynamic performance of the IPOS buck-boost is tested to show the voltage auto-balance between the two output capacitors and the closed-loop control effectiveness. Fig. 25 presents the experimental waveforms. It can be observed in Fig. 25 that the converter achieves equal capacitor voltages $V_{\rm C1}$ and $V_{\rm C2}$ (CH2 and CH4) in steady-state. After the load transitions, $V_{\rm o}$, $V_{\rm C1}$ and $V_{\rm C2}$ can remain stable.

VI. Conclusion

Bridgeless topology simplification guidelines are proposed to systematically simplify the dual-converter cell-based IPOP and IPOS bridgeless topologies to identify, category, and derive different bridgeless topology families. Meanwhile, the simplification methods are applied to the exemplified converter cells to show how the simplified topologies, categorized as S-IPOP, S-I-IPOS, and S-II-IPOS (cf., Fig. 2∼Fig. 6). Moreover, combining the state-of-the-art bridgeless topologies, these obtained simplified topologies are reviewed in comparison with their original IPOP and IPOS topologies and their performance discussions are presented in Section II-D. Besides, several

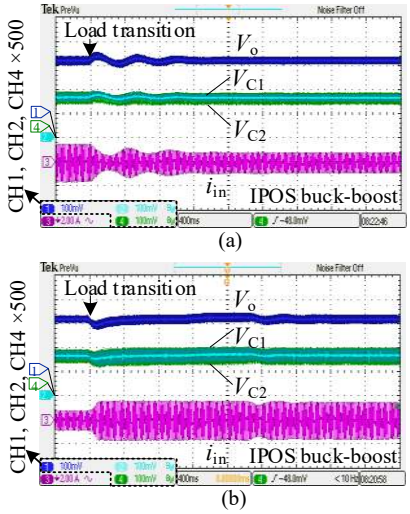

Fig. 25. Dynamic tests at the 110-Vac input voltage (output voltage $V_{\rm o}$ [50 V/div], capacitor voltages $V_{\rm C1}$, $V_{\rm C2}$ [50 V/div], input current $i_{\rm in}$ [2 A/div], and time [400 ms/div]): (a) 100 W to 50 W and (b) 50 W to 100 W.

special cases of the topology simplifications are given to explain why and how they are modified.

Additionally, based on the same design specifications, a consistent design procedure is proposed for a fair quantitative topology benchmarking, which only includes the same series components in the database and considers each component's cost, thermal, and electrical models to conduct component selections in the compared topologies. As case studies, given the penalty of using tapped inductors in the S-I-IPOS and S-II-IPOS buck-boost (cf., Section II-D), only the IPOP buck-boost (also seen as S-IPOP buck-boost) and IPOS buck-boost, along with the conventional one are selected and compared by applying the consistent design. The obtained benchmarking results imply that among the compared topologies, the IPOP buck-boost has the minimum volume and lowest power losses at the rated power. However, the component cost of the conventional buck-boost is only around 63% of the IPOS and IPOP buck-boost. Finally, tests of the three prototypes verify the theoretical analysis.

REFERENCES

[1] Q. Huang and A. Q. Huang, "Review of GaN totem-pole bridgeless PFC," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 187–196, Sep. 2017.

[2] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 427–435, Feb. 2011.

[3] L. Huber, Y. Jang, and M. M. Jovanović, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May. 2008.

[4] F. Musavi, W. Eberle, and W. G. Dunford, "A high-performance single-phase bridgeless interleaved PFC converter for plug-in hybrid electric vehicle battery chargers," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1833–1843, Jul./Aug. 2011.

[5] B. Huang, G. Torrico, X. Ma, and Y. Liang, "High efficiency telecom rectifier designed for wireless communication networks," in *Proc. Int. Telecom. Energy Conf.*, pp. 1–6, 2011.

[6] V. Bist and B. Singh, "An adjustable-speed PFC bridgeless buck-boost converter-fed BLDC motor drive," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2665–2677, Jun. 2014.

[7] H. Ma, J.-S. Lai, C. Zheng, and P. Sun, "A high-efficiency quasi-single-stage bridgeless electrolytic capacitor-free high-power AC-DC driver for supplying multiple LED strings in parallel," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5825–5836, Aug. 2016.

[8] Z. Chen, P. Davari, and H. Wang, "Single-phase bridgeless PFC topology derivation and performance benchmarking," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9238–9250, Sep. 2020.

[9] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," *IEEE Trans. Power Electron.*, vol. 56, no. 4, pp. 1147–1157, Apr. 2009.

[10] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "New efficient bridgeless Cuk rectifiers for PFC applications," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3292–3301, Jul. 2012.

[11] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, "New bridgeless DCM sepic and Cuk PFC rectifiers with low conduction and switching losses," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 873–881, Mar. 2011.

[12] H.-Z. Yang, H.-W. Chiang, and C.-Y. Chen, "Implementation of bridgeless Cuk power factor corrector with positive output voltage," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 3325–3333, Jul./Aug. 2015.

[13] B. Zhao, A. Abramovitz, and K. Smedley, "Family of bridgeless buck-boost PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6524–6527, Dec. 2015.

[14] Y. Jang and M. M. Jovanović, "Bridgeless high-power-factor buck converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 602–611, Feb. 2011.

[15] X. Lin and F. Wang, "New bridgeless buck PFC converter with improved input current and power factor," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 7730–7740, Oct. 2018.

[16] Z. Chen, B. Liu, P. Davari, and H. Wang, "Efficiency enhancement of bridgeless buck-boost PFC converter with unity PF and DC split to reduce voltage stresses," in *Proc. Ann. Conf. Ind. Electron. Soc.*, pp. 1187–1192, 2018.

[17] J.-W. Shin, S.-J. Choi, and B.-H. Cho, "High-efficiency bridgeless flyback rectifier with bidirectional switch and dual output windings," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4752–4762, Sep. 2014.

[18] D. D. C. Lu and W. Wang, "Bridgeless power factor correction circuits with voltage-doubler configuration," in *Proc. Power Electron. Drive Syst.*, pp. 1037–1042, 2011.

[19] J. C. Salmon, "Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase AC supplies and using either single or split DC rail voltage outputs," in *Proc. Appl. Power Electron. Conf. Expo.*, pp. 473–479, 1995.

[20] J. C. Salmon, "Circuit topologies for single-phase voltage-doubler boost rectifiers," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 521–529, Oct. 1993.

[21] J. W. Kolar, J. Biela, and J. Minibock, "Exploring the pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2% efficiency vs. 7kW/din3 power density," in *Proc. Int. Power Electron. Motion Control Conf.*, pp. 1–21, 2009.

[22] Y.-S. Kim, B.-K. Lee, and J. W. Lee, "Topology characteristics analysis and performance comparison for optimal design of high efficiency PFC circuit for telecom," in *Proc. Int. Telecomm. Energy Conf.*, pp. 1–7, 2011.

[23] V. Nithin, P. S. Priya, R. Seyezhai, K. Vigneshwar, and N. S. Sumanth, "Performance evaluation of bridgeless and phase shifted semi bridgeless interleaved boost converters (IBCS) for power factor correction," in *Proc. Sustain. Energy Int. Syst.*, pp. 119–124, 2013.

[24] F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "Evaluation and efficiency comparison of front end AC-DC plug-in hybrid charger topologies," *IEEE Trans. Smart Grid*, vol. 3, no. 1, pp. 413–421, Mar. 2012.

[25] M. Mirjafari, S. Harb, and R. S. Balog, "Multiobjective optimization and topology selection for a module-integrated inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4219–4231, Aug. 2015.

[26] R. M. Burkart and J. W. Kolar, "Comparative life cycle cost analysis of Si and SiC PV converter systems based on advanced η-ρ-σ multiobjective optimization techniques," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4344–4358, Jun. 2017.

[27] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5515–5527, Dec. 2013.

[28] S. Busquets-Monge, J.-C. Crebier, S. Ragon, E. Hertz, D. Boroyevich, Z. Gurdal, M. Arpilliere, and D. K. Lindner, "Design of a boost power factor correction converter using optimization techniques," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1388–1396, Nov. 2004.

[29] D. Damasceno, L. Schuch, and J. R. Pinheiro, "Design procedure to minimize boost PFC volume concerning the trade-offs among switching frequency, input current ripple and soft-switching," in *Proc. Power Electron. Spec. Conf.*, pp. 2333–2338, 2005.

[30] K. Raggl, T. Nussbaumer, G. Doerig, J. Biela, and J. W. Kolar, "Comprehensive design and optimization of a high-power-density single-phase boost PFC," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2574–2587, Jul. 2009.

[31] Infineon Tech., "CoolMOS$^{\mathrm{TM}}$ SJ MOSFETs selection guide, common CoolMOS$^{\mathrm{TM}}$ applications and topologies," *Infineon Tech., Munich, DE*, 2019. [Online].

[32] R. Burkart and J. W. Kolar, "Component cost models for multi-objective optimizations of switched-mode power converters," in *Proc. Energy Conv. Congr. Expo.*, pp. 2139–2146, 2013.

[33] Y. Zhang, Master's thesis.

[34] X. Liu, J. Xu, Z. Chen, and N. Wang, "Single-inductor dual-output buck-boost power factor correction converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 943–952, Feb. 2015.

[35] H. Wu, S.-C. Wong, C. K. Tse, S. Y. R. Hui, and Q. Chen, "Single-phase LED drivers with minimal power processing, constant output current, input power factor correction, and without electrolytic capacitor," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6159–6170, Jul. 2018.

[36] Z. Chen, P. Davari, and H. Wang, "A bridgeless buck-flyback PFC converter with high PF and dead angles eliminated," in *Proc. Power Electron. ECCE Asia*, pp. 1420–1427, 2019.

[37] G. Spiazzi and S. Buso, "Power factor preregulators based on combined buck-flyback topologies," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 197–204, Mar. 2000.

[38] M. O. Badawy, Y. Sozer, and J. A. De Abreu-Garcia, "A novel control for a cascaded buck-boost PFC converter operating in discontinuous capacitor voltage mode," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4198–4210, Jul. 2016.

[39] M. Mahdavi and H. Farzaneh-Fard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4153–4160, Sep. 2011.

[40] M. Mahdavi and H. Farzaneh-Fard, "Bridgeless Cuk power factor correction rectifier with reduced conduction losses," *IET Power Electron.*, vol. 5, no. 9, pp. 1733–1740, Nov. 2012.

[41] Z. Ouyang, Z. Zhang, O. C. Thomsen, and M. A. E. Andersen, "Planar-integrated magnetics module (PIM) in hybrid bidirectional DC-DC converter for fuel cell application," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3254–3264, Nov. 2011.

[42] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Magnetic integration of the LCL filter in grid-connected inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1573–1578, Apr. 2014.

[43] H. Ye, Z. Yang, J. Dai, C. Yan, X. Xin, and J. Ying, "Common mode noise modeling and analysis of dual boost PFC circuit," in *Proc. Int. Telecomm. Energy Conf.*, pp. 575–582, 2004.

[44] K. Raggl, T. Nussbaumer, and J. W. Kolar, "Guideline for a simplified differential-mode EMI filter design," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1031–1040, Mar. 2010.

[45] T. Nussbaumer, K. Raggl, and J. W. Kolar, "Design guidelines for interleaved single-phase boost PFC circuits," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2559–2573, Jul. 2009.

[46] Infineon Appl. Note, "An-v02-00-en: PFC boost converter design guide 1200 W design example," *Infineon Tech., Munich, DE*, 2016. [Online].

[47] Infineon Appl. Note, "An-201708-pl52-025: High-efficiency 3 kW bridgeless dual-boost PFC demo broad," *Infineon Tech., Munich, DE*, 2017. [Online].

[48] Magnetics Technical Documents, "Power cores catalog 2017," *Magnetics, Pittsburgh, PA, US*, 2017. [Online].

[49] V. Vlatković, D. Borojević, and F. C. Lee, "Input filter design for power factor correction circuits," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 199–205, Jan. 1996.

[50] Infineon Tech., "CoolSiC$^{\mathrm{TM}}$ -revolution to rely on, SiC solutions enabling radical new product designs with best system cost-performance ratio," *Infineon Tech., Munich, DE*, 2017. [Online].

[51] Aavid, "Aavid board level heatsink catalog," *Boyd Co., Pleasanton, CA, US*, [Online].

[52] Ohmite, "P series heatsinks forged pin fin heatsink for TO-220 and TO-264 devices," *Ohmite Manufacturing Co., Warrenville, IL, US*, [Online].

[53] Vishay Intertechnology Inc., "Rectifiers," *Vishay Intertechnologoy Inc., Malvern, PA, US*, 2017, [Online].

[54] Infineon Tech., "SiC Silicon Carbide diode 5th generation thinQ! 650 V SiC schottky diode IDH16G65C5," *Infineon Tech., Munich, DE*, 2012. [Online].

[55] H. Wang, "Capacitive DC links-design, control and its impact on the reliability of power electronic systems," Ph.D. dissertation, AAU, Aalborg, DK, 2018.

[56] Vishay Intertechnology, Inc., "Device application note AN608A: power MOSFET basics: understanding gate charge and using it to assess switching performance," *Vishay Intertechnology, Inc., Malvern, PA, US*, 2016, [Online].

[57] W. Konrad, G. Deboy, and A. Muetze, "A power supply achieving titanium level efficiency for a wide range of input voltages," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 117–127, Jan. 2017.

[58] Magnetics, "Curve fit equation tool," *Magnetics, Pittsburgh, PA, US*, 2018, [Online].

[59] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. Comp. Power Electron.*, pp. 36–41, 2002.

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