Broadband 300-GHz Power Amplifier MMICs in InGaAs mHEMT Technology

Laurenz John, Axel Tessmann, Arnulf Leuther, Philipp Neininger, *Student Member, IEEE*, Thomas Merkle, and Thomas Zwick, *Fellow, IEEE*

***Abstract*—In this article, we report on compact solid-state power amplifier (SSPA) millimeter-wave monolithic integrated circuits (MMICs) covering the 280–330-GHz frequency range. The technology used is a 35-nm gate-length InGaAs metamorphic high-electron-mobility transistor (mHEMT) technology. Two power amplifier MMICs are reported, based on a compact unit amplifier cell, which is parallelized two times using two different Wilkinson power combiners. The Wilkinson combiners are designed using elevated coplanar waveguide and air-bridge thin-film transmission lines in order to implement low-loss 70-Ω lines in the back-end-of-line of this InGaAs mHEMT technology. The five-stage SSPA MMICs achieve a measured small-signal gain around 20 dB over the 280–335-GHz frequency band. State-of-the-art output power performance is reported, achieving at least 13 dBm over the 286–310-GHz frequency band, with a peak output power of 13.7 dBm (23.4 mW) at 300 GHz. The PA MMICs are designed for a reduced chip width while maximizing the total gate width of 512 μm in the output stage, using a compact topology based on cascode and common-source devices, improving the output power per required chip width significantly.**

***Index Terms*—InGaAs mHEMT, solid-state power amplifier, sub-mm-wave operation.**

I. Introduction

In recent years, the interest in the submillimeter-wave frequency regime around 300 GHz for communication, radar, and imaging applications has been growing. As the power-gain cutoff frequencies ($f_{\max}$) of III-V HEMT and heterojunction bipolar transistor (HBT) devices have increased beyond 1 THz, broadband integrated circuits have been demonstrated at frequencies above 200 GHz. Both high-resolution radar/imaging and high-data-rate communication systems benefit from the large absolute bandwidths, which are achievable at these frequencies.

In order to develop high-dynamic-range transmit and receive solutions at submillimeter-wave frequencies, transistor technologies featuring high cutoff frequencies, good noise figures, and high levels of output power are required. In combination with a multilayer back-end-of-line (BEOL), highly integrated radio frequency (RF) front ends for frequencies above 200 GHz are feasible.

The InGaAs metamorphic high-electron-mobility transistor (mHEMT) technology used in this work has demonstrated state-of-the-art low-noise amplifiers [1], [2] as well as chipsets for broadband radar [3] and communication [4] applications with low noise figures above 100 GHz. Furthermore, a multilayer BEOL permits the realization of highly integrated front ends including multiplier, mixing, and amplifier circuits on a single-chip front end as demonstrated with the integrated 220–260-GHz InGaAs mHEMT radar front end in [3].

The generation of high RF-power levels, however, has been an issue of InGaAs mHEMT devices, as the bias voltage for safe long term operation is typically in the range of 1.0–1.5 V, which is limiting the power density on device level. In comparison, over the frequency band of 200–350 GHz, the highest output power levels have been reported by solid-state power amplifier (SSPA) millimeter-wave monolithic integrated circuits (MMICs) realized in InP HBT and InP HEMT technologies [5]–[10] biased at 1.8–2.2 V. In [5], 17–24-dBm output power was reported between 180–265 GHz and at a narrow frequency band around 300 GHz, up to 13.5 dBm has been demonstrated in [7], both using a 250 nm InP HBT technology. Broadband InGaAs mHEMT based SSPA MMICs, on the other hand, have reported up to 6.8–8.6-dBm of output power over the 280–320-GHz frequency band in [11].

In this article, we report on broadband SSPA MMICs with more than 13-dBm output power over the 284–310-GHz frequency band, using a 35-nm InAlAs/InGaAs mHEMT technology. The motivation for the development of SSPAs in this HEMT technology is the subsequent integration in broadband multi-functional radar and communication systems and MMICs [4], [12], [13]. State-of-the-art 300-GHz imaging [12] and communication [14], [15] systems implemented in this technology are currently operating with output power levels around 5 dBm, using the PA described in [32]. In order to increase the operating distance of these systems, which is typically below 50 m, and

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L. John, A. Tessmann, A. Leuther, P. Neininger, and T. Merkle are with the Fraunhofer Institute for Applied Solid State Physics IAF, 79108 Freiburg, Germany (e-mail: laurenz.john@iaf.fraunhofer.de; axel.tessmann@iaf.fraunhofer.de; Arnulf.Leuther@iaf.fraunhofer.de; philipp.neininger@iaf.fraunhofer.de; thomas.merkle@iaf.fraunhofer.de).

T. Zwick is with the Institute of Radio Frequency Engineering and Electronics, Karlsruhe Institute of Technology (KIT), 76131 Karlsruhe, Germany (e-mail: thomas.zwick@kit.edu).

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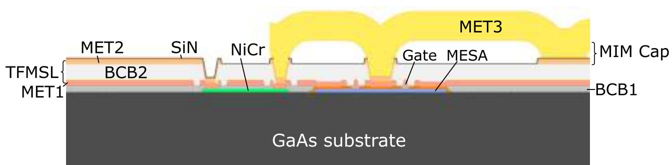


Fig. 1. Layer stack of Fraunhofer IAF's 35-nm InGaAs mHEMT technology with three metal layers and air-bridge technology.

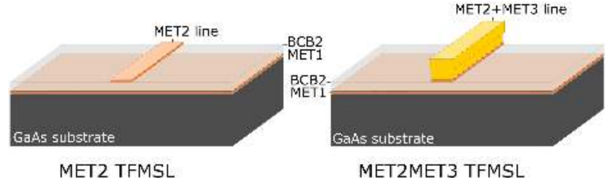


Fig. 2. TFMSL interconnections which are typically used in Fraunhofer IAF's three-layer BEOL process including the top metal layer in air-bridge technology.

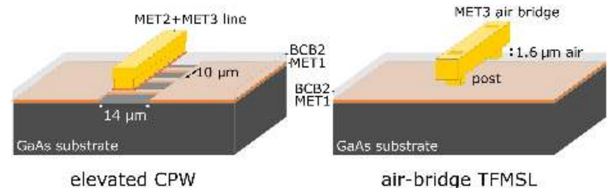


Fig. 3. Elevated CPW (left) and thin-film air-bridge (right) transmission lines, which permit the implementation of low-loss high-impedance transmission lines.

demonstrate real-world scenarios at distances well above 100 m, the 300-GHz output power performance on MMIC level needs to be improved above 20 mW, which is demonstrated in this work.

When considering packaging and on-chip integration of PA circuits, there are many reasons to strive for very compact dimensions of the PA circuit. Due to high losses of on-chip transmission lines at submillimeter wave frequencies, a compact PA design is vital to reduce unnecessary losses in the power combining network. Furthermore, in order to permit the integration of the PA into multifunctional transmit MMICs as well as facilitate the packaging into waveguide modules, e.g., avoiding cavity resonances in the cavity above the MMIC, the width of the PA MMIC should also be as small as possible. At 300 GHz, for example, cavity modes can theoretically exist and be excited if the width of the cavity is not below 500 μm [16]. Increasing the width of the MMIC beyond this limit, will possibly increase the expense for MMIC packaging, if additional measures for cavity-mode suppression are needed. The PA cores of this work, therefore, were designed for a reduced chip width while maximizing the total number of gate fingers in the output stage, and hence, maximizing the achievable output power at the required chip width.

In the following section, we first give a brief overview on the 35-nm mHEMT technology used in this work. In Sections III to V, the design of two PA MMICs is described, based on a compact unit amplifier cell, which is parallelized using Wilkinson power combiners. The on-wafer measured performance of the PA circuits is shown in Section VI and a detailed discussion and comparison to the state of the art is given in Section VII.

II. 35-nm mHEMT Technology

The technology used in this work is Fraunhofer IAF's $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ mHEMT technology with 35-nm gate length. The metamorphic HEMT structure is grown by molecular beam epitaxy on 100-mm semi-insulating GaAs wafers. To adapt the lattice constant, a metamorphic buffer with a linear $In_xAl_{0.48}Ga_{0.52-x}As$ ($x = 0 \rightarrow 0.52$) transition is grown. The active devices are defined by a two step electron beam lithography and are encapsulated in benzocyclobutene (BCB1 in Fig. 1). A detailed description of the front-end-of-line process is given in [17].

The mHEMT devices feature an increased gate-drain recess, which allows a drain-source voltage for power amplifier applications around 1.5 V. The off-state breakdown voltage ($BV_{off-state}$) of this technology variant is above 4 V. This 35-nm mHEMT technology features an f_T above 500 GHz and an f_{max} exceeding 1 THz. The maximum transconductance is 2500 mS/mm and the maximum drain current density is 1300 mA/mm.

The cross section and available layers of the front side process, which is used in this work is shown in Fig. 1. The BEOL process includes 50-$\Omega/\square$ NiCr thin film resistors and an 80-nm-thick chemical vapor deposition (CVD) deposited SiN layer used for on-wafer metal–insulator–metal (MIM) capacitors. Three metal layers (MET1-MET3) are available for the design of compact matching networks with thin-film microstrip line (TFMSL) interconnects on the wafer front side. The electron beam evaporated Au-based first and second metal layers are defined in a lift-off process. MET3 is a 2.7-μm-thick plated Au layer in air-bridge technology. The transmission lines, which are realized with this three-layer metal stack and are used for the wiring in this work, are discussed in the following section.

III. Thin-Film Transmission Lines

The relevance of a compact PA design regarding the feasibility of packaging into waveguide modules, on-chip integration as well as efficient power combining was introduced in Section I. In order to realize a compact PA core, independent of backside processing and the substrate height of the GaAs substrate, compact multifinger cascode and common-source (CS) cells have been developed, using TFMSL interconnections for the matching networks.

TFMSL wiring permits a compact matching network implementation and the accurate in-phase matching of parallelized multifinger devices in close proximity, realizing broadband PA MMICs with reduced chip width. These advantages of using thin benzocyclobutene (BCB) layers for TFMSL wiring has been described and investigated for GaAs pHEMT [18] and InP HEMT [19], [20] technologies as well as this InGaAs mHEMT technology [11], [21], [22] in detail previously.

Figs. 2 and 3 show the cross section of four different thin-film transmission lines, which are used for wiring in the matching and power combining networks in this work. These interconnections differ strongly in their respective range of feasible characteristic

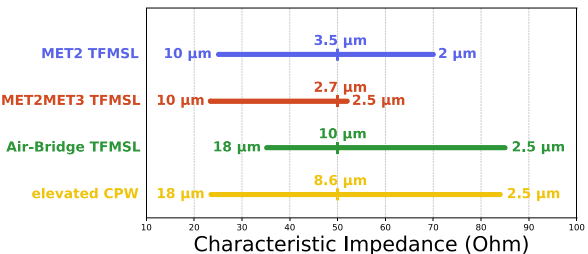


Fig. 4. Simulated feasible impedance range of the four transmission lines depicted in Figs. 2 and 3. The line width, which is required for the minimum impedance, the maximum impedance as well as a 50-Ω line impedance, is also shown in µm.

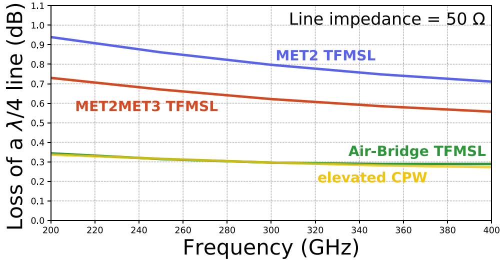


Fig. 5. Loss of the thin-film transmission lines depicted in Figs. 2 and 3 for a length of λ/4. The loss is normalized to a quarter wavelength at the respective frequencies. The line impedance of each transmission line is 50 Ω.

impedances as well as insertion loss, as depicted in Figs. 4 and 5, respectively, and are discussed in the following.

The TFMSL interconnections depicted in Fig. 2 (MET2 TFMSL and MET2MET3 TFMSL), which are implemented in the matching networks of the reported PA circuits, have been widely used for the design of compact MMICs in this InGaAs mHEMT technology for a wide variety of applications [22]–[24]. MET1 is implemented as substrate shielding dc and RF ground and the TFMSL signal line is routed in MET2, using the 1.4-μm-thick BCB layer (BCB2) between MET1 and MET2 as dielectric substrate. MET3 can additionally be used to increase the conductor thickness of the signal line in order to reduce the losses and increase the current carrying capability, as depicted in Fig. 2 on the right (MET2MET3 TFMSL).

Realizing high impedance as well as low-loss transmission lines is, however, an issue for the TFMSL interconnections depicted in Fig. 2. Due to the low thickness of the BCB2 layer, the required width of a 50-Ω transmission line is only 3.5 μm for the MET2 TFMSL and 2.7 μm including the MET3 layer, respectively (see Fig. 4). The insertion loss of a quarter wavelength transmission line is, as a result of the narrow line width, in the range of 0.6 to 0.8 dB around 300 GHz (see Fig. 5), which significantly reduces the efficiency of power combining networks in this wiring environment. Furthermore, the feasible impedance range of the MET3-reinforced TFMSL is limited by the 2.5-μm minimum-width design rule for MET3, which limits the maximum feasible line impedance to 53 Ω (see Fig. 4).

In order to decrease the insertion loss and realize transmission lines with higher characteristic line impedances, which is necessary for the required impedance transformation in most 50-Ω power combining concepts, the two transmission lines shown in Fig. 3 are investigated to increase the combining efficiency of the power combiners in Section V. By partially removing the MET1 ground plane underneath the MET2 layer, as depicted on the left in Fig. 3, an elevated coplanar waveguide (CPW) with increased distance between RF ground and TFMSL signal line is realized, permitting the implementation of interconnections with line impedances well above 70 Ω .

Similar elevated CPW transmission lines have been studied for GaAs and silicon substrates in [25]–[27], providing higher wave impedances and lower attenuation compared with conventional CPWs. The simulated insertion loss of this elevated CPW is reduced to 0.3 dB for a line length of λ/4 and 50-Ω line impedance. The ground-to-ground MET1 spacing is 14 μm in this example. In order to permit the implementation of bends while preventing odd-mode propagation and improve the shielding of the GaAs substrate, the two ground planes are connected using 1-μm wide stripes in a distance of 10 μm. Both the 14-μm ground-to-ground spacing as well as the spacing of the stripes are chosen based on values, which are typically used in 300-GHz CPW circuits in this technology [17]. Using these dimensions, the implementation of both low-loss interconnections as well as comparatively compact transmission-line elements like bends, for example, is feasible.

The same advantages of increased impedance range and low insertion loss apply for the air-bridge TFMSL interconnection shown in Fig. 3 on the right. By using the additional 1.6-μm "air substrate," the substrate height of this air-bridge TFMSL is increased and, hence, high impedance transmission lines with low insertion loss are feasible. The number of posts, which are required to hold up the air bridge, is strongly dependent on the routing of the transmission line. The simulated data depicted in Fig. 5 is, therefore, considering an ideal transmission line without any posts. Air-bridge transmission lines have been previously reported in two-metal-layer BEOL technologies [27]–[30], typically requiring an opening in the MET1 ground plane for the posts of the air-bridge interconnection. Since the posts of the air-bridge TFMSL depicted in Fig. 3 are set on top of the BCB2 layer, the impact of the posts is strongly diminished and not considered in this section. The simulated insertion loss of this 50-Ω air-bridge TFMSL is 0.3 dB at 300 GHz, very similar to the elevated CPW.

Since the required area for signal routing is significantly increased for the elevated CPW and air-bridge TFMSL compared to the MET2 and MET2MET3 TFMSL, they are only implemented in the Wilkinson power combiners of the power amplifier MMICs discussed in Section V. Due to their better folding possibilities [22], the TFMSL interconnections are used for the design of the compact unit amplifier cell described in the following section.

IV. 300-GHz Unit Amplifier Design

In this section, the design of a compact 300-GHz unit amplifier cell (UA) is described. Section IV-A is focused on the design considerations of the compact unit amplifier topology, which

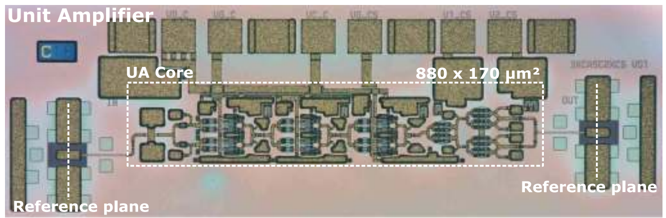


Fig. 6. Chip photograph of the fabricated unit amplifier MMIC. The required chip area of the 5-stage PA core with 8-finger cascode and CS PA cells is $0.17 \times 0.88\ \text{mm}^2$. The amplifier uses a CS output stage with two 8×16 μm-finger-width devices in parallel. The gate width of the three cascode stages is 8×10 μm.

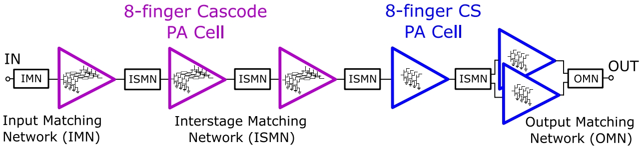


Fig. 7. Block diagram of the unit amplifier MMIC depicted in Fig. 6. The detailed schematic of the five-stage unit amplifier is shown in Fig. 8.

is parallelized in the following sections. The UA modeling is described in Section IV-B.

A. Unit Amplifier Design Considerations

Figs. 6 and 7 show the chip photograph and block diagram of the compact UA MMIC, respectively. The simplified circuit schematic of the five-stage amplifier cell is depicted in Fig. 8. The amplifier topology of the UA was developed based on the four-stage amplifier MMIC reported in [11], including optimized matching networks, as well as an additional CS output stage with two parallel 8×16 μm CS devices. The 8-finger cascode devices in the input stages are implemented to provide high gain, while the CS transistors in the output stage permit the maximization of the total gate width in the output stage, increasing the achievable output power at the given chip size. The design considerations of the UA topology shown in Fig. 6 are discussed in the following in detail.

Compared to CS transistors, devices in cascode configuration can provide larger levels of small-signal gain and are often used in mHEMT PA circuits [24], [32]. However, the classical cascode, where the gate of the CG transistor is shorted for RF frequencies, does not provide significantly larger output power levels than a CS transistor while maintaining a large-signal condition for save long-term operation. Since only the CG device contributes to the output voltage swing, an RF-shorted gate potential at the CG device can lead to large voltage swings in saturation, causing soft compression, and device degradation. In order to safely increase the output-power level of a PA cell in cascode configuration, the drain-source voltage of both the CS and the CG device have to be stacked and swing in phase, which is known as stacked-FET and series-connected devices in literature [9], [37].

At a given dc-bias point, the cascode can provide high small-signal gain, but under large-signal operation, both the CS and the CG transistor must contribute to the output voltage swing in order to prevent soft compression. In order to identify the appropriate geometry of the cascode cells of the UA, two design parameters are considered: the size of the shunt MIM capacitors C_{SHUNT} at the CG transistor and the length L_{MSL} of the TFMSL interconnection between the CS and the CG device.

Fig. 9 shows the simulated MSG/MAG and stability factor of a 2×10-μm cascode for different values of L_{MSL} and C_{SHUNT}. For shunt-capacitor values larger than 200 fF, the cascode is only conditionally stable around 300 GHz and the MSG is independent of the length L_{MSL}, at least in the considered range of up to 40 μm. In this case, the MSG of the cascode at 300 GHz is 15 dB, compared to the 7-dB MSG of a CS transistor. For $C_{\mathrm{SHUNT}} < 200$ fF, the cascode is unconditionally stable over a certain frequency band around 300 GHz, depending on the values of L_{MSL} and C_{SHUNT}.

The simulated $\mathrm{OP}_{3\mathrm{dB}}$ 3-dB gain compression power for a 2×10-μm cascode at 300 GHz is depicted in Fig. 10. The length of the microstrip line L_{MSL} was swept from 10–40 μm, and the range of C_{SHUNT} is 30–200 fF. For large values of C_{SHUNT} and a short interconnection between the CS and CG device ($L_{\mathrm{MSL}} = 10$ μm), the achieved output power performance of 4.63 dBm was found to be not significantly improved compared to a 2×10-μm CS single device, which delivers a maximum $\mathrm{OP}_{3\mathrm{dB}}$ of 4.5 dBm at 300 GHz. However, by optimizing the values of C_{SHUNT} and L_{MSL} within the considered range, the output power can be increased by 1.8 dB ($\mathrm{OP}_{3\mathrm{dB}} = 6.44$ dBm) in simulation. This increased output power performance complies with the prospects and limitations of stacked HEMT devices described in [38].

Based on these considerations, the PA topology and 8-finger-cascode geometry of this work is chosen. It is important to note that Fig. 10 only shows the exemplary cascode performance under large-signal operation at 300 GHz. In order to meet the given output power and linearity objectives not only in a narrow frequency range, the dependency of the large-signal performance on the cascode geometry has to be considered over the full frequency band of interest.

As a result of the analysis previously, multifinger cascode devices are only used in the input stages, providing high gain over the targeted 280–350-GHz frequency band. The capacitance of C_{SHUNT} is chosen to be 100 fF and the length of the interconnection between the CS and CG device (L_{MSL}) is 20 μm. This way, the cascode is unconditionally stable with around 12-dB MAG over the 280–350-GHz frequency band (see Fig. 9), representing a good tradeoff between high gain and output-power performance. Smaller C_{SHUNT} values would reduce the gain significantly, limiting the gain benefit of the cascode. With a longer transmission line L_{MSL} the cascode is only conditionally stable at 350 GHz and a constant output-power performance cannot be achieved over the full frequency band of interest in simulation.

The objective of the UA design was the development of a very compact PA core and consequently, to achieve high output power per required chip width. To achieve this, the compact 8-finger cascode cell depicted in Fig. 11 was developed. The minimum required width of a cascode, however, is limited by the size of the shunt capacitors at the CG devices. In comparison, two parallel

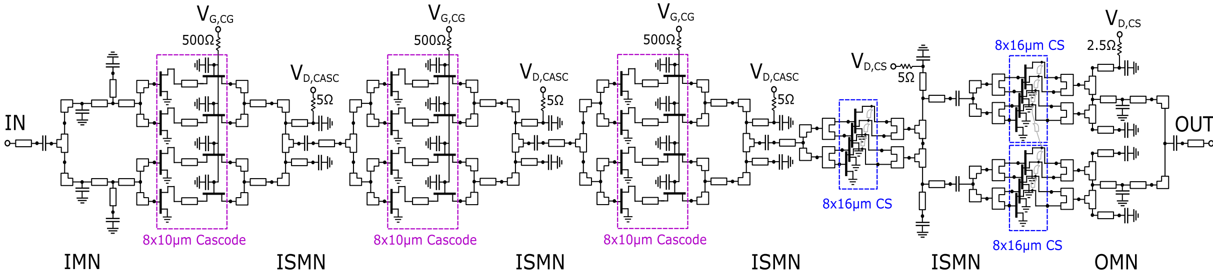


Fig. 8. Simplified schematic of the five-stage UA cell. A more detailed schematic of the 8-finger cascode and CS devices is depicted in Figs. 11 and 12, respectively, including the gate biasing as well as stabilization elements.

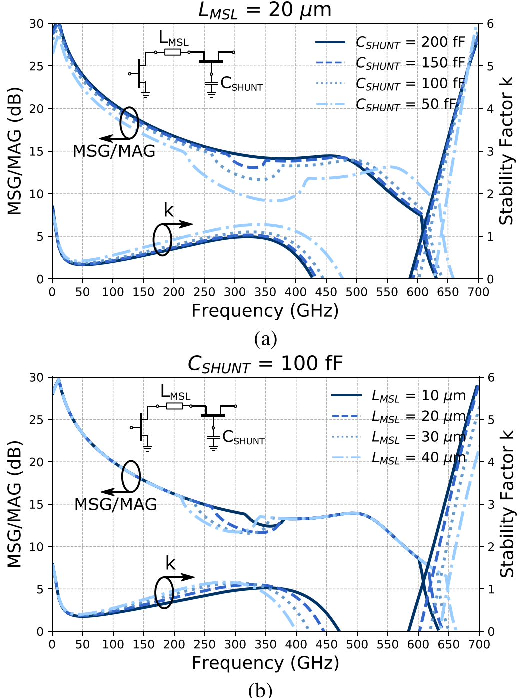


Fig. 9. Simulated MSG/MAG and stability factor of a 2-finger cascode with 10-µm finger width: (a) for different C_{SHUNT} values at $L_{\mathrm{MSL}} = 20$ µm, and (b) for different L_{MSL} values at $C_{\mathrm{SHUNT}} = 100$ fF.

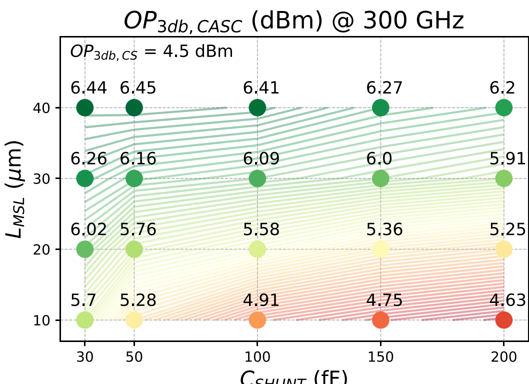


Fig. 10. Simulated $\mathrm{OP}_{3\mathrm{dB}}$ 3-dB gain compression output power of a 2-finger cascode with 10-μm finger width for different values of C_{SHUNT} and L_{MSL} at 300 GHz.

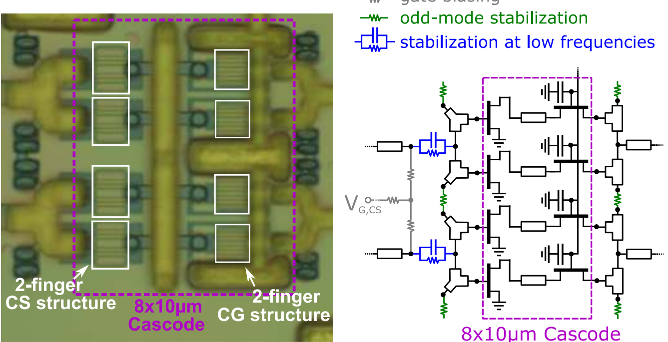


Fig. 11. Chip photograph and equivalent circuit of the 8-finger cascode PA cell with feeding structures.

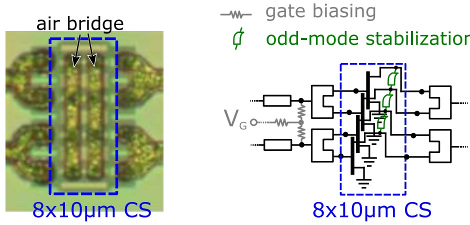


Fig. 12. Chip photograph and equivalent circuit of the 8-finger CS PA cell with feeding structures.

8-finger CS transistors (see Fig. 12) require approximately the same chip width as an 8-finger cascode cell as can be seen in the chip photograph of the UA in Fig. 6. For this reason, a CS output stage permits doubling the number of gate fingers in the output stage, compared to a cascode device. Since the cascode cannot provide the same level of output power as a CS device with twice the number of gate fingers, while providing enough gain, the UA topology depicted in Fig. 7 is used.

B. Compact PA Cell Modeling and Simulation

Figs. 11 and 12 show the close-up view of the 8-finger cascode and CS devices, respectively, as well as the detailed equivalent circuits. The 8-finger transistors of the UA are modeled by parallelizing four 2-finger transistors without feeding structures in close proximity. The feeding structures of the 2-finger devices are included in the EM-simulated multifinger transistor shell and

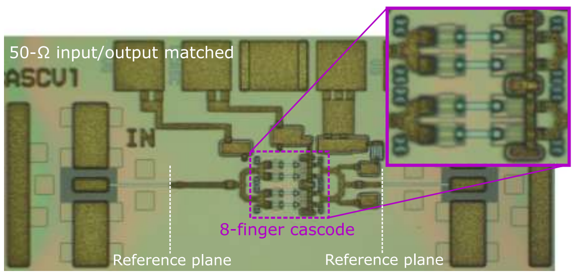


Fig. 13. Chip photographs of the prematched 8-finger cascode cell depicted in Fig. 11. Measured and simulated S-parameters are shown in Fig. 14.

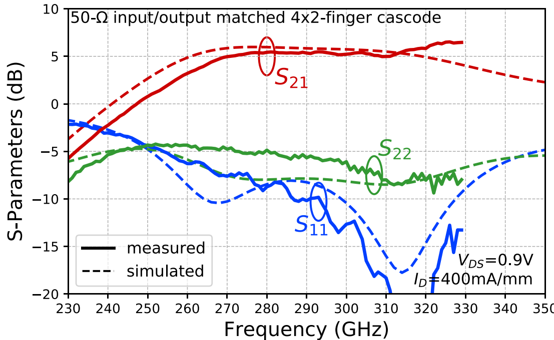


Fig. 14. Measured and simulated S-parameters of the prematched 8-finger cascode cell depicted in Fig. 13.

are optimized as a part of the matching networks. This permits an accurate in-phase feeding of the parallelized 2-finger devices and broadband matching at reduced chip width. Due to their most simple and symmetric device layout, 2-finger HEMT devices typically provide the largest bandwidths and transistor models with the best accuracy, compared to multifinger devices. This advantage of 2-finger devices was discussed in detail for this InGaAs mHEMT technology in [11]. The 2-finger transistor models, which are used to model the multifinger devices, are based on a multiport modeling approach with an electrical equivalent circuit model of the extrinsic transistor shell, which is based on the actual structure and layout of the transistor [33].

The chip photograph of a prematched 8-finger (4 × 2-finger) cascode cell is shown in Fig. 13. Measured S-parameters of the 50-Ω input/output matched 8-finger cascode cell are depicted in Fig. 14, showing good agreement between measurement and simulation. The measured small-signal gain of the compact 8-finger cascode device is in the range of 5–6 dB around 300 GHz.

The UA's TFMSL matching networks are fully EM simulated using keysight ADS momentum and CST microwave studio. Simplified models of the matching networks were first developed using momentum EM/circuit co-simulation in ADS, which allows for a time-efficient optimization of the design. The final implementation of the compact networks was simulated and optimized using CST, due to the increased accuracy provided by the three-dimensional EM solver. The load targets of the cascode stages were defined in large-signal load-pull simulations. For the 16-μm finger-width CS devices in the last two stages of the UA, gain-power tradeoff load impedances were defined considering

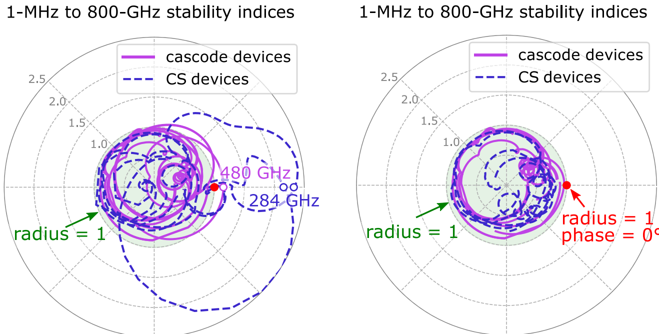


Fig. 15. Simulated stability indeces of the UA (a) without any circuit elements for stabilization and (b) including the stabilization elements depicted in Fig 11 and Fig. 12. The simulated frequency range is 1 MHz to 800 GHz. (a) w/o stabilization. (b) w/ stabilization.

large-signal load-pull simulations as well as *in situ* load-pull measurement data at 300 GHz [36].

In order to ensure stability and suppress possible odd-mode oscillations, stabilization elements have been implemented at the input of the first cascode stage as well as the output of all cascode and CS multifinger devices described previously. The implementation of air bridges between the drain fingers of multifinger CS transistors was investigated and described in detail in [22]. The same approach is used in the CS device depicted in Fig. 12, where the drain fingers are connected via two lines of parallel air bridges.

The layout of the 2-finger CG structure, which is implemented in the 8-finger cascode cell depicted in Fig. 11, was optimized to reduce the required chip area. As a result of this layout optimization, the implementation of air bridges between the drain fingers of the parallelized CG devices is not possible within the design rules of the process. Therefore, 5-Ω shunt resistors are connected to the parallel drain feeders of the cascode cells, as shown in Fig. 11. The low-frequency and odd-mode stabilization elements depicted at the cascode input in Fig. 11 are only implemented in the first cascode stage at the input of the UA, in order to improve the robustness of the design for future system integration.

The stability was simulated during the design process, using the S-probe stability analysis method described in [34] and [35]. Using this technique for circuit analysis, the stability index (product of reflection coefficients) is calculated and evaluated in simulation at each input and output of the active 2-finger devices. By checking the stability indices of the parallel devices against the oscillation criterion, odd-mode stability is ensured.

Fig. 15 shows the polar plots of the simulated 1-MHz to 800-GHz stability indices of the UA with and without the abovementioned odd-mode stabilization elements. Depicted are 12 stability indices, simulated at the input/output of one of the outer 2-finger devices of each stage. In order to ensure stability not only within the frequency band of interest, the critical point (1,0) must not be encircled at any given frequency [35]. This criterion is satisfied for the stabilized UA core, as depicted in Fig. 15(b). Without the implementation of air bridges, the CS stages show potential in-band instabilities around 284 GHz [see Fig. 15(a)]. Since the in-band stability of the cascode cells is

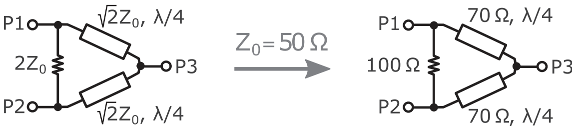


Fig. 16. Schematic of the 3-dB Wilkinson power divider/combiner for an arbitrary system impedance Z_0 (left) as well as for an system impedance of 50 Ω (right).

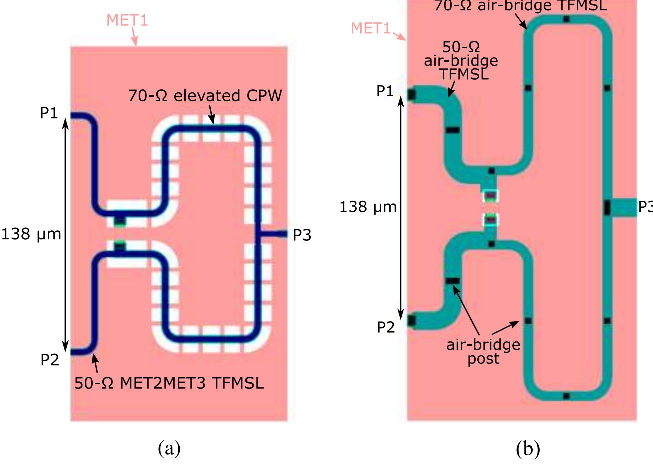


Fig. 17. Layouts of two Wilkinson power combiners, realized with (a) elevated CPW (Wilkinson1) and (b) air-bridge TFMSL (Wilkinson2).

ensured by the choice of C_{SHUNT} and L_{MSL} as described previously, the criterion for stability is only violated for frequencies around 480 GHz, if no measures for stabilization are taken. The implemented odd-mode stabilization, however, ensures stability up to frequencies above 650 GHz, which is the frequency range where the cascodes can potentially oscillate (stability factor k is below one in Fig. 9).

V. 300-GHz High-Power Amplifier MMICs

The parallelization of the UA cell described previously is realized using Wilkinson power combiners [31], which are providing the necessary isolation in order to prevent odd-mode oscillation and load tuning between the parallelized UA cells. This kind of power combiner realized with TFMSL interconnections has been widely used in InP HBT SSPA MMICs at frequencies around 240 GHz as well as 300 GHz [5]–[7], providing high levels of output power at the respective frequencies.

The schematic of a 3-dB Wilkinson power divider/combiner is depicted in Fig. 16. In the case of a 50-Ω system impedance, a characteristic impedance of approximately 70 Ω is required for the λ/4 lines of the Wilkinson combiner. Realizing this 70-Ω line impedance, while simultaneously achieving a low insertion loss, is an issue for the TFMSL interconnections, which are typically implemented in matching networks in this works BEOL, as discussed in Section III and shown in Figs. 4 and 5. Therefore, the elevated CPW and air-bridge TFMSL, which were introduced in Section III and permit the low-loss implementation of 70-Ω transmission lines, were used for the design of two Wilkinson power combiners, depicted in Fig. 17.

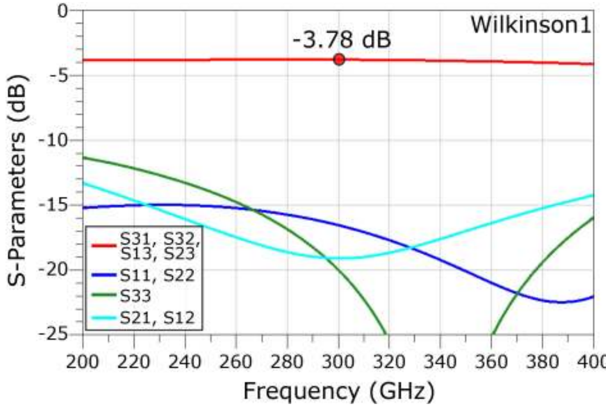


Fig. 18. Simulated S-parameters of the Wilkinson combiner Wikinson1.

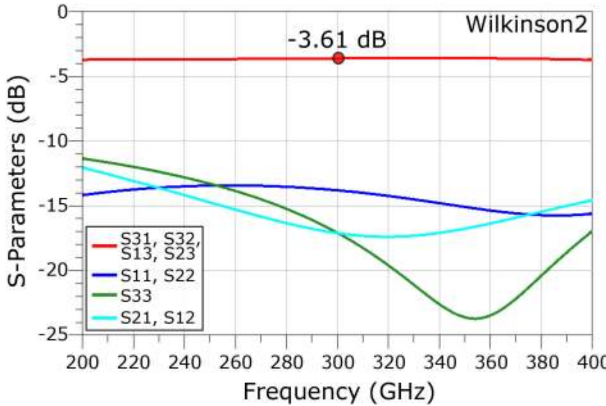


Fig. 19. Simulated S-parameters of the Wilkinson combiner Wikinson2.

The simulated S-parameters of the two Wilkinson combiners Wilkinson1 and Wilkinson2 are shown in Figs. 18 and 19, respectively. Wilkinson2, which is implemented using the air-bridge TFMSL, is achieving an insertion loss around 3.6 dB at 300 GHz, compared to the simulated 3.8-dB insertion loss of Wilkinson1. The insertion loss of the 70-Ω λ/4 transmission lines is in simulation around 0.3 dB. The main additional sources of the overall insertion loss of 0.6 to 0.8 dB are the 100-Ω isolation resistor as well as the 50-Ω line extensions at port 1 and port 2. Due to the finite size of the parallel isolation resistor, even for even-mode excitation, additional losses are introduced. The 50-Ω transmission line extensions are required to realize the 138-μm spacing between Port 1 and Port 2, which is the distance of the output ports of two parallel UA cores.

The input and output return loss of both combiners is better than 13 dB over the frequency band of interest above 260 GHz, while achieving at least 15–dB isolation between Port 1 and Port 2. The most critical part of the on-chip Wilkinson combiner design is the implementation of the 100-Ω isolation resistor, which is limiting the insertion loss as well as the simultaneous realization of a better input/output return loss and isolation. Ideally, the impact of the dimensions of this resistor and its connection to the λ/4 lines need to be as small as possible. By optimizing this crucial element of the Wilkinson combiners

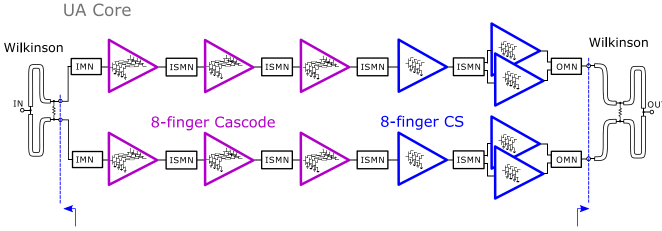
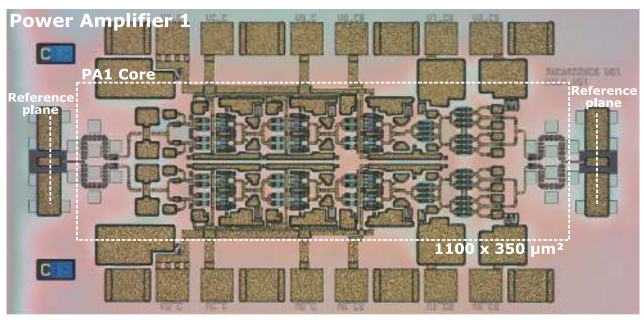
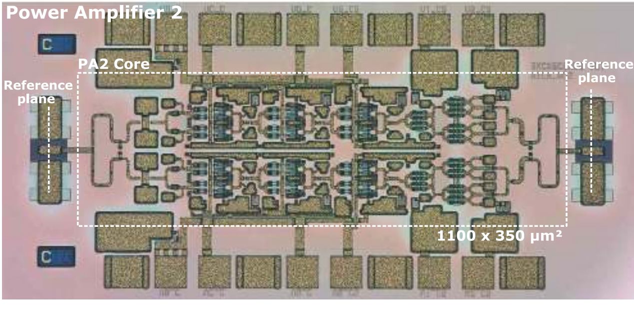


Fig. 20. Block diagram of the fabricated power amplifier MMICs PA1 and PA2, which are depicted in Fig. 21. The amplifiers use the UA topology of Fig. 7 and the Wilkinson power combiners of Fig. 17.



(a)



(b)

Fig. 21. Chip photographs of the fabricated PA MMICs PA1 and PA2. The required chip area of the 5-stage PA core is 0.35×1.1 mm^2. These amplifiers use the Wikinson power combiners shown in Fig. 17 to parallelize the UA cell depicted in Fig. 6. (a) Chip photograph of PA1. (b) Chip photograph of PA2.

depicted in Fig. 17, an improvement of the simulated return loss and isolation in Figs. 18 and 19 should be feasible.

Two high-power amplifier MMICs PA1 and PA2 have been developed and fabricated, based on the UA cell discussed in Section IV and the two Wilkinson power combiners Wilkinson1 and Wilkinson2. PA1 is using Wilkinson1 to parallelize the UA core, and PA2 was implemented using Wilkinson2. A corresponding block diagram of the five-stage amplifiers is depicted in Fig. 20, and 21 shows the chip photographs of both amplifier MMICs. Both PA cores require a total chip area of approximately 0.35 $\times$ 1.1 mm^2, including all matching networks and the first stage of shunt capacitors in the bias insertion network and excluding RF/dc-pads. The total gate width in the output stage, which is implemented with this topology on only 0.35-mm required chip width, is 512 μm.

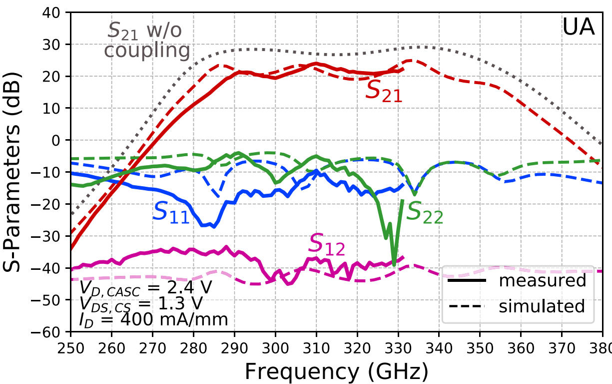


Fig. 22. Measured and simulated S-parameters of the 5-stage unit amplifier MMIC. The cascode stages are biased at 2.4 V supply voltage ($V_{\rm DS} \approx 1.2$ V) and $I_{\rm d} = 400$ mA/mm. The CS output stages are biased at $V_{\rm DS} = 1.3$ V and $I_{\rm d} = 400$ mA/mm. The dotted line shows the ideal simulated S_{21}, without considering the limited isolation of the measurement system. The dashed lines represent the simulation results considering the poor isolation between input and output.

VI. Measurement Results

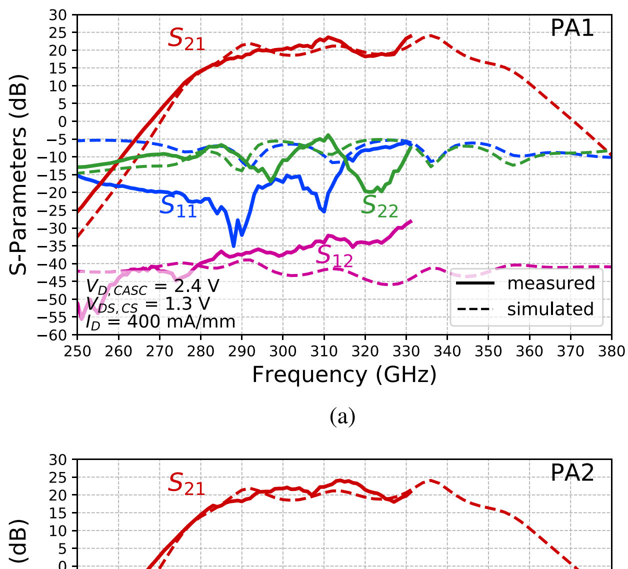
The on wafer 200–330-GHz S-parameter measurements were done using an Agilent N5224A PNA system and VDI WR-3.4 extension modules. The entire setup was calibrated to the probe tip of the RF-probes by performing a thru-reflect-line calibration, using an impedance standard substrate (ISS).

The measured *S*-parameters of the UA are depicted in Fig. 22. The unit amplifier was designed for the 280–350-GHz frequency range, showing a measured small-signal gain ripple of around 5 dB. This gain ripple is mainly caused by the poor isolation of the on-wafer measurement setup. Since the UA's measured S_{12} is only around −40 dB, the depicted periodic gain variation at gain levels above 20 dB can be observed. By including a simple model for the RF-probe overcoupling, a similar behavior is observed for the simulated *S*-parameters in Fig. 22. The measured *S*-parameters of PA1 and PA2 are depicted in Fig. 23. Both amplifiers achieve a measured small-signal gain around 20 dB for the frequency range above 290 GHz.

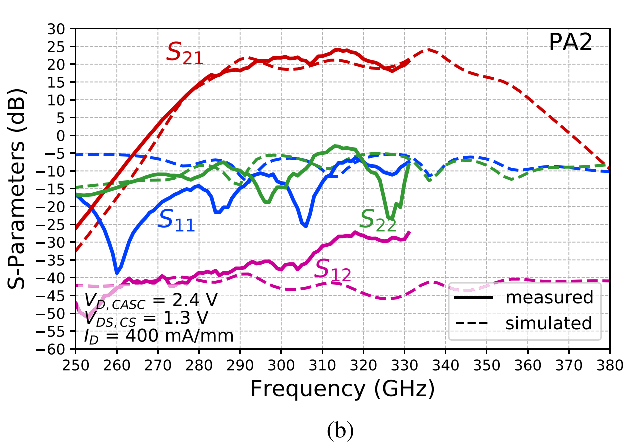
We also carried out on-wafer scalar power measurements, using in-house built frequency multiplier and amplifier modules to synthesize the input signal around 300 GHz. The output power of the PA MMICs was measured using an VDI Erickson PM5 power meter. The whole setup was calibrated to the probe tip of the RF probes, using an ISS.

Fig. 24 shows the measured transducer gain and output power versus frequency for CW operation of the UA. The frequency was swept from 280–328 GHz with 2-GHz step size at −5-dBm available source power. The CS devices in the output stages were biased with 1.3-V drain-source voltage at 400 mA/mm. The drain-supply voltage of the cascode stages is around 2.4 V ($V_{\rm DS} \approx 1.2$ V) at 400 mA/mm.

The UA's measured output power is in the range of 8 dBm to 9.7 dBm over the 285–328-GHz frequency range, measured at about 6-dB gain compression. The large-signal gain at this input power level is around 14–15 dB. The UA MMIC includes an 100-μm-long MET2 TFMSL port extension between the RF-pads



(a)



(b)

Fig. 23. Measured and simulated *S*-parameters of the 5-stage MMICs PA1 and PA2. The cascode stages are biased at 2.4 V supply voltage ($V_{\mathrm{DS}} \approx 1.2$ V) and $I_{\mathrm{d}} = 400$ mA/mm. The CS output stages are biased at $V_{\mathrm{DS}} = 1.3$ V and $I_{\mathrm{d}} = 400$ mA/mm. (a) *S*-parameters of PA1. (b) *S*-Parameters of PA2.

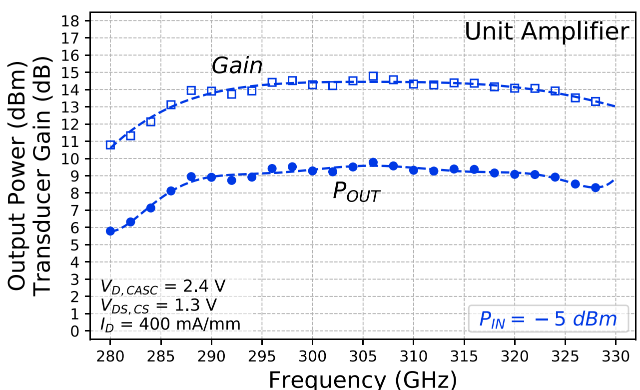


Fig. 24. CW measured transducer gain and output power of the UA MMIC between 280 and 328 GHz with 2-GHz step size at −5-dBm input power.

and the input/output of the UA core, as depicted in Fig. 6. This port extension is introducing additional losses of approximately 0.8–1.0 dB at the output, which can be omitted by moving the RF-pad closer to the output of the UA cell.

The measured transducer gain and output power of PA1 and PA2 are shown in Figs. 25 and 26, respectively, measured at a constant input power versus frequency. Depicted are the results at −5-dBm as well as at −2-dBm input power. The CS devices

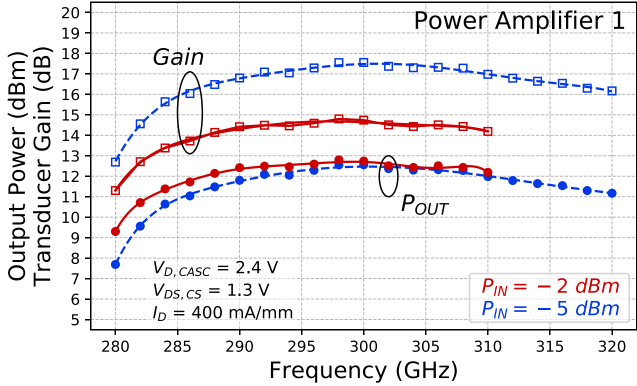


Fig. 25. CW measured transducer gain and output power of the PA1 MMIC between 280 and 328 GHz with 2-GHz step size at −5-dBm and –2-dBm input power.

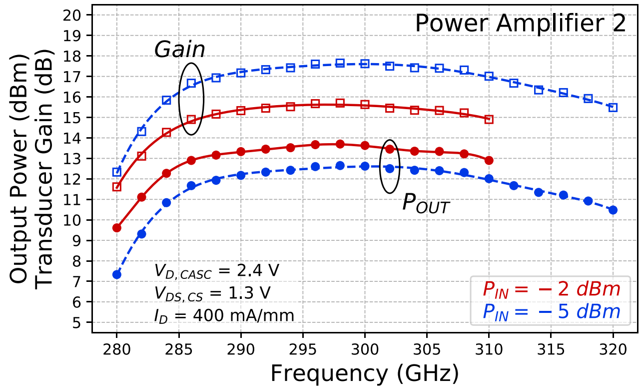


Fig. 26. CW measured transducer gain and output power of the PA2 MMIC between 280 and 328 GHz with 2-GHz step size at −5-dBm and –2-dBm input power.

in the output stages of PA1 and PA2 were biased with 1.3 V drain-source voltage and the cascode cells with 2.4 V ($V_{\mathrm{DS}} \approx$ 1.2 V).

The measured maximum output power level of PA1 is 12.9 dBm, measured at 300 GHz. PA2 achieves up to 13.7 dBm measured output power around 300 GHz, and at least 13 dBm (20 mW) over the 286– 310-GHz frequency range. The better output-power performance of PA2 is believed to be mainly due to the lower insertion loss of the air-bridge Wilkinson power combiner (see Figs. 18 and 19), as well as lower losses between the output of the Wilkinson combiner and the RF-pad. The RF-pad of PA1 is connected using a MET2MET3 TFMSL interconnection, while PA2 is connected via an air-bridge TFMSL. Additionally, since the two Wilkinson combiners do not show a perfect 50-Ω load to the parallelized UA cells, the load at device level in the output stage will differ on a small scale between the UA, PA1, and PA2. Judging from the observed large-signal gain and output-power roll-off above 310 GHz of PA1 and PA2 compared to the unit amplifier cell, the Wilkinson power combiners need to be slightly optimized in order to further increase the large-signal bandwidth.

Fig. 27 shows the measured transducer gain versus output power for CW operation of PA2. The frequency was swept from

TABLE I
COMPARISON OF SSPA MMICS (‡) AND MODULES (#) AROUND 300 GHZ

Ref.	Frequency (GHz)	S_{21} (dB)	$P_{\mathrm{out,sat}}$ (dBm)	$\mathrm{Gain}_{\mathrm{sat}}$ (dB)	Chip area of PA core* (mm x mm)	V_{DC} (V)	PAE (%)	P_{out} per required width of PA core* (mW/mm)	Technology
[6]‡	290 – 307.5	20 – 23.5	7.8 – 10	10 – 12	0.25 x 1.25	1.95	1.1	40.0	250-nm InP HBT
[7]‡	301	13 – 13.5	13.5	11.8	0.5 x 0.5	∼2.2	1.5	44.8	250-nm InP HBT
[8]‡	300 – 305	20	9.5 – 9.8	8	0.4 x 0.4	1.8	1.1	23.9	250-nm InP HBT
[9]‡	326 – 340	16.6	8.6 – 12.6	3 – 7	0.7 x 0.8	1.8	1.1	26.0	130-nm InP HBT
[10]#	338	14.6	10	3	0.3 x 0.8	2.2	3.5	52.8**	Sub-50-nm InP HEMT
[32]#	275 – 320	15 – 22	3 – 5	13 – 15	0.4 x 1.0	0.9	2.3 – 4.2	12.5**	35-nm InGaAs mHEMT
[24]‡	280 – 310	15 – 19	6.7 – 8.3	12.5 – 14	0.4 x 0.8	0.9	0.9	16.9	35-nm InGaAs mHEMT
[11]‡	280 – 320	13 – 19	6.8 – 8.6	11.5 – 13.5	0.16 x 0.8	1.3	2.1	45.3	35-nm InGaAs mHEMT
This Work‡	280 – 328	20 – 26	9.6 – 13.7	11.5 – 13.8	0.35 x 1.1	1.3	0.8 – 2.4	67.0	35-nm InGaAs mHEMT

V_{dc}: Applied drain-source voltage (V_{DS}) and collector-emitter voltage (V_{CE}) of single HEMT and HBT devices, respectively.
*: PA core: required chip area including matching networks and the first stage of shunt capacitors in the bias insertion network, without RF/dc-pads.
**: only packaged results are published, 1.5 dB losses between waveguide flange and MMIC are estimated and included.

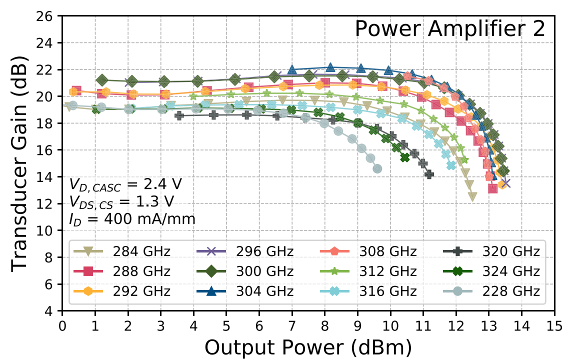


Fig. 27. Measured transducer gain versus measured output power of PA2 between 284 and 328 GHz with 4-GHz step size.

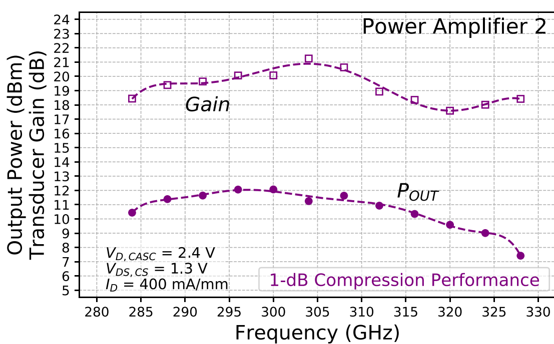


Fig. 28. CW measured transducer gain and output power at 1-dB gain compression of the PA2 MMIC versus frequency. The cascodes were biased at 2.2 V supply voltage ($V_{\mathrm{DS}} = 1.1$ V) and $I_{\mathrm{d}} = 400$ mA/mm. The CS output stages were biased at $V_{\mathrm{DS}} = 1.3$ V and $I_{\mathrm{d}} = 400$ mA/mm.

284–328 GHz with 2-GHz step size. Alongside high output power levels above 20 mW, the power amplifier also shows a good linearity and compression behavior. The measured $\mathrm{OP}_{\mathrm{1dB}}$ 1-dB gain compression power of PA2 is above 10 dBm over the 284– 316-GHz frequency band, achieving a maximum $\mathrm{OP}_{\mathrm{1dB}}$ of 12 dBm at 20-dB gain around 300 GHz, as shown in Fig. 28.

VII. COMPARISON TO STATE OF THE ART

Table I shows a summary of the presented SSPA MMIC PA2 in comparison to existing results of state-of-the-art SSPA MMICs in InGaAs mHEMT technology, a selection of InP HBT MMICs as well as an InP HEMT based module around 300 GHz. The

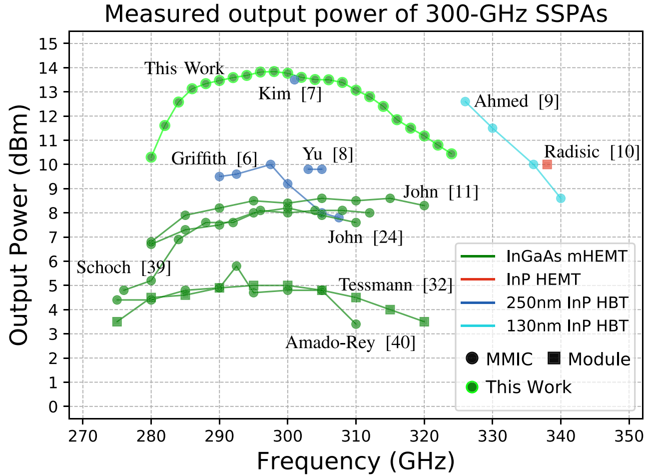


Fig. 29. Measured output power of SSPA MMICs and modules around 300 GHz. A detailed comparison of the depicted power amplifiers is shown in Table I.

state of the art in terms of measured output-power performance including a selection of prior art is additionally plotted in Fig. 29 for the 270–350-GHz frequency range.

The reported MMICs achieve state-of-the-art output-power performance for SSPA MMICs around 300 GHz. Compared to InP HBT and HEMT SSPAs, where Kim *et al.* [7] have demonstrated up to 22.4 mW at a single frequency of 301 GHz, at least 20 mW of output power were measured for a large bandwidth of 25 GHz around 300 GHz. Furthermore, more than 10-mW output power performance is achieved over the 280–324-GHz frequency band, while operating the mHEMT devices at significantly lower voltages, in comparison to InP-based SSPA MMICs.

The focus of the presented PA MMICs was the design of a very compact PA core, to achieve high output power at a narrow chip width. The output power per required chip width of 67 mW/mm is improved by a factor of four compared to previously published cascode topologies in this mHEMT technology [24]. Since the output stage with two 8-finger CS devices in parallel does not require a larger chip width than the 8-finger cascode gain stages, the output power per required chip width is significantly increased compared to the results presented in [11], achieving approximately 5-dB more output power by doubling the required chip width of the PA core.

VIII. Conclusion

This article describes the design and implementation of broadband PA MMICs realized in a 35-nm InGaAs mHEMT technology. More than 20 mW of measured output power are demonstrated for the first time over a 25-GHz large-signal bandwidth around 300-GHz, setting the state of the art for broadband SSPA MMICs at this frequency range.

Two Wilkinson power combiners in elevated CPW and airbridge TFMSL environment are investigated, which permit the efficient parallelization of a compact unit amplifier cell, implemented in the BEOL of this mHEMT technology using thin-film wiring. Compared to previously published 300-GHz SSPA MMICs in III-V technologies, the measured output power level per required PA core width of 67 mW/mm is notably improved by at least 27 %. This improvement is mainly due to the very compact implementation of the UA cell, using highly parallelized two-finger devices in close proximity, which allows for a broadband matching while maximizing the total gate width on the smallest chip size possible. With this approach, a total gate width of 516 μm is implemented on a small chip width of only 0.35 mm, allowing on-chip and module integration.

The investigated topology, based on multifinger cascode and CS cells, achieves excellent linearity and a measured OP_{1dB} 1-dB gain compression power above 10 mW, which is vital for the usage in THz communication systems and represents a significant improvement to previously reported cascode topologies in this mHEMT technology [24], [32], [40].

Hence, the optimization of the power combining networks and further parallelization of the presented PA-cell permits the development of broadband 20–50-mW SSPA MMICs based on InGaAs mHEMT devices, which are required for high-resolution radar/imaging and high-data-rate communication applications at THz frequencies around and above 300 GHz.

Acknowledgment

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Laurenz John received the M.S. degree in electrical engineering and information technologies from the Karlsruhe Institute of Technology, Karlsruhe, Germany, in 2016.

He is currently a Research Engineer with the Fraunhofer Institute for Applied Solid State Physics IAF. Since 2016, he has been involved in the design and characterization of InGaAs mHEMT devices and integrated circuits on GaAs and Si substrates for mm-wave and sub-mm-wave frequency applications. His current research interests include MMIC and PA design for radar and communication applications at frequencies above 200 GHz.

Axel Tessmann received the Dipl.-Ing. and Ph.D. degrees in electrical engineering from the University of Karlsruhe, Karlsruhe, Germany, in 1997 and 2006, respectively.

In 1997, he joined the Microelectronics Department, Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg, Germany, where he is involved in the development of monolithically integrated circuits and subsystems for high-resolution imaging systems and high data rate wireless communication links. He is currently a Group Manager of the Millimeter-Wave Packaging and Subsystem Group, Fraunhofer IAF. His main research interests include the design and packaging of millimeter-wave and submillimeter-wave ICs using high electron mobility transistors on GaAs, GaN, and InP as well as circuit simulation and linear and nonlinear device modeling.

Arnulf Leuther received the Dipl. -Phys. and Ph.D. degrees in physics from the Technical University of Aachen, Aachen, Germany, in 1992 and 1996, respectively.

Since 1996, he has been with the Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg, Germany. His major research interests include the development of HEMT technologies for sensor and communication systems up to 600 GHz.

Philipp Neininger (Student Member, IEEE) received the B.S. and M.S. degrees from the Karlsruhe Institute of Technology, Karlsruhe, Germany, in 2014 and 2017, respectively. He is currently working toward the Ph.D. degree with the Fraunhofer Institute for Applied Solid State Physics IAF, Freiburg, Germany.

Since 2017, he has been with the Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg, Germany. His research interests include mmW power combining and high power density composite semiconductor chip design in Ka band and beyond.

Thomas Merkle received the M.Sc. degree in electrical engineering from the University of Stuttgart, Stuttgart, Germany, in 1999, and the Ph.D. degree in electrical engineering from the University of Ilmenau, Ilmenau, Germany, in 2006.

He joined the Fraunhofer Institute for Applied Solid State Physics IAF, Freiburg im Breisgau, Germany, where he worked in the field of nonlinear characterization and modeling of GaAs and GaN high-electron-mobility transistors, and the design of millimeter-wave monolithic integrated circuits up to 110 GHz. From 2005 to 2010, he was a Postdoctoral Fellow with CSIRO ICT Centre, Sydney, NSW, Australia, with a focus on active integrated antennas for phased-array communication links at 71–86 GHz. From 2010 to 2013, he was a Senior Research Engineer with the Sony Technology Center, Stuttgart, where he was responsible for the design of submillimeter-wave ICs and SiPs. In 2013, he joined Fraunhofer IAF overseeing research projects in the area of millimeter-wave and submillimeter-wave wireless communications, radar, and related device technologies.

Thomas Zwick (Fellow, IEEE) received the Dipl.-Ing. (M.S.E.E.) and the Dr.-Ing. (Ph.D.E.E.) degrees in electrical engineering from the Universität Karlsruhe (TH), Karlsruhe, Germany, in 1994 and 1999, respectively.

From 1994 to 2001, he was a Research Assistant with the Institut fr Höchstfrequenztechnik und Elektronik (IHE), the Universität Karlsruhe (TH), Germany. In February 2001, he joined IBM as Research Staff Member at IBM T. J. Watson Research Center, Yorktown Heights, NY, USA. From October 2004 to September 2007, he was with Siemens AG, Lindau, Germany. During this period, he managed the RF development team for automotive radars. In October 2007, he became a Full Professor with the Karlsruhe Institute of Technology (KIT), Germany. He is the Director of the Institute of Radio Frequency Engineering and Electronics (IHE), KIT. He coedited 3 books, has authored or coauthored 120 journal papers, more than 400 contributions at international conferences and 15 granted patents. His research interests include wave propagation, stochastic channel modeling, channel measurement techniques, material measurements, microwave techniques, millimeter wave antenna design, wireless communication, and radar system design.

Dr. Zwick research team received more than 10 best paper awards on international conferences. He served on the technical program committees (TPC) of several scientific conferences. In 2013, he was General Chair of the international Workshop on Antenna Technology (iWAT 2013) in Karlsruhe and in 2015 of the IEEE MTT-S International Conference on Microwaves for Intelligent Mobility in Heidelberg. He also was TPC Chair of the European Microwave Conference 2013 and General TPC Chair of the European Microwave Week 2017. From 2008 to 2015, he was a President of the Institute for Microwaves and Antennas. He was selected as a Distinguished IEEE Microwave Lecturer for the 2013 to 2015 period with his lecture on QFN Based Packaging Concepts for Millimeter-Wave Transceivers. Since 2017, he has been a member of the Heidelberg Academy of Sciences and Humanities. In 2019, he became the Editor-in-Chief of the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS.