Broadband GaN MMIC Doherty Power Amplifier Using Continuous-Mode Combining for 5G Sub-6 GHz Applications

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***Abstract*— This article presents a broadband fully integrated Doherty power amplifier (DPA) using a continuous-mode combining load. It is illustrated that the continuous-mode impedance condition in back-off and saturation for Doherty operation can be achieved with a simple impedance inverter network (IIN) that can be realized using lumped components in gallium nitride (GaN) monolithic microwave integrated circuits (MMICs). A DPA was designed and fabricated using the 250-nm GaN process to validate the proposed architecture and design methodology. The fabricated DPA chip attains around 8 W saturated power from 4.1 to 5.6 GHz. About 38.5%–46.5% drain efficiencies are achieved at 6-dB output power back-off within the entire design band. When driven by a 100-MHz OFDM signal with 6.5-dB peak-to-average power ratio (PAPR), the proposed DPA achieves better than −45-dBc adjacent channel leakage ratio (ACLR) and higher than 38% average efficiency at 4.4 and 5.2 GHz after digital predistortion.**

***Index Terms*— Broadband, continuous-mode, Doherty power amplifier (DPA), gallium nitride (GaN), load modulation, monolithic microwave integrated circuit (MMIC).**

I. Introduction

With increasing deployment of small cell networks during the roll-out of 5G, system designers face significant challenges in managing power consumption and heat dissipation of wireless base stations. To meet high data rates and large capacity, the signal bandwidth and peak-to-average power ratio (PAPR) will continue to increase. Shifting from the single antenna to multiple input multiple output (MIMO) transmissions imposes further challenges in transmitter design and system integration. This drives demands for not only wideband high-efficiency power amplifiers (PAs) but also compact size and easily integratable circuits. Because of high power density, high efficiency, and wideband performance, gallium nitride (GaN) monolithic microwave integrated circuit (MMIC) PAs have been seen as a promising replacement for discrete designs to preserve valuable space in the tightly clustered MIMO antenna arrays in the 5G sub-6 GHz band.

To improve back-off efficiency, many PA architectures such as outphasing and Doherty PA (DPA) were proposed, and the related bandwidth extension techniques have received much attention [1]–[12]. Besides, researchers proposed new back-off efficiency improvement technologies for broadband applications, such as the load modulated balanced amplifier (LMBA) [13]–[15], distributed efficiency PA [16], [17], and unbalanced PA [18]. Despite these explorations, DPA has been one of the most widely used techniques because of its simple structure and high reliability, and bandwidth extension techniques for DPA have also made great progress. By introducing techniques such as voltage mode combining [3], [4], broadband transformer [6]–[8], and postmatching [9], the DPA bandwidth can be greatly extended.

Many reported wideband DPAs in the sub-6 GHz band are based on the microstrip design with printed circuit board (PCB) implementation [9]–[12], [19]–[21], which corresponds to high power requirements for macro base stations. The PCB structures such as large phase peaking network make the related DPAs difficult to be integrated at sub-6 GHz. Researchers have also explored different techniques to design wideband DPAs with complementary metal oxide semiconductor (CMOS) process [3]–[8], [22]–[24]; however, low breakdown voltage results that these DPAs can only be used in low power user terminals. With the advent of 5G Era, the power drop of single RF chain in base station brought by the application of array technology brings new demands for wideband MMIC DPAs in compound process, such as GaN. Although wideband DPA based on compound process has also

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been studied, it is much less reported than DPAs using CMOS process or PCB implementation [25]–[31]. Limited by the manufacturing process and operating band, MMIC DPAs at sub-6 GHz often use simple circuit structures, such as compact impedance inverter network (IIN) [25] and zero degree phase peaking network [27], which limit the bandwidth.

As one of the most popular broadband design methodologies, continuous-mode (CM) operation has been successfully used in integrated PAs on different integration processes [32]–[34]. Some efforts have also been made to introduce CM techniques in PCB DPA designs [35]–[39]. In [35]–[37], harmonic control was introduced in the post-matching network of CM-DPAs. In [38] and [39], CM-DPAs were realized using noninfinite peaking output impedance. In these PCB designs, large phase peaking networks were required to achieve the target CM impedance condition, which makes these DPA architectures not suitable for MMIC designs in the sub-6 GHz band, because the peaking network would introduce large loss and is not conducive in compact designs.

In this article, we proposed a novel DPA architecture which uses the CM combining load that is more suitable for MMIC designs. The design space of CM-DPA is further expanded. The CM impedance condition can be achieved using only one IIN without using peaking networks. A broadband GaN MMIC DPA is then designed and fabricated to validate the proposed architecture. The implemented CM-DPA chip presents back-off efficiency enhancement within a wide bandwidth in the 4.1–5.6-GHz band. To the best knowledge of the authors, it is the first time that the CM technique has been applied to MMIC DPA designs at the sub-6-GHz band. The remaining part of this article is organized as follows. Section II presents the theory of the proposed CM-DPA. Section III shows the detailed procedures of realizing the proposed DPA in GaN process. In Section IV, the experimental results are presented with a conclusion given in Section V.

II. Theoretical Analysis

The conventional CM-DPA combines the output power of two PAs, i.e., the class-AB biased carrier PA and the class-C biased peaking PA, via an IIN and a peaking network as shown in Fig. 1(a). A phase compensation network (PCN) is added at the carrier input to ensure that the combining phase and the combining load is set to $R_{\text{opt}}/2$. To achieve CM impedance at back-off, the peaking network is necessary to provide noninfinite peaking output impedance, which changes the combining load $R_{\text{opt}}/2$ to a complex value and then can be transferred to CM impedance [36], [38]. However, the CM impedance condition can only be satisfied at back-off as shown in Fig. 1(b). When the peaking PA turns on, no matter what the specific value of CM impedance is, it will degenerate to class-B impedance at saturation due to pure resistance combining load. This imperfect CM load modulation can cause a certain degree of performance degradation. More importantly, the goal of design space expansion is only realized at back-off, which limits the flexibility of circuit design. In addition, the phase shift of this peaking network must be large enough to provide required peaking output impedance, which makes this architecture difficult to be integrated.

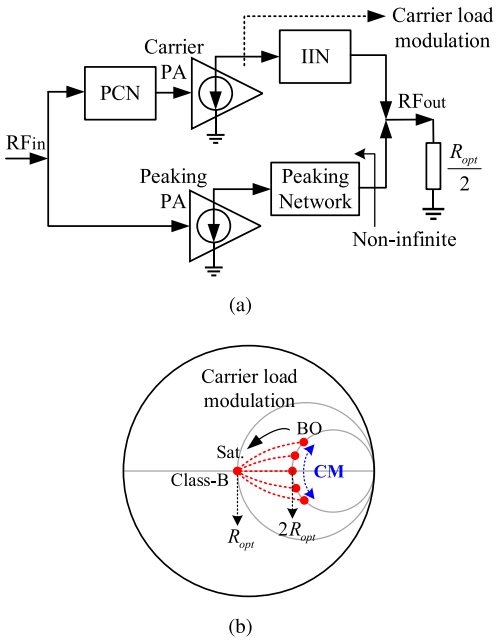

Fig. 1. Conventional CM-DPA architecture. (a) Block diagram and (b) carrier load modulation.

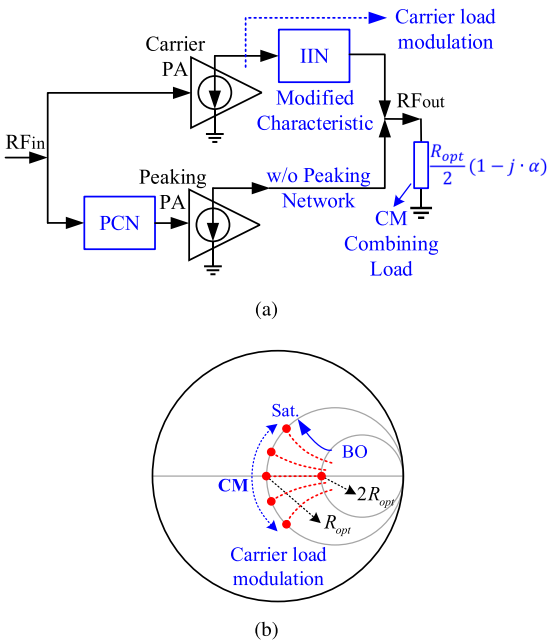

Fig. 2. Proposed CM-DPA architecture. (a) Block diagram and (b) carrier load modulation.

To further use the CM theory and explore a generalized CM-DPA design space, we propose a novel architecture using a CM combining load as shown in Fig. 2(a). Unlike the conventional CM-DPA, the CM combining load provides the potential to expand the DPA design space throughout the entire load modulation process. The related carrier load modulation can be modified to the results shown in Fig. 2(b). The noninfinite peaking output impedance is no longer required since the combining load partly provides complex impedance. Therefore, the peaking network can be removed and only IIN is retained. Because the peaking PA is directly connected to

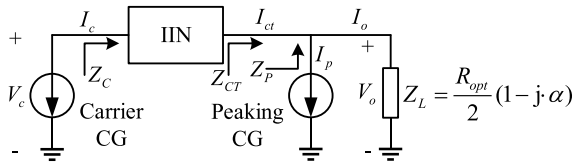

Fig. 3. Theoretical block diagram of the proposed CM-DPA.

the combining load, the design space of it can be expanded with CM operation at saturation. To ensure envisaged load modulation, the IIN should be designed based on the specific value of the combining load. The circuit of the proposed architecture is simpler than the conventional CM-DPA and is more suitable for MMIC implementations. The proposed DPA can potentially achieve wide bandwidth using different CM configuration while maintaining high-efficiency performance.

A. Impedance Condition in the Proposed CM-DPA

For theoretical analysis, the active devices in the proposed CM-DPA are represented by carrier and peaking current generators (CGs) as shown in Fig. 3. The impedance condition at the CG planes depends on the specific circuit structure of the IIN. The reasonable method to analyze the IIN structure is to use the CM impedance condition as the constraint to solve specific IIN parameters. In the following analysis, we take the class-B/J continuum impedance condition as an example.

For the class-B/J continuum, the combining loads of the proposed CM-DPA can be set as

$$Z_L = (R_{\text{opt}}/2)\cdot(1 - j\cdot\alpha) \tag{1}$$

where R_{opt} is the optimal impedance for class-B operation at saturation and α is the parameter related to different voltage waveforms and $-1 \le \alpha \le 1$ [40], [41]. The continuous values of the parameter α determine the set of class-B/J continuum solutions. Varying parameter α controls the phase shift between the voltage and current at the output current generator plane. For every α, there is thus a specific load impedance which can be calculated using equation (1) to run class-B/J operation. According to the nature of class-B/J continuum, these impedance values can provide the same output power level and efficiency. Therefore, based on the block diagram shown in Fig. 3, the impedance of the carrier and peaking branches for the proposed CM-DPA at the combining node can be calculated as follows:

$$Z_{\text{CT}} = \left(1 + \frac{I_p}{I_{\text{ct}}}\right)\frac{R_{\text{opt}}}{2}(1 - j\cdot\alpha) \tag{2}$$

$$Z_P = \left(1 + \frac{I_{\text{ct}}}{I_p}\right)\frac{R_{\text{opt}}}{2}(1 - j\cdot\alpha) \tag{3}$$

where I_{ct} and I_p are the current of the carrier and peaking branches at the combining node, respectively.

Common IINs can be regarded as matching network in a certain frequency band, and we adopt this assumption here. Based on the method introduced in [11], we can assume that the proposed IIN is matched to an impedance Z_T at both its two ports, and then the IIN ABCD matrix can be expressed as

$$\begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix} = \begin{bmatrix} \cos\theta_i & jZ_T\sin\theta_i \\ j\sin\theta_i/Z_T & \cos\theta_i \end{bmatrix} \tag{4}$$

where Z_T is regarded as the equivalent characteristic impedance of IIN and θ_i represents the phase shift. Therefore, the impedance at the carrier CG plane can be calculated as

$$Z_C = Z_T\frac{Z_{CT} + j\cdot Z_T\tan\theta_i}{Z_T + j\cdot Z_{\text{CT}}\tan\theta_i} \tag{5}$$

According to (5), θ_i can be expressed as

$$\theta_i = \arctan\left[\frac{(Z_{\text{CT}} - Z_C)\cdot Z_T}{j(Z_{\text{CT}}Z_C - Z_T^2)}\right]. \tag{6}$$

When $\alpha = 0$, the combining load $Z_L = R_{\text{opt}}/2$, and the proposed CM-DPA degenerates into the original DPA. To provide the required impedance for DPA operation, Z_T should be set to R_{opt}. Once the value of Z_T has been set, the only unknown IIN parameter is θ_i. We can use the CM impedance condition as the constraint to solve θ_i. However, the CM impedance condition may not be satisfied at the same time in the case of back-off and saturation. Therefore, we will discuss these two cases separately.

1) IIN Phase Parameter Condition at Back-off: At back-off, the peaking CG is off which means $I_p = 0$. According to (2), the carrier back-off impedance at the combining node should be

$$Z_{\text{CT,BO}} = (R_{\text{opt}}/2)\cdot(1 - j\cdot\alpha). \tag{7}$$

The required CM impedance condition at the carrier CG plane at back-off for Doherty operation can be expressed as

$$Z_{C,\text{BO}} = 2R_{\text{opt}}\cdot(1 \pm j\cdot\alpha). \tag{8}$$

Substituting (7) and (8) into (6), the value of θ_i can be solved. When $Z_{C,\text{BO}} = 2R_{\text{opt}}\cdot(1 - j\cdot\alpha)$, (6) has no analytic solution. When $Z_{C,\text{BO}} = 2R_{\text{opt}}\cdot(1 + j\cdot\alpha)$, the IIN phase parameter condition at back-off can be calculated as

$$\theta_i = -\arctan(3/\alpha). \tag{9}$$

2) IIN Phase Parameter Condition at Saturation: At saturation, the CM impedance condition should be satisfied by both the carrier and peaking CGs. For the peaking plane, to satisfy the required CM impedance condition, the magnitude and phase of I_{CT} and I_P should be the same, and then the impedance at the combining node can be obtained as

$$Z_{P,\text{sat}} = Z_{\text{CT,sat}} = R_{\text{opt}}\cdot(1 - j\cdot\alpha). \tag{10}$$

The required CM impedance condition at the carrier CG plane at saturation for Doherty operation can be expressed as

$$Z_{C,\text{sat}} = R_{\text{opt}}\cdot(1 \pm j\cdot\alpha). \tag{11}$$

Similarly, the IIN phase parameter condition at saturation can be calculated as

$$\theta_i = -\arctan(2/\alpha). \tag{12}$$

The IIN phase parameter obtained from different power levels is not the same, which means the CM impedance

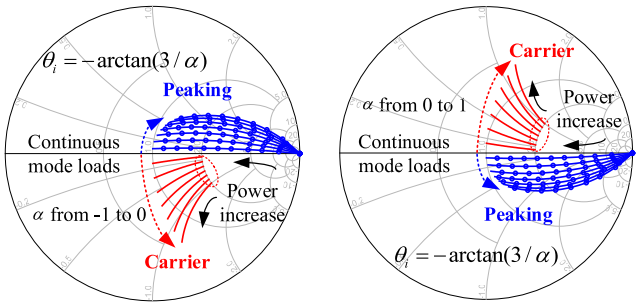

Fig. 4. Load modulation of Z_c and Z_p when $\theta_i = -\arctan(3/\alpha)$ on Smith chart with ref. impedance of R_{opt}. (a) α from 0 to 1. (b) α from -1 to 0.

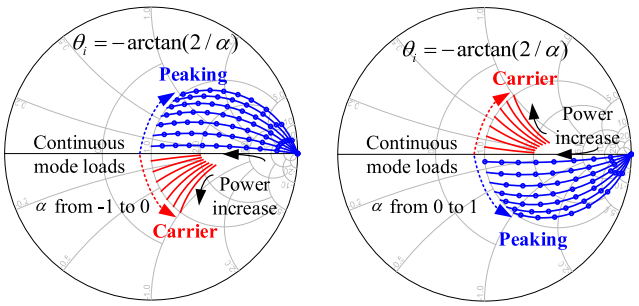

Fig. 5. Load modulation of Z_c and Z_p when $\theta_i = -\arctan(2/\alpha)$ on Smith chart with ref. impedance of R_{opt}. (a) α from 0 to 1. (b) α from -1 to 0.

condition could not be fully satisfied. Therefore, it is necessary to analyze the load modulation process under different IIN phase parameter conditions.

B. Load Modulation of the Proposed CM-DPA

From (2), (3), and (5), to obtain the load modulation process, the current variation with input signal should be given. The current of carrier and peaking CGs can be expressed as

$$I_c = I_{c,\max} \cdot \left(\frac{V_{\text{in}}}{V_{\text{in,max}}}\right) \tag{13}$$

$$I_p = \begin{cases} 0, & 0 \le V_{\text{in}} < V_{\text{in,max}}/2 \\ I_{p,\max} \cdot \left(\frac{2V_{\text{in}}}{V_{\text{in,max}}} - 1\right), & V_{\text{in,max}}/2 \le V_{\text{in}} \le V_{\text{in,max}} \end{cases} \tag{14}$$

where V_{in} is the input voltage, and $I_{c,\max}$ and $I_{p,\max}$ represent the maximum value of the carrier and peaking current, respectively. For symmetrical DPA configuration, $I_{c,\max} = I_{p,\max}$.

The IIN voltage and current relationship can be written as

$$\begin{bmatrix} V_c \\ I_c \end{bmatrix} = \begin{bmatrix} \cos\theta_i & jZ_T \sin\theta_i \\ j\sin\theta_i/Z_T & \cos\theta_i \end{bmatrix} \begin{bmatrix} V_o \\ I_{\text{ct}} \end{bmatrix}. \tag{15}$$

The output voltage at the load can be expressed as

$$V_o = (R_{\text{opt}}/2)(I_{\text{ct}} + I_p)(1 + j \cdot \alpha). \tag{16}$$

Therefore, the expression of I_{ct} can be obtained as

$$I_{\text{ct}} = \frac{I_c - j(\sin\theta_i/2)(1 + j \cdot \alpha)I_p}{j(\sin\theta_i/2)(1 + j \cdot \alpha) + \cos\theta_i}. \tag{17}$$

Substituting (14) and (17) into the corresponding impedance equations, the load modulation process can be obtained.

Fig. 4 shows the load modulation of Z_c and Z_p when $\theta_i = -\arctan(3/\alpha)$ on Smith chart with reference impedance of R_{opt}. When $\theta_i = -\arctan(3/\alpha)$, the carrier back-off impedance strictly satisfies the CM impedance condition, no matter how the value of α varies from -1 to 1. However, both Z_c and Z_p deviate from the CM impedance condition with an increase in input power. The larger the absolute value of α, the more obvious the deviation effect. Fig. 5 shows the load modulation of Z_c and Z_p when $\theta_i = -\arctan(2/\alpha)$. Similarly, the carrier and peaking impedance strictly satisfy the CM impedance condition at saturation, no matter how the value of α varies from -1 to 1. The deviation effect of the carrier impedance Z_C can be observed at back-off.

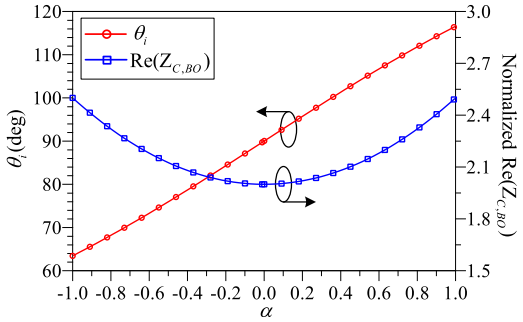

Fig. 6. IIN phase parameter θ_i and normalized Re($Z_{C,\text{BO}}$) versus the value of α when $\theta_i = -\arctan(2/\alpha)$.

Comparing the load modulation trajectory in Figs. 4 and 5, the deviation at saturation when $\theta_i = -\arctan(3/\alpha)$ is more obvious. The deviation when $\theta_i = -\arctan(2/\alpha)$ only makes the back-off impedance become slightly larger. This situation usually does not have a significant impact on the performance of DPAs. Moreover, $\theta_i = -\arctan(3/\alpha)$ means that the IIN phase changes more sharply with α, and this situation usually indicates that the corresponding network bandwidth is narrower [11]. Therefore, we will focus on the theoretical performance and design method when $\theta_i = -\arctan(2/\alpha)$. The back-off impedance of the proposed CM-DPA is not the perfect load for class-B/J operation when $\theta_i = -\arctan(2/\alpha)$, which slightly impacts the Doherty operation.

C. IIN Parameter and Theoretical Performance

From the load modulation shown in Fig. 5, the real part of carrier back-off impedance Re($Z_{C,\text{BO}}$) is larger than $2R_{\text{opt}}$ when $\theta_i = -\arctan(2/\alpha)$. In this situation, the carrier PA would be over-driven to a certain extent when $\alpha \neq 0$, and the over-driven level is directly related to Re($Z_{C,\text{BO}}$) [20], [42]. To show the relationship between different parameters more clearly, Fig. 6 presents the IIN phase parameter θ_i and normalized Re($Z_{C,\text{BO}}$) versus the value of α when $\theta_i = -\arctan(2/\alpha)$. When α changes from -1 to 1, the corresponding range of θ_i is from about 63.4° to 116.6°. Meanwhile, Re($Z_{C,\text{BO}}$) changes from 2.5 to 2.0, and then gradually increases back to 2.5. According to the method introduced in [42], we can define the over-driven

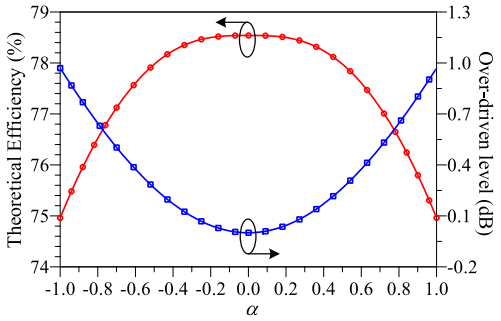

Fig. 7. Theoretical back-off efficiency and the corresponding over-driven level of the proposed CM-DPA.

level in dB as

$$\epsilon = 10\log_{10}\left[2 \cdot \frac{\mathrm{Re}(Z_{C,\mathrm{BO}})}{R_{\mathrm{opt}}}\right] - 6. \tag{18}$$

The dc and fundamental over-driven current is calculated as

$$I_{c,\mathrm{bo}}[0] = \frac{10^{\epsilon/10}(1 - 2\sin\theta_0 + 2\theta_0)}{\pi} \tag{19}$$

$$I_{c,\mathrm{bo}}[1] = \frac{8\sin\theta_0 - 10^{\epsilon/10}(2\sin\theta_0 + 4\theta_0 - \pi)}{2\pi} \tag{20}$$

where $(-\theta_0,\theta_0)$ is the over-driven phase range within a period

$$\theta_0 = \arccos(10^{-\epsilon/10}). \tag{21}$$

The theoretical efficiency can be calculated based on (19) and (20). Fig. 7 shows the back-off efficiency and over-driven level when $\theta_i = -\arctan(2/\alpha)$. Although the over-driven operation reduces the back-off efficiency when $\alpha \neq 0$, the degree of reduction is small. When we use different CM load modulation at different frequencies, a broadband CM-DPA can be realized. The theoretical performance of the proposed CM-DPA is calculated when the harmonic impedance is perfectly matched. However, in practical broadband MMIC designs, controlling the harmonic impedance using additional circuits might introduce more loss. Moreover, as long as the second-harmonic impedance is within a certain range, the reduction in efficiency is generally acceptable [43].

III. Design of the Proposed CM-DPA

To validate the proposed architecture, a broadband CM-DPA was implemented using the 250-nm GaN process from WIN Semiconductor. The target bandwidth was 4.3–5.8 GHz. A transistor size of 6 ×125 μm was chosen as the basic active device. The source of two basic transistors was then connected to common ground to provide larger power. This structure was used for both the carrier and peaking PAs. To ensure the stability of designed PA, stability circuits were designed for active devices. Fig. 8 shows the transistor connection and stability circuits. The stability circuits include an RC-tank for each basic transistor and a lossy inductor as shown in Fig. 8(b). Fig. 9 shows the simulated maximum gain and stability factor versus frequency of the circuits shown in Fig. 8(b). The designed stability circuit can effectively improve the stability. For the transistor size of 2 × 6 × 125 μm, the maximum drain current is 850 mA. The nominal drain bias voltage of

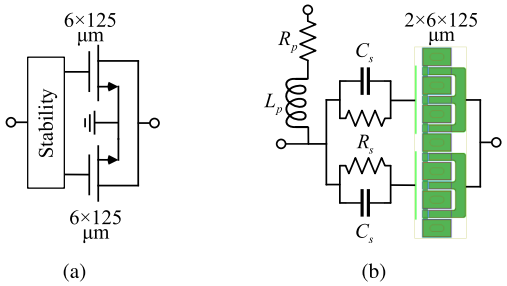

Fig. 8. Transistor connection and stability circuits. (a) Block diagram and (b) circuit structure.

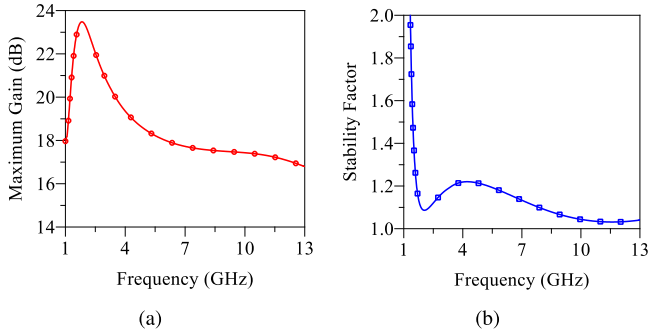

Fig. 9. Simulated results of stability circuits. (a) Maximum gain and (b) stability factor.

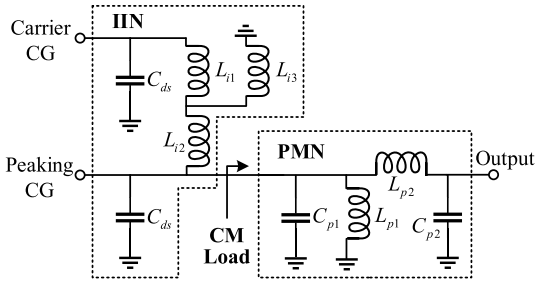

Fig. 10. Circuit structure of the proposed output network.

this process is 28 V. Therefore, R_{opt} can be set to around 50 Ω when considering the knee-voltage effect. It should be noted that when the optimal impedance value changes, the proposed architecture also provides design flexibility using IIN and PMN with different impedance transformation ratios.

A. Design of Output Network

From the theoretical analysis, the most important part for realization is to build the output network. The proposed output network consist of two parts: a postmatching network (PMN), which can transfer the terminal load to the CM combining load, and the IIN, which follows the analysis in Section II. Fig. 10 shows the circuit structure of the proposed output network. The proposed IIN includes the drain–source capacitor of active devices and three inductors, forming an equivalent transformer structure. The proposed PMN is a series–parallel hybrid matching structure. The commonly used matching network structures can all be used to design the IIN and PMN, and the output network shown in Fig. 10 is just a design

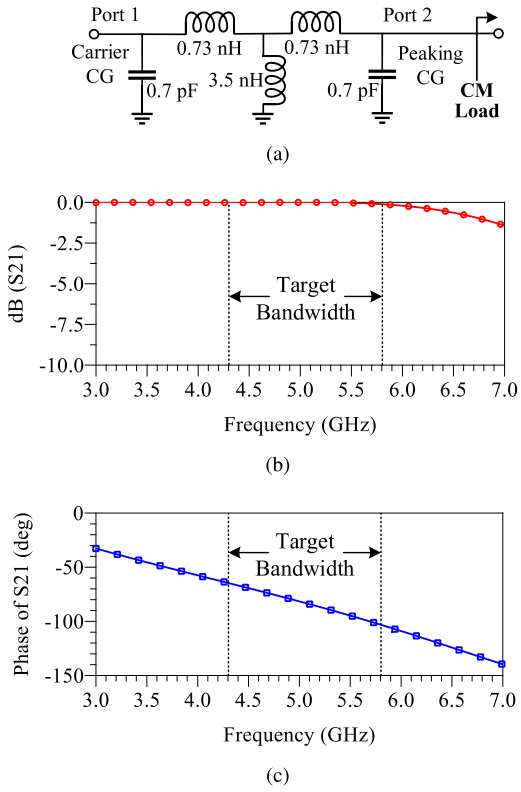

Fig. 11. Proposed IIN. (a) Circuit schematic; (b) frequency response of magnitude of S21; and (c) phase of S21.

example. The specific CM combining load is limited by the phase shift range of IIN, and therefore, IIN should be designed before PMN.

According to the analysis in Section II, the proposed IIN should match R_{opt} at both the ports. Therefore, the component value of IIN can be decided by the S-parameters when the two ports of IIN are matched. The optimization method introduced in [11] was used to find the specific component value based on the magnitude and phase of S21. The optimization goal should provide the smallest possible transmission attenuation and ensure the phase within the required range given in Section II. Fig. 11(a) shows the circuit schematic of the designed IIN, and Fig. 11(b) and (c) presents the corresponding magnitude and phase of IIN S21. Within the target bandwidth, a good matching was ensured, and the phase range of S21 was about $-67°$ to $-105°$.

After designing IIN, the PMN was designed based on the value of θ_i. According to the results given in Fig. 6, the value of α changed from about -0.8 to 0.5 when the range of θ_i was 67° to 105°. A low-pass LC matching circuit was used to transfer the load to a lower impedance. A parallel LC tank was used to tune the lower impedance to the CM combining load. Fig. 12(a) gives the specific value of the designed PMN components. Fig. 12(b) shows the PMN matching results on Smith chart with reference impedance of $R_{\text{opt}}/2$. The ideal CM impedance is also presented in Fig. 12(b). The realized combining load has good consistency with the ideal value. After completing the design of IIN and PMN, the carrier back-off impedance can be obtained. Fig. 13(a) presents the simulated

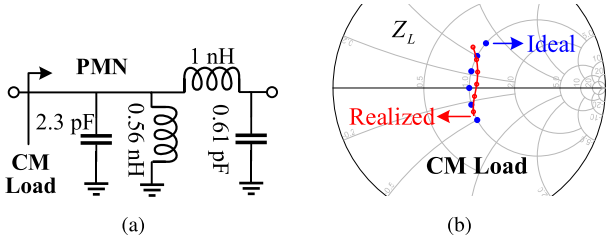

Fig. 12. Proposed PMN. (a) Circuit schematic and (b) PMN matching results on Smith chart with reference impedance of $R_{\text{opt}}/2$.

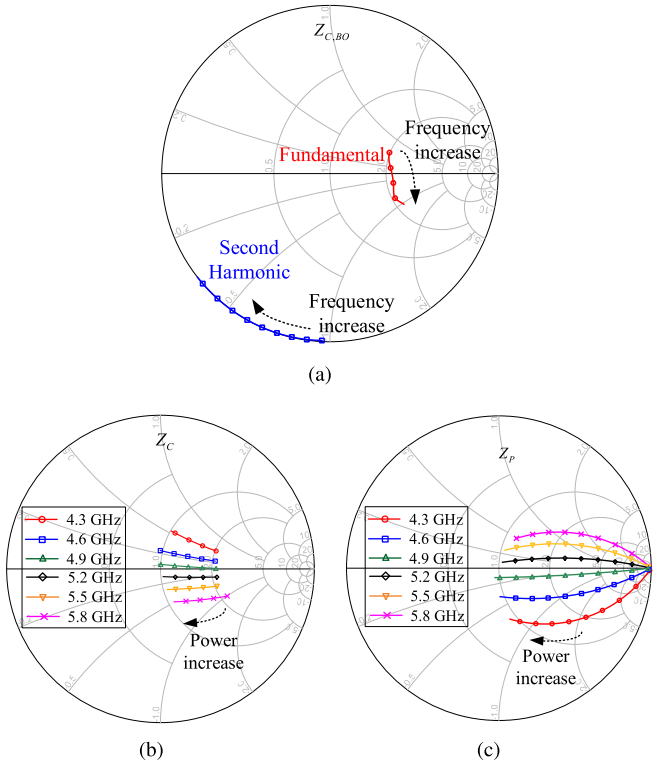

Fig. 13. (a) Simulated fundamental and second-harmonic back-off impedance at carrier CG plane on Smith chart with reference of R_{opt}; (b) simulated carrier load modulation trajectory at CG plane; and (c) simulated peaking load modulation trajectory at CG plane.

fundamental and second-harmonic back-off impedance at carrier CG plane on Smith chart with reference of R_{opt}. The fundamental back-off impedance has good consistence with the ideal CM impedance. For the second-harmonic impedance, mismatch exists, which would reduce the back-off efficiency. Nevertheless, the second-harmonic impedance presents pure reactance and the mismatch is controlled within a certain range. In this situation, the impact on back-off efficiency is limited [43]. The carrier and peaking load modulation trajectories at CG plane are also shown in Fig. 13(b) and (c). The trend of load modulation is in good agreement with the theory. The inductors used in the output network were finally transferred to metal lines.

B. Design of Input Network and Simulation Results

The input network of the proposed CM-DPA consists of several parts: a power divider to separate the input signal,

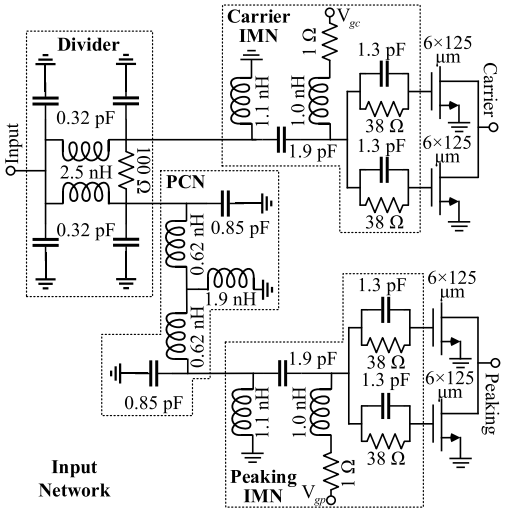

Fig. 14. Circuit schematic of the designed input network.

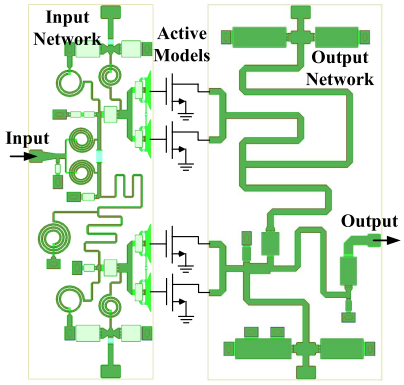

Fig. 15. EM simulation schematic of the designed CM-DPA.

a PCN to compensate the phase difference between the carrier and peaking branch, and input matching networks (IMNs). Fig. 14 shows the schematic of the designed input network, and the specific value of the used components is also given. The power divider used a symmetrical structure similar to the one introduced in [28]. The PCN used the same structure of the IIN, to provide the appropriate phase compensation value within the target bandwidth. The carrier and peaking IMNs used the same circuit structure and included the stability network mentioned early.

The used components in the input and output networks were tuned according to the layout, and the entire circuits of designed CM-DPA were EM-simulated using ADS from Keysight. The EM simulation schematic is shown in Fig. 15. Fig. 16 presents the simulated drain efficiency (DE) and gain versus output power of the proposed CM-DPA. Obvious Doherty operation can be observed throughout the designed band. To better present the broadband characteristic, the simulated DE and output power at different power levels versus operation frequency are shown in Fig. 17. The design CM-DPA achieves saturated DE of 55.3%–62.9% with output power from 39.8 to 40.7 dBm. At 6-dB output power back-off level, DE of 44.3%–54.1% can be obtained from 4.3 to 5.8 GHz.

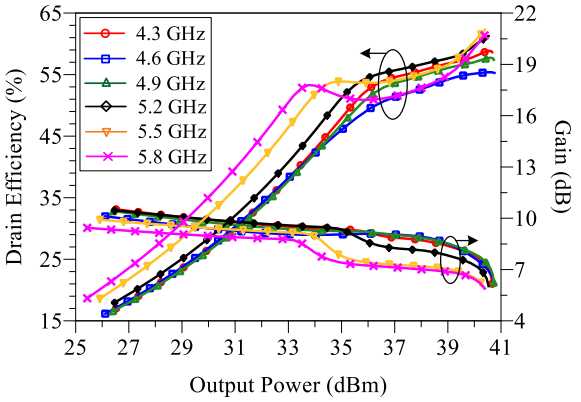

Fig. 16. Simulated DE and gain versus output power at different operation frequencies of the proposed CM-DPA.

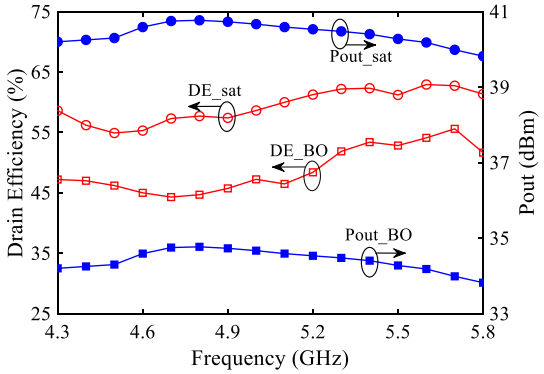

Fig. 17. Simulated DE and output power at different power levels versus operation frequency of the proposed CM-DPA.

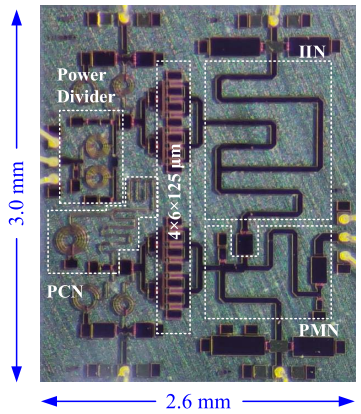

Fig. 18. Chip photograph of the fabricated CM-DPA.

IV. Measurements Results

Fig. 18 presents the photograph of the fabricated CM-DPA chip. The chip size is 2.6 × 3.0 mm^2. The RF and dc pads were wire-bonded to an evolution board (EVB) for measurement convenience. The insertion loss from the RF-in and RF-out TLs on EVB was de-embedded from the measurement results. Both continuous-wave (CW) and modulated signals were used to perform the measurements for the fabricated CM-DPA. During the measurements, drain supply voltages of carrier and peaking PAs kept constant. The quiescent current was 80 mA,

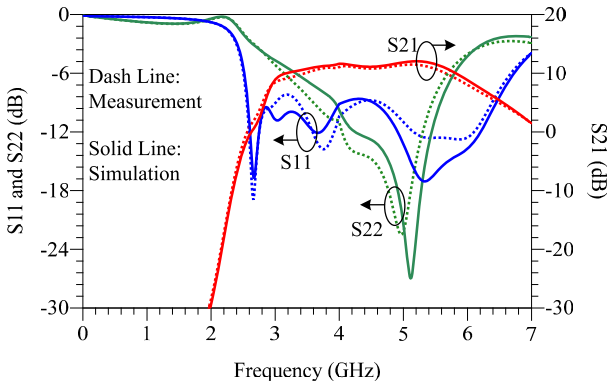

Fig. 19. Measured and simulated S-parameters.

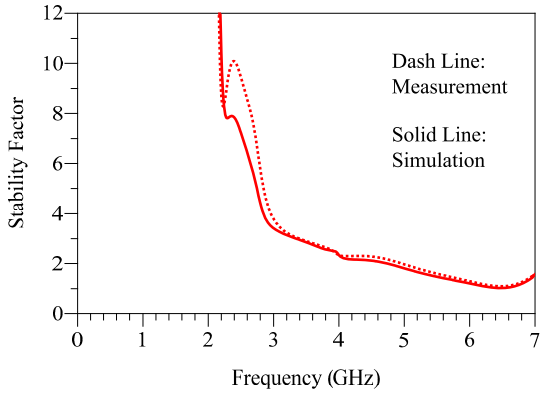

Fig. 20. Measured and simulated stability factor.

and the peaking gate bias voltage was −4.5 V. The bias configuration remained unchanged throughout all the measurements. Small-signal, large-signal, and modulated signal measurements were performed in turn to present the performance of the fabricated CM-DPA.

A. Small-Signal Measurements

First, the small-signal performance of the fabricated CM-DPA was measured by a ZVB8 vector network analyzer from Rhode & Shwarz (R&S). The measured S-parameters of the fabricated chip from 10 MHz to 7 GHz are presented in Fig. 19; meanwhile, the simulated S-parameters are also plotted on the same figure for comparison. It can be seen that the trend of measurement curves is in good agreement with the simulation values. The measured small-signal gain is a little lower than the simulated ones and kept higher than 9.5 dB from 3.30 to 5.75 GHz. Meanwhile, the input return loss is below −9 dB across the 3.36–6.36-GHz band. It should be noted that the GaN active device model from the process design kit (PDK) might not be that precise, which may result in the observed discrepancy between the measured and simulated S-parameters. Fig. 20 presents the measured and simulated stability factor of the fabricated CM-DPA from 10 MHz to 7 GHz. It can be seen that both the measured and simulated stability factors are high than 1.03 throughout the band, which means unconditional stability is achieved.

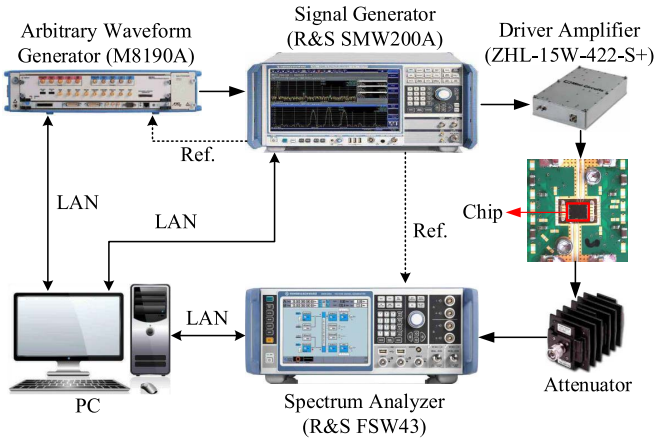

Fig. 21. Large-signal CW and modulated signal measurements' setup.

B. Large-Signal Measurements Under CW Signal Stimulation

The fabricated CM-DPA was then measured using CW signal at different frequencies. Fig. 21 shows the measurement setup of the large-signal CW and modulated signal measurements. The desired input signal was generated by a vector signal generator (R&S SMW200A) and then preamplified by a driver amplifier (Mini-Circuits ZHL-15W-422-S+) to enough power level. The PA output is attenuated and then monitored by a spectrum analyzer (R&S FSW43) to measure the output power and spectrum. Due to the limited modulation bandwidth of the used signal generator, an arbitrary waveform generator (M8190A) is adopted to generate wideband baseband signals during modulated signal measurements. The above-mentioned measurement instruments are all controlled by a computer through LAN connection.

The CM-DPA was tested from 4.1 to 5.6 GHz with 0.1-GHz frequency step. The realized frequency band was slightly shifted from simulation due to model inaccuracy. The measured DE and gain versus output power at different frequencies are shown in Fig. 22. Doherty operation is achieved throughout the measured band, and the back-off efficiency is obviously improved compared with class-B PA.

To demonstrate the wideband performance, the output power and DE at saturation and back-off versus frequency are shown in Fig. 23. Within the measured bandwidth, the fabricated CM-DPA achieves saturated DE of 51.7%–60.8% with output power of 38.4–39.5 dBm. At 6-dB back-off, 38.5%–46.5% DE was achieved. About 8.3–11.2-dB gain was measured at around 27-dBm output power level. The fractional bandwidth of the fabricated CM-DPA is 30.9%. Compared with the simulation results, the measured large-signal performance decreased a little, but the overall results are still in good agreement with the simulation data.

C. Measurements Under Modulated Signal Stimulation

To evaluate the performance when driven by modulated signals, a 64-QAM modulated signal with 100-MHz modulation bandwidth (BW_m) and 6.6-dB PAPR was used to measure the CM-DPA at 4.4 and 5.2 GHz. The fabricated CM-DPA was linearized by digital predistortion (DPD) with the memory

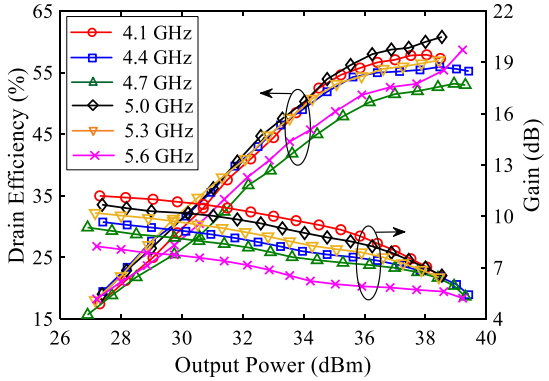

Fig. 22. Measured DE and gain versus output power at different frequencies.

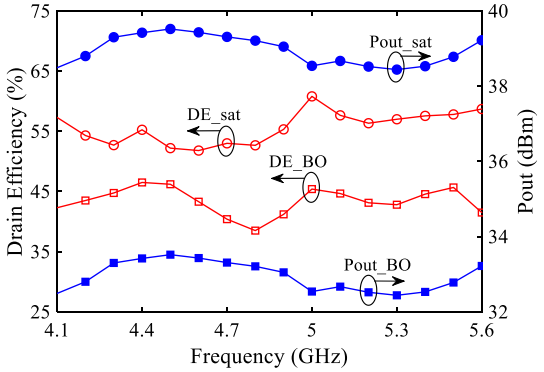

Fig. 23. Measured DE and output power versus frequency.

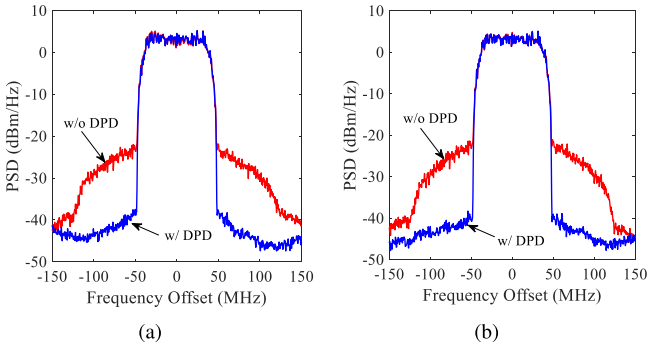

Fig. 24. Output spectrum of the proposed CM-DPA with and without DPD linearization at (a) 4.4 and (b) 5.2 GHz.

polynomial model. Fig. 24 shows the output spectrum with and without DPD at 4.4 and 5.2 GHz. The measured ACLRs were −30.4/−31.3 dBc at 4.4 GHz and −30.3/−30.5 dBc at 5.2 GHz without DPD. After DPD, the ACLRs were improved to −45.8/−46.5 dBc at 4.4 GHz and −45.4/−46.6 dBc at 5.2 GHz. Meanwhile, 32.5-dBm average output power was achieved with an average DE of 42.3% and 38.6% at the two frequency bands. Fig. 25 shows the output signal constellation, where the rms error vector magnitude (EVM_{rms}) of −23.7 and −23.2 dB is achieved at 4.4 and 5.2 GHz without DPD. After the DPD performed, the EVM_{rms} can be improved to −37.1 and −36.8 dB, respectively, at these two frequencies. The AM-AM and AM-PM characteristics with and without DPD are also shown in Fig. 26.

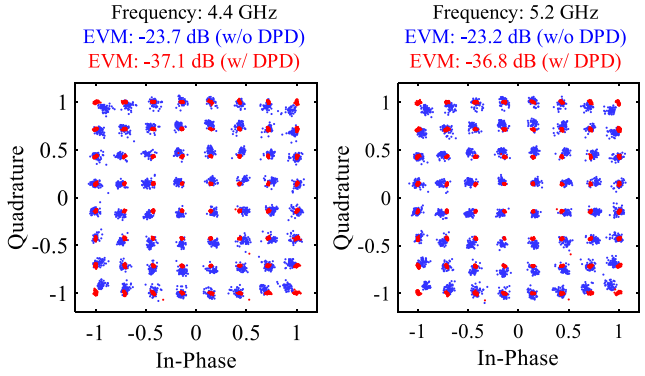

Fig. 25. Measured output constellation at 4.4 and 5.2 GHz under 64-QAM signal stimulation with 100-MHz bandwidth and 6.6-dB PAPR before and after DPD.

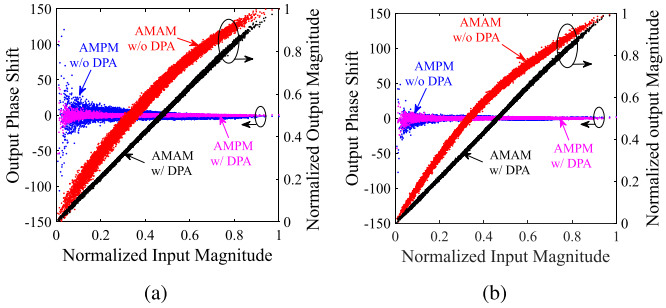

Fig. 26. AM-AM and AM-PM of the proposed CM-DPA with and without DPD linearization at (a) 4.4 and (b) 5.2 GHz.

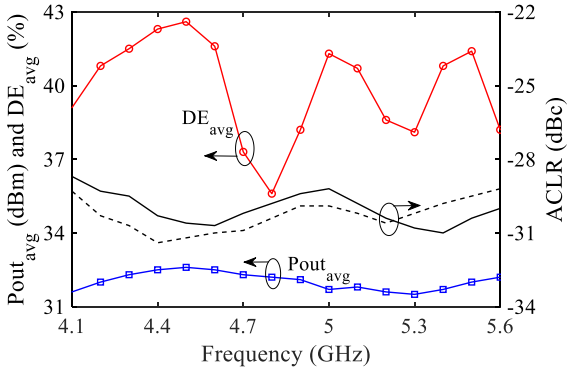

Fig. 27. Measured average DE, average output power, and ACLR versus frequency.

The nonlinearity of CM-DPA can be corrected very well after DPD. At other operation frequencies within the realized bandwidth, the ACLRs of the CM-DPA can also be improved to better than −45 dBc after DPD is performed, and the measured results are omitted here for saving space. To better present the wideband performance, the proposed CM-DPA was measured using the same 64-QAM 100-MHz modulated signal from 4.1 to 5.6 GHz with a step of 0.1 GHz. The measured average DE and output power versus the operation frequency are shown in Fig. 27. The average efficiency of 35.6%–42.7% is achieved within the operation band with an average output power of 31.5–32.6 dBm. Meanwhile, the fabricated CM-DPA achieves measured ACLR from −28.7 to −31.4 dBc.

TABLE I
PERFORMANCE COMPARISON OF STATE-OF-ART WIDEBAND INTEGRATED GaN PAs WITH BACK-OFF EFFICIENCY ENHANCEMENT

Ref.(Year)	This Work	[26]2014	[27]2015	[28]2018	[29]2019	[30]2019	[17]2021	[18]2021	[36]2016
Technique	CM-DPA	Asym. DPA	Asym. DPA	DPA	DPA	DPA	DEPA	Unbalanced Amplifier	CM-DPA$^{\natural}$
Frequency(GHz)	4.1-5.6	5.8-8.8	2.1-2.7	5.1-5.9	4.5-6.0	4.5-5.2	3.2-5.2	4.5-6.5	1.65-2.75
BW(GHz/%)	1.5/30.9	3.0/42	0.6/25.2	0.8/14.6	1.5/28.9	0.7/14.5	2.0/47.6	2.0/37.0	1.1/50
Pmax(dBm)	38.4-39.5	35-36	40.0-41.0	36.0-38.7	35-36	40.4-41.2	40.4-41.7$^{\sharp}$	32.2-34.3	44.5-46.3
DE@Sat.(%)	51.7-60.8	N/A	N/A	N/A	43-49	55-63	46-56$^{\sharp}$	27-37	60-77
PAE@Sat.(%)	41.2-49	30-45	N/A	43.2-47.3	31.8-40.7	45-51	N/A	N/A	N/A
OBO (dB)	6	9	7.6	6	6	6	8	6	6
DE@OBO (%)	38.5-46.5	N/A	48-62	32-51	24-32	47-50	35-50$^{\sharp}$	27-40	52-66
PAE@OBO (%)	32.4-39.8	31-39	N/A	31.6-49.5	22.5-27.6	40-45	N/A	N/A	N/A
Gain (dB)	8.3-11.2	8.5-9	12-14	14.4-17.3	7.6-11.6	8-11	8.5-11.5	8-11	9.3-11.7
Modulation	64-QAM	256-QAM	N/A	64/256-QAM	64-QAM	N/A	N/A	256-QAM	N/A
BW_m (MHz)	100	20	10	80	100	40	100	100/200	20
PAPR (dB)	6.6	8.5	7.2	10	8	7.7	7.8	7.2	7.5
Carrier Freq. (GHz)	4.4/5.2	7.0	2.14-2.65	5.8	5.0	4.9	3.2-5.2	5.0	1.65-2.75
$Pout_{avg}$ (dBm)	32.5	27.6	N/A	23.5/21.5	29.3	33	33.3-34.1	25.5	37.5-39
DE_{avg} (%)	42.3/38.6	38	45-53	N/A	29	51	35.7-47	30	46-62
EVM_{rms} (dB)	-23.7/-23.2	N/A	N/A	-28/-32	-30.5	N/A	N/A	-28.6/-26.9	N/A
ACLR (dB)	<-30.3	<-41	N/A	N/A	<-34	<-29	<-26.3	<-32.5	<-27.5
Chip Size (mm×mm)	2.6×3.0	2.9×2.9	2.65×1.9*	2.5×1.6	3.0×2.8	2.2×2.1	3.4×3.0	2.8×2.8	N/A
GaN Process (nm)	250	250	250	250	250	250	250	250	N/A

* - Partial output network is off-chip
$^{\sharp}$ - Pulse CW measurement with 10% duty cycle
$^{\natural}$ - PCB level fabrication using commercial GaN transistors

D. Performance Comparison

The performance of the proposed CM-DPA is summarized in Table I and compared with other state-of-art GaN MMIC PAs. The proposed CM-DPA achieves comparable efficiency within 30.9% fractional bandwidth. Compared with other DPA chips, the proposed CM-DPA shows better comprehensive performance in bandwidth and efficiency. The DEPA [17] achieves wider bandwidth with comparable efficiency performance, but it uses more complex structure with larger size. The unbalanced amplifier [18] also shows wider bandwidth while the efficiency is lower due to its lossy architecture. In summary, the proposed CM-DPA is a potential architecture to realize broadband MMIC PAs with high back-off efficiency.

V. CONCLUSION

The theory and implementation of fully integrated GaN DPA using CM combining load was presented in this article. Thanks to the introduction of the CM combining load, different CM load modulation can be realized using only one IIN, which reduced the complexity of the circuit structure. Using the proposed architecture, the bandwidth of MMIC DPAs can be successfully extended while maintaining good efficiency. The realized CM-DPA chip presents good back-off efficiency with 30.9% fractional bandwidth in the sub-6-GHz band. Meanwhile, from the results of modulated signal measurements, the proposed CM-DPA also showed good linearity with and without DPD correction. The simulation and measurement results validated the broadband and high back-off efficiency performance of the proposed CM-DPA architecture.

REFERENCES

[1] K. D. Holzer, W. Yuan, and J. S. Walling, "Wideband techniques for outphasing power amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 9, pp. 2715–2725, Sep. 2018.

[2] S. Li, T. Chi, J.-S. Park, H. T. Nguyen, and H. Wang, "A 28-GHz flip-chip packaged Chireix transmitter with on-antenna outphasing active load modulation," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1243–1253, May 2019.

[3] V. Vorapipat, C. S. Levy, and P. M. Asbeck, "Voltage mode Doherty power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1295–1304, May 2017.

[4] V. Vorapipat, C. S. Levy, and P. M. Asbeck, "A class-G voltage-mode Doherty power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3348–3360, Dec. 2017.

[5] Y. Cho, K. Moon, B. Park, J. Kim, and B. Kim, "Voltage-combined CMOS Doherty power amplifier based on transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 11, pp. 3612–3622, Sep. 2016.

[6] S. Hu, S. Kousai, J. S. Park, O. L. Chlieh, and H. Wang, "Design of a transformer-based reconfigurable digital polar Doherty power amplifier fully integrated in bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1094–1106, May 2015.

[7] S. Hu, S. Kousai, and H. Wang, "a broadband mixed-signal CMOS power amplifier with a hybrid Class-G Doherty efficiency enhancement technique," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 598–613, Mar. 2016.

[8] S. Hu, F. Wang, and H. Wang, "A 28-/37-/39-GHz linear Doherty power amplifier in silicon for 5G applications," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1586–1599, Jun. 2019.

[9] J. Pang, S. He, C. Huang, Z. Dai, J. Peng, and F. You, "A post-matching Doherty power amplifier employing low-order impedance inverters for broadband applications," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4061–4071, Dec. 2015.

[10] W. Shi, S. He, J. Peng, and J. Wang, "Digital dual-input Doherty configuration for ultrawideband application," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7509–7518, Sep. 2020.

[11] J. Pang, Z. Dai, Y. Li, M. Li, and A. Zhu, "Multiband dual-mode Doherty power amplifier employing phase periodic matching network and reciprocal gate bias for 5G applications," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 6, pp. 2382–2397, Jun. 2020.

[12] Y. Komatsuzaki, R. Ma, S. Sakata, K. Nakatani, and S. Shinjo, "A dual-mode bias circuit enabled GaN Doherty amplifier operating in 0.85–2.05 GHz and 2.4–4.2 GHz," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 277–280.

[13] D. J. Shepphard, J. Powell, and S. C. Cripps, "An efficient broadband reconfigurable power amplifier using active load modulation," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 6, pp. 443–445, Jun. 2016.

[14] J. Pang *et al.*, "Analysis and design of highly efficient wideband RF-input sequential load modulated balanced power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 5, pp. 1741–1753, May 2020.

[15] L. Chen, H. Liu, J. Hora, J. A. Zhang, K. S. Yeo, and X. Zhu, "A monolithically integrated single-input load-modulated balanced amplifier with enhanced efficiency at power back-off," *IEEE J. Solid-State Circuits*, vol. 56, no. 5, pp. 1553–1564, May 2021.

[16] P. Saad, R. Hou, R. Hellberg, and B. Berglund, "The continuum of load modulation ratio from Doherty to traveling-wave amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 12, pp. 5101–5113, Dec. 2019.

[17] G. Lv, W. Chen, X. Chen, F. M. Ghannouchi, and Z. Feng, "A fully integrated 47.6% fractional bandwidth GaN MMIC distributed efficient power amplifier with modified input matching and power splitting network," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 6, pp. 3132–3145, Jun. 2021.

[18] G. R. Nikandish, R. B. Staszewski, and A. Zhu, "Unbalanced power amplifier: An architecture for broadband back-off efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 367–381, Feb. 2021.

[19] H. Kang *et al.*, "Octave bandwidth Doherty power amplifier using multiple resonance circuit for the peaking amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 2, pp. 583–593, Feb. 2019.

[20] W. Shi *et al.*, "The influence of the output impedances of peaking power amplifier on broadband Doherty amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 8, pp. 3002–3013, Aug. 2017.

[21] X.-H. Fang, H.-Y. Liu, K.-K. M. Cheng, and S. Boumaiza, "Modified Doherty amplifier with extended bandwidth and back-off power range using optimized peak combining current ratio," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5347–5357, Dec. 2018.

[22] F. Wang and H. Wang, "A high-power broadband multi-primary DAT-based Doherty power amplifier for mm-Wave 5G applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 6, pp. 1668–1681, Jun. 2021.

[23] Y. Yin *et al.*, "A broadband switched-transformer digital power amplifier for deep back-off efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 2997–3008, Nov. 2020.

[24] N. S. Mannem, T.-Y. Huang, and H. Wang, "Broadband active load-modulation power amplification using coupled-line baluns: A multi-frequency role-exchange coupler Doherty amplifier architecture," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 3109–3122, Oct. 2021.

[25] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, and N. Rorsman, "A wideband and compact GaN MMIC Doherty amplifier for microwave link applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 922–930, Feb. 2013.

[26] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, and C. Fager, "A GaN MMIC modified Doherty PA with large bandwidth and reconfigurable efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3006–3016, Dec. 2014.

[27] S. Jee *et al.*, "Asymmetric broadband Doherty power amplifier using GaN MMIC for femto-cell base-station," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2802–2810, Sep. 2015.

[28] S.-H. Li, S. S. H. Hsu, J. Zhang, and K.-C. Huang, "Design of a compact GaN MMIC Doherty power amplifier and system level analysis with X-parameters for 5G communications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5676–5684, Dec. 2018.

[29] G. Nikandish, R. B. Staszewski, and A. Zhu, "Bandwidth enhancement of GaN MMIC Doherty power amplifiers using broadband transformer-based load modulation network," *IEEE Access*, vol. 7, pp. 119844–119855, 2019.

[30] G. Lv, W. Chen, X. Liu, F. M. Ghannouchi, and Z. Feng, "A fully integrated C-band GaN MMIC Doherty power amplifier with high efficiency and compact size for 5G application," *IEEE Access*, vol. 7, pp. 71665–71674, 2019.

[31] A. M. E. Abounemra *et al.*, "Systematic design methodology of broadband Doherty amplifier using unified matching/combining networks with an application to GaN MMIC design," *IEEE Access*, vol. 9, pp. 5791–5805, 2021.

[32] T.-W. Li, M.-Y. Huang, and H. Wang, "Millimeter-wave continuous-mode power amplifier for 5G MIMO applications," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 3088–3098, Jul. 2019.

[33] A. Alizadeh, M. Frounchi, and A. Medi, "Class-J_{23} power amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 10, pp. 3664–3675, Oct. 2019.

[34] D. Wang, W. Chen, X. Chen, F. M. Ghannouchi, and Z. Feng, "A broadband millimeter-wave continuous-mode Class-F power amplifier based on the deembedded transistor model," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 6, pp. 609–612, Jun. 2020.

[35] X. Chen, W. Chen, F. M. Ghannouchi, and Z. Feng, "A 1.1 GHz bandwidth, 46%–62% efficiency continuous mode Doherty power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4.

[36] X. Chen, W. Chen, F. M. Ghannouchi, Z. Feng, and Y. Liu, "A broadband Doherty power amplifier based on continuous-mode technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4505–4517, Dec. 2016.

[37] G. Naah and R. Giofre, "Empowering the bandwidth of continuous-mode symmetrical Doherty amplifiers by leveraging on fuzzy logic techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 3134–3147, Jul. 2020.

[38] W. Shi *et al.*, "Broadband continuous-mode Doherty power amplifiers with noninfinity peaking impedance," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 1034–1046, Feb. 2018.

[39] W. Shi *et al.*, "Design and analysis of continuous-mode Doherty power amplifier with second harmonic control," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 7, pp. 2247–2251, Jul. 2021.

[40] S. C. Cripps, P. J. Tasker, A. L. Clarke, J. Lees, and J. Benedikt, "On the continuity of high efficiency modes in linear RF power amplifiers," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 10, pp. 665–667, Oct. 2009.

[41] S. Saxena, K. Rawat, and P. Roblin, "Continuous class-B/J power amplifier using a nonlinear embedding technique," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 7, pp. 837–841, Jul. 2017.

[42] J. Moon, S. Jee, J. Kim, J. Kim, and B. Kim, "Behaviors of class-F and class-F^{-1} amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1937–1951, Jun. 2012.

[43] J. Pang, S. He, Z. Dai, C. Huang, J. Peng, and F. You, "Design of continuous-mode GaN power amplifier with compact fundamental impedance solutions on package plane," *IET Microw., Antennas Propag.*, vol. 10, no. 10, pp. 1056–1064, Jul. 2016.

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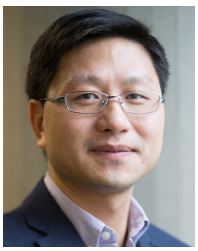

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