BSIM6: Symmetric Bulk MOSFET Model

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ABSTRACT

BSIM6 Model is the next generation Bulk RF MOSFET Model. Model uses charge based core with all physical models adapted from BSIM4 model. Model fulfills all quality tests e.g. Gummel symmetry and AC symmetry test and shows correct slopes for harmonic balance simulation. Model has been tested in DC, small signal, transient and RF simulation and shows excellent convergence in circuit simulation. Model is under standardization at Compact Model Council.

Keywords: BSIM6, BSIM4, Symmetry, Analog, RF, MOSFET, Compact Model

1 INTRODUCTION

BSIM4 was selected as industry standard compact MOSFET model in 2000 [1] and since then, its been used by major semiconductor companies and design houses. The beauty of BSIM4 lies in the flexibility to fit data from different technologies starting from 350nm to 28nm in production today [2]. The compact model consists of two main components - core model and real device models. The core is the ideal long channel model, which is threshold voltage based in case of BSIM4 [3]–[5]. The real device models are the models used to capture the effects in real devices e.g. short channel effect, channel length modulation, velocity saturation effect, quantum mechanical effect etc. The real device models of BSIM4 are physically derived expressions for different effects and have excellently captured the silicon data and provided accuracy in parameter extraction. Although BSIM4 is being used for all types of designs, Analog and RF designers have complained on symmetry issue in the model. To address this issue, BSIM group started BSIM6 development in late 2010. BSIM6 inherits all real device effects from BSIM4 but guarantees symmetry around V_{DS}=0 [6]–[10].

2 BSIM6 Model

BSIM6 has charge based core, which is derived from Poisson's solution for long channel MOSFET [11]–[13]. The reason for choosing charge based core is due to its physical nature as well as accuracy along with computational efficiency. Using Gauss' law, we have

$$V_G - V_{FB} - \Psi_S = -\frac{Q_{si}}{C_{ox}} = -\frac{Q_i + Q_b}{C_{ox}} \tag{1}$$

where V_G is the is the applied gate voltage, V_{FB} is the flat band voltage, Ψ_S is the surface potential. BSIM6 is the body referenced model, where gate, drain and source node voltages are with respect to applied body voltage. Q_i and Q_b are the inversion and bulk charge densities respectively. For uniformly doped MOSFET with gradual channel approximation, we have [11],

$$\frac{Q_{si}}{\Gamma C_{ox}\sqrt{V_t}} = \mp\sqrt{e^{-\frac{\Psi_S}{V_t}} + \frac{\Psi_S}{V_t} - 1 + e^{-\frac{2\Phi_F + V_{ch}}{V_t}}\left(e^{\frac{\Psi_S}{V_t}} - \frac{\Psi_S}{V_t} - 1\right)} \tag{2}$$

The -ve sign is taken when Ψ_S is positive and vice-versa. The bulk charge is given by

$$\frac{Q_b}{\Gamma C_{ox}\sqrt{V_t}} = \mp\sqrt{e^{-\frac{\Psi_S}{V_t}} + \frac{\Psi_S}{V_t} - 1} \tag{3}$$

and using (1) and (3), we have

$$V_G - V_{FB} - \Psi_S = -\frac{Q_i}{C_{ox}} \pm \Gamma\sqrt{V_t\left(e^{-\frac{\Psi_S}{V_t}} + \frac{\Psi_S}{V_t} - 1\right)} \tag{4}$$

where V_t is the thermal voltage and Γ is the body effect coefficient. Defining pinch-off potential as $\Psi_S = \Psi_P$, when inversion charge density is zero, above equation can be written as,

$$V_G - V_{FB} - \Psi_P = sign(\Psi_P)\Gamma\sqrt{V_t\left(e^{-\frac{\Psi_P}{V_t}} + \Psi_P - 1\right)} \tag{5}$$

Although above equation is an implicit equation for Ψ_P, the analytical solution does exist for it (thanks to Francois Krummenacher) [14]. For Ψ_S greater than few V_t, from (2) and (3), we have

$$-\frac{Q_i}{\Gamma C_{ox}\sqrt{V_t}} = \sqrt{\frac{\Psi_S}{V_t} + e^{\frac{\Psi_S - 2\Phi_F - V_{ch}}{V_t}}} - \sqrt{\frac{\Psi_S}{V_t}} \tag{6}$$

For charge based models, the inversion charge linearization is defined as [13],

$$-\frac{Q_i}{C_{ox}} = n_q(\Psi_P - \Psi_S) \tag{7}$$

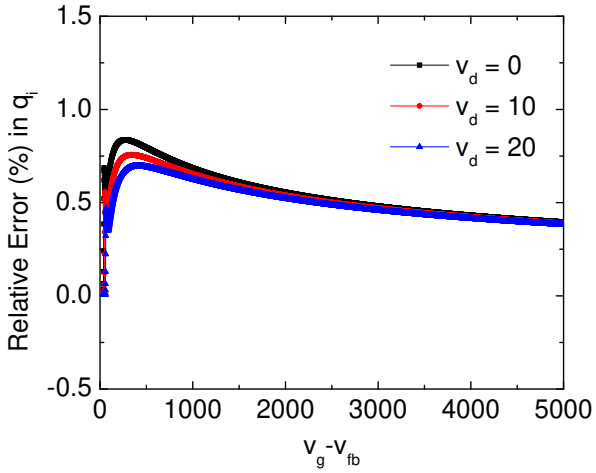


Figure 1: Relative error in the inversion charge density as a function of gate bias for different drain biases. Accuracy is better than 1% for all bias conditions.

where n_q is the slope factor. Using (7) in (6), we can get [13]

$$2q_i + ln(q_i) + ln\left[\frac{4n_q}{\gamma}\left(\frac{n_q}{\gamma}q_i + \sqrt{\psi_p - 2q_i}\right)\right] = \psi_p - 2\phi_f - v_{ch} \tag{8}$$

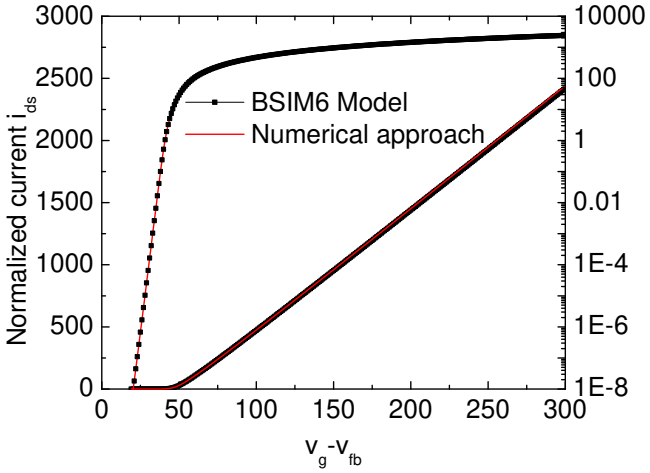
where $q_i = \frac{-Q_i}{2n_q C_{ox} V_t}$ is the normalized inversion charge density and $\psi_p = \frac{\Psi_P}{V_t}$ is the normalized pinch-off potential.

Eq. (8) is the core charge density equation, whose accuracy greatly affects the accuracy in final charge and current expressions. In earlier approaches [12], [13], both q_i terms inside second *log* term were neglected for evaluation of charge density at source and drain end. We found that using those approaches, the error could be in the order 2-6%. ***For BSIM6, eq.*** (8) ***has been analytically solved without ignoring first*** q_i ***term***[6]–[9]. Fig. 1 shows the relative error in q_i vs. normalized gate bias using BSIM6 compared to numerical solution, where it can be seen that *accuracy is better than 1%* for entire bias range.

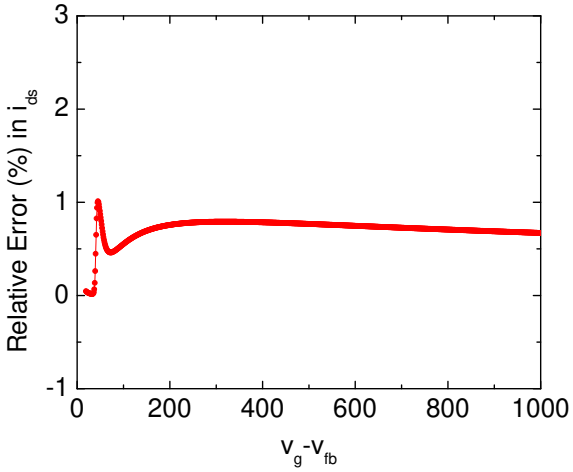
The drain to source current is obtained using well known drift-diffusion model as follows,

$$i_{ds} = \frac{(q_s^2 + q_s) - (q_d^2 + q_d)}{\frac{1}{2}\left[1 + \sqrt{1 + (\lambda_c(q_s - q_d))^2}\right]} \tag{9}$$

where q_s and q_d are the normalized charge densities at source and drain end respectively. The denominator term in above equation accounts for velocity saturation for short channel transistors; where $\lambda_c = \frac{2\mu_{eff}V_t}{VSAT \cdot L_{eff}}$ [15]. Note, the drain charge density q_d is effective charge density at drain, which is obtained using effective drain voltage accounting for V_d to V_{dsat} transition [16]. Fig. 2 show comparison of normalized current from BSIM6 model with numerical results [11], where error is in the order of 1%.



(a) Normalized i_{ds} vs. $v_g - v_{fb}$ using (9)



(b) Relative error in normalized current vs. $v_g - v_{fb}$.

Figure 2: Comparison of BSIM6 Model with numerical surface potential approach. It can be seen that model provides excellent accuracy compared to numerical surface potential approach.

3 Results and Discussion

During BSIM6 development, goal has been to keep in mind the smooth transition of BSIM4 users but providing symmetry around $V_{ds} = 0$. Most of the real device effect models are similar to BSIM4 model. Even if some of the real device models are not same as BSIM4, we have ensured that the parameter names are the same for easier extraction based on BSIM4 experience. The real device effect models were updated to ensure symmetry during DC and AC simulations.

Fig. 3, 4 show the famous Gummel symmetry test [17], [18] results for BSIM6 model. The drain current and all of its derivatives are continuous up to any order depending on the value of DELTA parameter, whose maximum value has been fixed to 0.5 to ensure that third derivative is always con-

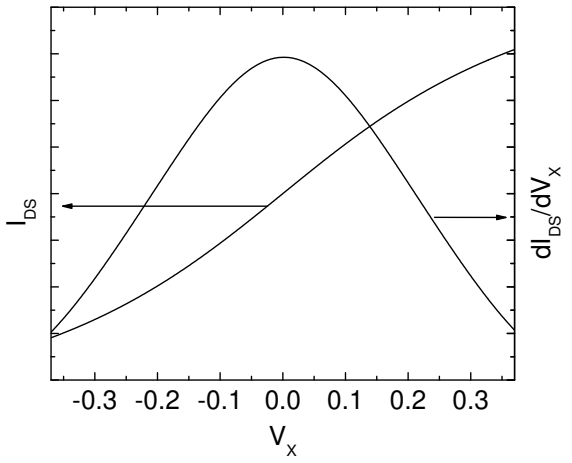


Figure 3: Gummel Symmetry Test: I_{DS} and $\frac{dI_{DS}}{dV_X}$ vs. $V_X = V_D$, where drain and source biases are swept in opposite direction.

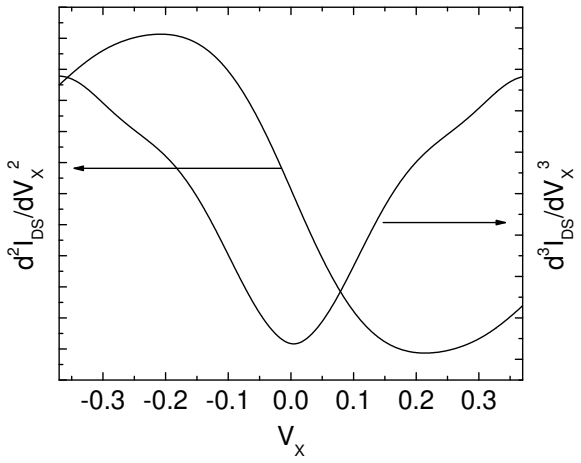


Figure 4: Gummel Symmetry Test: $\frac{d^2I_{DS}}{dV_X^2}$ and $\frac{d^3I_{DS}}{dV_X^3}$ vs. $V_X = V_D$, where drain and source biases are swept in opposite direction.

tinuous. The charges associated with drain and source nodes are obtained using Ward-Dutton charge partitioning scheme [19]. Fig. 5, 6 and 7 show the long channel capacitance plots, where it is shown that model behaves physically across bias range. From fig. 5 and 6, it is evident that transcapacitances C_{gs} and C_{gd} overlap each other for $V_{ds} = 0$ and transcapacitances C_{sg} and C_{dg} also overlap each other for $V_{ds} = 0$, which is an important condition for good compact model. Fig. 7 show the capacitances' behavior with drain bias, where it is shown $C_{gs} = C_{gd}$ and $C_{sg} = C_{dg}$ at $V_{ds} = 0$. The axis values are not shown for confidentiality reasons.

Another important quality test for compact MOSFET model is AC symmetry test proposed by Colin McAndrew [20]. It is must for a compact model to qualify this test for correct harmonics behavior. In fact, we had to update the junction capacitance model taken from BSIM4 to satisfy this test. Fig. 8 - 10 show the capacitance symmetry plots and their derivatives for BSIM6 model, which clearly demonstrate that model satisfies AC symmetry test. Fig. 11 and 12 show the model validation on measured characteristics from medium technology node. Model matches well with measured characteristics which demonstrate that BSIM6 has similar flexibility as BSIM4 for data fitting.

BSIM6 is under standardization at Compact Model Council [1]. Model has been rigorously tested and satisfies all quality tests for compact MOSFET model [20].

4 ACKNOWLEDGEMENT

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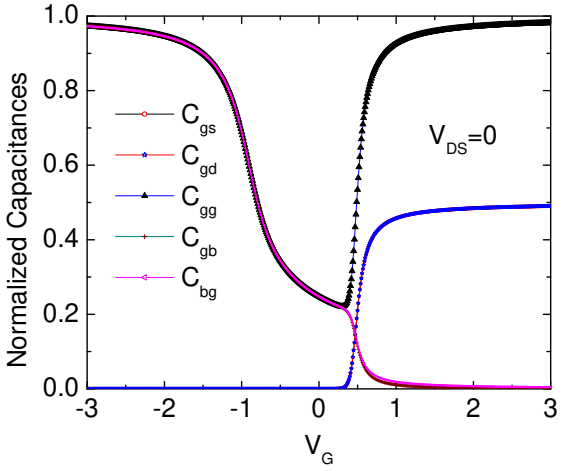

Figure 5: Normalized capacitances from BSIM6 model. Quantum mechanical and poly depletion effects have been added in the model (not shown here).

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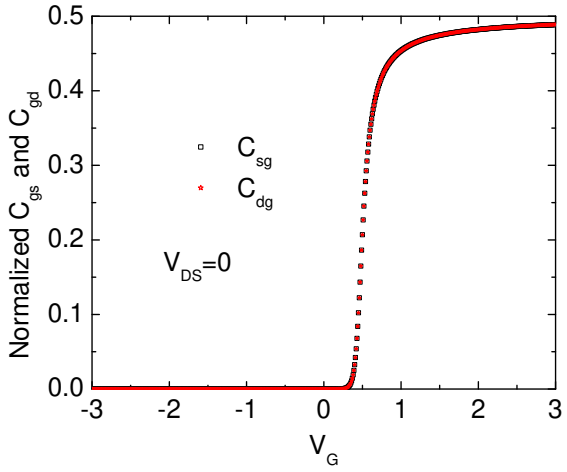

Figure 6: Transcapacitances C_{sg} and C_{dg} vs V_G for $V_{ds} = 0$. Both capacitances should be same at $V_{ds} = 0$ for good compact model.

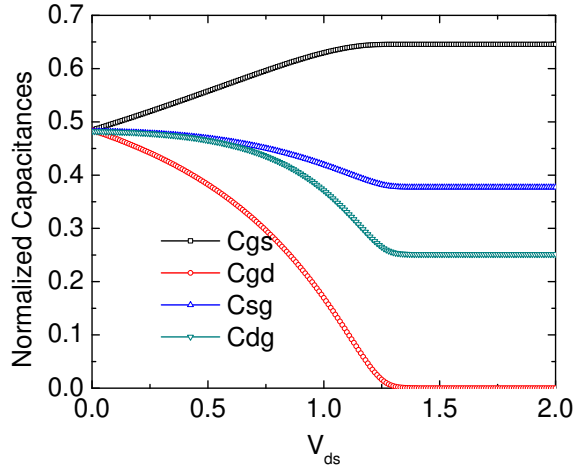

Figure 7: Transcapacitances associated with source and drain nodes with drain bias. C_{gs} and C_{gd} should be exactly same at $V_{ds} = 0$ for good compact model. Same is true for C_{sg} and C_{dg}.

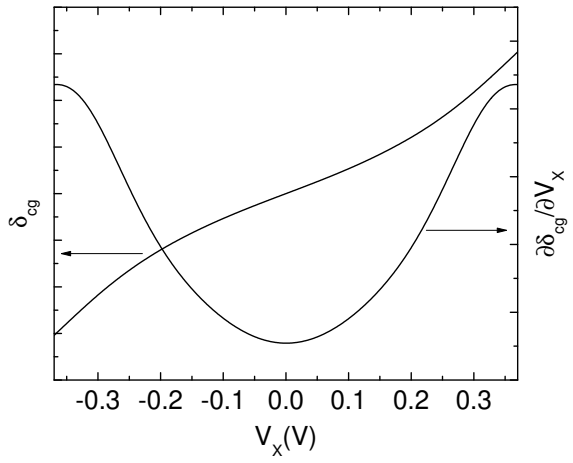

Figure 8: AC Symmetry Test: $\delta_{cg} = \frac{i_{g-}}{i_{g+}} = \frac{C_{gs}-C_{gd}}{C_{gs}+C_{gd}}$ and its derivative vs. $V_X = V_D$, where drain and source biases are swept in opposite direction.

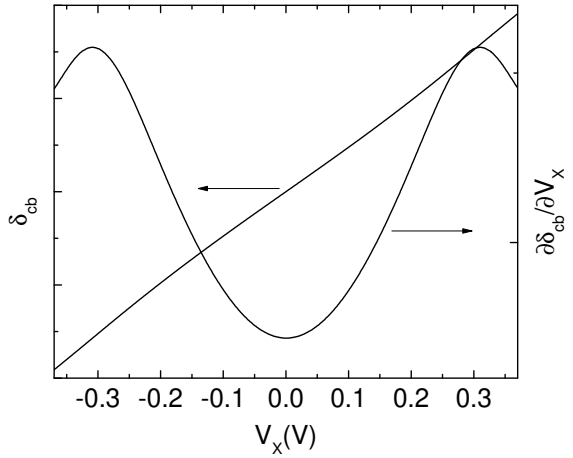

Figure 9: AC Symmetry Test: $\delta_{cb} = \frac{i_{b-}}{i_{b+}} = \frac{C_{bs}-C_{bd}}{C_{bs}+C_{bd}}$ and its derivative vs. $V_X = V_D$, where drain and source biases are swept in opposite direction.

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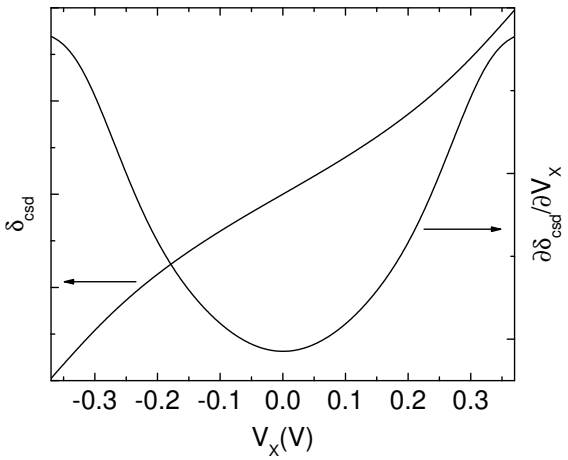
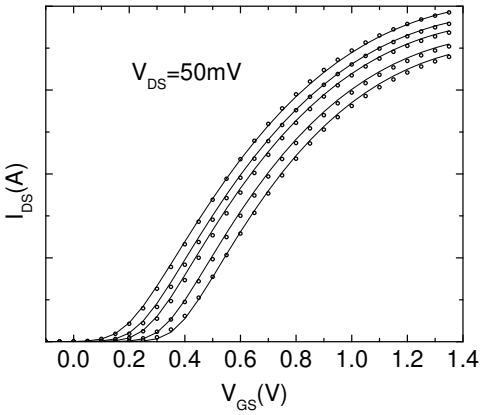
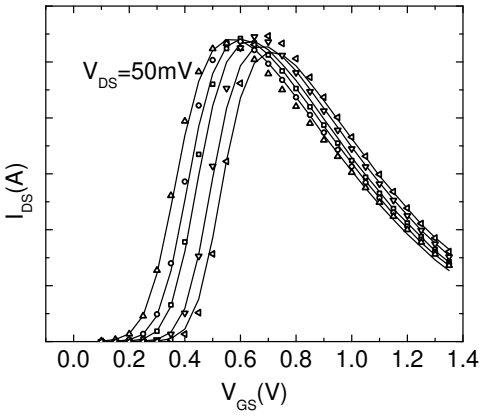


Figure 10: AC Symmetry Test: $\delta_{csd} = \frac{(i_{s-}+i_{d-})+(i_{s+}-i_{d+})}{(i_{s-}-i_{d-})+(i_{s+}+i_{d+})} = \frac{C_{ss}-C_{dd}}{C_{ss}+C_{dd}}$ and its derivative vs. $V_X = V_D$, where drain and source biases are swept in opposite direction.

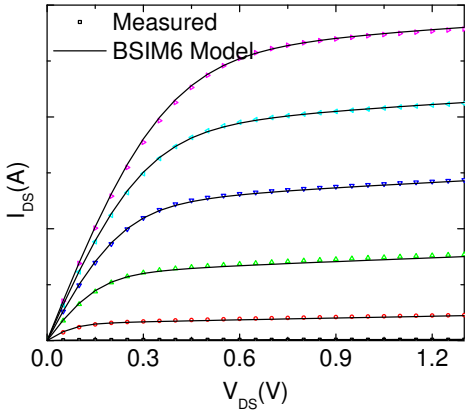


(a)



(b)

Figure 11: Model validation on measured transfer characteristics: (a) I_{DS} vs. V_{GS} for $V_{DS} = 50mV$. (b) g_m vs. V_{GS} for $V_{DS} = 50mV$.



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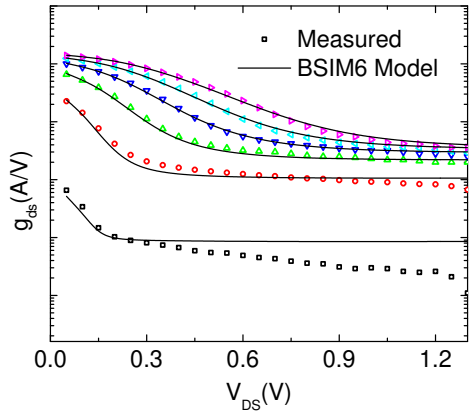

(b)

Figure 12: Model validation on measured output characteristics: (a) I_{DS} vs. V_{DS} and (b) g_{ds} vs. V_{DS} for different gate voltages.

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