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Built-in Loopback Test for IC RF Transceivers

Jerzy J. Dąbrowski, *Member, IEEE*, and Rashad M. Ramzan, *Student Member, IEEE*

***Abstract*—The essentials of the on-chip loopback test for integrated RF transceivers are presented. The available on-chip baseband processor serves as a tester while the RF front-end is under test enabled by on-chip test attenuator and in some cases by an offset mixer, too. Various system-level tests, like bit error rate, error vector magnitude, or spectral measurements are discussed. By using this technique in mass production, the RF test equipment can be largely avoided and the test cost reduced. Different variants of the loopback setup including the bypassing technique and RF detectors to boost the chip testability are considered. The existing limitations and tradeoffs are discussed in terms of test feasibility, controllability, and observability versus the chip performance. The fault-oriented approach supported by sensitization technique is put in contrast to the functional test. Also the impact of production tolerances is addressed in terms of a simple statistical model and the detectability thresholds. This paper is based on the present and previous work of the authors, largely revised and upgraded to provide a comprehensive description of the on-chip loopback test. Simulation examples of practical communication transceivers such as WLAN and EDGE under test are also included.**

***Index Terms*—Built-in self test (BiST), design for testability (DfT), loopback test, on-chip test, RF test, RF transceivers, structural test.**

I. Introduction

OVER THE years of its development, production test of digital ICs has reached a significant degree of maturity. This progress has been enabled by several techniques, such as fault simulation, test-pattern generation, and the built-in-self-test (BiST). Unlike this, much less success has been achieved in the analog/RF and mixed-signal ICs domain, where functional testing has been widely used and the major advances have been in the capabilities of expensive automatic test equipment (ATE). At present, the advancing complexity and performance of mixed-signal and RF ICs are pushing functional test methods and the ATE to the edge of their limits [1], [2]. In this context, alternative approaches based on analog fault modeling, design for testability (DfT) and BiST, so far not appreciated by industry, are appealing and can alleviate the problem [3]. While borrowed from the digital "world", the underlying concepts appear very different due to the continuous nature of analog/RF circuits, their sensitivity to small parameter variations and the problem of tolerances as well.

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The authors are with the Department of Electrical Engineering, Linköping University, SE-581 83 Linköping, Sweden (e-mail: jdab@isy.liu.se; rashad@isy.liu.se).

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In fact, for the analog ICs of low- or mid-frequency a couple of DfT/BiST solutions have been proposed [3] (including the IEEE Std. 1149.4). For RF ICs, however, it has not been the case because of a variety of phenomena, typical of RF circuits, such as parasitic coupling, loading, noise, etc., [4] that result in tradeoffs between built-in testability and the required chip performance. The tradeoffs and the chip area overhead, which are key factors in RF design for test, can be largely mitigated by sharing the available on-chip resources and chip reconfiguration technique [5], [6].

For a highly integrated mixed-signal circuit, its analog-to-digital (A/D) and digital-to-analog (D/A) converters and a digital signal processor (DSP) available on one chip can be used to test the analog/RF part. In this case, the DSP can serve both as a test pattern generator and response analyzer implementing in this way the BiST technique. Usually, the analog/RF BiST requires also other circuits available on chip, like switches or attenuators, to enable signal paths for the test mode. In particular, digital IC radio transceivers can be subjected to BiST by using a loopback setup [7]–[9]. The advantage of this approach is that all the RF front-end blocks are under test and catastrophic defects can be easily detected. A loopback element, usually an attenuator, between the transmitter output and receiver input is required to match the signal level. In normal operation mode the loopback attenuator can be disabled so that the transceiver performance is practically not affected [30]. On the other hand, this technique makes parametric fault detection and fault diagnosis difficult for limited controllability and observability. In other words, the test response from a given RF block (such as an amplifier, mixer, filter) can be obscured by the transfer function and parameter variations of the following blocks in the signal path. Also, the quality of test stimuli after passing a chain of blocks cannot be guaranteed. This problem has been discussed, e.g., in [10] for the functional tests in terms of circuit parameter variations and the fault coverage. For an arbitrary analog system, defined as a signal path with the primary input and output, only some of the block-level tests can be translated to system-level tests.

To improve testability of RF transceivers, a concept of *structural test* (i.e., fault-oriented) [11]–[15] supported by signal path sensitization can be implemented [16], [17]. In another approach, called *alternate test* (alternative test), the standard specs are measured indirectly based on equivalent measurements [18]–[21].

Both the fault-oriented test and the specs-oriented alternative test claim simple and fast measurements to replace detailed specification tests which apply at the block and system-level as well. Usually, in the loopback test (LBT) we depart from the detailed block-level tests, thereby saving the test time and the test cost. Also we are interested in optimizing the LBT for its maximum efficiency in terms of fault detectability and the measurement performance, respectively.

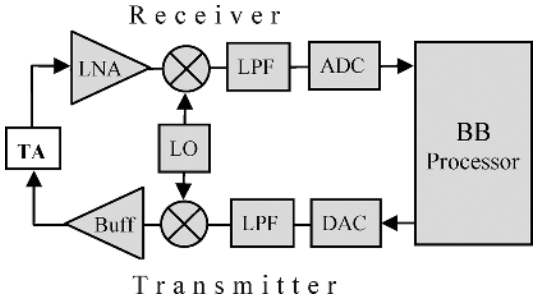

Fig. 1. Direct loopback test setup for IC transceiver.

In this paper, the essentials of the on-chip LBT for integrated RF transceivers are presented. In Section II, the feasibility of the LBT for various transceiver architectures is discussed. It is shown that in most cases not only an attenuator but also an extra mixer placed between the Tx output and Rx input is needed. A detailed discussion on the offset loopback setup suitable for TRx with a shared local oscillator and direct RF modulation is given in Section III. In Section IV different loopback measurements are presented in terms of the fault-oriented and specs-oriented approach. Test sensitization techniques that improve fault detectability are discussed in Section V. Section VI addresses the LBT setup with enhanced controllability and observability achieved by means of the bypassing technique and RF detectors. Masking effects due to parameter tolerances are analyzed in Section VII. In Section VIII, simulation results of two typical transceivers under LBT are presented. Conclusions are formulated in the last section.

II. Feasibility of Loopback Test

For chips containing a transmitter and a receiver the LBT is an attractive technique. To enable the on-chip loopback setup the test signal from the Tx must be fed back to the Rx via a test attenuator (TA) as shown in Fig. 1. This approach is consistent provided Tx and Rx operate at the same frequency and the frequency synthesizer (LO) only serves up- and down-conversion, respectively, while the modulation process is performed at baseband. Those conditions are sufficient unless the frequencies required for up- and down-conversion are different, and the LO only can provide one of them at a time. In other words, unless LO has one output, which in the normal transmit- and receive mode toggles between the two frequencies. This would be typical of a one-step Tx and a low-IF Rx [33, Ch.5], which operate at the same radio-frequency but the up-conversion proceeds from baseband to RF while the down-conversion from RF to non-zero IF. In this case the LBT can be enabled in two ways. If the system is narrowband (such as Bluetooth of 1 MHz BW) the transmitted baseband signal can be up-converted in the BB processor to IF compensating thereby for the existing incompatibility between Tx and Rx, so the setup shown in Fig. 1 still holds. This is viable due to the fact that in low-IF Rx the IF is usually chosen half the bandwidth. As opposed to this, using this technique for a wideband system (such as Wi-Fi of 20 MHz BW) would impose more stringent requirements on DAC due to much larger band required during test and power consumption as a consequence.

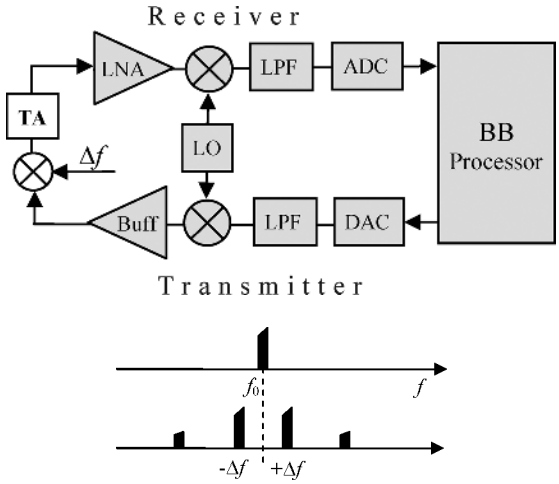

Fig. 2. (a) Loopback setup using offset mixer. (b) Conversion of spectrum in offset mixer.

TABLE I
Offset Frequency Δf Required in Loopback Test

Rx architecture*)	FDD	TDD	
		Direct LO modulation	BB modulation & upconversion
Zero-IF	$\lvert f_{Rx} - f_{Tx} \rvert$	–	– **)
Low-IF		f_{IF}	f_{IF}
Remarks	*Separate LO carriers*	*LO shared by Tx and Rx*	

*) *one-step Tx is assumed,* **) *offset mixer not needed*

Instead, a modified loopback setup making use of an offset mixer can be employed, as shown in Fig. 2. The offset mixer is driven at one input (LO port) by an RF signal from Tx, and at the other- by an extra carrier of the frequency equal to the IF. In this way the test signal at the Rx input consists of a lower- and upper band, which upon down-conversion turn into the IF signal and its image, respectively. If the signal has an asymmetric spectrum the image tends to corrupt the signal at IF, but this problem is not different from the image rejection in normal reception and it is usually maintained by IQ technique. The accompanying harmonics [see Fig. 2(b)] would be suppressed by the receiver IF filters.

Obviously, the same setup would also hold for frequency division duplex (FDD) transceivers where Tx and Rx use different carrier frequencies. The requirements for the offset frequency for typical variants of highly integrable transceivers, adopting the offset mixer technique, are summarized in Table I [31]. Addressed are the commonly used architectures based on a zero-IF or low-IF Rx and a one-step Tx. An important class among them is time division duplex (TDD) systems which use direct RF modulation (*modulating voltage control oscillator (VCO)*).

Those transceivers have already been addressed in terms of the LBT [22], but the proposed setup demands an RF signal with large delay corresponding to the data rate. Since long transmission lines are indispensable in this case, this technique is not feasible for the on-chip LBT. In another approach [21], the authors

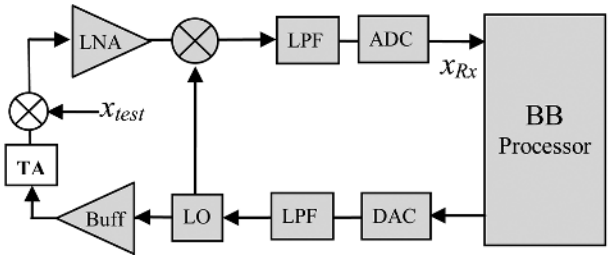

Fig. 3. Offset loopback setup for direct RF modulation.

introduced a frequency divider between Tx and Rx to reduce the phase modulation index in the loopback path. In effect the modulated signal is retained in down-conversion but to accomplish this task the carrier frequency (also subjected to division) must be recovered to meet the receive band. If the carrier frequency is reduced to f_0/N the frequency of a complement carrier is f_0 $(1 \pm 1/N)$. In this case an offset mixer and a tuned RF oscillator are needed. In practice, this oscillator should be implemented as an extra frequency synthesizer and it can be costly, especially when on-chip inductors for the VCO are needed.

Unlike this, in Section III, we discuss some opportunities which enable the loopback self-test for that class of transceivers by making use of a simple baseband signal generator.

III. Offset Loopback Test

The on-chip self-test for TDD transceivers with directly modulated local oscillator (LO), shared between Tx and Rx is appealing, since many low cost implementations adopt this architecture to save chip area and power (e.g., Bluetooth).

Consider an angle modulated signal $A\cos(\omega_0 t + \varphi_{BB}(t))$ available at the LO output and applied both to the offset mixer and to the down-conversion mixer as shown in Fig. 3. Using a test signal $x_{test}(t)$ the product achieved in Rx would be

$$x_{\mathrm{Mix}}(t) \propto x_{\mathrm{test}}(t)\cos(\omega_0 t + \varphi_{BB}(t) + \alpha) \times \cos(\omega_0 t + \varphi_{BB}(t)) \tag{1}$$

where α represents the phase shift (delay) due to the different signal paths from LO to the down-conversion mixer. Here, we have neglected the delay experienced by BB signal $\varphi_{BB}(t)$ since its bandwidth is much lower than the carrier frequency $f_0 = \omega_0/2\pi$. Upon the lowpass filtering the received signal would be

$$x_{Rx}(t) \propto x_{\mathrm{test}}(t) \times \cos\alpha. \tag{2}$$

It is easy to see that the BB signal $\varphi_{BB}(t)$ plays no role as it gets cancelled in Rx, so while in test mode we can refrain from performing the angle modulation. Instead, by using the offset mixer we perform the amplitude- or binary phase shift keying (BPSK) modulation [31], [25]. Clearly, $x_{\mathrm{test}}(t)$ is indispensable here and otherwise only a dc signal can be received, which is difficult to differentiate from dc offset in Rx. If Rx is of low-IF type, $x_{\mathrm{test}}(t)$ should be up-converted to the IF of the Rx, whereas for zero-IF Rx $x_{\mathrm{test}}(t)$ can be an arbitrary BB signal provided it falls in the receive band. In this way, the front-end blocks involved in the test loop are under test as intended. In practice,

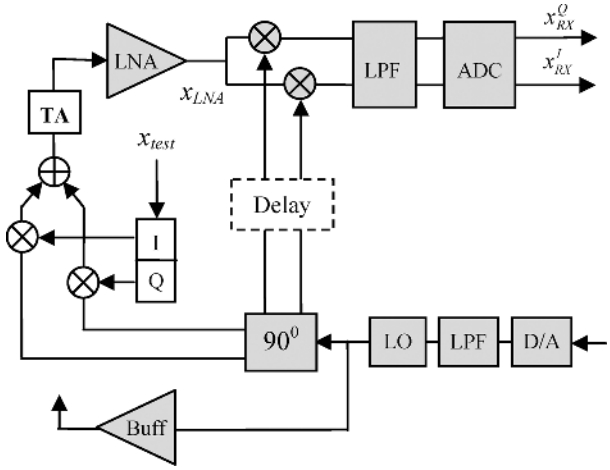

Fig. 4. Loopback setup with quadrature offset mixer.

x_{test} can be a simple digital signal, available from Tx, without shaping, pseudorandom or regular such as a symmetrical square wave. Additionally, implementing the offset mixer as a simple switching mixer (preferably passive), results in BPSK modulation, since x_{test} can be thought to toggle between $+1$ and -1 or $+1$ and zero [33, Ch. 6.2.1].

The offset loopback setup can be upgraded to address also the IQ impairments in Rx. For this purpose x_{test} can be split in I and Q component in BB processor or by using a serial to parallel register. A relevant test setup is shown in Fig. 4 where the offset mixer is also of IQ type and the interconnection between the quadrature LO (i.e., 90° phase splitter) and the IQ mixer is carefully laid out to avoid any imbalance between I and Q paths. Only one TA is used in this circuit so a large signal from the splitter is applied to the LO port of the mixer while x_{test} to the RF port where the possible overdrive should be avoided. As shown, the Tx's output buffer is excluded from the loop when the IQ mode is used.

We assume the LO is unmodulated and the carrier directly applied to the receiver mixer consists of $A\cos\omega_0 t$ and $A\sin\omega_0 t$, so at the LNA output we have

$$x_{\mathrm{LNA}}(t) \propto x^{I}_{\mathrm{test}}(t)\cos(\omega_0 t + \alpha) + x^{Q}_{\mathrm{test}}(t)\sin(\omega_0 t + \alpha). \tag{3}$$

Next, assuming there is no IQ mismatch the received signal can be estimated as

$$\begin{aligned} x^{I}_{Rx}(t) &\propto x^{I}_{\mathrm{test}}(t)\cos\alpha + x^{Q}_{\mathrm{test}}(t)\sin\alpha \\ x^{Q}_{Rx}(t) &\propto x^{Q}_{\mathrm{test}}(t)\cos\alpha - x^{I}_{\mathrm{test}}(t)\sin\alpha. \end{aligned} \tag{4}$$

As seen, the phase lag α introduces a crosstalk between I and Q receive paths and unless it is small a high error rate can result during reception. To avoid this deficiency an extra delay can be introduced into the signal path from LO to the Rx mixer so that α is compensated (see Fig. 4). This delay can be kept during the normal operation mode as well. Clearly, a design constraint for this block is the performance of the LO carrier.

To see the advantage of the quadrature offset mixer consider an IQ phase mismatch to appear as a common fault. The mismatch can be modeled by a phase offset θ so that the LO carrier

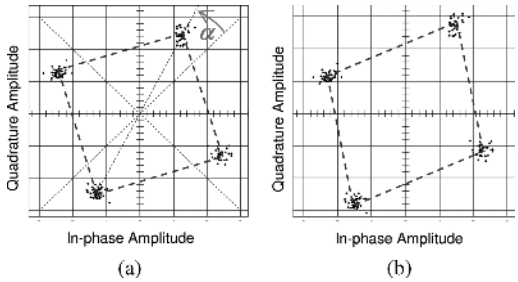

Fig. 5. Received 4-QAM constellations (a) with rotation of $\alpha = 16^\circ$ and (b) with rotation of $\alpha = 16^\circ$ and skew of $\theta = 5^\circ$ evoked by IQ phase imbalance.

in the direct path to Rx mixer will be $A\sin\omega_0 t$ and $A\cos(\omega_0 t+\theta)$, while in the test path after LNA it will be

$$x_{\mathrm{LNA}}(t) \propto x^I_{\mathrm{test}}(t)\cos(\omega_0 t+\alpha+\theta)+x^Q_{\mathrm{test}}(t)\sin(\omega_0 t+\alpha). \quad (5)$$

As a result, we obtain

$$\begin{aligned} x^I_{Rx}(t) &\propto x^I_{\mathrm{test}}(t)\cos\alpha + x^Q_{\mathrm{test}}(t)\sin(\alpha-\theta) \\ x^Q_{Rx}(t) &\propto x^Q_{\mathrm{test}}(t)\cos\alpha - x^I_{\mathrm{test}}(t)\sin(\alpha+\theta). \end{aligned} \quad (6)$$

With $\theta = 0$ the constellation of the received signal is only rotated by some angle that is easy to see for 4-QAM case [see Fig. 5(a)]. Putting $x^I_{\mathrm{test}}(t)$ and $x^Q_{\mathrm{test}}(t)$ equal ± 1, from (4) we find $(x^I_{Rx})^2 + (x^Q_{Rx})^2 = 2$ for any value of α. Here, we refer to the zero-IF receiver, but only using a small modification it holds for the low-IF receiver, too.

With θ different from zero the constellation additionally gets skewed (rhombus shape is observed) displaying the quadrature error as shown in Fig. 5(b). As compared to the square-shaped constellation of Fig. 5(a), here the diagonals are subject to scaling with factors $(1+\sin\theta)$ and $(1-\sin\theta)$, respectively. A possible amplitude IQ mismatch entails other distortions as well [35].

The above model mainly refers to the IQ phase imbalance produced by the splitter (LO) that equally affects the offset mixer and the down-conversion mixer. A great care must be taken not to introduce an extra IQ mismatch by the test circuitry, which could obscure the IQ test. Implementation of the LBT adopting IQ offset mixer is a challenge. Also it is perhaps the only way to run the IQ test on a chip for the VCO-modulated transceivers with shared LO.

A shortcoming of this approach is that the modulation performed in LO escapes the test since it is cancelled in the Rx mixer. Also, the LO phase noise, like the baseband signal $\varphi_{BB}(t)$ in (1), cannot be measured using the loopback setup.

Basically, it is possible to remove modulation from phase modulated signals $\cos(\omega_0 t+\varphi_{BB}(t))$ and $\sin(\omega_0 t+\varphi_{BB}(t))$ providing thereby a quadrature LO suitable to receive the baseband stimulus. For this purpose, one can refer to the following identities:

$$\begin{aligned} \cos\omega_0 t &= \cos(\omega_0 t+\varphi_{BB})\cos\varphi_{BB}+\sin(\omega_0 t+\varphi_{BB})\sin\varphi_{BB} \\ \sin\omega_0 t &= \sin(\omega_0 t+\varphi_{BB})\cos\varphi_{BB}-\cos(\omega_0 t+\varphi_{BB})\sin\varphi_{BB}. \end{aligned} \quad (7)$$

In this case, four mixers are required in the LO path while the offset mixer and x_{test} in the loopback path can be skipped. Also extra digital-to-analog converters (DACs) are needed to convey $\cos\varphi_{BB}(t)$ and $\sin\varphi_{BB}(t)$ produced by the baseband processor. The overhead claimed by the test circuitry is significant, so implementation of this test setup on a chip is rather problematic. Also, a possible IQ mismatch in the LO path and accuracy of DACs can badly affect the test performance. The test of a directly modulated VCO in the loopback mode has been addressed in [21] and [22] as mentioned, but their on-chip implementation seems impractical as well.

IV. Specs- and Fault-Oriented Loopback Test

For RF receivers and transmitters a number of different tests have been specified. They mainly address receiver sensitivity and selectivity, and in the case of a transmitter the power levels and spectral purity [2, Ch. 5], [35]. Some of the RF tests are complicated and time consuming so in mass production even when performed on a chip, they are considered costly. For this reason, more time effective fault-oriented structural tests and specs-oriented alternative tests have been proposed. Those tests are based on fault modeling [11]–[15], [23], and require optimization to attain maximum test efficiency. To make the RF LBT model tractable in terms of the simulation time, fault abstraction which covers various on-chip defects and unintended local- or global process variations, characteristic of the employed technology is needed.

While for the alternative test approach (specs oriented) the optimization of test signals is necessary to boost correlation between the test response and the specs [18]–[21], in the fault-oriented test a typical strategy is in tuning the test stimuli (or response) for maximum sensitivity of the test response to possible faults [16], [17]. In some cases measurements similar to standard tests can be conducted but always in favor of fault detection and/or the reduced test time. For example, the elevated-bit error rate (BER) test requires by a few orders of magnitude less symbols than the standard BER test resulting thereby in significant time savings [32].

The concept of the fault-oriented test is justified all the more, in mass production the simple *go/no-go* strategy is obeyed while diagnosis in not the issue. Moreover, investigation of specification oriented tests reveals that they tend to be redundant with respect to some faults, but also incapable of detecting others.

V. Sensitization Techniques

A. BER and EVM Test

Detection of some faults in the loopback signal path proves difficult. To alleviate the problem the sensitization techniques can be used. The conditions to enhance sensitivity of a fault-oriented test response can be formulated based on behavioral modeling [16], [17]. Specifically, for the error vector magnitude (EVM) test, a very low signal power at the Rx input can be anticipated. By observation that at the Rx output

$$\mathrm{EVM}^2 = \frac{1}{\mathrm{SNR}_{\mathrm{out}}} \quad (8)$$

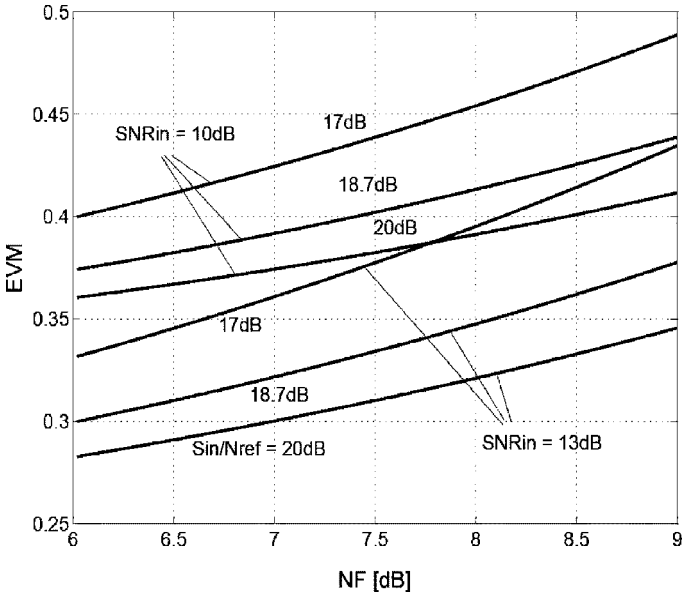

Fig. 6. EVM response versus receiver NF for $S_{\rm in}$ and $\mathrm{SNR}_{\rm in}$ measured at Rx input.

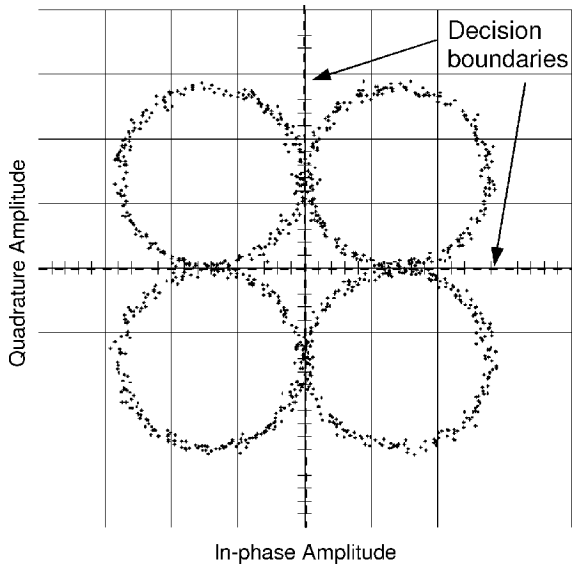

Fig. 7. Received 4-QAM constellation with inherent noise and tone interferer ($f_{\rm int}$ = 1.6 MHz) added at transmitter baseband (data rate R = 11 MS/s).

and signal-to-noise ratio (SNR) in the Rx path gets degraded due to

$$\mathrm{SNR}_{\rm out} = \frac{\mathrm{SNR}_{\rm in}}{1 + \frac{N_{\rm ref}}{N_{\rm in}}(F_{Rx} - 1)} \tag{9}$$

where $N_{\rm in}$, $N_{\rm ref}$, F_{Rx} are the input noise, reference noise and noise factor, respectively, we find

$$\frac{d\mathrm{EVM}^2}{dF_{Rx}} = \frac{N_{\rm ref}}{S_{\rm in}} \tag{10}$$

where $S_{\rm in}$ denotes the signal power at the Rx input. The relevant plot showing EVM versus NF and the involved parameters is given in Fig. 6. The specs shown correspond to the Wi-Fi transceiver. Specifically, for $S_{\rm in} = -83$ dBm and bandwidth $B = 20$ MHz the reference noise is $N_{\rm ref} = -174$ dBm/Hz$+10\log B = -101$ dBm so $(S_{\rm in}/N_{\rm ref})_{\rm dB} = 18$ dB.

The conditions to sensitize the BER test can be derived from constellations which represent the modulated signal in Rx. The physical defects that degrade noise factor add extra noise to the noisy constellation points. The constellation points that are close to the decision boundaries tend to cross over and they result in the reception errors. Then BER is raised, and the defect is visible. To place the constellation points close to the decision borders both low $S_{\rm in}$ and low $\mathrm{SNR}_{\rm in}$ are useful (the latter provides more scattering). An alternative approach is to introduce a single-tone interferer at Tx baseband that makes the reference constellation points split in circles, which adhere to the decision boundaries as shown in Fig. 7 [17]. Upon more noise the constellation points close to the boundaries tend to crossover.

In another approach, the optimum $\mathrm{SNR}_{\rm out}$ for the BER test can be found based on a mathematical model for probability of symbol errors in a demodulator with additive white Gaussian noise. Specifically, for coherent 4-QAM system this probability is

$$p_e = erfc\sqrt{\frac{\mathrm{SNR}_{\rm out} \times B}{R_b}} - \frac{1}{4}erfc^2\sqrt{\frac{\mathrm{SNR}_{\rm out} \times B}{R_b}} \tag{11}$$

where R_b and B stand for the bit-rate and the equivalent system bandwidth, respectively [34, Ch. 7.3]. To attain the optimum in practice, a technique based on geometric translation of the constellation points can be used [32]. By means of a vector V which points to the origin we can shift the constellation points toward the decision boundaries only changing the signal power while the noise component is preserved. The scattered points at Rx baseband are translated as illustrated in Fig. 8. Upon the translation the SNR can be reduced from $\mathrm{SNR}_{\rm out}$ to an arbitrary value

$$\mathrm{SNR}^*_{\rm out} = \mathrm{SNR}_{\rm out}\left(1 - \frac{|V|}{|x_0|}\right)^2 \tag{12}$$

where $|x_0|^2$ is the signal power without noise and we assume $|x_0| > |V|$. In this case p_e depends on the reduced value of SNR defined by (12).

The test stimulus used in this case should feature high SNR as opposed to the previously addressed approaches. Based on this model one can identify the optimum translation vector for a given signal [combining (9), (11), and (12)] so that maximum sensitivity $\mathrm{d}p_e/\mathrm{d}F_{Rx}$ is attained. This is equivalent to achieving the best detectability of impairments in the Rx noise factor. The optimum can be found at $\mathrm{SNR}^*_{\rm out} \cong 1.35$ for various power levels at the receiver input as shown in Fig. 9.

Hence, using (12) the optimum V can be calculated to enable the advanced BER test. Around the maxima, the plots $\mathrm{d}p_e/\mathrm{d}F_{Rx}$ are rather flat so in practice the test sensitivity does not suffer much from imprecise tuning for the optimum.

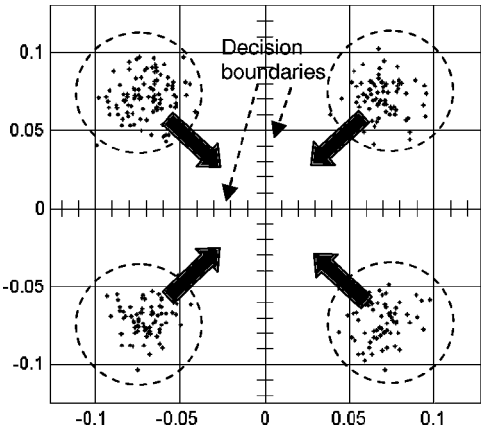

Fig. 8. Constellation of 4-QAM signal in Rx with noise under geometrical translation.

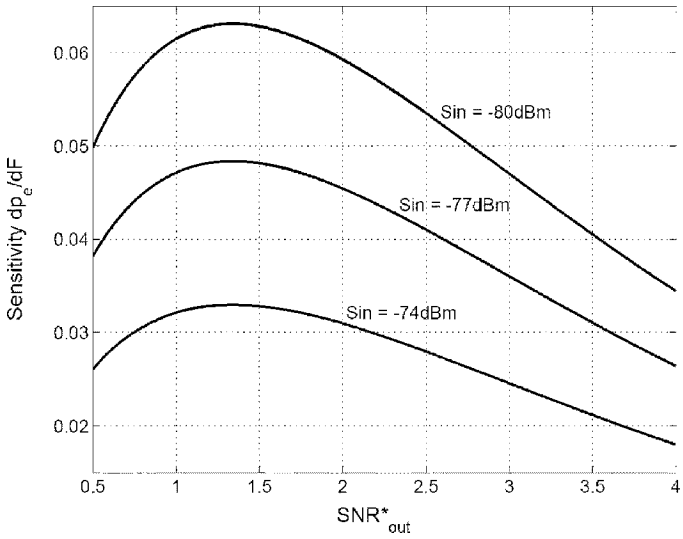

Fig. 9. Sensitivity of symbol error probability versus reduced SNR for different input signal power and $\mathrm{SNR_{in}} = 20$ dB.

The test sensitivity $\mathrm{d}p_e/\mathrm{d}F_{Rx}$ suffers when the input signal power is increased and also when SNR at the receiver input is reduced. For example, the maximum sensitivity shown in Fig. 9 is reduced approximately by a factor of 2 for 6 dB drop in $\mathrm{SNR_{in}}$. In this case the maximum is becoming less pronounced as well. The explanation is that in both cases the Rx is getting more immune to extra inherent noise that, in fact, deteriorates the test detectability.

For more insight also the probability p_e can be plotted versus $\mathrm{SNR_{out}}$ for various translation vectors as shown in Fig. 10. The translation is quantified according to (11) using a factor

$$\beta = \left(1 - \frac{|V|}{|x_0|}\right)^2. \tag{13}$$

The smaller β value the larger the translation effect. The optimum translation is well pronounced for larger values of $\mathrm{SNR_{out}}$ (say, $>$ 16 dB), where the slope $\mathrm{d}p_e/\mathrm{dSNR_{out}}$ achieves maximum for $\beta = 10\text{e-}3 \ldots 40\text{e-}3$, i.e., when

$$\frac{\partial^2 p_e}{\partial \mathrm{SNR_{out}} \partial \beta} = 0 \tag{14}$$

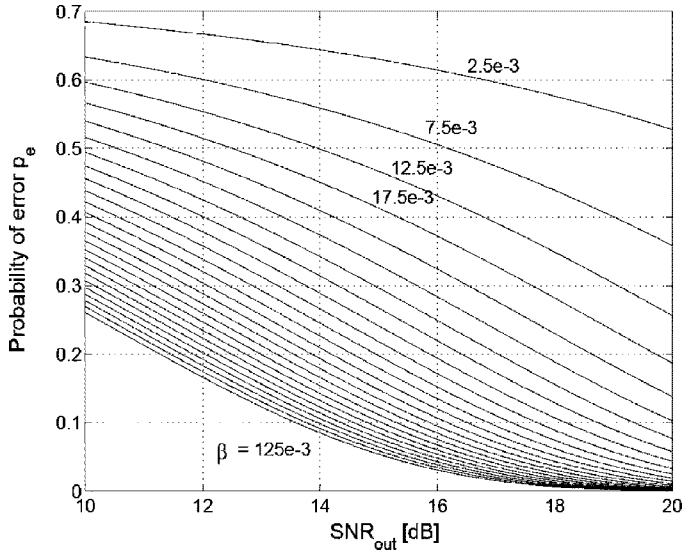

Fig. 10. Symbol error probability versus SNR at Rx output for $\mathrm{SNR_{in}} = 20$ dB, $S_{\mathrm{in}} = -80$ dBm and different translation factors.

while it is smaller both for larger and smaller values of β. Specifically, for $\mathrm{SNR_{out}} = 17$ dB we find by inspection the maximum slope at $\beta = 22.5\text{e-}3 \ldots 32.5\text{e-}3$ resulting in $\mathrm{SNR^*_{out}} = 1.125 \ldots 1.625$ which matches well the maxima $\mathrm{d}p_e/\mathrm{d}F_{Rx}$ identified in Fig. 9. For lower values of $\mathrm{SNR_{out}}$ (also for lower $\mathrm{SNR_{in}}$) the maximum $\mathrm{d}p_e/\mathrm{dSNR_{out}}$ is much less pronounced so the sensitization is less effective.

B. Gain- and Linearity Test

As compared to BER and EVM loopback tests, more straightforward sensitization techniques are feasible for gain and linearity tests. Specifically, the loop gain can be estimated by signal power measurement at the receiver output and thereby display possible impairments in the loop gain. In this case all blocks contribute to the test response in the same way

$$P_{\mathrm{out}} = G_{Tx} G_{\mathrm{TA}} G_{Rx} P_{\mathrm{in}} \tag{15}$$

so if the gain is locally degraded the maximum sensitivity to linear range. This fault is achieved using maximum input power P_{in} and maximum gain of an attenuator, G_{TA} (which is simply the least attenuation). Also, the impact of noise on the measured signal is reduced in this way. An obvious disadvantage of this test is the limited observability and controllability, i.e., a drop in one gain can be easily masked by an increase in another.

Additionally, if the on-chip test attenuator (TA) is linear and it can also be fine tuned, it is possible to measure the compression point, P1dB (1 dBcp) of the Rx while keeping the Tx power fixed. Conversely, if the Tx power can be varied then with fixed TA the Tx P1dB can be estimated as well. In this case, TA should provide a large enough attenuation so that the observation path through Rx does not obscure the measurement. In other words, the Rx should operate within its linear range.

Unless the absolute measure of P1dB or gain is an issue the on-chip calibration is not required, rendering the test feasible. In production test, a chip under test would be compared to the

test sample of large enough number of chips, characterized on bench prior to the actual test.

Another test for linearity, such as the IP3 test can be sensitized as well. IP3 or IM3 can be measured using spectral analysis when a two-tone stimulus is applied [33, Ch.2], [35]. For the direct loopback setup with a highly linear TA the input-referred IP3 follows:

$$\frac{1}{\mathrm{IP3}} \cong \frac{1}{\mathrm{IP3_{Tx}}} + \frac{G_{Tx}G_{\mathrm{TA}}}{\mathrm{IP3_{Rx}}}. \tag{16}$$

Specifically, the sensitivity to impairments in the Rx IP3 can be raised by using a larger G_{TA}, while with a small enough G_{TA} the Rx operates within linear range so Tx IP3 can be well tested. This approach will work if the contribution of the Rx and Tx is similar. It should be noted that the IP3 test is an important complement to BER or EVM test in case of defects that mostly affect IP3.

C. Effect of TA on Loopback Tests

It is possible to design a highly linear test attenuator, so that it has a minor impact on the total IP3 of a transceiver in the loopback mode. Circuit implementations of TAs with the input $\mathrm{IP3} > 20$ dBm have been reported [26], [30], [37]. The TA circuit can be disabled in the normal operation mode in order not to affect the chip performance. The possible to achieve isolation can be as large as 60 dB for a single stage CMOS attenuator at 1 GHz and for multi-stage architecture it is respectively larger [37].

The impact of TA on the BER/EVM test is discussed beneath. The TA noise performance can be described by (9) where the noise factor F is replaced by TA's loss (1/Gain). The relation between the TA input and output follows:

$$\mathrm{SNR_{out}} \cong \frac{\mathrm{SNR_{in}}}{1 + \frac{\mathrm{SNR_{in}}N_{\mathrm{ref}}}{S_{\mathrm{out}}}}. \tag{17}$$

The corresponding plots achieved for $N_{\mathrm{ref}} = -100$ dBm are shown in Fig. 11. When $\mathrm{SNR_{in}}$ is large enough, $\mathrm{SNR_{out}}$ attains its maximum value $S_{\mathrm{out}}/N_{\mathrm{ref}}$, e.g., with $S_{\mathrm{out}} = -80$ dBm the $\mathrm{SNR_{out}}$ is not better than 20 dB, as shown. Larger values of $\mathrm{SNR_{out}}$ that are useful for the enhanced BER test or spectral tests, can be achieved using more signal power, but also the value of $\mathrm{SNR_{in}}$ plays a role. For example, with $S_{\mathrm{out}} = -60$ dBm the $\mathrm{SNR_{out}}$ can approach 40 dB when $\mathrm{SNR_{in}} > 50$ dB. Should the latter condition be excessive, even more signal power must be used.

When an offset mixer is used the model defined by (17) still holds provided the mixer is passive. A passive mixer would be preferred for this application as it is usually more linear than an active mixer. As discussed in previous subsection linearity of the loopback elements is critical especially when spectral tests are applied. Reported CMOS designs prove feasibility of a highly linear passive mixer with $\mathrm{IIP3} > 5$ dBm. Moreover when the offset mixer follows TA their equivalent IP3 is decided by TA. In practice, the attenuation of TA ($> 30 \ldots 40$ dB) makes the signal low enough to neglect nonlinearity of this mixer.

Global process variations should not badly affect the test blocks as long as the transistors are operational as on/off switches. On the other hand, the probability of possible local faults (defects) in the test blocks would be limited by the common rule of thumb that the test circuitry should fit within 10% of the chip area.

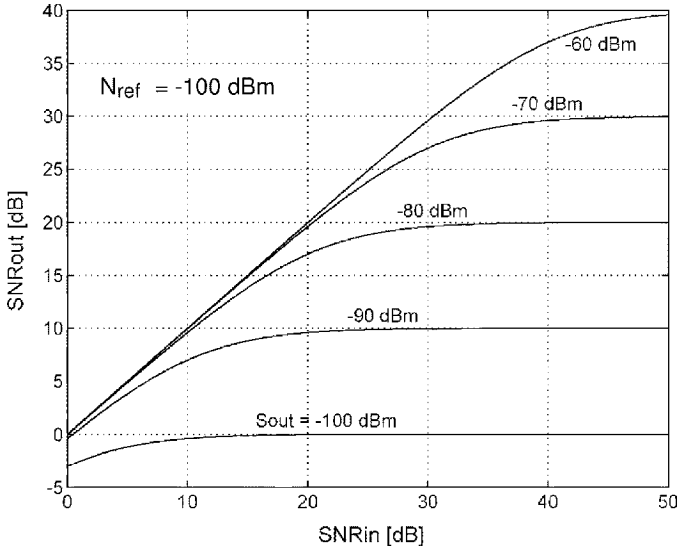

Fig. 11. Transfer function of SNR in test attenuator.

VI. Enhanced Controllability and Observability

A. Bypassing Technique

The advantage of the loopback setup is evident in terms of the limited test circuitry and simple test signatures like BER or EVM that facilitate chip testing. However, the test controllability and observability on the chip are limited. Simple insertion of test points in today RF circuits is basically accepted at baseband only. In particular, faults affecting the RF blocks achieve different detectability depending not only on their strengths, but also on fault location and the type of test. For example, impairment in noise factor or gain of LNA in the EVM or BER test response would be much more pronounced than even stronger impairments in the downconversion mixer. This is because LNA decides the receiver noise factor F_{Rx} by raising the signal level before the mixer adds its noise. Invoking the Friis formula [33, Ch. 2]

$$F_{Rx} = F_{\mathrm{LNA}} + \frac{F_{\mathrm{Mix}} - 1}{G_{\mathrm{LNA}}} + \frac{F_{\mathrm{other}} - 1}{G_{\mathrm{LNA}}G_{\mathrm{Mix}}} \tag{18}$$

we find the corresponding sensitivities to the mixer parameters to be attenuated by the LNA gain. To overcome this drawback the bypassing technique can be used [30], [38]. Fault diagnosis is also supported in this way. When LNA is bypassed, as shown in Fig. 12, the faulty down-conversion mixer (with degraded F) can achieve as good detectability as the faulty LNA in the basic loopback setup. The LNA gain is replaced here by the attenuation of the enabled MOS switch. At the same time LNA is disabled to break the unwanted signal path and to circumvent loading. With this circuit, we avoid using a multiplexer which would degrade the Rx gain in the normal operation mode.

The bypass switches have minor effect on the chip performance in the normal operation mode if they are appropriately sized. For example, for LNA with an input transistor of

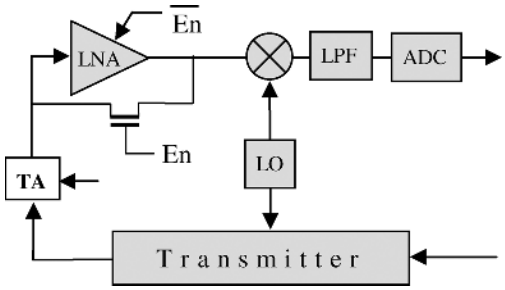

Fig. 12. RF test path with bypassed LNA.

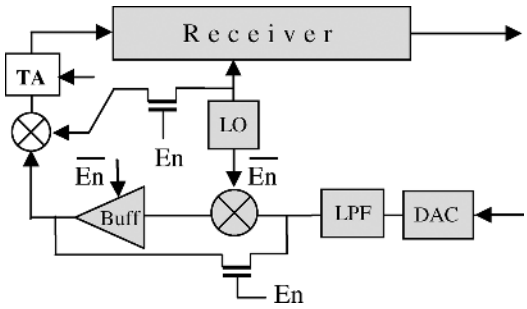

Fig. 13. RF test path with bypassed up-conversion mixer .

200 μm/0.13 μm a bypass switch of 10 μm/0.13 μm proves sufficient so the parasitic capacitance (when OFF) is almost negligible [38].

Like LNA the Tx output buffer can be bypassed, too. On the other hand, if the offset mixer is put on chip to enable the LBT, it can also support bypassing of the Tx- or Rx mixer. The test setup shown in Fig. 13 enables bypassing of the Tx front-end in order to emphasize possible impairments in receiver IP3. Specifically, the total loop IP3 obeys the formula

$$\frac{1}{\mathrm{IP3}} \cong \frac{1}{\mathrm{IP3_{Tx}}} + \frac{G_{Tx}}{\mathrm{IP3_{Test}}} + \frac{G_{Tx}G_{\mathrm{Test}}}{\mathrm{IP3_{Rx}}} \tag{19}$$

so when the Tx front-end is excluded, the contribution of Tx and the test blocks (offset mixer and TA) is significantly reduced. At the same time, to compensate for G_{Tx} drop, G_{Test} can be increased using TA. The baseband signal in Tx must be kept low enough to avoid nonlinear distortions in the bypass switch.

At the expense of more area overhead, different test configurations can be introduced as well, e.g., a loop closed at baseband. In this case the baseband blocks (DAC, ADC, and filters) would be under test while the RF front-end was bypassed. The design requirements for those test blocks would be much relaxed due to their low-frequency application.

B. RF Detectors

Observability of an RF front-end under test can be enhanced by using RF detectors [27]–[29]. The RF detectors convert RF into a proportional dc signal, usually making use of transistor nonlinearity. The high frequency products which occur can be suppressed by an on-chip capacitor.

A typical RF detector occupies small area on a chip and saves power since its transistors can be minimum sized. Also a large input impedance is achieved in this way ($>$ 5 kΩ) so loading effects on the chip are avoided [29].

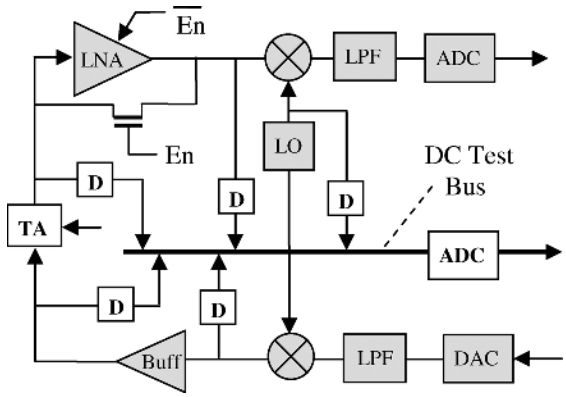

Fig. 14. Loopback test setup with RF detectors and dc test bus.

A possible test setup using the RF detectors and a dc test bus is shown in Fig. 14. In this case the RF signal can be measured at several nodes so that on-chip fault diagnosis is enhanced as well. Specifically, measurements of gain and P1dB are viable. However, for accuracy of the measurements, calibration of the detectors, including the dc bus plus ADC is needed [36]. Obviously, once calibrated they enable calibration of the loopback elements as well.

VII. Masking Effect by Tolerances

By using simulation it is possible to capture the effect of fault masking by tolerances for different types of faults and locations. Since the "worst-case" analysis provides over-pessimistic estimates while the Monte Carlo technique tends to suffer from excessive simulation effort, one can refer to behavioral models. The problem can be discussed using a simple statistical model and the sensitivity analysis [16], [24].

For a test response w (such as BER/EVM or power gain) its variance with respect to parameters x_i (such as F, IP3, or gain) of the involved RF blocks would be

$$\sigma_0^2 = \sum_i \left(\frac{\partial w_0}{\partial x_i}\right)^2 \sigma_{xi}^2 \tag{20a}$$

$$\sigma_f^2 = \sum_i \left(\frac{\partial w_f}{\partial x_i}\right)^2 \sigma_{xi}^2. \tag{20b}$$

As shown in Fig. 15, a fault drives the test response from w_0 to w_f and to detect this fault a large enough distance between the corresponding mean values μ_0 and μ_f is required. Otherwise, detection with a low confidence level would be achieved, and a significant number of "false rejects" or "escapes" during the test might be expected. Here, we assume

$$|\mu_f - \mu_0| \geq 3\,(\sigma_0 + \sigma_f) \tag{21}$$

which is equivalent to probability of fault masking equal 0.0013 for Gaussian distribution. For a given transceiver under test and given fault, solution of (20) provides the lowest detectable value of that fault, referred to as the *detectability threshold* (DT). To identify a DT, say DT_j the corresponding parameter x_j is excluded from (20a) and (20b) and defined as a fault $DT_j = \Delta x_j$ and (21) is solved. Fig. 16 illustrates results obtained for a given transceiver under EVM- and gain test for faults, which

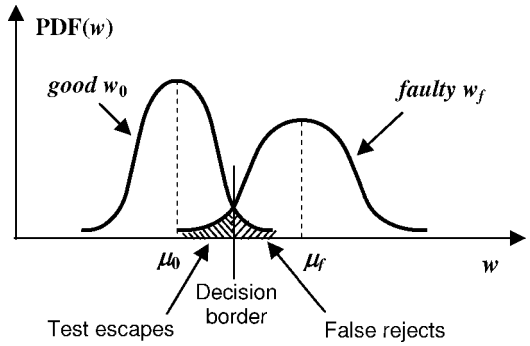

Fig. 15. PDF of test responses for good- and faulty chip.

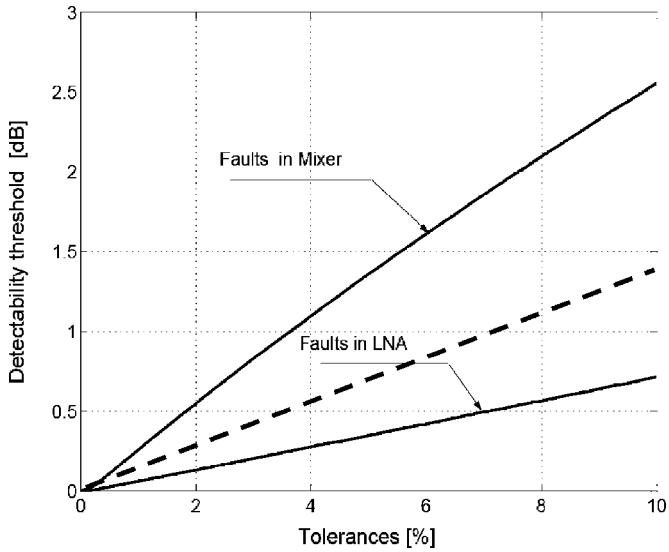

Fig. 16. Detectability thresholds ΔG (ΔNF) for EVM test (solid lines) and for gain test (dashed line).

degrade both NF and gain ($\Delta\mathrm{NF} = -\Delta\mathrm{G}$) in LNA and in the down-conversion mixer. All the parameter tolerances of the transceiver were assumed to be of 3σ, i.e., $t_{xi} = 3(\sigma_{xi}/x_i) \cdot 100\%$. In practice, those tolerances can be kept below 5% provided the blocks are designed as differential circuits, so that the corresponding detectability thresholds are relatively low. In submicrometer CMOS implementations also on-chip correction is usually needed.

As shown, the EVM test displays its advantage over the gain measurement for faults located in LNA provided both NF and gain are affected that, in fact, is a typical case. The respective DTs are much lower for the same tolerances. On the other hand the DTs for gain test do not depend on fault location in the loop that is advantage of the gain test. Finally, when the LNA is bypassed during the EVM or BER tests, the mixer achieves DTs similar to the LNA that makes the bypassing even more profitable. For BER test the DTs are similar to those of EVM.

Basically, the detectability thresholds can be reduced at the expense of lower confidence level. Unfortunately, reduction of DTs entails a significant increase in probabilities of misclassification. Since the DTs (expressed in decibel scale) appear roughly proportional to $|\mu_f - \mu_0| = n(\sigma_0 + \sigma_f)$ for tolerances $< 10\%$ the reduction of DTs by a factor of 2, e.g., from 2 to 1 dB, elevates the probability of misclassification from 0.0013 (for $n = 3$) to 0.066 (for $n = 3/2$). Obviously, this tradeoff is significant in practice because of the costs associated with shipping defective parts and rejecting good parts.

It should be noted that for a given test the DTs are an alternative measure of the test performance. Specifically, for the corresponding fault coverage the problem of defining an adequate fault set (with continuous values) is usually critical while with the DTs approach it is practically evaded.

TABLE II
TRANSCEIVER MODEL SPECIFICATIONS

	Block	NF [dB]	G [dB]	IIP3 [dBm]
Rx	LNA	4	18	-7
	Mixer	16	10	+3
	LPF/PGA	13	20	+14
Tx	Mixer	6	-5	+6
	Buffer	11	3	-3

VIII. SIMULATION EXAMPLES

A. WLAN Transceiver Under BER Test

A functional model of WLAN transceiver (TRx) corresponding to 802.11b Std. has been implemented in MATLAB. The model is arranged as a direct conversion Tx and zero-IF Rx, and it operates as a QPSK system (4-QAM) with 11 MS/s and carrier frequency of 2.4 GHz. The Tx makes use of a highly linear passive mixer with NF close to the conversion loss. The Rx exploits a typical active mixer with much larger NF. A direct LBT setup is used where the test response is measured at Rx baseband by symbol error rate (SER) analyzer. Observe that for a QPSK system we can assume BER to be half of the measured SER [34, Ch. 7]. The basic specifications for the transceiver components are given in Table II and can be considered typical values [39]. The Tx output power is -10 dBm. Additive white Gaussian noise (AWGN) sources have been used to adjust NF parameters. To sensitize the test as discussed in Section V-A, two variants are implemented. In *Variant* 1 the signal is supplemented with noise in Tx and its power is reduced in TA to bring the constellation points close to the decision boundaries. In *Variant* 2 the Tx signal is kept clean and the received signal is subjected to translation of the constellation points. To limit the simulation time of BER test a pseudo-random sequence (PRBS) of 1000 symbols has been chosen with a corresponding resolution $1\mathrm{e}-3$. In this case, the elevated error rates justify this choice.

Based on this model one can "inject" defects into different blocks and measure the test responses. At this abstraction level the defects are represented by impairments in gain and NF. The SER test performance has been verified based on three faults: F_1: fault in Tx output buffer; F_2: fault in LNA; F_3: fault in Rx mixer (I or Q), each degrading both gain and NF by 3 dB ($\Delta G = -3$ dB, $\Delta NF = 3$ dB as impairments in gain are usually accompanied by similar impairments in NF). Those values can be considered representative fault samples that should be

TABLE III
ERROR COUNT $\#E_k$ IN BER TEST SIMULATION FOR VARIOUS SNR_{in} AND S_{in} AT RX INPUT

	SNR_{in}															
	10 dB				**7 dB**				**4 dB**				**1 dB**			
S_{in}	**FF**	**F_1**	**F_2**	**F_3**	**FF**	**F_1**	**F_2**	**F_3**	**FF**	**F_1**	**F_2**	**F_3**	**FF**	**F_1**	**F_2**	**F_3**
-76 dBm	3	4	5	3	28	33	33	28	99	99	98	99	254	265	266	254
-80 dBm	6	18	17	9	36	43	44	35	101	121	117	106	266	271	276	265
-84 dBm	19	49	54	26	50	95	95	61	126	168	170	137	278	300	297	278

well-detected in terms of CMOS process variations and acceptable detectability thresholds as discussed in Section VII. We consider single faults only as they are more likely than multiple faults.

Table III provides simulation results of BER test in *Variant* 1 for various power levels and SNR at the Rx input. The count $\#E_k$ of measured incorrect symbols, received for kth fault, is given in column F_k, whereas the fault-free response $\#E_0$ in column FF.

As predicted before, the faults are best visible at the lowest signal power while the lowest SNR is not the best choice. At -76 dBm the faults are hardly detected except for $SNR_{in} = 1$ dB where small increments ($\#E_k$–$\#E_0$) can be observed. Decreasing signal power makes the test more sensitive and larger increments in SER can be observed. At -80 dBm the maximum sensitivity is achieved with $SNR_{in} = 4$ dB, and for a more noisy signal at $SNR_{in} = 1$ dB the SER goes up but the noise imposed by faults is less meaningful. On the other hand, for a less noisy signal fewer symbols (constellation points) approach the decision boundaries and the faults are less pronounced either. With a signal power reduced to -84 dBm the maximum sensitivity moves towards $SNR_{in} = 7$ dB and this maximum is larger than the other maxima as the noise imposed by faults is more meaningful when the stimulus is less noisy.

Although all the faults have the same strength, fault F_3 (in the Rx mixer) is usually less pronounced in the test response as it is masked by the LNA gain. Fault F_1 and F_2 achieve in practice the same detectability. Fault F_1 in the Tx buffer, is mainly visible for the drop in gain rather than for increase in NF as the noisy stimulus does not suffer much from impairments in NF of this block. In other words, the inherent noise of the Tx buffer is not meaningful as compared to noise conveyed by the powerful stimulus.

To summarize, achieving high test sensitivity with this technique is viable by a very low signal power at the Rx input. This can be difficult to guarantee on a chip because of limited isolation between Tx and Rx. To evade the problem the translation technique can be used instead.

Consider *Variant* 2 of the BER LBT. In this case the test setup is complemented by a translation block placed in front of the SER detector. The translation block transforms each received QPSK symbol $x(k) = [x_I(k), x_Q(k)]$ using the following formula:

$$\hat{x}_I(k) = x_I(k) - V_I \times \mathrm{sgn}(x_I(k))$$
$$\hat{x}_Q(k) = x_Q(k) - V_Q \times \mathrm{sgn}(x_Q(k)) \quad (22)$$

where $V_I, V_Q \in R^+$ are the coordinates of the translation vector while the $\mathrm{sgn}(\cdot)$ function secures the desired direction of this translation. To achieve maximum sensitivity, SNR should attain the optimum value $SNR^*_{out} \approx 1.35$ (see Fig. 9). For this purpose V can be estimated from (11) where $|x_0|$ is the measured effective value of the baseband signal $x(k)$ (without noise) while SNR_{out} corresponds to a fault-free circuit under given signal power at the receiver input. In this variant the stimulus is a clean signal, with $SNR_{Tx} \approx 40$ dB at Tx output. If the TA attenuation is not very large, SNR_{out} can be relatively large as well so $|x_0|$ can be estimated from $x(k)$ samples (symbols) neglecting the signal variance (noise contribution).

Compared to *Variant* 1 the optimum SNR can be achieved at a higher signal power, i.e., using less attenuation in TA. A fault-free model achieves in simulation $SNR_{out} = 33.54$ dB (2260) and from (11) we can find $|V| = 0.039 \times \sqrt{2}$ so that SNR of 1.35 is attained.

The simulation results obtained with PRBS stimuli for different power levels are shown in Table IV. The same faults as

TABLE IV
ERROR COUNT $\#E_k$ IN BER TEST WITH TRANSLATION

S_{in} dBm	**Fault free SNR** dB		**#Errors**			
	@Rx inp	@Rx out	**FF**	**F_1**	**F_2**	**F_3**
-60	36.8	33.5	230	346	335	263
-70	29.4	24.5	228	362	367	268
-80	19.8	14.6	231	369	371	268

in *Variant* 1 are used. The 3 dB drop in gain results in $|x_0|$ to be $\sqrt{2}$ times less than for the fault-free circuit so $|V|$ should be tuned accordingly.

Observe that SNR measured at Rx input (TA output) and the plots in Fig. 11 are in good match (SNR at TA input ≈40 dB). From the increments $\#\mathrm{E_k}$–$\#\mathrm{E_0}$ we can evaluate sensitivity of the test that is much higher compared to *Variant*1. It is mainly because of high SNR of the stimulus. Also much larger signal power (at Rx input) can be used in this case so that the required signal attenuation is moderate and the effect of limited isolation between the Tx and Rx is mitigated. Here, we demonstrate a good performance for 50 dB attenuation rather than >70 dB such as required in *Variant* 1. As shown in Table IV the sensitivity decreases when the signal is stronger (compare also with Fig. 13). However, using larger signal power at the Rx input can deteriorate the test performance. For example, with $\mathrm{S_{in}} = -60$ dBm the increment $\#\mathrm{E}_2 - \#\mathrm{E}_0 = 105$ while for $\mathrm{S_{in}} = -50$ dBm it is only 46. This difference can be understood looking into SNR and the noise level at the receiver input. In the first case it is $\mathrm{N}_{in} = -60$ dBm $-$ 36.8 dB $= -96.8$ dBm and in the other $\mathrm{N_{in}} = -50$ dBm $-$ 38.7 dB $= -88.7$ dBm which makes 8.1 dB difference (6.45 ×) while SNR only differs by 1.9 dB (1.55 ×). These numbers can be applied to (9) to see that upon impairments in F_{Rx} the stronger signal evokes less change in $\mathrm{SNR_{out}}$. For even stronger signal $\mathrm{SNR_{in}} \approx 40$ dB but N_{in} is still $\gg N_{\mathrm{ref}}$ so in spite of a larger SNR the test will be desensitized.

Tuning the translation vector V according to the signal power improves test performance in terms of process variations. Also we are avoiding over-sensitization of the test that can easily occur at larger power since in this case $|V| \approx |x_0|$ and upon a drop in gain, $|x_0| - |V| < 0$ if $|V|$ is not updated accordingly. As a result most of the constellation points are transferred across the decision boundaries and the SER can easily approach 1 which can be considered the saturation of test. As a consequence impairments in gain of the TRx blocks that are acceptable in normal operation can saturate the test even for chips with good noise performance.

With a fixed $|V|$, selected for a standard value of $|x_0|$, the BER test with translation can work well provided a low enough power is used. Even larger test sensitivity can be achieved in this case [32]. However, the limited on-chip isolation between Tx and Rx can hamper this approach.

Finally, consider a test setup in *Variant* 2 where bypassing of LNA is implemented. The respective bypassing switch has a loss of 3 dB. The simulation results for faults $\mathrm{F_1}$ and $\mathrm{F_3}$ are shown in Table V. Specifically, the fault in receive mixer ($\mathrm{F_3}$) achieves very good detectability, comparable to LNA ($\mathrm{F_2}$) shown in Table IV.

TABLE V
ERROR COUNT $\#\mathrm{E_k}$ IN BERT WITH TRANSLATION FOR LNA BYPASSED

$\mathrm{S_{in}}$ dBm	Fault free SNR dB		#Errors		
	@Rx inp	@Rx out	FF	$\mathrm{F_1}$	$\mathrm{F_3}$
-60	36.8	19.9	229	373	364
-70	29.4	9.9	229	358	355

B. WLAN Transceiver Under Linearity Test

Here, we consider a TRx under LBT for linearity. The model defined in Section VIII-A is used again, and the IP3 and gain specifications are as shown in Table II. Also we assume the Rx can operate in low gain mode to tolerate a maximum input signal of -10 dBm during normal operation. The mixer gain is fixed and in this case the LNA gain and LPF/PGA gain are as low as 3 and 7 dB, respectively, while the corresponding IP3 is 3 and 20 dB.

For the considered TRx in the loopback mode the $\mathrm{IP3}_{Tx}$ prevails over the $\mathrm{IP3}_{Rx}$. From (14) we find the contribution of Rx to be $(\mathrm{G}_{Tx}\mathrm{G_{TA}}/\mathrm{IP3}_{Rx})$ as compared to $(1/\mathrm{IP3}_{Tx})$ of Tx. Their ratio is equal to $\mathrm{G_{TA}} \times 44.2$ or $\mathrm{G_{TA}} \times 1.9$ in large and low gain mode, respectively.

If $\mathrm{G_{TA}} < 0.001$ (0.01) the contribution of $\mathrm{IP3}_{Rx}$ can be neglected so $\mathrm{IP3}_{Tx}$ can be well measured. Conversely, by increasing $\mathrm{G_{TA}}$ one can expect the $\mathrm{IP3}_{Rx}$ to be more pronounced (especially for the contribution ratio > 10). However, in the high gain mode there is a signal level limit imposed on $\mathrm{G_{TA}}$. Assuming the maximum signal at the Rx output +10 dBm (2 V_{pp}) and -10 dBm at the Tx buffer output, we find $\mathrm{G_{TA}} < 20 - (18 + 10 + 20) = -28$ dB (158×10^{-5}). In the low gain mode we find $\mathrm{G_{TA}} < 0$ dB which is not meaningful since $\mathrm{G_{TA}}$ will be less than -3 dB in practice. With those gain limits the IP3 contribution of Rx compared to Tx will only be < 0.07 and < 0.95 in the high and low gain mode, respectively. The measurement of $\mathrm{IP3}_{Rx}$ will be obscured in this way, but some impairments in $\mathrm{IP3}_{Rx}$ can be detected as we show beneath.

The TRx under test was implemented using MATLAB software. Specifically, for IP3 we have referred to the third-order polynomial model [33, Ch. 2] and for each block we defined

$$A_{\mathrm{IP3}}^2 = \frac{4}{3} \times \left| \frac{a_1}{a_3} \right| \tag{23}$$

where A_{IP3} is IP3 expressed as a sine amplitude in volts ($\mathrm{IP3(dBm)} = 10 \log \mathrm{A}_{\mathrm{IP3}}^2 + 10$), while a_1 and a_3 are the polynomial coefficients (a_1 is the fundamental voltage gain).

To test the TRx in the loopback setup a two tone signal of 4 and 6 MHz was applied at the Tx baseband. Using the FFT of the output response, IM3 can be measured directly while IP3 can be found from $\mathrm{IP3} = P_{\mathrm{in}} + |\mathrm{IM3}|/2$.

As seen from the latter formula, during test the IM3 achieves sensitivity 2 × larger than IP3 (in decibel scale). In Fig. 17 the fast Fourier transfer (FFT) spectrum of the two-tone response received at baseband is shown using coherent sampling. The intermodulation products of interest are located around the primary tones at 2 and 8 MHz, and the measured IM3 is -18.2 dB (large gain mode). The power of each tone at Tx baseband is -8 dBm and $G_{\mathrm{TA}} = -50$ dBm. Hence, the corresponding IP3 =1.1 dBm while from (23) we find 0.6 dBm.

The noise models are included here as in the previous example. Observe that SNR is increased by the FFT processing gain equal $10 \log(N/2) = 39$ dB, so in fact, SNR ≈33 dB (as in Section VIII-A for -60 dBm at Rx input).

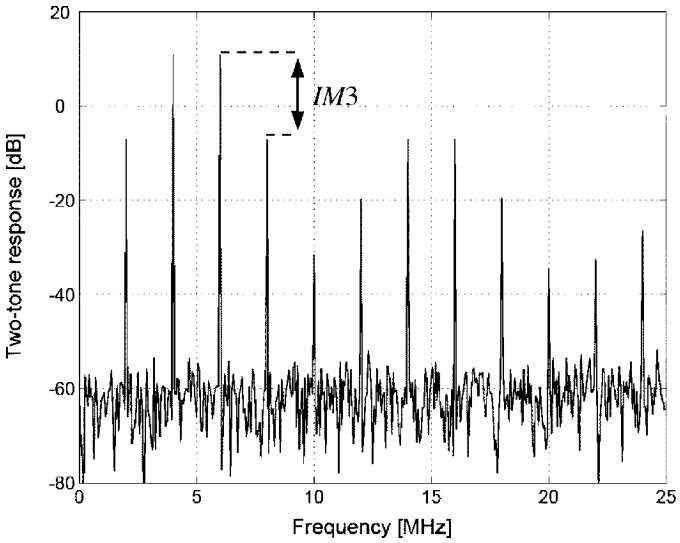

Fig. 17. Two-tone FFT response of TRx measured in loopback setup (f_S =1024 MHz and $N = 2^{14}$ samples).

To verify the test we consider impairments in IP3 to occur in different blocks of the TRx. The impairments (faults) are chosen to be 3 dB each, while the corresponding gains are assumed not to be affected. As explained before a possible reduction of gain tends to obscure an IP3 fault and in such a case the loop gain measurement or BER test would be preferred.

The test results are summarized in Table VI where $\mathrm{F1}, \mathrm{F2}, \ldots, \mathrm{F5}$ stand for single IP3 faults in Tx mixer, Tx buffer, LNA, Rx mixer, and LPF/PGA, respectively. IM3 is measured since it is more pronounced than IP3. With high TA attenuation ($G_{\mathrm{TA}} = -50$ dB) the faults in Tx are well visible. Specifically the IM3 measured for F2 differs form the fault-free response by more than 6 dB. As opposed to this the faults in Rx are perfectly masked by GTA in this case, and to make them detectable GTA is set to -3 dB which is a maximum value. At the same time the Tx baseband power is reduced by 25 dB in order to prevent the Rx saturation ($<$ 10 dBm at output). In this case, the faults in Rx mixer (F4) and in LPF (F5) are well seen as well. When LPF/PGA is set to the low-gain mode its contribution to IP3 (and IM3) is less and F4 becomes even more pronounced (IM3 differs $>$ 4 dB from FF-case). Unfortunately, in either case F1 and F3 are more difficult to detect, and this is attributed to the masking effects. Specifically, making F3 in LNA more visible, requires a larger gain in the signal path preceding LNA. In fact, it can hardly be achieved since this gain is already at its maximum. To detect those faults only more observability can help. Impairments in IP3 are usually accompanied by impairments in P1dB (ideally P1dB is less from IIP3 by 9.6 dB). So in this case they can be measured by RF detectors directly.

C. EDGE Transceiver With Direct Modulation Under EVM/BER Test

An EDGE transceiver has been modeled using Agilent's ADS software. The transceiver operates in TDD mode where a directly modulated LO is shared between Tx and Rx. To enable the LBT the setup shown in Fig. 4 is used that directly supports QPSK modulation. The EDGE 8-PSK can be encoded at Tx baseband and then up-converted in the offset mixer. During test the LO only serves as a carrier generator since any phase modulation is cancelled in the Rx mixer.

The phase lag α has a profound impact on the test measurements. Fig. 18 displays the EVM test for the fault-free TRx. In vicinity of $\alpha = 45°$ for QPSK, and $\alpha = 22.5°$ for EDGE 8-PSK the EVM tends to rise enormously that might suggest a fault exists. In fact, this is due to the maximum crosstalk between I and Q path in Rx as discussed in Section III. Otherwise, the EVM value is pretty stable with α. Upon a NF/gain fault the EVM tends to rise as shown Fig. 19, but for α close to its critical value this can be a non-monotonic relation. As seen, at lower signal power much better test sensitivity is achieved (70 dB attenuation).

TABLE VI
MEASUREMENT OF IM3 [DB] BY TWO-TONE TEST

G_{TA} dB	FF	F_1	F_2	F3	F_4	F_5
-50	18.16	17.12	11.71	18.16	18.16	18.16
-3 *)	39.59	39.50	39.36	39.01	36.19	36.83
-3 **)	42.38	42.25	42.05	41.58	37.87	41.36

*) *Rx in high-gain mode,* **) *only LPF in low-gain mode*

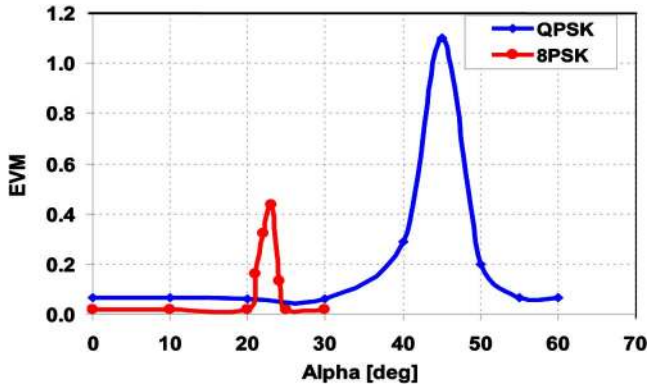

Fig. 18. EVM for fault free circuit versus rotation α for QPSK and EDGE.

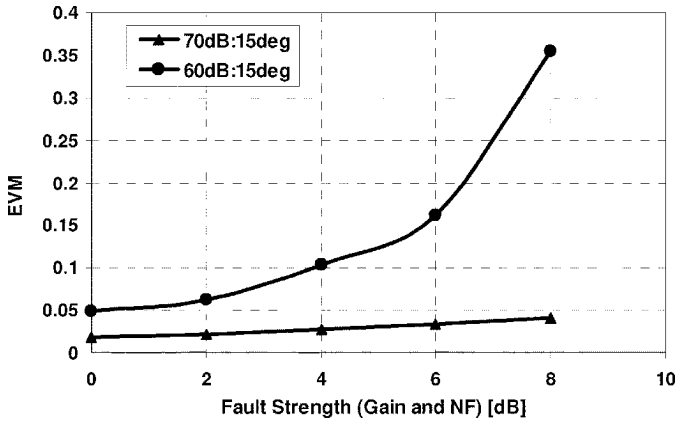

Fig. 19. EVM for EDGE 8-PSK versus fault in LNA for $\alpha = 15°$. Both gain and NF of LNA are degraded.

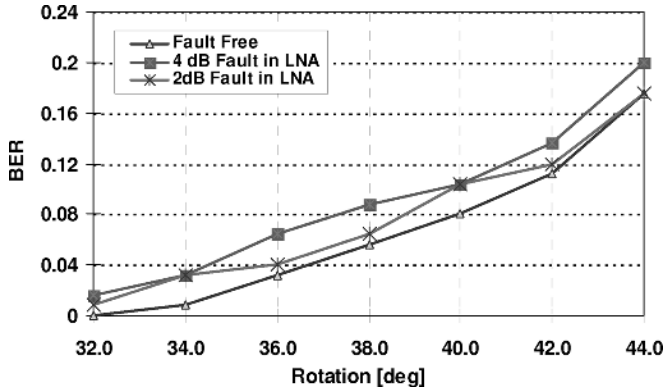

Fig. 20. Impact of phase delay α on BER in QPSK for fault free- and faulty circuit (two faults of different strength in LNA are shown).

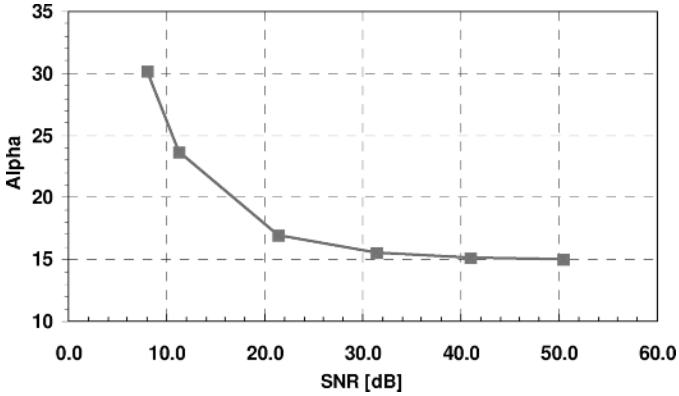

Fig. 21. Effective α versus SNR (original value of α is 15°).

With larger values of α also BER test is less reliable. As shown in Fig. 20 the stronger fault (4 dB) not necessarily gives larger BER values and to avoid it α should be compensated accordingly. In this model the noisy constellation points tend to scatter unevenly and for lower values of SNR the effective α is substantially changed compared to its original value as illustrated in Fig. 21.

The EVM meter implemented in ADS defines the constellation reference points in a way that it is sensitive to IQ imbalance. In particular, impairments in gain/NF in one leg of the down-conversion IQ mixer or the IQ phase mismatch resulting in skew effect, can be well detected in this test despite LNA gain prevents SNR to change much. This test is illustrated in Fig. 22. When both gain and NF are degraded the EVM is the same as for the fault in gain only. If only mixer NF is degraded the fault is hardly detected (not shown on in Fig. 22).

IX. Conclusion

As the RF integrated circuits operate at gigahertz frequencies and are becoming increasingly complex, in mass production the standard tests aimed at detailed specifications of the involved RF blocks appear impractical and costly in terms of the instrumentation and test time. Direct RF measurements on wafers require extra contact points that tend to degrade the chip performance while parasitics of the needle probes hinder the measurements.

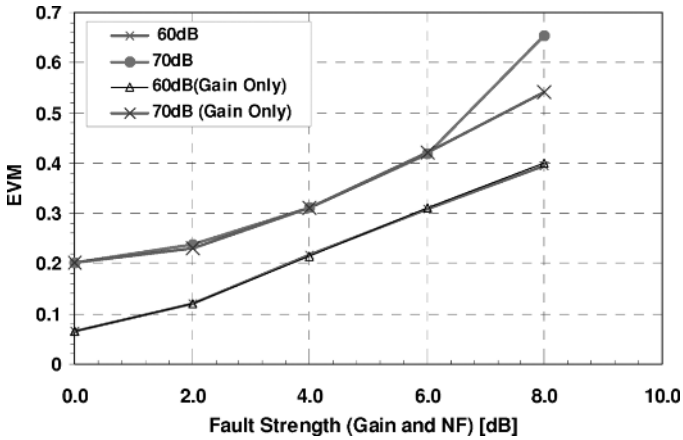

Fig. 22. EVM for QPSK versus fault in down-conversion mixer (in one mixer only, I or Q), $\alpha = 15°$.

Those drawbacks can be evaded by a BiST technique based on the loopback setup where baseband measurements are used instead. In this case, test signatures such as BER, EVM, loop gain, or the received baseband spectrum are useful to detect defects or possible impairments in the RF specifications. Unfortunately, the other blocks in the loopback path often tend to obscure the respective faults. To improve test observability the sensitization techniques can be used. In this case the test stimulus or response (such as the elevated BER by translation technique) is optimized for maximum fault detection or maximum correlation between the measured response and the specification according to the type of test.

As discussed in this paper, in production test it is useful to put the LBT in the fault-oriented perspective where the test responses aim at detecting faults directly, rather than reflecting basic specifications of the front-end blocks. Even though in both cases the test responses can be represented by the same physical quantities the respective measured values can be very different for different test pattern attributes and/or different test setup specifications applied.

The test observability at RF can be enhanced further by embedded RF detectors. Those detectors and the loopback elements (attenuator and offset mixer) usually require calibration that is not a trivial task to be performed on a chip. Linearity of the loopback elements can be crucial while their noise figure appears less significant since a large attenuation is usually required. With nonlinear behavior the possible impairments in linearity of the RF blocks can be obscured or false rejects can occur during test. In practice, the test circuitry can be transparent to the chip operation and low area overhead can be maintained.

A straightforward extension of the loopback setup is in bypassing of certain blocks in the loop path. The bypassing technique improves test controllability and is helpful in raising the test sensitivity for different fault locations. Also fault diagnosis, which is vital during chip characterization, is supported in this way. The blocks intended for bypassing such as LNA should be designed for test, specifically to avoid signal losses and harmful loading effects.

Fault detection can also be hampered by process tolerances. To capture this effect a behavioral model supported by simple

statistical analysis can be used as an alternative to the computer-intensive Monte Carlo approach. With this technique as proposed in this paper the detectability thresholds for various faults can be identified and also different tests can be compared for detectability. Since the parameter tolerances tend to drive the RF circuits out of specs, in submicrometer technologies the design for correction (DfC) is practically a must and it should be combined with DfT. By DfC the impact of tolerances on test is largely mitigated but the need for test is not diminished.

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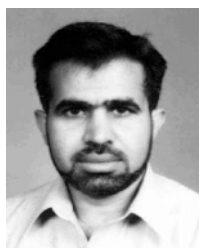
Jerzy J. Dąbrowski (M'03) received the Ph.D. and D.S. degrees from Silesian University of Technology, Gliwice, Poland.

Currently, he is an Associate Professor with Linköping University, Linköping, Sweden. He has specialized in macromodeling and simulation of analog and mixed-signal circuits. His recent research interests are in RF ICs design and design-for-testability for analog/RF circuits. He published over 80 research papers in international journals and conference proceedings, and one monograph. He holds 12 patents (as a coauthor) in switched-mode power supplies and electronic instrumentation.



Rashad M. Ramzan (S'03) received the B.E. degree with honors from University of Engineering and Technology Lahore, Lahore, Pakistan, in 1994, the M.S. degree from Royal Institute of Technology, Stockholm, Sweden, in 2003. He is currently pursuing the Ph.D. degree in testable and reconfigurable RF circuits from Linköping University, Linköping, Sweden.

After graduation, he joined Advanced Engineering Research Organization and worked on mixed signal system design for four years. In 1999, he joined Enabling Technology Islamabad, a branch office of the same company in Irvine, CA. At Enabling Technology, he was a part of the team who designed a media processing ASIC for VoIP application for future IP telephony. His research interests are mainly focused on fully integrated transceivers and design for testability.