BUILT-IN SELF CALIBRATION FOR PROCESS VARIATION IN SINGLE-LOOP CONTINUOUS-TIME SIGMA-DELTA MODULATORS

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ABSTRACT

A novel built-in self calibration technique for single-loop continuous-time sigma-delta modulators is proposed. Using out-of-band test signal injection and digital cancellation, this technique provides an area efficient, highly digital calibration structure to counteract gain variations in the loop filter. The calibration methodology and mathematical analysis are presented using a 2nd order multibit sigma-delta modulator as a proof of concept. The effect of the finite gain-bandwidth of amplifiers is included when evaluating the calibration method. The proposed technique is validated through corner simulations using behavioral models and it shows that degradation in the signal-to-noise-plus-distortion ratio can be counteracted.

Index Terms— Analog-to-digital converter (ADC), continuous-time, sigma-delta modulator, digital calibration, process variations.

1. INTRODUCTION

During the last years, continuous-time (CT) sigma-delta ($\Sigma\Delta$) analogue-to-digital converters (ADCs) have become very popular as they offer inherent anti-aliasing filtering and low power dissipation. However, CT implementations suffer from several non-idealities such as process variations, excess loop delay (ELD), jitter sensitivity and non-linearity of the feedback digital-to-analogue converter (DAC) in the multibit case. The CT filter in the modulator is highly susceptible to process variations as its coefficients depend on the absolute value of resistors and capacitors. While the matching between capacitors or resistors is in the order of 1% or less, the product of their absolute values can vary up to $\pm 40\%$. This leads to a deviation from the desired noise-transfer-function (NTF) and, potentially, to an increment of the in-band-noise (IBN) and instability. Consequently, correction techniques, such as [1, 2, 3, 4], are generally required so as to counteract such deviation.

2. PROPOSED CALIBRATION TECHNIQUE

Calibration methods, based on correction techniques for CT filters [1, 2], have been widely used in single-loop (SL) CT $\Sigma\Delta$ ADCs to correct the deviation of the loop filter coefficients. Most of these techniques employ area consuming replica circuits in a master-slave configuration. Recently, calibration techniques using automatic tuning have been proposed, such as [3] and [4]. The latter technique is used on-line in a SL modulator with spread zeroes. Furthermore, a test tone is injected before the quantizer at the frequency of the spread zero and the coefficients deviation is detected by correlating the output of the modulator with such injected signal. Due to the finite step in the capacitor array, a small in-band residual tone is still present after the calibration is completed affecting the overall performance of the modulator. The proposed calibration technique counteracts this limitation by injecting an out-of-band tone and using the aforementioned detection by correlation technique. By doing so, no in-band residual tone is present after calibration. Besides, loop filters with and without spread zeroes can benefit from it and on-line operation is still available. The $\Sigma\Delta$ modulator that has been selected as a test case with the proposed calibration circuitry included is shown in Figure 1. The chosen modulator consists of an Op-Amp-RC based 2nd order loop filter with 33-levels quantizer and an oversampling-ratio (OSR) of 16. Its target signal-to-noise-plus-distortion ratio (SNDR) is 70 dB over a bandwidth of 10 MHz. The loop filter is a cascade of integrators in feedback form (CIFB) along with DAC_3 in order to compensate for ELD and a feedforward coefficient, d_2. The calibration circuitry consists of a test signal generation block, a deviation sensing block and an array control block. It is worth to notice that all calibration blocks are highly digital, having only the arrays of passives and two DACs as analog or mixed-signal blocks. The test signal generation block processes a signed-binary signal with a period equal to 16 times the clock period ($T_w = 16\,T_s$) and injects two different signals: (a) $w_1(n)$ in the 1st feedback branch through DAC_{k1}, and (b) $w_2(n)$ right before the quantizer through DAC_{k2}.

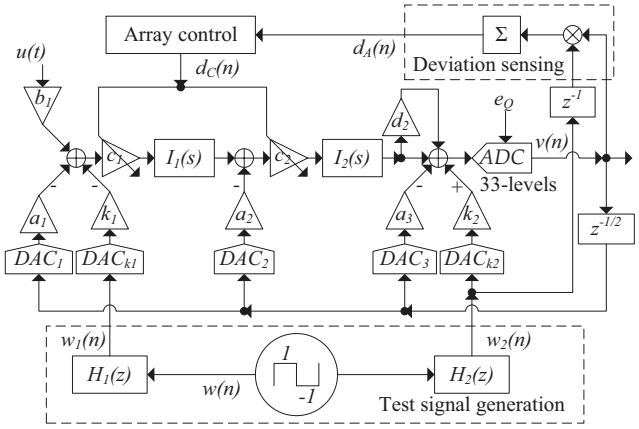

Fig. 1. Block diagram of a 2nd order $\Sigma\Delta$ modulator with the proposed calibration circuitry.

This work has been supported by Swedish Research Council (VR) under Digitally Enhanced RF/Analogue for Wireless Radios project.

Without loss of generality, a normalized sampling rate of 1 ($T_s = 1$) is considered.

The idea behind digital cancellation is to find $H_1(z)$ and $H_2(z)$ so as to cancel $w_1(n)$ and $w_2(n)$ before the quantizer when there are no deviations in the integrators coefficients. If there is a mismatch between these coefficients, part of $w_1(n)$ will not be cancelled and will appear at the output of the modulator. This leakage is detected by the deviation sensing block as it has been proven already in [4] and [5], by multiplying a delayed version of $w_2(n)$ with $v(n)$ and accumulating this product. Based on such detection, the array control block switches an array of passives to tune the coefficients.

When considering process variations, it is assumed that the RC products will suffer the same spread, Δ_{RC}, and that the mismatch between ratios of R or C is negligible. Same assumptions have been considered in earlier publications and verified through measurements [6]. The Δ_{RC} spread will affect the gain, $\frac{1}{RC}$, of each integrator which is given by the products of $b_1\, c_1$ and $a_1\, c_1$ for the 1st integrator and by c_2 and $a_2\, c_2$ for the 2nd integrator. As the spread will be the same for all RC products, it can be mapped as a coefficient error $(1 + \Delta_{RC})$ that will be inserted before each $I_i(s)$. Furthermore as the coefficients a_3 and d_2 can be implemented by ratios of R or C, their effect would be negligible.

2.1. Calibration considering only process variations

In order to provide a better understanding of the calibration method, only process variations are considered. Later on, the effect of finite gain-bandwidth of amplifiers will be added and the calibration structure will be analyzed.

Impulse invariant transformation has been used throughout this work in order to find both the loop filter (LF) coefficients as well as the digital blocks $H_1(z)$ and $H_2(z)$. The output of the modulator, when only the quantization noise and the test signal are considered, is found by applying superposition and is given by:

$$V(z)|_{u=0} = E_Q(z)\, NTF_{E_Q}(z) + W(z)\, TF_W(z) \tag{1}$$

where $NTF_{E_Q}(z)$ is the continuous to discrete time (CT-DT) noise-transfer function (NTF) transformation when only the quantization noise $E_Q(z)$ is considered and is used to obtain the CT LF coefficients from a DT transfer function (TF). $TF_W(z)$ is the CT-DT TF transformation when only the test signal $W(z)$ is considered and is given by:

$$\begin{aligned} TF_W(z) = {} & NTF_{E_Q}(z)\cdot \\ & (-LF_W(z)\, H_1(z) + k_2\, H_2(z)) \end{aligned} \tag{2}$$

where $LF_W(z)$ is the CT-DT transform of the path that the test signal travels through the loop filter. For $\Delta_{RC} = 0$, it is given by:

$$\begin{aligned} LF_W(z) &= \mathcal{Z}\left\{ \mathcal{L}^{-1}\left[k_1\, c_1\, c_2\, (d_2+1)\cdot DAC_{k1}(s)\, s^{-2}\right]\Big|_{t=n\,T_s}\right\} \\ &= k_1\, c_1\, c_2\, (d_2+1)\left(\frac{1}{2}\frac{1}{z-1} + \frac{1}{(z-1)^2}\right) \end{aligned} \tag{3}$$

From (2) it is possible to see that, in order to cancel the test signal, $H_2(z)$ should be:

$$H_2(z) = \frac{H_1(z)\, LF_T(z)}{k_2} \tag{4}$$

According to (3) and (4), if $k_2 = k_1\, c_1\, c_2\, (d_2 + 1)$ and $H_1(z) = 1$, $H_2(z)$ will be equal to the last factor of (3). Unfortunately, this solution is not implementable because if $W(z)$ is processed by such $H_2(z)$, its output would be unbounded. In order to counteract this issue, $H_1(z)$ is set to:

$$H_1(z) = \left(1 - z^{-1}\right)^2 \tag{5}$$

Consequently, assuming $k_2 = k_1\, c_1\, c_2\, (d_2+1)$, $H_2(z)$ will be given by:

$$H_2(z) = \frac{1}{2}\left(z^{-1} + z^{-2}\right) \tag{6}$$

Moreover, as it can be seen from (5) and (6), these functions can be easily implemented in the digital domain.

So far it has been assumed that $k_2 = k_1\, c_1\, c_2\, (d_2 + 1)$. If the transient output of $H_1(z)$ and $H_2(z)$ are plotted when processing $W(z)$, it can be seen that $W_1(z) = \{-2, 0, 2\}$, while $W_2(z) = \{-1, 0, 1\}$, meaning that DAC_{k1} and DAC_{k2} would have same number of levels but different output amplitude. To make both DACs identical, $H_1(z)$ has been divided by 2 in the digital domain. Consequently, k_2 is now given by:

$$k_2 = \frac{1}{2}\, k_1\, c_1\, c_2\, (d_2 + 1) \tag{7}$$

In order to validate the digital cancellation principle as well as the calibration technique, MATLAB transient simulations were run with the calibration circuitry in open loop configuration. This was obtained by removing the array control block and setting a specific spread Δ_{RC} in the integrator's coefficients. Figure 2 shows the power spectral density (PSD) of the modulator's output $v(n)$ and the output of the accumulator, $d_A(n)$ when $\Delta_{RC} = \{-15, 0, 15\}\%$. First it is possible to observe that, when $\Delta_{RC} = 0\%$, $w_1(n)$ and $w_2(n)$ will cancel each other and the accumulation of the product will be located around zero. This cancellation is also noticeable by observing the corresponding PSD. As expected, when there is a positive or negative spread, the accumulation will be negative or positive respectively and an out-of-band residual tone will appear. Taking into account this behavior, a simple control logic for the array control block has been developed, as illustrated by the following pseudocode:

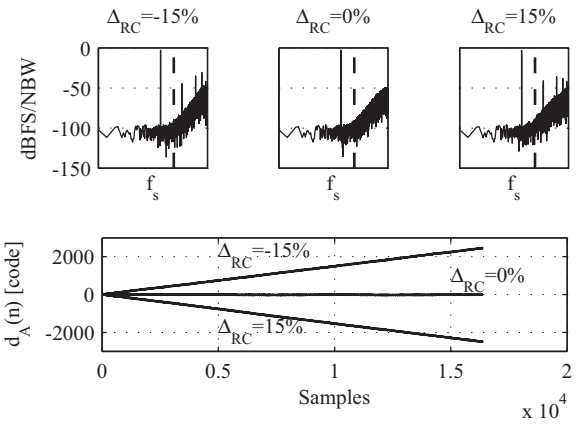

Fig. 2. PSD of the modulator's output, $v(n)$, and accumulator's output, $d_A(n)$, when $\Delta_{RC} = \{-15, 0, 15\}\%$.

if $d_A(n) > threshold$ **then**

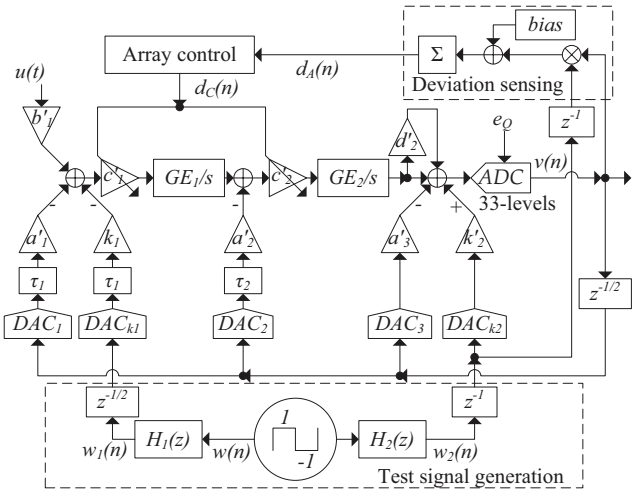

Fig. 3. Block diagram of a 2nd order ΣΔ modulator with the proposed calibration circuitry when considering finite amplifier's GBW.

if $d_C(n) \neq d_{C,max}$ **then**
$d_C(n+1) = d_C(n) + 1$
end if
else if $d_A(n) < -threshold$ **then**
if $d_C(n) \neq d_{C,min}$ **then**
$d_C(n+1) = d_C(n) - 1$
end if
else
$d_C(n+1) = d_C(n)$
end if

where $threshold$ is a value to account for small variations around zero of $d_C(n)$ when $\Delta_{RC} = 0\%$, and $d_{C,max}$ and $d_{C,min}$ are the respectives maximum and minimum codes of the passives array used to tune the coefficients.

2.2. Calibration considering process variations and finite integrator gain-bandwidth

As $w_1(n)$ goes through the integrators before being cancelled by $w_2(n)$, it is obvious that finite gain-bandwidth in the amplifiers have to be considered for the calibration technique to operate correctly. As shown in Figure 3, gain-bandwidth (GBW) induced errors can been modeled as a gain error, GE_i, plus a time delay, τ_i [7]. New values for the loop filter coefficients, a'_i, b'_i, c'_i and d'_i, are computed by an iterative method in order to compensate for both the gain errors and the time delays.

The cancellation circuit is affected by both gain errors, GE_1 and GE_2, and the time delay τ_1. In order to compensate for the time delay τ_1, one clock cycle delay has been introduced after $H_2(z)$. Disregarding the half clock cycle introduced after $H_1(z)$, the new CT-DT TF transformation when only the test signal $W(z)$ is considered, $TF_{W,GBW}(z)$, is now given by:

$$TF_{W,GBW}(z) = NTF_{E_Q}(z)\left(-LF_{W,GBW}(z)\,H_1(z) + k_2\,H_2(z)\,z^{-1}\right) \quad (8)$$

while the CT-DT transform of the path that the test signal travels

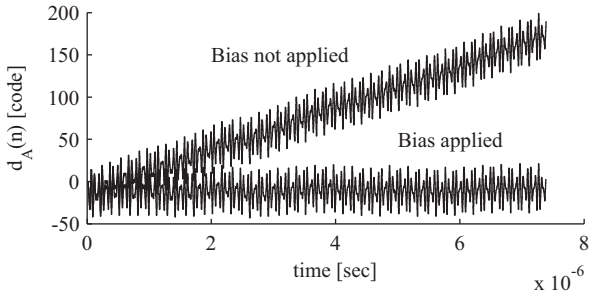

Fig. 4. Output of the accumulator, $d_A(n)$, when $\Delta_{RC} = 0$ with and without biasing factor applied.

through the loop filter is now given by:

$$LF_{W,GBW}(z) = k_1\,c'_1\,c'_2\,(d'_2+1)\left(\frac{1}{2}\frac{\tau_1^2+1-2\,\tau_1}{z-1} + \frac{\tau_1-1}{(z-1)^2} + \frac{\frac{-\tau_1^2+2\,\tau_1}{z-1} + \frac{\tau_1}{(z-1)^2}}{z}\right) \quad (9)$$

Taking (9) into account, the gain errors can be easily accounted for by computing a new value for k'_2 as given by:

$$k'_2 = \frac{1}{2}\,k_1\,c'_1\,c'_2\,(d'_2+1) \quad (10)$$

However, assuming the same $H_1(z)$ given in (5), $H_2(z)$ will now be equal to:

$$H'_2(z) = \frac{1}{2}\left(\tau_1^2+1-2\,\tau_1 - \frac{2\,\tau_1^2-1-2\,\tau_1}{z} + \frac{\tau_1^2}{z^2}\right) \quad (11)$$

From (11) it is possible to see that, unless $\tau_1 = 1$, both the complexity of the $H'_2(z)$ as well as the required number of levels in DAC_{k2} would increase. As τ_1 is a function of the GBW of both Op-Amps, a solution could be to set certain GBWs in order to obtain $\tau_1 = 1$. As this solution would restrict the freedom in the design of the Op-Amps, an alternative is proposed. If $H'_2(z)$ is kept as $H_2(z)$, the cancellation of $w(n)$ will not be complete, when $\Delta_{RC} = 0$, and a residue will appear. This phenomenon has two main consequences: (a) when $\Delta_{RC} = 0$, a residual tone will be present, and (b) the accumulation of $(W_2(z)\,z^{-1}\cdot V(z))$ will be biased. Both the magnitude of such tone as well as the bias will be proportional to the deviation of τ_1 from 1. The existence of a residual tone is not so detrimental as it is located out-of-band and can be filtered in digital domain. However, a biasing factor has to be inserted before the accumulator in order to return the accumulation back to 0 when $\Delta_{RC} = 0$, as shown in the deviation sensing block in Figure 3. The value of this bias factor can be determined by performing a transient simulation of the circuit in calibration open loop when $\Delta_{RC} = 0$ and plotting the accumulator value. Finally, as $\tau_1 \approx 0.22$ due to the selected GBW values for the integrators, half a clock cycle delay has been inserted after $H_1(z)$ in order to bring the total delay of $LF_{W,GBW}(z)$ closer to 1. In order to illustrate this concept, behavioral simulations have been performed in Cadence AMS simulator using finite GBW amplifiers in the integrators and $\Delta_{RC} = 0\%$. Figure 4 shows the output of the accumulator, $d_A(n)$, with and without biasing factor applied. The biasing factor found through simulation is added before the accumulator, restoring the accumulation to 0.

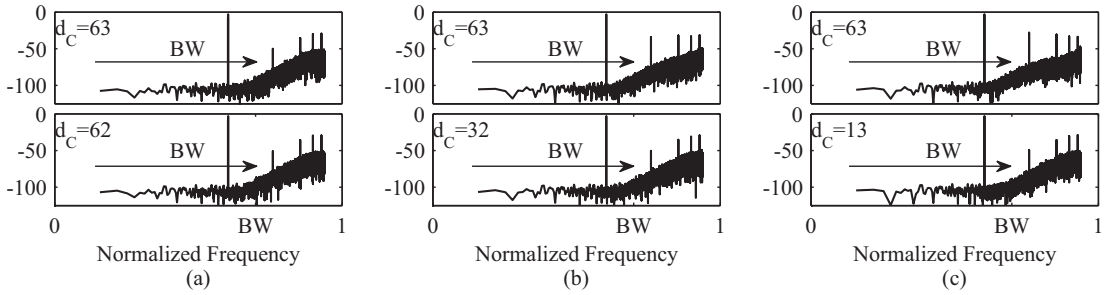

Fig. 5. PSD of $v(n)$ with and without calibration under corners. $P_{sig} = -3$ dBFS and $f_{Sig} = 1/3\, f_B$. (a) Corner = Minimum. (b) Corner = Typical. (c) Corner = Maximum.

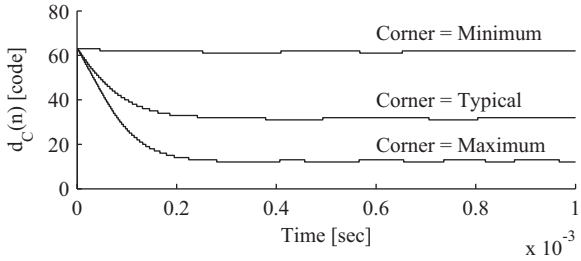

Fig. 6. Output of array control block, $d_C(n)$, under corners.

3. SIMULATION RESULTS

In order to validate the proposed built-in calibration method, several behavioral simulations have been performed in Cadence AMS environment. All digital blocks are coded in Verilog, the amplifiers are modeled in Verilog-A and the DACs and quantizer are modeled in Verilog-AMS. The passives, which set the loop filter coefficients, are implemented using a 90nm CMOS process. Coefficient tuning is performed by means of a 6-bit capacitor array, providing a tuning range and tuning accuracy of $\pm 40\%$ and 1.04% respectively [1]. The initial value for the array is in the higher end of the tuning code $(d_C(n) = 63)$ which is equivalent to start with a -40% bias with respect to the designed coefficients. This inital value is set to ensure the stability of the modulator when the calibration process begins.

The calibration technique has been tested by performing transient simulations when the passives suffer variations as dictated by the design kit's corner models. Figure 5 illustrates the PSD of the modulator's output, $v(n)$, both when the circuit is on its initial (uncalibrated) condition as well as after calibration is applied. Figure 6 shows the output of the control circuit, $d_C(n)$, that switches the capacitor array. In the minimum case, the final value of $d_C(n)$ experiences almost no change as its initial value is already in the higher end. Consequently, its initial and final PSDs show also negligible differences and a SNDR of 72.7 dB. In the typical case, however, $d_C(n)$ decreases to its middle value and the change between the initial and the final PSD is now noticeable with an initial and final SNDR of 69.1 dB and 72.2 dB respectively. After calibration, both the noise as well as the power of the injected tone (1st out-of-band tone) decrease. Finally, in the maximum case, $d_C(n)$ decreases, as expected, down to the lower end of the calibration code and the difference between the initial and the final PSD is even more pronounced with an initial and final SNDR of 65 dB and 72.1 dB respectively. It is also worth to notice the similarity between the three PSDs after calibration, both in their shape and measured SNDR.

4. CONCLUSION

A novel on-line calibration technique for single-loop CT $\Sigma\Delta$ modulators has been proposed. Out-of-band test signal injection combined with digital cancellation is introduced to allow detection by correlation in single-loop structures without in-band residual tone. With the help of a 2nd order $\Sigma\Delta$ modulator as a test-case, its concept along with mathematical analysis have been presented. The influence of the finite gain-bandwidth of amplifiers in the calibration operation has been investigated and solutions have been proposed. Corner simulations using behavioral models have demonstrated the effectiveness of the calibration. It has been shown that 7 dB degradation in the SNDR can be avoided. Finally, due to the intensive use of digital circuitry, this technique allows an area efficient nanometer CMOS solution.

5. REFERENCES

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