Journal of the Korean Physical Society, Vol. 41, No. 6, December 2002, pp. 963∼966

Built-in Self-Test Implementation for an Analog-to-Digital Converter

Kwisung Yoo, Minho Kwon, Geumhwan Bahng, Sangyun Hwang, Hoon Lee,
Jungyoon Lee, Daesik Seo, Jaeseok Kim, Sungho Kang and Gunhee Han*
Department of Electrical and Electronic Engineering, Yonsei University, Seoul 129-742

(Received 23 April 2002)

As integrated circuit fabrication techniques advance, a complex system can be integrated on a single chip: namely, a system-on-a-chip (SOC). A SOC consists of many intellectual property (IP) building blocks, including analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) which should provide certain built-in self-test (BIST) scheme to minimize the testing cost. Due to the analog nature of ADCs and DACs, digital BIST schemes are not applicable. This paper proposes a simple ADC BIST scheme based on a ramp test. The proposed BIST scheme is verified by simulation with a 6-bit pipelined ADC. Simulation results show that the proposed ADC BIST scheme can detect not only catastrophic faults but also some parametric faults. The total gate count of the proposed BIST circuit is about 150.

PACS numbers: 85.40.Qx
Keywords: BIST, ADC BIST

I. INTRODUCTION

As IC fabrication techniques have been improved, a complex system can be implemented on a chip. The test cost of a SOC often overwhelms the design and the fabrication cost due to the complexity of the implemented system [1,2]. Because the price of the automatic test equipment drastically increases as the system speed and complexity increases, various Built-In-Self-Testing (BIST) techniques have been introduced to reduce the test cost [3–8]. Most of the reported BIST schemes are limited to a digital system and a memory. Few analog BIST schemes have been reported [9–12] and this field is still in its primitive stage. The absence of compact circuits to measure analog value and the fuzzyness of the criterion make the analog BIST challenged.

ADCs and DACs are commonly included in a SOC. ADC/DAC BIST is becoming a bottleneck of the SOC testing, though. Most of the reported ADC/DAC schemes require large overhead while the efficiency is low [13–16]. Common ADC testing involves measuring effective resolution and histogram with sinusoidal test input signal.

This dynamic testing requires Digital Signal Processor (DSP) for calculating Fast Fourier Transform (FFT) or accumulators and memories which require large overhead. Measurement of the Integral Nonlinearity (INL) error and the Differential Nonlinearity (DNL) error with ramp test signal is the other ADC testing method which is suitable for BIST due to the small overhead.

*E-mail: ykwisung@cad.yonsei.ac.kr; Fax: +82-2-312-4584

Although the ADC is an analog block, the output of ADC is digital. This property provides possibility to implement ADC BIST scheme with compact digital circuit. This paper proposes a simple ADC BIST scheme. Section II proposes the ADC BIST scheme and its implementation, section III provides verification results of the proposed scheme through simulation.

II. ADC BIST SCHEME AND IMPLEMENTATION

The proposed BIST system is depicted in Figure 1. As the analog test signal is applied to ADC's input, the ADC generates digital code corresponding to the input signal. Only with digital code, the error detector decides whether the ADC has any fault or not.

The ramp signal generator should have higher linearity

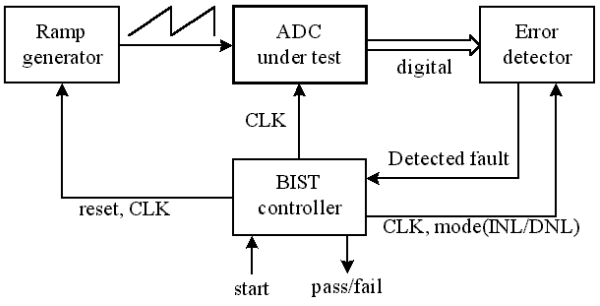


Fig. 1. BIST block diagram.

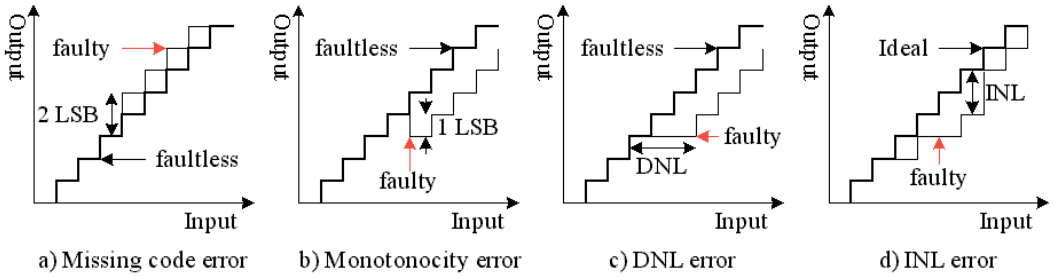


Fig. 2. Error definition.

than the ADC under test [17]. A high linearity ramp signal generator using Switched-Capacitor (SC) circuit was reported in [18]. The ramp test signal can be supplied by external equipment and shared by many ADCs under testing in parallel. The ramp test signal varies within dynamic range of ADC for proper operation and should be increased by 1 LSB per clock. Since the analog input is increased by 1 LSB per clock, the ADC output should be increased by 1 LSB per sample. If there exists any fault then the ADC output may be not increased by 1 LSB per sample.

Four types of errors are defined as in Table 1 and depicted in Figure 2 to detect faulty circuits. Here $x(n)$ is ADC output code for nth sample.

If the magnitude of two consecutive sample difference, $x(n) - x(n-1)$ is greater than 1 LSB then it means that the ADC output increases more than 1 LSB while the input signal is increased by 1 LSB. The ADC can be considered to be faulty, namely missing code error. If the sign bit of the difference is negative, then it means that the ADC output decreases even while the input signal is monotonically increased. This type of fault is defined as monotonocity error. If the ADC generates sample of same value more than 3 consecutive samples, $x(n-1) = x(n) = x(n+1)$, it means that ADC output is kept constant even while the input signal is increased by 3 LSBs. This fault corresponds to the DNL error. Ideally, if two consecutive samples output are identical then ADC under test can be considered as faulty circuit. However, due to some uncertainty in analog circuits, the boundary of the DNL error should be relaxed at least to 3 samples.

The INL/gain error is defined by the difference between the ADC's output and the ideal output that is obtained by counting the clocks in the ramp signal generator. The INL/gain error can be caused either by the nonlinearity or by the gain error of the ADC under test.

Table 1. Error definition.

	Definition
Missing code error	$x(n) - x(n-1) \geq 2LSB$
Monotonocity error	$x(n) - x(n-1) < 0$
DNL error	$x(n-1) = x(n) = x(n+1)$
INL/gain error	$ideal(n) - x(n) > boundary$

Figure 3 shows the block diagram of the proposed error detector. Assuming that the counter/register loads the ADC output which means previous sample at phase ϕ_4, the difference between the ADC output and the counter/register output is calculated at phase ϕ_1. If the counter/register output and ADC output are identical then flip-flop 3 is set to '0' at phase ϕ_3. If next sample is identical with previous two samples then the flip-flop 4 is set to '1' at phase ϕ_2. This means that the INL error occurs. The flip-flop 3 should be initially set to '1' for proper operation.

If the subtractor output except LSB has any '1', it means that the difference of two consecutive samples is more than 1 LSB. Therefore, ORing of all output bits except LSB detects the missing code error.

If there is underflow in the subtractor output, it means that the present sample is lesser than the previous sample. Therefore, monotonocity error can be detected with sign bit of subtractor output.

The counter/register is initially reset and counts the clock in ramp signal generator for the INL/gain error detection. This means that the counter represents ideal ADC output in the INL/gain error detection mode. If the difference between the ADC output and the counter/register exceeds certain limit (2^m) in the INL/gain error detection mode, then it means that there exists the INL error or the gain error. This boundary is checked by ORing of upper $(N-m)$ bits in the subtractor output.

III. SIMULATION RESULT

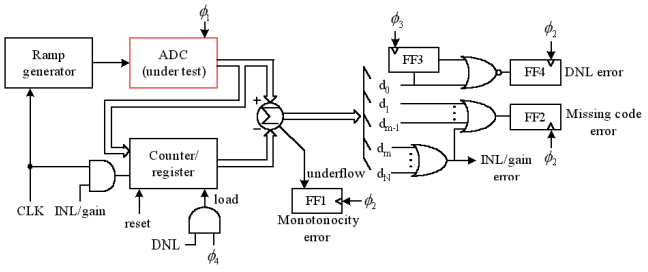
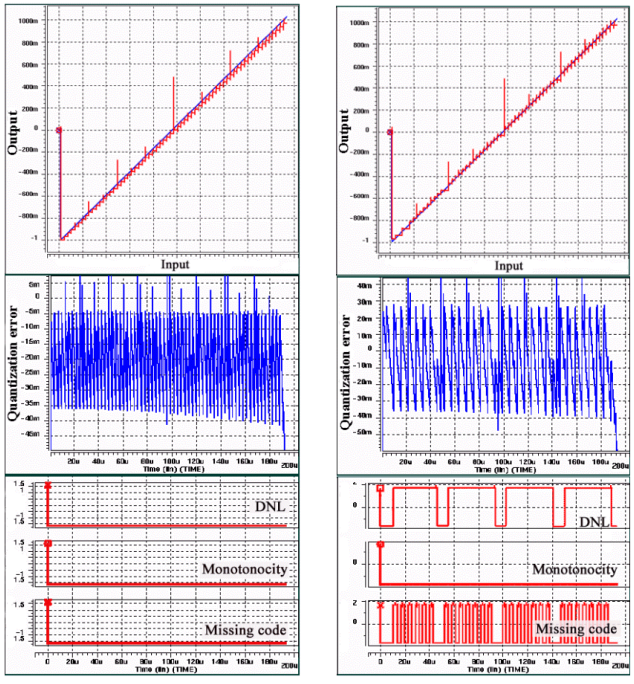


Fig. 3. Error detector.

Table 2. Result of simulation.

	Cause of fault	Type of error observed			Result of BIST		
		Missing code	Monoto-nocity	DNL	Missing code	Monoto-nocity	DNL
TC1	Normal circuit						
TC2	Offset	○		○	○		○
TC3	Offset	○		○	○		○
TC4	Gain	○		○	○		○
TC5	Gain & offset	○		○	○		○
TC6	Open	○		○	○		○
TC7	Short (internal node)	○	○		○	○	
TC8	Short (VSS)	○	○		○	○	
TC9	Short (VDD)	○	○		○	○	
TC10	Short (VDD)	○		○	○		○



a) Normal circuit (TC1) (b) TC with offset fault (TC2)

Fig. 4. Simulation example of TCs.

The proposed scheme is verified by the simulation with 6 bit pipelined ADC. Various test circuits that have arbitrary faults are simulated. These test circuits include both catastrophic faults such as open or short and parametric faults such as an amplifier gain error and a comparator offset error. Figure 4 shows the examples of simulation results. The topmost figure shows the input and the output of the ADC under test. The output of the ADC is converted to analog value with an ideal DAC for comparison purpose. The middle figure shows the ADC quantization error. The bottom figure shows the result of the error detector that is observed at the input node of each flip-flop. Any pulse in bottom figure represents corresponding errors.

The test ADC is designed to have dynamic range from -1 to 1, and offset binary code output to simplify the simulation. That is, 1 LSB corresponds to 31.25 mV. Thus, if absolute value of ADC's quantization error is greater than this value, then the ADC is considered as a faulty circuit.

Table 2 summarizes examples of simulation results. Besides of the example circuits shown in Table 2, various test circuits are simulated and the proposed BIST successfully detected faulty circuits that can be identified by a person. Though, certain circuits that have minor faults pass the BIST and inspection by a person as well.

IV. CONCLUSION

This paper proposes a compact ADC BIST scheme whose gate count is only about 150. Extensive simulation results proved that the proposed BIST scheme detects most of faulty ADCs that can be identified by person. Due to noise or any uncertainty in real circuits, the test should be performed several times and final decision should be made by BIST controller. Several circuits with minor faults pass the BIST and human inspection. These faults can be detected by more complex BIST the with price of overhead.

ACKNOWLEDGMENTS

This work was supported by a Korea Research Foundation grant (KRF 2000-042-E00029). CAD tools were supported by IC Design Education center.

REFERENCES

[1] Z. Barzilai, J. Savir, G. Markowsky and M. G. Smith, IEEE Trans. Computer, **C-30**, 996 (1981).

[2] Juin-Ming Lu and Cheng-Wen Wu, *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition* (Paris, March, 2000), p. 710.

[3] J. Park, H. Chang and O. Song, *Proceedings of the Second IEEE Asia Pacific Conference* (Cheju, Aug., 2000), p. 273.

[4] K. Zarrineh, R. D. Adams, T. J. Eckenrode and S. P. Gregor, *Proceedings of the International Test Conference* (Atlantic City, Oct., 2000), p. 547.

[5] M. M. Hafed and G. W. Roberts, *Proceedings of the IEEE Custom Integrated Circuits Conference* (Orando, May, 2000), p. 83.

[6] M. B. Santos, F. M. Goncalves, M. Ohletz and J. P. Teixeira, IEEE International Conference on Electronics, Circuits and Systems **2**, 419 (1998).

[7] E. J. Oh, S. H. Kim, D. I. Lee and H. Y. Choi, J. Korean Phys. Soc. **40**, 193 (2002).

[8] S. J. Park, D. K. Youn, T. H. Kim, S. W. Kang, H. K. Oh, K. G. Doh and Y. S. Moon, J. Korean Phys. Soc. **40**, 749 (2002).

[9] L. Carro, E. Cota, M. Lubaszewski, Y. Bertrand, F. Azais and M. Renovell, *Proceedings of the Ninth Asian Test Symposium* (2000), p. 78.

[10] J. Velasco-Medina, L. Rayane and M. Nicolaidis, *International Conference on Computer Design* (1999), p. 330.

[11] M. F. Toner and G. W. Roberts, *Proceedings of the IEEE Custom Integrated Circuits Conference* (Santa Clara, May, 1995), p. 525.

[12] L. S. Hurst, The Institution of Electrical Engineers, 381 (1998).

[13] K. Arabi, B. Kanminska and J. Rzeszut, *IEEE/ACM International Conference on Computer-Aided Design* (San Jose, Nov., 1994), p. 491.

[14] F. Azais, S. Bernard, Y. Bertrand and M. Renovell, *Proceedings of the European Test Workshop* (Cascais, May, 2000), p. 53.

[15] M. Renovell, F. Azais, S. Bernard and Y. Bertrand, *Proceedings of the 18th IEEE VLSI Test Symposium* (Montreal, April, 2000), p. 247.

[16] S. K. Sunter and N. Nagi, *Proceedings of the International Test Conference* (Nov., 1997), p. 389.

[17] Jing Wang; E. Sanchez-Sinencio and F. Maloberti, Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems **2**, 908 (2000).

[18] David A. Johns, Ken Martin, *Analog Integrated Circuit Design* (Wiley, New York, 1997), Chap. 10.