Built-In Self-Test Methodology for A/D Converters

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Abstract

A (partial) Built-In Self-Test (BIST) methodology is proposed for analog to digital (A/D) converters. In this methodology the number of bits of the A/D converter that needs to be monitored externally in a test is reduced. This reduction depends, among other things, on the frequency of the applied test signal. At low test signal frequencies only the least significant bit (LSB) needs to be monitored and a "full" BIST becomes feasible. An analysis is made of the trade-off between the size of the on-chip test circuitry and the accuracy of this BIST technique.

Keywords: A/D Converter, Mixed-Signal Test, BIST, Statistical Fault Analysis.

1 Introduction

With the advances in the area of mixed analog-digital Integrated Circuits (ICs), faster and more complex mixed-signal testers are needed to meet ever more demanding test specifications. Mixed-signal testers with such high performance on speed, precision, memory and noise are very expensive. Thus for analog and mixed-signal devices, a significant reduction of test costs can be achieved by reducing test time or by applying less complex tests on less expensive equipment. Test time and, thereby, test cost reduction can be achieved by moving some of the tester functions onto the chip itself or by testing more circuits on one IC in parallel. The amount of different circuitries on one IC that can be tested in parallel depends on the number of test pins available per IC and on the capabilities of the tester used. If all of the necessary tester functions are moved onto the IC, a Built-In Self-Test (BIST) strategy is created and an expensive tester is no longer needed.

The most frequently encountered parts on mixed signal circuits are the A/D and D/A converters, which bridge the gap between digital and analog systems. A/D and D/A converters are therefore parts for which on-chip processing of test data is attractive. Little has been published on on-chip testing of these converters [1]-[4]. This paper describes a methodology which can reduce the test costs of A/D converters by means of on-chip processing. As a result, the number of output bits, per A/D converter, to be acquired by the tester and the amount of test data to be processed by the tester is reduced. For ICs with multiple A/D converters on-chip, the reduction of test bits per A/D converter, allows for testing more A/D converters in parallel, which will reduce the overall test time. The same effect, test time reduction, is achieved by a reduction of the test data to be processed by the tester. The ultimate goal is to perform the test signal generation and all the test data processing on-chip, creating a complete BIST solution where no expensive mixed-signal tester is needed. In this research, only the possibilities of on-chip test data processing are explored. For on-chip test signal generation see DeWitt et al.[1] and Robert et al.[6].

An important aspect of a test method is the measurement errors which lead to so-called type I and type II errors. In the case of a type I error, a good device is rejected by the test; and in the case of a type II error, a faulty device is accepted by the test. The probability and the magnitude of the measurement errors is a measure for the quality of the test and depends on the accuracy of the performed test. In the case of an on-chip test, the accuracy of the test performed is related to the size of the on-chip test circuitry.

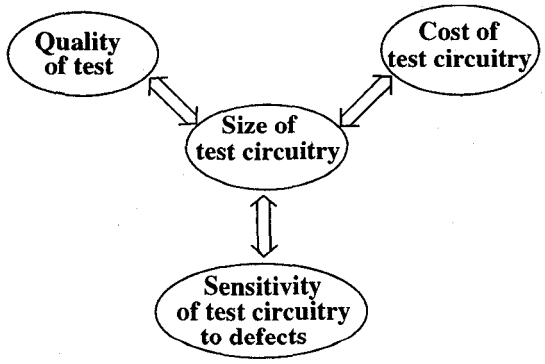

Figure 1: Issues related to the size of the test circuitry

In addition to this dependency, the size of the on-chip test circuitry has a direct relation to the cost of the test circuitry and to the fault sensitivity of the test circuitry itself. In Figure 1 these relations are illustrated. In the process of finding on-chip test schemes these four issues should be taken into account and a trade-off has to be made.

The following section will discuss the proposed BIST scheme for A/D converters, followed by an analysis of the measurement error in section 3. In section 4, the resulting simulation and measurement results are compared. Finally, section 5 presents the conclusions of this work.

2 BIST methodology

A/D converters are tested under both, static and dynamic conditions. Parameters used for testing the "static" behavior of A/D converters are the offset voltage, gain, Differential Non Linearity (DNL) and Integral Non Linearity (INL). Although these parameters are denoted as "static", they can also be defined under dynamic test conditions. In the so-called dynamic tests, the Total Harmonic Distortion (THD) and the introduced noise power are the main test parameters [4].

In Figure 2 a (partial) BIST scheme is shown, which can be used for testing both the "static" and "dynamic" behavior of the A/D converter. The Least Significant Bit (LSB) up to bit q are processed and tested off-chip; the remaining bits, bit $q+1$ up to the Most Significant Bit (MSB), are tested on-chip with a counter clocked if q goes from *1* to *0*.

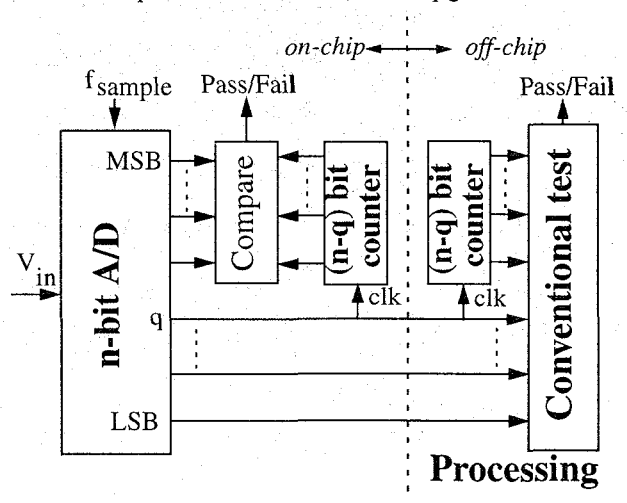

Figure 2: (Partial) BIST scheme

In order to be able to reconstruct the output codes of the converter, the frequency of the output signal at bit q must satisfy Shannon's theorem. This means that at least two samples are to be taken over one period of q (one sample at each state). As a result, the minimal number of bits needed, q_{min}, is determined by the frequency of the applied test signal $f_{stimulus}$, the sample frequency of the A/D converter f_{sample}, the number of bits of the converter n and the linearity specifications of the converter given by *NL*. For a sawtooth stimulus this gives:

$$q_{min} = ceil\left({}^{2}\log\left(\frac{f_{stimulus}}{f_{sample}}2^{n+1} + NL\right)\right) \qquad \textbf{(EQ 1)}$$

where "*ceil*" means that the term in brackets is rounded off to the larger integer. The *NL* in (EQ 1) is the largest allowed difference between the ideal and non-ideal transfercurves of the A/D converter over a range of $2^{q_{min}-1}$ codes which is determined by:

$$NL = min\{DNL \cdot 2^{q_{min}-1}, INL \cdot 2\} \qquad \textbf{(EQ 2)}$$

with *DNL* and *INL* the Differential Non Linearity and Integral Non Linearity specifications of the A/D converter. As long as (EQ 1) is satisfied, it will be possible to determine the total codeword from the value of the q least significant bits. It is clear that the higher the frequency of the test signal the more bits need to be processed and tested off-chip.

The test strategy illustrated in Figure 2 is capable of performing both static and dynamic tests as described in [8]. In the remainder of this article only the "static linearity errors" will be tested by monitoring the LSB ($q=1$) while the functionality of the A/D converter is tested by comparing the remaining bits of the converter with a counter which is clocked by the LSB. This way an approach is made to a "full" and easy to implement BIST which does not require too much chip area [7].

When a ramp is applied to the A/D converter it will be converted into a binary code at the sample frequency of the converter. The linearity of the A/D converter can be tested by monitoring the LSB because it contains the linearity information as is illustrated in Figures 3a and 3b.

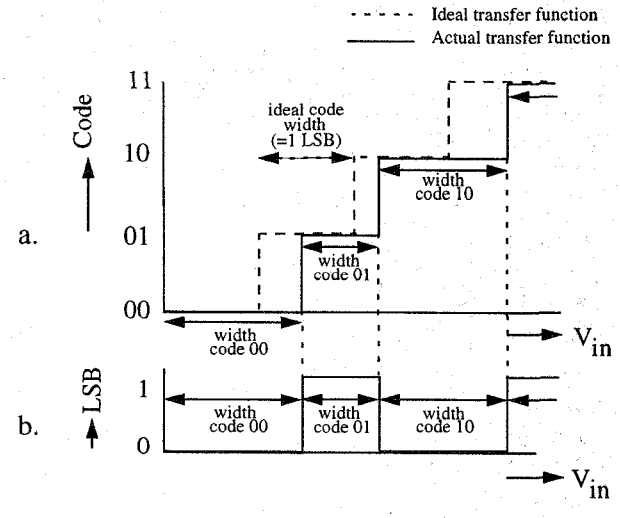

Figure 3: LSB contains linearity information

The linearity of the converter is determined by counting the number of samples taken of every code as is shown in Figure 4. The counter starts counting when the LSB makes a transition, at the next transition the contents of the counter is compared with an upper and a lower limit given by the DNL specifications of the A/D converter after which a pass/fail decision is made for the tested code. This way all code widths are successively tested on DNL, during one ramp input.

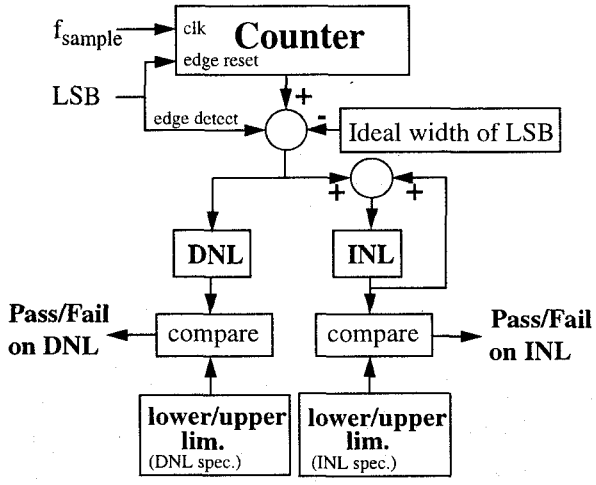

Figure 4: LSB processing block

The INL of each transition is determined from the DNL test by successively adding the determined DNL values of each code, from the first code, up to the code for which the INL is determined. The INL values are compared with the upper and lower limits given by the INL specifications of the A/D converter.

The number of samples taken per code can be changed by changing the slope of the input ramp as the sample frequency of an A/D converter is constant. The number of samples that can be taken per code is determined by the size of the counter used in the "LSB processing" block in Figure 4. The larger the counter the more samples can be taken per code and the more accurate the test will be.

3 Error analysis

The counting process for the LSB, used to determine the code widths, introduces measurement errors, just like the conventional test approach. The exact transition moments and thus the transition voltages relative to the sample moments are not known because of the sampling or counting process (Figure 5). It is only possible to determine between which samples the transition has taken place.

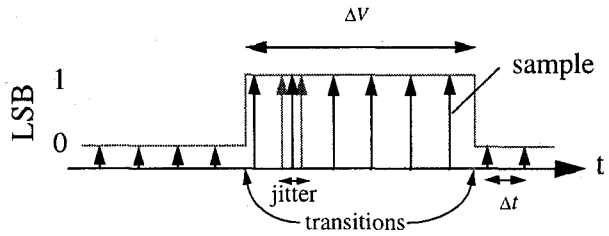

Figure 5: Transitions for one code relative to samples.

Because of this uncertainty four different conditional probabilities can be distinguished in a test [9]:

- *P(device = accepted | device = good)*

  The probability that a good device is accepted.

- *P(device = rejected | device = good)*

  The probability that a good device is rejected by the test. This is the **type I error** probability.

- *P(device = accepted | device = faulty)*

  The probability that a faulty device is accepted by the test, the **type II error** probability.

- *P(device = rejected | device = faulty)*

  The probability that a faulty device is rejected.

For a cost-effective and reliable test, the probabilities of type I and type II errors must be very small compared to the probabilities *P(accepted | good)* and *P(rejected | faulty)*. The probability of a type II error is especially crucial because of the stringent quality demands as posed by customers (10-100 P.P.M. (parts per million) may have a type II error [5]). An analysis of the sample and counting process is necessary in order to find the probabilities of type I and type II errors as a function of the number of counts per code width. Eventually, the lowest number of counts needed per code width for an accurate BIST should be found in order to keep the test circuitry small.

The upper and lower limits, i_{max} and i_{min}, of the number of samples per code width can be determined from the upper and lower limits of the code widths, ΔV_{max} and ΔV_{min}, by:

$$i_{min}(\Delta s) = ceil\left(\frac{\Delta V_{min}}{\Delta s}\right) \quad \text{(EQ 3)}$$

$$i_{max}(\Delta s) = floor\left(\frac{\Delta V_{max}}{\Delta s}\right) \quad \text{(EQ 4)}$$

where 'floor' means that the term in brackets is rounded off to the lower integer and Δs is the voltage step made between two samples of the ramp input:

$$\Delta s = \alpha \cdot \Delta t = \frac{\alpha}{f_{sample}} \quad \text{(EQ 5)}$$

with α the slope of the input ramp. In the following, a code width will be rejected by the counting process if $i < i_{min}$ or $i > i_{max}$ and is accepted if $i_{min} \le i \le i_{max}$.

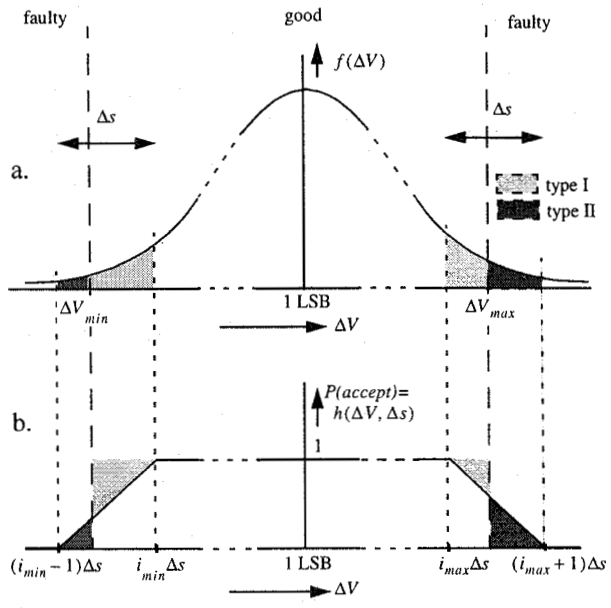

Figure 6: Distribution and P(accept) of a code width

Figure 6a shows the distribution of a single code width which is determined by the circuitry within the A/D converter and Figure 6b gives the probability that a code width is accepted by the counting process. The probability that a code width is accepted by the test increases and decreases linearly in the regions $((i_{min}-1)\Delta s ; i_{min}\Delta s)$ and $(i_{max}\Delta s ; (i_{max}+1)\Delta s)$ because of the uniform distribution of the sample moments with respect to the transition moments (Figure 5). The hatched areas in Figure 6 indicate the type I and type II errors. The probability that a type I or type II error occurs in a measurement of one code as a function of Δs is determined by:

$$P_{typeI}(\Delta s) = \int_{\Delta V_{min}}^{i_{min}(\Delta s)\Delta s} (1 - h(\Delta V, \Delta s)) f(\Delta V) d\Delta V + \int_{i_{max}(\Delta s)\Delta S}^{\Delta V_{max}} (1 - h(\Delta V, \Delta s)) f(\Delta V) d\Delta V \quad \text{(EQ 6)}$$

$$P_{typeII}(\Delta s) = \int_{(i_{min}(\Delta s)-1)\Delta S}^{\Delta V_{min}} h(\Delta V, \Delta s) f(\Delta V) d\Delta V + \int_{\Delta V_{max}}^{(i_{max}(\Delta s)+1)\Delta S} h(\Delta V, \Delta s) f(\Delta V) d\Delta V \quad \text{(EQ 7)}$$

where $f(\Delta V)$ is the distribution or probability density function of a code width and $h(\Delta V, \Delta s)$ the probability function of a code width being accepted by the sample process.

The probability that the whole A/D converter satisfies the DNL specifications is given by:

$$P(good)_{whole} = P(good_{code1}, good_{code2}, \ldots, good_{codeN}) \quad \text{(EQ 8)}$$

with N the number of codes available ($=2^n$). If the standard deviations of the code widths are the same and if there is only a small correlation between the different code widths then (EQ 8) can be simplified to [12]:

$$P(good)_{whole} = P(good)_{one}{}^{N} \quad \text{(EQ 9)}$$

In the case of a flash A/D converter, which was used for the verification of the theory derived, the variances of all code widths are equal and the correlation between the code widths is given by [12]:

$$r = -\frac{1}{N-1} \quad \text{(EQ 10)}$$

Thus the more bits the flash A/D converter has, the smaller the correlation between different code widths will be and the more (EQ 9) becomes a valid approximation. In the case of a 6-bit A/D converter, the correlation between the code widths is small and the error made by using (EQ 9) can be neglected.

The overall type I and II error probability in the DNL measurement can be approximated by the binomial distributions given in (EQ 11) and (EQ 12) if the standard deviation of the different code widths are the same and if the correlation between the code widths is small [12]:

$$P_{type\,I\,overall} = \sum_{k=1}^{N} \binom{N}{k} (P_{typeI})^k P(accept|good)^{N-k} \quad \text{(EQ 11)}$$

$$P_{typeIIoverall} = \sum_{k=1}^{N} \binom{N}{k} (P_{typeII})^k P(accept|good)^{N-k} \quad \text{(EQ 12)}$$

with $P_{type\,I}$ and $P_{type\,II}$ determined from (EQ 6) and (EQ 7) and $P(accept|good)$ determined by:

$$P(accept|good) = \int_{\Delta V_{min}}^{\Delta V_{max}} h(\Delta V, \Delta s) f(\Delta V) d\Delta V \quad \text{(EQ 13)}$$

In the given analysis, errors introduced by non-linearity and noise of the input ramp, by jitter noise and by the transition noise, were not taken into account. Jitter noise introduces a variation in the time when samples of the input

signal are taken (Figure 5). Transition noise can cause toggling of the LSB which means that there is no exact transition. Toggles in the LSB can be removed by means of a simple digital filter [12].

4 Simulation and experimental results

The theory derived in the previous section has been verified by means of simulations and experiments on 6-bit flash A/D converters. A batch of 364 converters was used for the measurements. Converters with gross defects, probably caused by spot defects, were taken out, as only the influence of parametric variation was taken into account in the theory. Gross faults introduced by spot defects have such a large impact on the code widths of the converter that these faults will also be detected by the BIST method.

A flash A/D converter consists of a resistor string which determines the transition voltages and comparators which "compare" the input with these transition voltages. The standard deviation of a code width is determined by the standard deviation of the resistors and the standard deviation of the offset voltages of the comparators. From circuit simulations it was found that the standard deviation of the code widths should be in between 0.16-0.21 LSB. For the next simulations to determine the type I and type II error probabilities a standard deviation of 0.21 LSB has been taken (worst case). The correlation between the code widths was found to be small (r=-0.02) according to the circuit simulations and theory (EQ 10).

First simulations and measurements were performed under increased performance specifications. This was done in order to perform a statistically justified measurement. A very accurate measurement, taking approximately 1000 samples per code width has been performed as a reference. The simulations and measurements showed that only 30 % of the flash A/D converters are good under the increased DNL specifications of $\pm$ 0.5 LSB (is normally $\pm$ 1 LSB for the used converter).

Figure 7 gives the simulated probabilities of type I and type II errors, as a function of the stepsize Δs, for a DNL specification of $\pm$ 0.5 LSB. The region of the stepsize is chosen such that a 4-bit counter can be used to determine the code widths. The same simulations have been performed with the stepsize in the region of a 5, 6 and 7 bits counter.

For the measurements an intermediate value for Δs was used in the region where i_{max} has a maximal counter value (in the case of a 4-bit counter, i_{max}=16 and Δs=0.091 LSB). The measurement and simulation results, of the type I and II error probabilities as a function of the counter size used to determine the code widths, are listed in Table I.

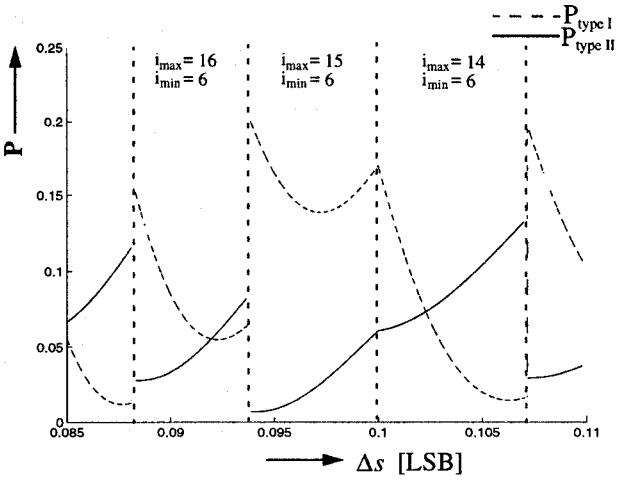

Figure 7: $P_{type\ I}$ and $P_{type\ II}$ as a function of Δs

Comparing the type I and II error probabilities shows that the type I and type II error probabilities have a similar trend for the simulations and for the measurements. The type I error probabilities of the measurements are twice as high as the type I error probabilities of the simulations. This difference between the measurements and simulations

Table 1: Simulation and Measurement with stringent DNL specs. ($\pm$ 0.5 LSB)

Counter (# bits)	P(Type I,II) SIM. *I*	SIM. *II*	MEAS. *I*	MEAS. *II*	Max. error made *[LSB]*
4	0.065	0.045	0.13	0.03	0.09
5	0.025	0.045	0.06	0.03	0.05
6	0.015	0.015	0.04	0.02	0.02
7	0.015	0.005	0.02	0.01	0.01

can be explained by the fact that the type I and type II error probabilities are sensitive to small changes in the step size and therefore also to small changes in the slope of the input ramp according to (EQ 5). The simulation and measurement results agreed much better if Δs was actually smaller (~0.002 LSB smaller for 4, 5 and 6-bit counters) in the measurements. Therefore the slope of the applied ramp in the measurements was probably slightly too steep. The type I error probabilities are approximately halved if the size of the counter is increased by one bit according to both the measurements and simulations.

The probability that an A/D converter is faulty on the actual DNL specifications of $\pm$ 1 LSB is very small (1.4×10^{-4}). This may seem a very high yield but it should be noted that only faults introduced by parametric variations were taken into account and faults caused by spot

defects were not. Table 2 shows the (simulated) measurement error probabilities for actual specifications. The results show that the type II error probabilities are very small for all counters; within the required 10-100 P.P.M. This means that even with a relatively small counter of 4 bits, a reliable BIST is possible. The quality of the conventional test, where 4096 samples are taken for the test of all the codes, can be compared to the BIST with a 7-bit counter.

Table 2: Simulation results actual specs (± 1 LSB)

Counter (# bits)	*P(type I,II) *10^{-6}*		Max. error made *[LSB]*
	I	*II*	
4	40	70	1/8
5	20	40	1/16
6	10	25	1/32
7	5	15	1/64

5 Conclusion

By simple digital functions which perform on-chip signal processing, the number of test pins and the number of sampled test data points can be reduced in the case of "static" and "dynamic" tests of A/D converters. For chips containing more than one A/D converter the proposed methodology has a major advantage, since several A/D converters can easily be tested in parallel which reduces the test time and test costs significantly.

When only a "static" test is needed, the number of test pins can be reduced to one by doing an on-chip test on all the output bits of the A/D converter with the exception of the LSB which is tested separately on or off-chip. By doing a test on all the output bits except the LSB, the functionality of the A/D converter is tested. The linearity of the A/D converter is tested by monitoring the LSB which can be done on-chip, making BIST feasible.

The magnitude of the measurement error and thus of type I and type II errors introduced by the BIST strategy depends on the number of samples taken per code. The number of samples taken per code is controlled by the slope of the input ramp and determined by the size of the counter used to monitor the LSB. The measurement error is halved each time the size of the counter is increased. The probability of the type I errors is approximately halved if the size of the counter is increased by one bit. If a seven-bit counter is used to monitor the LSB then the quality of the test is the same as the quality of the conventional histogram test used in the production test. Even with a smaller counter, a reliable test is possible according to the simulations. This means that with limited hardware usage a BIST solution is possible.

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