

## BUSFET - A Novel Radiation-Hardened SOI Transistor

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### Abstract

A partially-depleted SOI transistor structure has been designed that does not require the use of specially-processed hardened buried oxides for total-dose hardness and maintains the intrinsic SEU and dose rate hardness advantages of SOI technology.

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## I. INTRODUCTION

Silicon-on-Insulator (SOI) technology offers hardness advantages over bulk-silicon or epitaxial-silicon technologies for space and military applications. Properly designed SOI circuits are less prone to single-event upset (SEU) from energetic cosmic particles in space, high-altitude aircraft, or terrestrial systems and can function without upset or failure after exposure to extremely high dose rate pulses of ionizing irradiation [1]. It is impossible to fabricate conventional bulk-silicon circuits that can function at dose rate levels achievable by properly designed SOI circuits. Because of the high levels of SEU and dose rate radiation hardness obtainable by SOI circuits, system applications not realizable with bulk-silicon circuits can be realized. On the other hand, the total dose hardening of SOI devices can be more difficult than bulk silicon because of back-channel leakage caused by charge trapping in the buried oxide.

Two factors can reduce the radiation hardness of SOI circuits. These are floating body effects that degrade SEU and dose rate hardness, and back-channel leakage that degrades total dose ionizing radiation hardness. To reduce floating body effects, body ties can be used to tie the body to a fixed potential (normally the source) [2]. Unfortunately, these body ties can significantly increase the size of transistors (and thus ICs) and connect to the body region only at the extreme ends of the transistor width. This can make them impractical for high-density circuits and can limit their effectiveness for dose rate upset and SEU hardening.

The total dose hardening of SOI ICs can be more difficult than hardening bulk-silicon ICs due to the SOI buried oxide. Total dose ionizing radiation-induced back-channel leakage occurs as positive charge is trapped in the buried oxide near the silicon/oxide interface. Typical SOI buried oxides contain numerous defects that result in considerable radiation-induced charge trapping [3]. As charge is trapped in the buried oxide, the silicon becomes inverted at the silicon/buried oxide back channel, forming a conducting path between the source and drain. Note that the source and drain go all the way through the silicon for a standard thin-film SOI transistor. Techniques have been developed to fabricate hardened SOI buried oxides that minimize radiation-induced positive charge buildup near the back-channel interface [4,5]. Unfortunately, the processing techniques used to harden buried oxides make hardened buried oxides more expensive. Moreover, at present, hardened buried oxides are not commercially available. One can also minimize back-channel leakage by increasing the silicon channel thickness such that the source and drain do not penetrate completely through the silicon. For this case, inversion of the back channel will not lead to a conductive path between source and drain and the total-dose hardness is considerably improved [6]. Unfortunately, this approach leads to large increases in junction area and an increase in charge collection volume reducing the dose rate and SEU hardness.

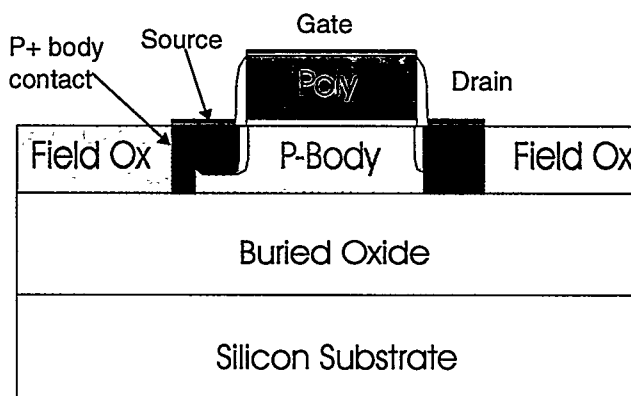


Figure 1: BUSFET cross section.

In this paper, we describe a novel body-tied partially-depleted SOI transistor structure that should be hard to total dose ionizing irradiation, while maintaining the high dose rate and SEU hardness levels intrinsic to thin-film SOI technology. We call this transistor the Body Under Source FET (BUSFET). For the BUSFET, total-dose hardness is obtained through the transistor structure and it is conceptually not necessary to use specially processed hardened buried oxides to minimize radiation-induced back-channel leakage. The BUSFET body-tie structure also requires less area than standard body ties making BUSFET body ties more practical for high-density circuits. In this summary, we describe the fabrication and operation of the BUSFET, and use 3-D modeling to support the validity of the BUSFET structure for minimizing back-channel effects. Total dose data on fabricated BUSFETs will be presented in the full paper.

## II. BUSFET DESCRIPTION

The BUSFET transistor structure is very similar to that of a standard MOS SOI transistor structure. A total of only two additional mask levels are required to fabricate a typical partially-depleted SOI IC using the BUSFET design. In this section, we describe the basic structure of the BUSFET and a process flow for obtaining the BUSFET structure.

The cross section for the BUSFET is shown in Fig. 1. The BUSFET is similar to a standard partially-depleted SOI MOSFET with two main exceptions. 1) The source does not extend completely through the top silicon layer. 2) Next to the source is a heavily doped p-type region that serves as the body contact. The effects of radiation-induced back-channel leakage in the BUSFET are significantly reduced or eliminated because the source region does not go completely through the silicon layer. Thus, there is no direct conducting path between the source and drain even if the back-channel interface is inverted by charge trapping in the buried oxide due to total dose ionizing irradiation.

The process flow for fabricating a BUSFET transistor is very similar to that for a typical partially-depleted SOI transistor. To fabricate a BUSFET CMOS IC, only two additional mask levels (one for n-channel transistor drains and

p+ body contacts, and one for p-channel transistor drains and n+ body contacts) are required. Note that p-channel BUSFETs are not likely required for total-dose hardening, but the body tie associated with the BUSFET p-channel transistor may be required for SEU and dose rate hardening, and reducing floating body circuit effects. A possible process flow for fabricating an n-channel BUSFET is outlined in Figure 2 (this portion of the process flow only includes the unique steps required to make a BUSFET; additional steps not specific to the BUSFET are required for fabricating the complete IC). Step 1: The polysilicon gate is defined using standard photolithographic and etching techniques. Step 2: n-type lightly doped drains (LDDs) are implanted into the source and drain regions. The depth of the LDD implants extends only partially through the silicon layer. Step 3: LDD spacers are deposited and defined using standard processing techniques. Using the same mask as for the LDD implants, a second n-type implant is performed to heavily dope the source and drain contact regions. Like the LDD implant, this implant goes only partially through the silicon layer. Step 4: A deep n-type implant is performed to form the drain region. This mask level is one of the two additional mask levels required for fabricating BUSFETs. Note that this mask level is also used to form the n+ body contact for p-channel transistors (not shown). Step 5: A deep p-type implant is performed to make the p+ body tie contact. This is the second additional mask level required to fabricate BUSFETs. It also is used to form the deep p+ drain regions for p-channel transistors. Step 6: A silicide strap is formed over the p+ body tie and source contact, physically shorting the two together, as well as, the polysilicon gate and drain. Note that the area consumed by the body tie leads to only a negligible (if any) increase in area. The width of the source/body contact region is determined primarily by the area required by the silicide strap and design rule constraints. This area is approximately the same for either the source contact alone or for the source and body contact together. One process variation that may be required to minimize the depth of the back-channel inversion layer, and thus, minimize the conductive path between source and drain, is to use a retrograde doping profile for the body region. This involves only adjusting the body region implant and does not require any additional mask levels. The process flow for fabricating a p-channel BUSFET (if required) is analogous to that for an n-channel transistor.

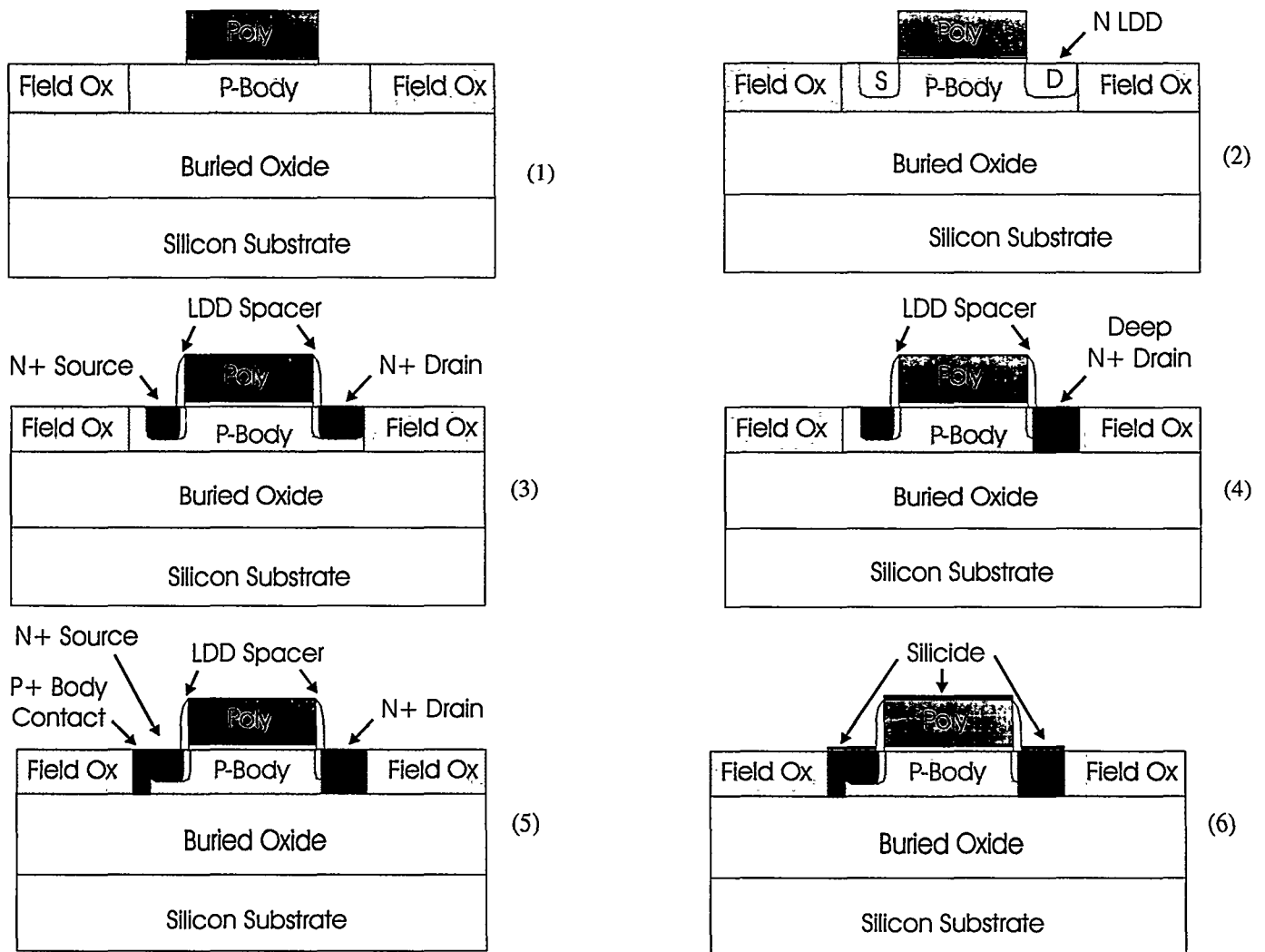
### III. 3-D TOTAL-DOSE SIMULATION

We have performed device simulations using the 3-D code Davinci to compare the total-dose response of a partially-depleted SOI BUSFET to a standard partially-depleted SOI MOSFET fabricated in a 0.35- $\mu\text{m}$  gate length 3.3-V technology. The total-dose response is simulated by adding a sheet of radiation-induced charge at the back-channel interface and examining the subthreshold current-voltage characteristics. In reality, charge generated in the buried oxide by total dose ionizing radiation is non-uniformly trapped throughout the oxide, and the trapping efficiency and charge yield depend on the local electric field. In these simplified

simulations, we assume 100% trapping efficiency and charge yield, and that all of the charge is trapped at the back-channel interface (the worst-case scenario for charge location). Note that the charge density introduced in the simulations can be directly related to a worst-case total accumulated dose irradiation level. For example, 1 krad( $\text{SiO}_2$ ) of irradiation generates  $8.1 \times 10^{15}$  electron-hole pairs/ $\text{cm}^3$ . If all of the carriers generated in the buried oxide escape recombination and become trapped at the interface, they correspond to a certain back-channel interface charge density ( $Q_{bc}$  in Figs. 3 and 4). We also assume a retrograde body doping profile with a back-channel concentration of  $10^{18} \text{cm}^{-3}$ , a top silicon thickness of 180 nm, a source depth of 90 nm, and a buried oxide thickness of 370 nm. In the standard SOI n-channel transistor (Fig. 3), we see significant back-channel leakage at very low radiation-induced charge densities. As discussed previously and as illustrated in the bottom panel of Fig. 3, this is because the back-channel charge inverts the silicon near the interface and creates a direct conducting path between the source and drain regions. This path leads to a considerable leakage current as bias is applied to the drain (3.3 V in these simulations). By about 10 krad( $\text{SiO}_2$ ) of total dose, the standard SOI transistor shows considerable back-channel leakage ( $>10^{-7}$  A). In reality, leakage will not occur until a somewhat higher irradiation level because not 100% of the generated charge will be trapped, and the charge trapped will not necessarily all be located at the interface. In contrast, Fig. 4 shows the total-dose response of the SOI BUSFET. Even at very high levels of radiation ( $>30$  Mrad( $\text{SiO}_2$ )), there is no significant back-channel leakage. Again, keep in mind that because of our worst-case assumptions a back-channel interface charge density of  $10^{16} \text{cm}^{-2}$  would not actually be reached until a considerably higher irradiation level (if ever). In any case, the BUSFET structure has significantly improved the back-channel total-dose hardness. For the conditions presented here, the back-channel hardness has been increased by more than three orders of magnitude. Of course, the overall hardness will also depend on the hardness of the gate oxide and the field isolation. As illustrated in the lower panel of Fig. 4, although a back-channel inversion layer exists, there is no conducting path between the source and drain because the source is not deep enough to complete the leakage path. Optimizing the BUSFET design involves tradeoffs between variables such as the body doping level, the depth of the shallow source, and the thickness of the top silicon film. Note that as technologies evolve to lower operating voltages, higher body doping levels are used. This trend further improves both the total dose ionizing radiation response and the effectiveness of the body tie under the source. Simulated SEU performance will be presented in the full paper.

### IV. DISCUSSION

To harden SOI circuits to total dose ionizing irradiation, existing technologies use either specially processed buried oxides or very thick silicon layers. The typical steps required to fabricate a hardened buried oxide can be very expensive and unproven in a manufacturing environment. The special

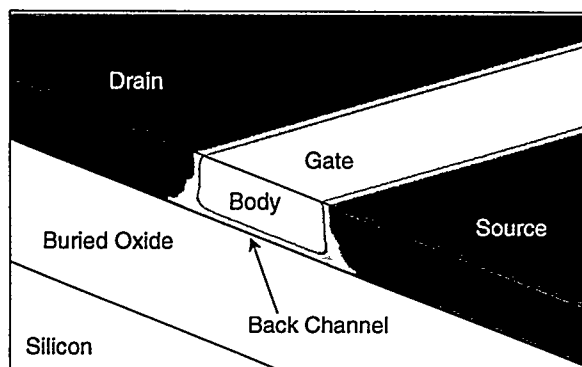
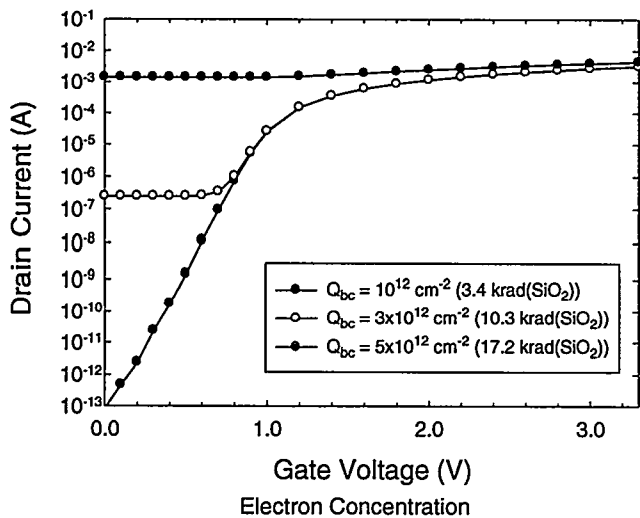


**Figure 2:** Process flow for fabricating an SOI BUSFET: step 1: poly gate definition, step 2: LDD implant, step 3: LDD definition, and shallow source and drain implants, step 4: deep n+ drain, step 5: p+ body contact implant, and step 6: silicide contact and strap definition.

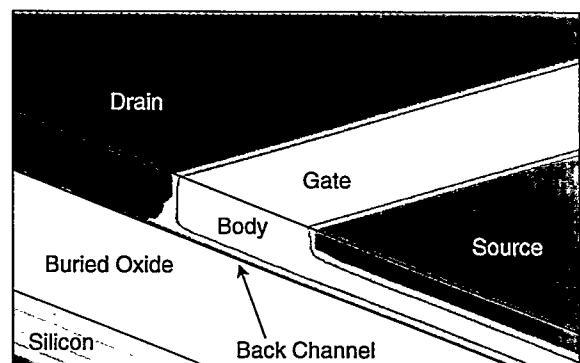
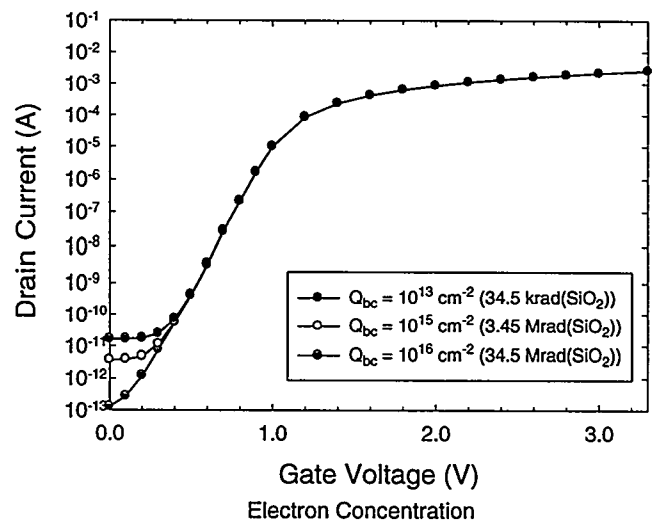
processing costs can increase the cost of hardened SOI substrates by more than a factor of two over standard SOI substrates. The equipment required to harden an SOI buried oxide is not obtainable from standard commercial equipment suppliers. Although techniques to harden buried oxides have been demonstrated [4,5], hardened buried oxides are not commercially available. This makes hardened SOI wafer availability tenuous at best, especially as the commercial need for non-hardened SOI wafers increases [7]. Eliminating back-channel leakage simply by increasing the thickness of the silicon layer has serious drawbacks that negate most of the advantages of thin-film SOI technology. If the silicon layer is very thick, the source and drain regions will not penetrate completely through the silicon layer so there is no conducting path for back-channel leakage. However, because the source and drains do not go completely through the silicon layer, the amount of p-n junction area and the charge collection depth will be greatly increased. As a result, the dose rate upset and SEU hardness will be reduced. This will also greatly increase parasitic capacitance causing circuits to operate slower or consume more power; therefore, they will be less attractive to

commercial or rad-hard users. Because the back-channel leakage path has been eliminated in the BUSFET, specially processed hardened substrates are not required for total dose hardening. Additionally, because the BUSFET is fabricated using a thin-film silicon layer and the drain contact goes completely through the silicon layer, p-n junction area and charge collection depth are still minimized compared to bulk CMOS ICs. Note that the source and p+ body-tie contacts are physically shorted together. As a result the source/body junction will not significantly add to the amount of active p-n junction area that can contribute to high dose rate photocurrents. Hence, the BUSFET will be hard to total dose ionizing irradiation (back-channel leakage), while maintaining the SEU and dose rate hardness advantages inherent to SOI technology.

The BUSFET body tie scheme is also superior to conventional body ties [2]. Only a small p+ body-tie contact region is required and thus the body-tie area is minimized. This makes the BUSFET body tie attractive to both commercial and radiation-hardened circuit designers. Also,



**Figure 3:** The simulated response of a standard partially-depleted SOI MOSFET to radiation-induced charge buildup at the back-channel interface. Top) Subthreshold I-V characteristics as a function of back-channel interface charge density. Bottom) Plot of electron concentration for a back-channel charge density of  $5 \times 10^{12} / \text{cm}^2$  illustrating the conducting path between the drain and the source.



**Figure 4:** The simulated response of a partially-depleted SOI BUSFET to radiation-induced charge buildup at the back-channel interface. Top) Subthreshold I-V characteristics as a function of back-channel interface charge density. Bottom) Plot of electron concentration for a back-channel charge density of  $10^{16} / \text{cm}^2$ . Note that although the back-channel interface is inverted, there is no conducting path between the drain and the source.

because the body-tie contact connects to the body under the source, all sites along the width of the channel are connected to the source potential. This should significantly reduce voltage drops along the width of the body and greatly increase the effectiveness of the body tie, especially for wide devices [8].

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