C_{OSS} Losses in 600 V GaN Power Semiconductors in Soft-Switched, High- and Very-High-Frequency Power Converters

Grayson Zulauf, *Student Member, IEEE*, Sanghyeon Park, *Student Member, IEEE*, Wei Liang, *Student Member, IEEE*, Kawin North Surakitbovorn, *Student Member, IEEE*, and Juan Rivas-Davila, *Senior Member, IEEE*

***Abstract*—We report losses from charging and discharging the parasitic output capacitor, C_{OSS}, in Gallium Nitride (GaN) power devices with voltage ratings over 600 V_{DS}. These losses are of particular importance in soft-switched circuits used at MHz switching frequencies, where the output capacitance of the device is charged and discharged once per switching cycle during the device's off-time. This process is assumed lossless. We measure C_{OSS} losses from 5–35 MHz sine, square, and Class-Φ_2 waveshapes in enhancement-mode and cascode devices, and find that losses are present in all tested devices, equal or greater than conduction losses at MHz frequencies, and exponentially increasing with dV/dt. The cascode device outperforms the e-mode devices under 300 V, but the e-mode devices are preferred above this operating voltage. Furthermore, we show that, within a device family, losses scale linearly with output energy storage. Packaging appears to have only a minor effect on these losses. Finally, we demonstrate 10 MHz, 200 W dc–dc converters with varying device configurations, showing that, even with constant circulating currents, moving to larger devices with lower $R_{DS,ON}$ actually degrades efficiency in certain applications due to C_{OSS} losses. In the high-voltage, high-frequency range, these reported losses must be optimized simultaneously with conduction losses on a per-application basis.**

***Index Terms*—DC–AC power conversion, dc–dc power conversion, gallium compounds, power semiconductor devices, power transistors, resonant power conversion.**

I. Introduction

SOFT-SWITCHED converters, where power devices are switched under zero-voltage and/or zero-current conditions, have significantly expanded the feasible operating frequency range for power converters. These converters reduce the frequency dependence of switching losses, leaving only gating losses and the ability to absorb parasitics as the roadblocks to ever-higher frequency operation. Because passive component values reduce as $1/f_{SW}$, high-frequency (HF, 3–30 MHz) and very-high-frequency (VHF, 30–300 MHz) converters are miniaturized and faster relative to their counterparts that are switched in the conventional 100s-of-kHz regime [1]. Power device selection in these soft-switched converters is a simple exercise—assuming the device capacitance is absorbed by the waveshaping network (as in the Class-E [2] or Class-Φ_2 [3]), the designer *theoretically* needs to select the lowest $R_{DS,ON}$ among the devices with 1) an output capacitance (C_{OSS}) that can be absorbed and 2) an input capacitance (C_{ISS}) that can be driven at the switching frequency. Implicit in this process is the assumption that losses in the power device are only generated by $I^2R_{DS,ON}$ losses during the on-time of the device; during its off-time, when the device can be modeled as a nonlinear capacitor with the value and energy storage of C_{OSS}, the power device is mostly assumed to generate no losses. Crucially, these soft-switching assumptions remove the frequency dependence of device losses.

Across the key figures-of-merit for high-frequency switching applications, newly commercialized Gallium Nitride (GaN) power devices outperform their silicon counterparts [4], making them attractive for these HF and VHF soft-switching converters. The introduction of these new GaN devices into fielded HF and VHF power converters has run into a pernicious nonideality in dynamic $R_{DS,ON}$, however, where electron trapping causes 2–5$\times$ higher on-resistance for the first few μs of conduction time [5]–[7]. This degrades the expected performance of the transistor by increasing its effective resistance. GaN manufacturers have devoted significant resources to successfully mitigating this issue (for example, see [8]), and recent studies report an increase of only 10% in on-resistance for sub-μs conduction times [7].

Despite this success, designers using high-voltage GaN transistors in the HF/VHF range continue to report unexplained losses that exceed their expected values by nearly an order-of-magnitude [9], [10]. Dynamic $R_{DS,ON}$ is an unlikely culprit behind these losses, as [10] only conducts mA-levels of current through the power device. In this paper, we show that these losses can be explained by quantifiable losses in the output capacitance of these GaN high-electron-mobility transistors (HEMTs). Even in soft-switched converters, the energy stored in the output capacitance of power devices is not completely recovered.

Manuscript received October 16, 2017; revised December 23, 2017; accepted January 25, 2018. Date of publication January 31, 2018; date of current version September 28, 2018. This work was supported in part by the National Science Foundation, in part by the TomKat Center for Sustainable Energy, in part by the Stanford Graduate Fellowship program, Cadence Design Systems, and in part by Airbus. Recommended for publication by Associate Editor S. K. Mishra. *(Corresponding author: Grayson Zulauf.)*

The authors are with Stanford University, Stanford, CA 94305 USA (e-mail: gzulauf@stanford.edu; spark15@stanford.edu; liangw@alumni.stanford.edu; north@stanford.edu; jmrivas@stanford.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2018.2800533

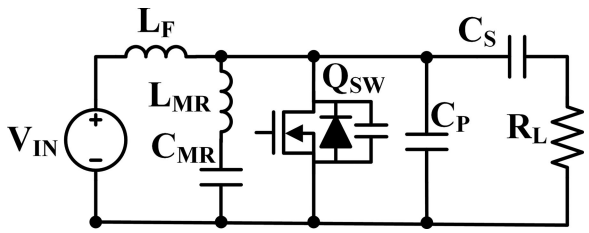


Fig. 1. Class-Φ_2 topology, with $L_S = 0$ to maximize output power. Q_{SW} is driven with a gate signal of the desired frequency and duty cycle.

These C_{OSS} losses have not been reported in the literature or by GaN device manufacturers. C_{OSS} losses due to hysteresis were documented in superjunction Si devices [11], [12], but nonlinearity in GaN C_{OSS} is only cited with respect to dead-time and the time needed to achieve zero-voltage-switching (ZVS) [13]–[16]. Designers using GaN either do not swing across the full device voltage or are not operating at HF/VHF [15]–[18], so these losses might not be large enough to prompt investigation. For example, [16] mentions that wide-bandgap devices dissipate roughly 10% of the stored energy in C_{OSS}, but subsequently proceed to ignore this in the tested Silicon Carbide (SiC) device and do not provide results for specific devices. [19] found soft-switching losses in cascode GaN devices due to avalanche breakdown, but not during normal operation. Even surveys of GaN challenges at HF ignore C_{OSS} losses [20], [21].

In this paper, we measure these C_{OSS} losses in high-voltage GaN power devices. This loss mechanism, not dynamic $R_{DS,ON}$, appears to limit operation at HF and VHF at the device voltages explored here. In Section II, we design, fabricate, and characterize three high-power, HF and VHF soft-switched converters using GaN HEMTs, finding unexpectedly high losses in the GaN devices. In Section III, we use a Sawyer–Tower circuit [22] to analyze losses in the output capacitance of three commercially available devices and fit the losses using a Steinmetz equation. In Section IV, we inject signals with higher voltage slew rates, showing exponentially increasing losses with increasing $\mathbf{dv/dt}$. In Section V, we demonstrate this loss mechanism in all-GaN dc–dc converters operating at 10 MHz and 200 W output power, showing that C_{OSS} losses account for the degradation in efficiency between simulation and measurement. Furthermore, lower $R_{DS,ON}$ devices actually result in *worse* measured efficiency in particular applications. In Section VI, we conclude this paper and provide direction for future work.

II. Unexpected Losses in Class-Φ_2 Converters

We construct three Class-Φ_2 converters, with the topology shown in Fig. 1, operating at switching frequencies of 10, 30, and 54.24 MHz, to demonstrate high-power operation with GaN power devices and inductors implemented as printed circuit board (PCB) traces. These converters each deliver an expected maximum output power of over 1000 W to a 50 Ω RF load with an input voltage range of 150 to 250 V.

A. Simulated Converters

Three converters were designed and simulated using the Class-Φ_2 methodology outlined in [3]. Only three companies manufacture commercially available 600 V_{DS} or greater devices—Transphorm, GaN Systems, and Panasonic—limiting the selection space for this application [20]. We preferred an enhancement-mode device due to prior work on losses in cascode devices in ZVS applications [19], and selected GaN Systems GS66504B HEMT [23] as the best combination of $R_{DS,ON}$, C_{OSS}, and C_{ISS} for the planned family of converters.

TABLE I
Simulation Results (250 V_{IN}, $R_L = 50\ \Omega$) for the Class-Φ_2 Converters, Using Manufacturer HEMT Models and Achievable Quality Factors

Parameter	10 MHz	30 MHz	54.24 MHz
P_{IN}	1185 W	1046 W	1003 W
η	94.5%	93.5%	93.5%
$I_{RMS,HEMT}$	10.9 A	9.6 A	10.9 A
$P_{DISS,HEMT}$	5.4 W	10.5 W	17.1 W
$V_{DS,MAX}$	603 V	606 V	540 V

Simulations were performed in LTSpice using manufacturer-provided models that include parasitic inductance and resistance and device self-heating. Design values are shown in Table II. Capacitor quality factors were taken directly from the datasheet and inductor parasitics were derived using the model outlined in [24]. Inductor footprints were selected to achieve quality factors of approximately 100 for L_{MR} and L_F.

Table I shows the key simulation results. Most importantly, the HEMT power dissipation should be easily extracted at full converter power operation. We also note that the manufacturer-provided model uses an $R_{DS,ON}$ *lower* than the nominal datasheet value when the simulated HEMT is fully enhanced, resulting in a total power dissipation less than that predicted by $I_{RMS}{}^2 \cdot R_{DS,ON}$. This appears designed to approximate losses associated with lingering dynamic $R_{DS,ON}$, as the manufacturer models demonstrate increased power dissipation with increasing frequency despite nearly constant current.

B. Operating Measurements

The converters were fabricated with board thicknesses of 1, 2, and 6 mm, selected to achieve a quality factor of approximately 100 for both L_F and L_{MR} in each converter at the operating frequency. Simulated and measured waveforms match well (see Fig. 2). The constructed converters are shown in Fig. 3 and Table II shows the key components.

Upon initial testing, the temperature rise of the HEMT was so extreme that the converters could not operate for more than $\sim 150\ \mu$s out of every 3 ms, despite the low-simulated HEMT power dissipation and good matching between the simulated and measured waveforms. This HEMT power dissipation was nearly an order of magnitude higher than the simulated value, as approximated by thermometric measurements (recorded using the FLIR A655sc infrared camera). R_{TH} was calibrated by reverse biasing the device and recording the dc power and device temperature at four operating points, allowing an extrapolated continuous power to be estimated as

$$P_{HEMT} = \frac{T_C - T_{AMB}}{R_{TH}} \frac{100}{D_{PULSE}}. \quad (1)$$

TABLE II
PASSIVE COMPONENTS IN THE CLASS-Φ_2 CONVERTERS

Component	Design Value	Manufacturer, Part Number
L_{MR}	1100 nH	h = 6 mm, r_O = 15 mm, r_I = 10.7 mm, N_T = 50
	250 nH	h = 2 mm, r_O = 14 mm, r_I = 6.2 mm, N_T = 27
	76.5 nH	h = 1 mm, r_O = 10 mm, r_I = 5.1 mm, N_T = 22
L_F	450 nH	h = 6 mm, r_O = 10 mm, r_I = 4.7 mm, N_T = 22
	125 nH	h = 2 mm, r_O = 11 mm, r_I = 4 mm, N_T = 17
	50 nH	h = 1 mm, r_O = 8 mm, r_I = 4.3 mm, N_T = 16
C_{IN}	15 μF	5x Knowles Syfer 2220Y5000105KXTWS2 + 1x Panasonic EEU-ED2G100
C_{MR}	65 pF	2x AVX 1808HA300JAT2A + 1x GRM42A5C3F050DW01L
	30 pF	2x AVX 1206GA150JAT1A
	30 pF	2x AVX 1206GA150JAT1A
C_P	200 pF	2x AVX 1808AA101KAT1A
	30 pF	2x AVX 1206GA150JAT1A
	30 pF	AVX 1808HA300JAT2A
C_S	23.4 nF	6x TDK C3225C0G2J392K125AA
	3.9 nF	TDK C3225C0G2J392K125AA
	3.9 nF	TDK C3225C0G2J392K125AA
R_L	50 Ω	Pasternack PE7411-50 attenuator + MSO9404A 50 Ω input
Drain probe	—	Agilent N2875A

For cells with multiple lines, the first line corresponds to the 10 MHz converter, the second line to the 30 MHz, and the third line to the 54.24 MHz.

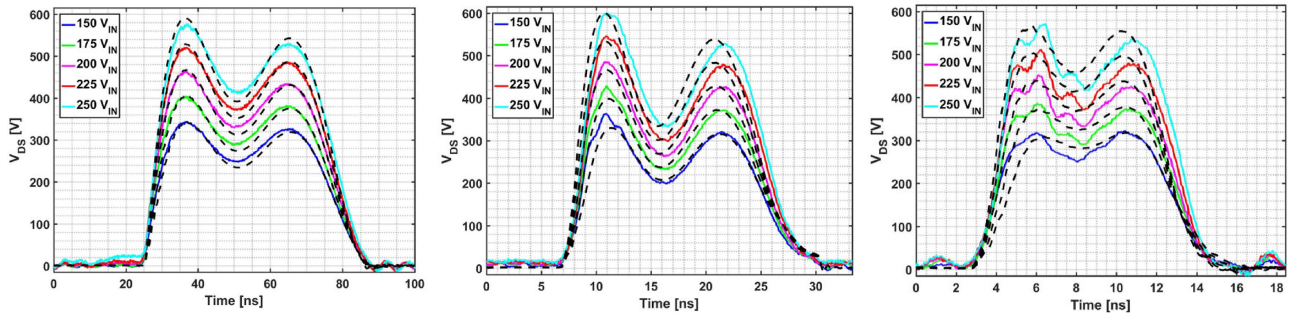


Fig. 2. Measured (solid lines) and simulated (dotted black lines) V_{DS} for the demonstrated Class-Φ_2 converters (left is 10 MHz, middle is 30 MHz, and right is 54.24 MHz). Input voltage increases with higher vertical line position on the graph. Measured maximum $\mathbf{dV/dt}$ across the HEMT is 70 $\mathbf{V/ns}$ (10 MHz), 152 $\mathbf{V/ns}$ (30 MHz), and 250 $\mathbf{V/ns}$ (54.24 MHz).

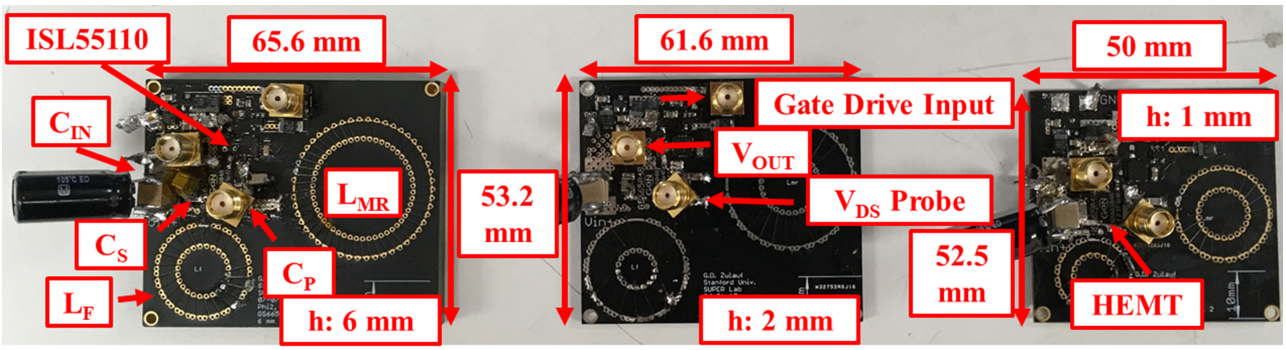


Fig. 3. Fabricated Class-Φ_2 converters (left is 10 MHz, middle is 30 MHz, and right is 54.24 MHz), with annotations showing key measurements and component locations. Component locations are identical on all three converters.

While this method has a number of shortcomings—including the magnification of errors due to the low pulse rate, ignoring the effects of device heating, and thermal coupling from the PCB inductors—the extra losses are so extreme to demand investigation without precise knowledge of their exact magnitude. Fig. 4 shows this wide difference between simulated and measured losses with varying input voltage and pulse width in all three converters.

We first suspected that missed zero-voltage-switching might be the primary loss driver. To exclude this as the source, we conservatively calculated device losses if soft-switching were missed by 50 V with constant capacitance at the $V_{DS} = 0$ value

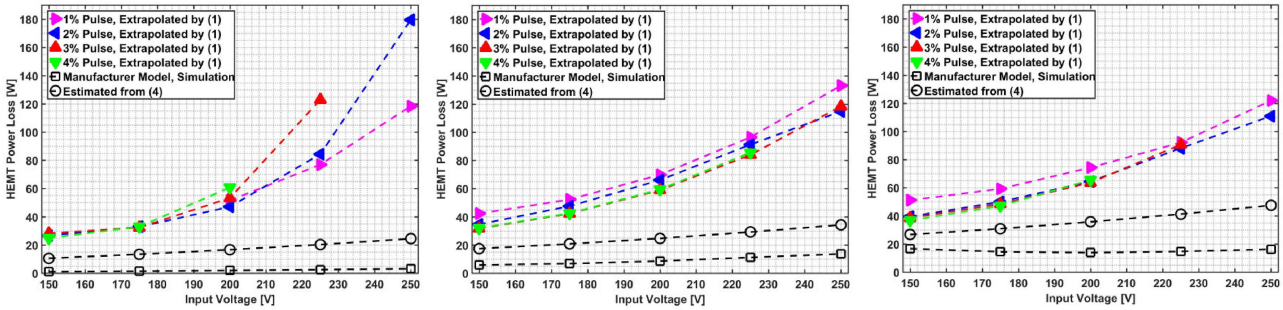


Fig. 4. Comparison between predicted and thermally measured HEMT losses for three Class-Φ_2 converters (left is 10 MHz, middle is 30 MHz, and right is 54.24 MHz). Thermal measurements are only included if device temperature exceeded 30 °C.

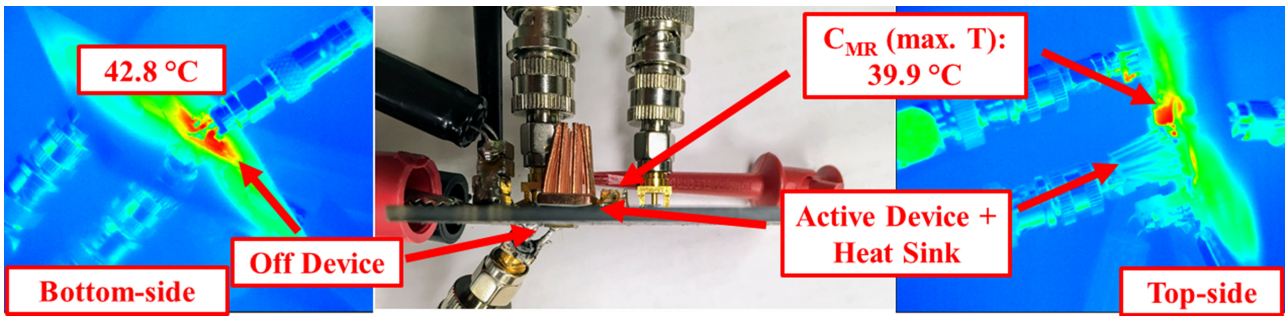


Fig. 5. 30 MHz Class-Φ_2 converter operating with 5% pulse rate, 250 V_{IN}, and after a 10-min. soak with air-cooling and a heatsink on the top-side device. The middle image shows the converter during the thermal soak testing, with the angle selected to show both sides of the board. A higher temperature on the off-state device (left) than the operating device (right) verifies that the off-state device is indeed a heat source.

of 242 pF [23]

$$E_{\mathrm{OSS,CYCLE}} = \frac{1}{2}(242\,\mathrm{pF})(50\,\mathrm{V})^2 = 0.30\,\mu J \qquad (2)$$

$$P_{\mathrm{SS,100\%PULSE}} = E_{\mathrm{OSS,CYCLE}} \mathrm{f_{SW}}. \qquad (3)$$

These soft-switching losses would add 3.0 W (10 MHz), 9.1 W (30 MHz), and 16.4 W (54.24 MHz) of dissipated power. Gating losses, calculated as $\mathrm{P_{GATE}} = \mathrm{C_{ISS}\,f_{SW}\,V_{GATE}}^2$, amount to a maximum of 0.57 W for the 54.24 MHz converter driven at 9 V. We combine these loss mechanisms to estimate a very conservative loss in the HEMT as

$$\mathrm{P_{HEMT}} = \mathrm{P_{GATE}} + \mathrm{P_{SS}} + R_{\mathrm{DS,ON}} {I_{\mathrm{RMS}}}^2, \qquad (4)$$

with $\mathrm{R_{DS,ON}}$ taken as the 150 °C value (258 mΩ). This loss is shown in Fig. 4 for each converter, and, as expected with conservative assumptions, it is indeed much larger than those predicted by simulation. Even this conservative loss estimate, however, does not approach the observed losses in the devices, and an alternate explanation is required.

C. "Off-State" Losses

Very high dynamic $\mathrm{R_{DS,ON}}$ during the on-time of the device could be the source of these losses. Prior work, however, has noted significant "off-state" losses in wide-bandgap devices, including GaN HEMTs [9] and GaN diodes [10] operating in the HF and VHF regimes and SiC MOSFETs and diodes [25]. [9] and [25] add a second device with its gate tied low in parallel with the operating device to assess the losses in a nonconducting device, and we repeated the procedure here with the Class-Φ_2 converters discussed above.

Unfortunately, at the frequencies of interest, the two devices must be physically proximal to reduce parasitic inductances, and adequate thermal isolation cannot be achieved. This thermal cross coupling makes it difficult to quantify the losses in the off-state device [9], and we can only verify that the off-state device is a heat source. To perform this, we connected a large air-cooled heatsink to the operating device while leaving the off-device passively cooled. At even a 5% pulse rate at 300 Hz pulse frequency, the off-state device shows significant heating, as shown in Fig. 5 for the 30 MHz converter. Higher temperature in the off-state device than in the switching device verifies that the off-state device is indeed a source of dissipated power.

This experiment verified that losses during the off-time of the device were a significant source of dissipated power, and we sought an alternate method to quantify these losses associated with the charging and discharging of the device output capacitance.

III. Sawyer–Tower Evaluation of C_{OSS} Losses

A. Measurement Methodology

To test this hypothesis, we seek to measure losses associated with charging and discharging the parasitic output capacitance in these GaN power devices. To make the measurement circuit

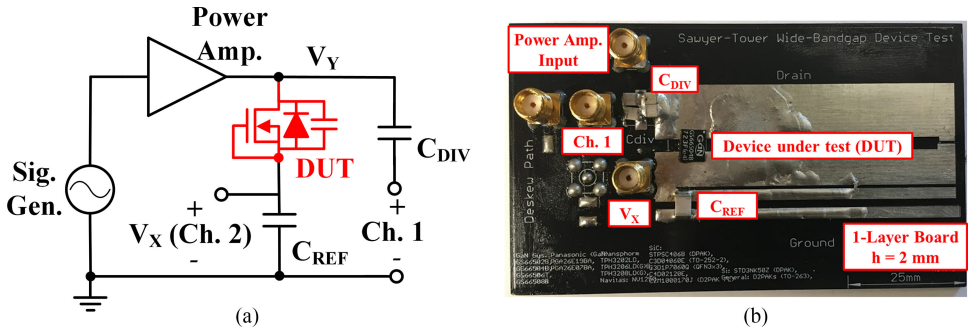


Fig. 6. Sawyer–Tower circuit used to test capacitance characteristics of the device under test (DUT) [11]. Components are given in Table III. (a) Schematic for Sawyer–Tower setup. (b) Manufactured board, with GS66504B shown as DUT.

extensible to a variety of devices and materials, the circuit must be capable of capturing losses that are either hysteretic or resistive in nature. Furthermore, as these losses (in GaN devices) have, to date, been unreported in the literature, we expect that they are only important at HF and VHF with large, fast voltage swings, and therefore, the selected measurement method must be capable of measuring sub-μJ differences in energy levels with 650 V voltage swings at frequencies above 30 MHz.

Fundamentally, we are measuring the characteristics associated with a capacitor—albeit a nonlinear capacitor—and there exist a variety of measurement methods, most of which were developed to measure the ferroelectric characteristics of candidate materials. The work in [26]–[28] provides a broad survey of these methods for power electronics candidates, and we briefly discuss each surveyed method with three others found elsewhere in the literature.

We cannot use a standard *LCR* impedance meter, as the circuit operation in the resonant converters constitutes a large-signal swing across the device output capacitance, which may have characteristics that are quite different than the small-signal injection method used by these meters [11], [12]. The two "*in situ*" methods, which characterize the capacitor-under-test in an operating converter either as a resistor-capacitor-diode (RCD) snubber or output capacitor [27], are not usable when the capacitor-under-test is inextricably paralleled with an antiparallel diode, as it will be in these power devices. Any conduction losses would not be easily separated from C_{OSS} losses, complicating the measurements. The quasi-dc charge-discharge circuit [29], where a slowly varying dc voltage is used to charge and then discharge the circuit, is valuable for large-signal characterization but not usable at the frequency range of interest in this study. Finally, a direct thermal measurement of the losses in a device paralleled with an operating converter [25] is not possible at VHF, where the devices cannot be adequately thermally isolated without introducing parasitic inductances that render the circuit untunable.

The Sawyer–Tower circuit, as shown in Fig. 6(a), was originally designed to measure hysteresis in ferrorelectric materials [22], and was previously used to measure hysteretic C_{OSS} losses in superjunction silicon MOSFETs [11], [12]. It is capable of capturing both resistive and hysteretic losses in linear and nonlinear capacitors. The accuracy of the loss measurements is only limited by the accuracy of the two voltage measurements

TABLE III
PART NUMBERS FOR THE TEST SETUP SHOWN IN FIG. 6

Component	Manufacturer	Part number
C_{DIV}, 1 pF	Vishay	4x VJ1111D1R0BXRAJ
C_{REF}, 1000 pF	AVX	1812AA102KAT1A
Probe, Ch. 1	Agilent	N2873A
Probe, Ch. 2	Agilent	N2875A
Power amplifier	ENI	A1000 RF PA

in Fig. 6(a), V_Y and V_X. The operating frequency and applied voltage are similarly limited only by the specifics of the test setup. In our case, the applied voltage is limited to 650 V_{DS} by the device rating and the bandwidth of the power amplifier limits the operating frequency to 35 MHz.

The charge on series capacitors must be equal, and the charge on the nonlinear device capacitor (Q_{OSS}) can be deduced from the voltage on the known capacitance, C_{REF}. C_{REF} also provides a dc offset to reverse-bias the device under test's (DUT) body diode. The voltage across the device is $V_Y - V_X$, and Q_{OSS} is equal to the charge on C_{REF} [11], [12]

$$Q_{OSS} = V_X C_{REF}. \tag{5}$$

The energy during a charge or discharge cycle is

$$E_{OSS} = \int_{Q_1}^{Q_2} V_{DS}(Q)\, dQ. \tag{6}$$

The energy dissipated in a cycle (E_{DISS}) is the sum of the energy to charge and the energy from discharging the capacitor.

We aim to detect sub-μJ differences across a 650 V swing at VHF, requiring further care in the measurement setup. The skew between V_X and V_Y is calibrated to compute the $V_{DS} \cdot dQ$ product. The 1 pF capacitor forms a capacitive divider with the probe to bring the V_Y measurement into the probe specification. Skew and the attenuation between C_{DIV} and the Ch. 1 probe are measured at 10, 20, and 30 MHz, and the nearest of these calibration points is used for each measurement.

In addition, we perform a thermometric estimation of the losses to compare to the electrically measured E_{DISS}. The power dissipated is estimated from the temperature rise of the device, as measured by an infrared camera (FLIR A655sc). The E_{DISS} per cycle is calculated from this thermometrically measured value by dividing the power by the frequency. In the remainder of this

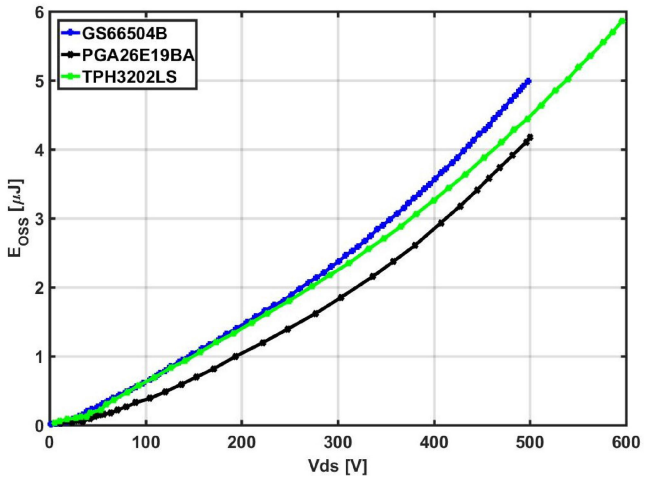


Fig. 7. Energy stored in the output capacitance of each device tested, from the graphs provided in the respective datasheets [23], [30], and [31].

paper, where appropriate, thermally and electrically measured losses are plotted together to provide a comparison between the measurements at each operating point.

B. Measured C_{OSS} *Losses*

Three companies have commercially released GaN devices with voltage ratings greater than or equal to 600 V_{DS}, and we select one device from each with similar E_{OSS} characteristics (see Fig. 7). The TPH3202LS [30] is cascode-type, while the PGA26E19BA [31] and GS66504B [23] devices are enhancement-mode (e-mode). Key device parameters are summarized in Table IV. The three devices have similar E_{OSS} curves, as shown in Fig. 7, and the GS66504B device has the highest E_{OSS} across the V_{DS} range.

The devices were tested using the circuit of Fig. 6(a) at frequencies from 5 to 35 MHz and device voltages from 50 to 600 V_{DS}. Frequency is limited to 35 MHz by the power amplifier. Voltage was not increased further if any of the following statements held:

1) the power amplifier exceeded its drive capabilities;
2) the device experienced thermal runaway;
3) V_X exceeded the relevant probe specifications.

Fig. 8 shows one particular test point, driving the PGA26E19BA device at 5 MHz with 610 V_{PP} across the DUT. Fig. 8(a) shows the measured voltage across the device, and when V_{DS} is plotted against Q_{OSS} [see Fig. 8(b)], E_{DISS} is the area between the charge and discharge curves. In contrast with the superjunction Si devices tested in [11] and [12], the enhancement-mode GaN devices do not exhibit the convex discharge curve that is characteristic of ferroelectric materials, and the Q_{OSS}–V_{DS} curves for these devices exhibit near linearity. The cascode device, which includes a low-voltage Si MOSFET to achieve normally-off operation, exhibits a characteristic knee around 25 V, corresponding to a sharp decline in small-signal C_{OSS} [30] and similar to the waveshape reported in the superjunction Si devices [11]. Fig. 9(a) highlights the effect of this low-voltage silicon MOSFET.

Measured losses with a sine wave input are shown in Fig. 10, with the *x*-axis, V_{DS}, as the peak drain-source voltage. Good agreement between the Sawyer–Tower and thermal measurements validate the loss source and lend confidence to the measurements. E_{DISS} increases with both increasing voltage and frequency for all three devices, with the exception of a small decrease at 100–150 V_{DS} for the TPH3202LS device. This decrease is likely measurement error at very low E_{DISS}.

We would like to extrapolate the measured losses to frequencies and voltages that have not been measured, and fit a voltage and frequency dependence for each device. The Steinmetz equation provides a general fitting for a power-law dependence on voltage ($\mathbf{V}$) and frequency ($\mathbf{f}$) [32]

$$E_{DISS} = k \cdot f^{\alpha} \cdot V^{\beta}. \tag{7}$$

Steinmetz fits are plotted in Fig. 10, with fitting parameters summarized in Table V. The E_{DISS} per cycle for the e-mode devices exhibits a nearly square root frequency dependence and a square voltage dependence. The cascode device (TPH3202LS) appears to have three separate regions of voltage dependence. There is little voltage dependence under 100 V_{DS}, and no Steinmetz fit is performed for this region. In the second region, between 100 and 300 V_{DS}, the voltage dependence is similar to the e-mode devices ($\beta = 1.46$). Above 300 V, the losses increase rapidly, as V^4. Neither the root cause of the three regions of voltage dependence or the different voltage dependence from the e-mode devices can be ascertained without access to the underlying device construction, which is proprietary. We hypothesize that the low-voltage Si MOSFET contributes only asymptotically at low voltage, accounting for the region below 100 V_{DS}, and the 100–300 V_{DS} region is the combination of the GaN device and these Si MOSFET losses. Above 300 V_{DS}, we speculate that the normally-on GaN device dominates. This normally-on device appears to have quite different loss characteristics from the normally-off e-mode devices.

Simulation models for the e-mode devices essentially exclude C_{OSS} losses, with simulated losses over 100× lower than measured losses at full voltage swing. The simulation model for the TPH3202LS part appears to *overpredict* the C_{OSS} losses [see Fig. 10(c)]. The manufacturer, however, provides a single model for the entire TPH3202L series without differentiating between packages. We tested the PQFN package, as this lower-inductance package will be preferred at HF/VHF, but the model, the development of which is detailed in [33], uses the package characteristics of a larger TO-220 package. This causes an overestimate of both low-voltage hysteresis and $\mathbf{dV/dt}$ ringing [see Fig. 9(b)]. A package-specific model would be necessary to design at HF/VHF.

Across manufacturers and device families, total E_{OSS} (see Fig. 7) or energy-related output capacitance (see Table IV) cannot be used to estimate relative losses, as the GS66504B has the highest E_{OSS} but outperforms the other two tested devices by 2–5× at full voltage swing. At low V_{DS}, the cascode device outperforms the e-mode devices tested here, but the V^4 dependence above 300 V_{DS} rapidly erodes this advantage at higher voltages. Furthermore, all three devices have increasing loss with increasing frequency. This dependence is not reported

TABLE IV
DATASHEET PARAMETERS (TYPICAL) FOR THE GaN DEVICES TESTED

Device	$R_{DS,ON}$, 25 °C (mΩ)	C_{OSS}, 400 V (pF)	E_{OSS}, 400 V (μJ)	$C_{O(ER)}$ (pF)
GS66504B	100	33	3.6	44 (400 V)
PGA26E19BA	140	30	3.0	33 (480 V)
TPH3202LS	290	29	3.2	36 (480 V)

Note that we tested a device from *every manufacturer* with commercially available GaN power devices with voltage ratings over 600 V_{DS}.

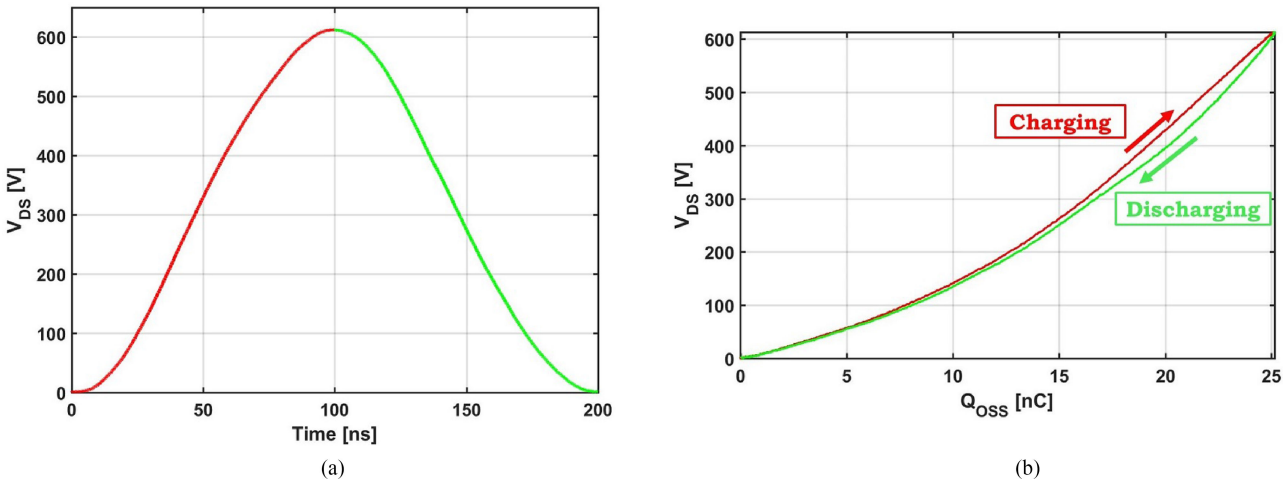


Fig. 8. Measured voltage across the device, from the PGA26E19BA device testing with 610 V_{DS} at 5 MHz. Charge and discharge periods in (a) correspond to the E_{OSS} charging and discharging periods in (b). (a) Measured device voltage versus time. (b) V_{DS} versus Q_{OSS}.

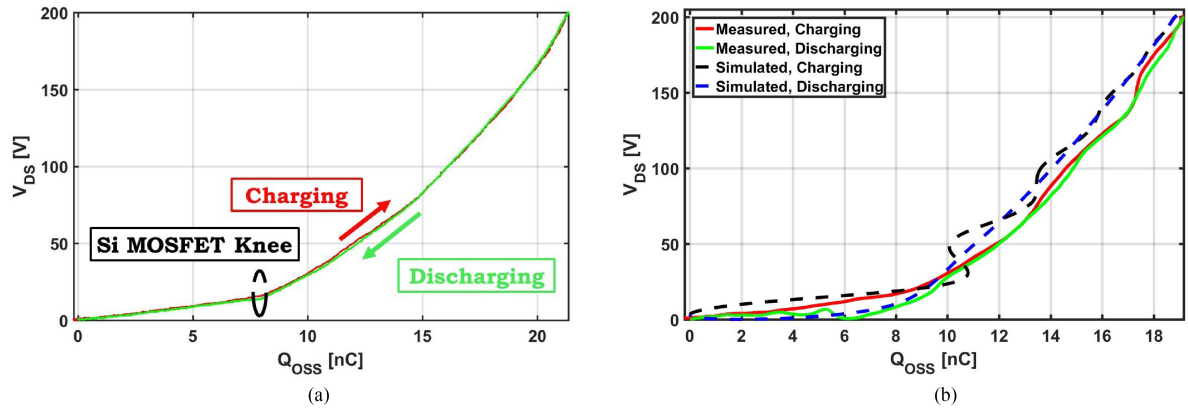


Fig. 9. Measured V_{DS} versus Q_{OSS} for the TPH3202LS device at two different frequencies and voltage swings. Note the knee in the curve in (a), which corresponds to that seen in [11] and [12] in silicon superjunction MOSFETs. In (b), we compare the manufacturer-provided model (TO-220 package) and the measured results (PQFN package). (a) 200 V_{DS} swing at 5 MHz. (b) 200 V_{DS} swing at 35 MHz, with simulation waveforms.

in the silicon superjunction devices [11], [12], which showed no frequency dependence up to the measured 100 kHz. Furthermore, the frequency dependence invalidates the assumption that a fixed percentage of total E_{OSS} is dissipated in the device [16].

The Steinmetz fits predict between 0.2 μJ (5 MHz, GS66504B) and 2.2 μJ (35 MHz, TPH3202LS) energy dissipated per cycle for a sine wave with $V_{PP} = V_{DS,MAX}$, corresponding to tens of watts of loss at VHF. For example, operating the *best* studied device (GS66504B) at 30 MHz and 650 V_{DS} would result in 15.8 W of dissipated power, swamping conduction losses in most applications.

C. C_{OSS} Loss Comparisons

These initial measurements indicate significant variation in both loss magnitude and voltage dependence across device type and manufacturer. We further explore how the losses scale within a family and attempt to ascertain the relative loss contributions of the packaging and the device itself. The detailed device constructions are proprietary to the device manufacturers, and this

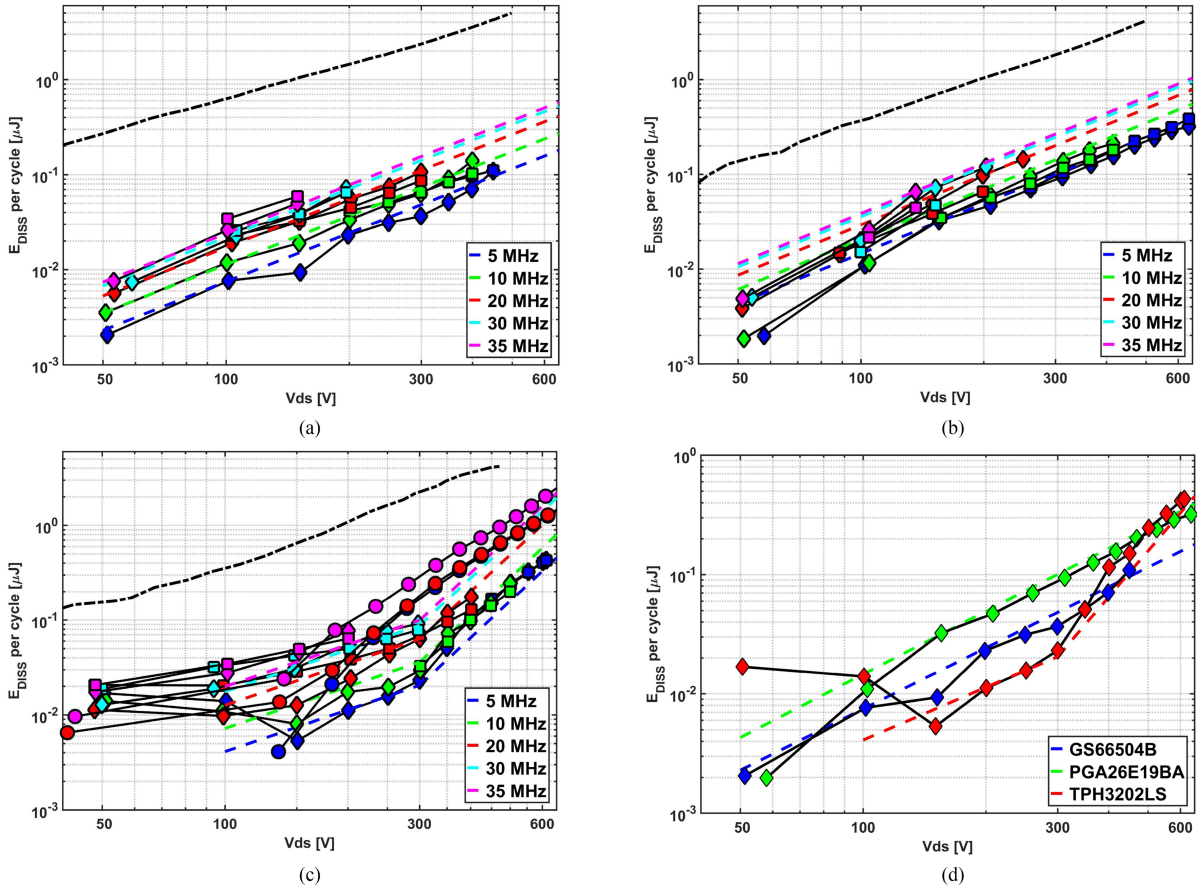


Fig. 10. Sawyer–Tower measurements (△), thermometric measurements (□), Steinmetz fits ("–") from Table V, and total E_{OSS} (dot-dash lines). Simulation model losses are added to (c) at 5, 20, and 35 MHz (○). Subfigure (d) plots the 5 MHz electrical measurements and fittings for all three devices to highlight the differences in waveshape between the enhancement-mode and cascode devices. (a) GaN Systems GS66504B. (b) Panasonic PGA26E19BA. (c) Transphorm TPH3202LS. (d) 5 MHz curves, reproduced to compare devices.

TABLE V
STEINMETZ PARAMETERS FOR C_{OSS}-RELATED LOSSES IN COMMERCIALLY AVAILABLE GaN DEVICES

Device	k [μJ/(V · Hz)]	α	β
GS66504B	$2.84 \cdot 10^{-10}$	0.6	1.70
PGA26E19BA	$1.96 \cdot 10^{-9}$	0.5	1.76
TPH3202LS, V $<$ 300 V	$1.78 \cdot 10^{-11}$	0.8	1.46
TPH3202LS, V $\geq$ 300 V	$8.72 \cdot 10^{-18}$	0.8	4.01

Steinmetz fits are shown in Fig. 10.

limits the extent to which we may understand the core loss driver beyond attempting to divide loss contributions from the die and the packaging.

We compare losses between the following devices to attempt to disassociate the die losses from the package losses and to understand how losses scale within a family:

1) two die sizes in one package, PGA26E19BA and PGA26E07BA;
2) two die sizes in different packages, GS66504B and GS66508B;
3) same die size in two different packages, GS66508T and GS66508B.

The die size conclusions are assumptions based only on datasheet parameters (with no access to proprietary information on the internal construction of the devices); the two GS66508x parts have identical electrical parameters, so we assume the same internal part, and the PGA26ExxBA parts are footprint-compatible and scaled with respect to capacitance, current, and $R_{DS,ON}$ characteristics, so we assume the die has been scaled commensurately. Table VI summarizes the key parameters for the devices compared in this section.

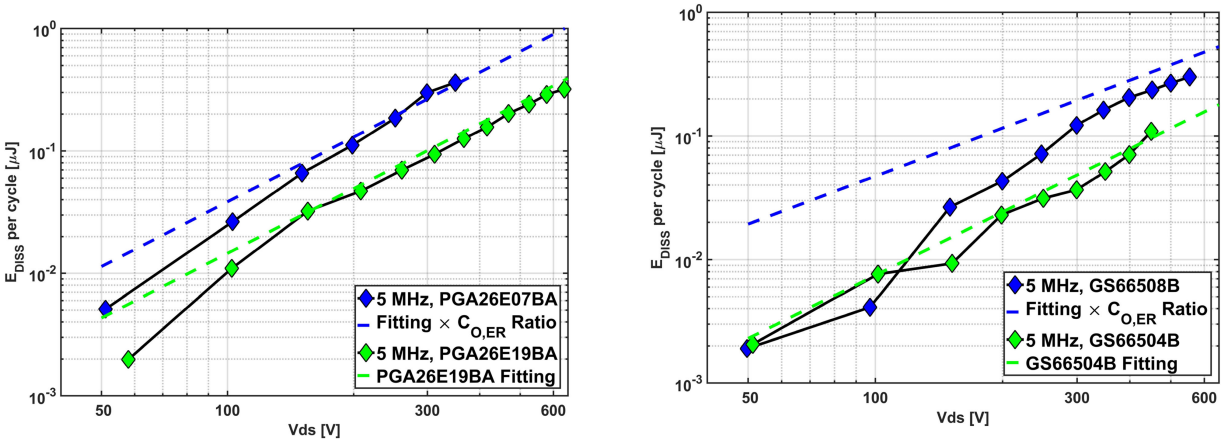
Fig. 11 shows the first two comparisons enumerated above. We find that, for an identical package, the losses scale precisely with $C_{O,ER}$, providing a simple method for scaling the losses reported here to other devices within a family. When the die size is increased and the package is also changed [see Fig. 11(b)], a simple $C_{O,ER}$ scaling of the losses provides a good ballpark estimation of the losses but, in this particular case, overestimates the measured losses by about 50% above 300 V_{DS}. Taken together, these two plots indicate that the device itself is the key C_{OSS} loss driver, although changes in packaging cannot be neglected for precise loss estimates.

Fig. 12 compares two (assumed) identical dies in a top-side cooled (GS66508T) and bottom-side cooled (GS66508B) package. The measured losses appear to converge as the $\mathbf{dV/dt}$ is increased, either at large voltage swings at 5 MHz or for the

TABLE VI
KEY PARAMETERS FOR DEVICES COMPARED IN FIGS. 11 AND 12

Comparison	Device	$\mathbf{R_{DS,ON}}$, 25 °C (mΩ)	$\mathbf{C_{O(ER)}}$ (pF)	Package size and code
Fixed package, scaled die	PGA26E19BA	140	33	7.9 mm × 7.9 mm
	PGA26E07BA	56	87	
Scaled package, scaled die	GS66504B	100	44	5.01 mm × 6.56 mm
	GS66508B	50	88	6.98 mm × 8.38 mm
Different package, fixed die	GS66508T	50	88	6.96 mm × 4.48 mm, "T"
	GS66508B	50	88	6.98 mm × 8.38 mm, "B"

$C_{O,ER}$ values are for the same voltage where compared directly. $R_{DS,ON}$ values are the nominal datasheet values at 25 °C.



(a) (b)

Fig. 11. Comparison in losses at 5 MHz between scaling the die size in a fixed package (a) and scaling both the die size and package size (b). (a) Fixed package, scaled die (PGAxxE19BA). (b) Scaled package and scaled die (GS66504B, GS66508B).

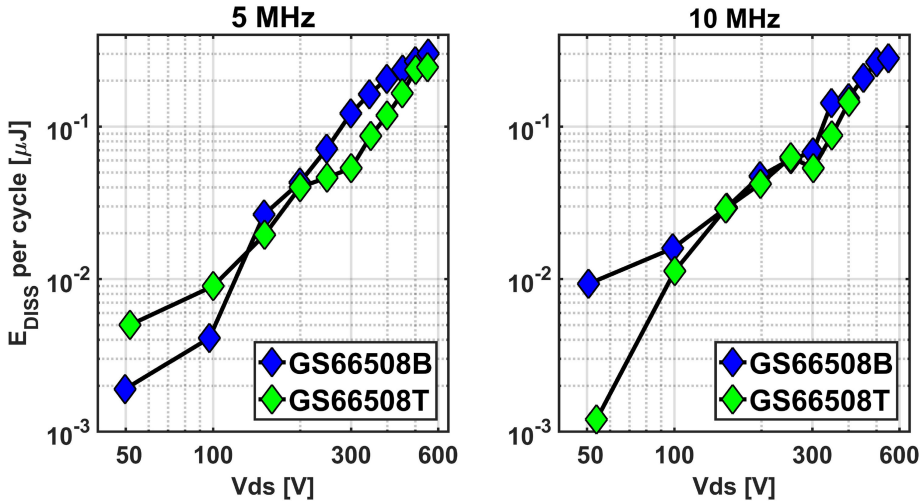


Fig. 12. Comparison in electrical loss measurements at 5 MHz and 10 MHz with an (assumed) identical die and two different packages. GS66508T is top-side cooled and GS66508B is bottom-side cooled.

10 MHz measurements, and the losses are similar within the measurement tolerance of our test setup.

With a small number of commercially available parts and without access to proprietary data on device construction, we are limited in the definitive conclusions we can draw on the loss mechanism and its scaling with size and package. Nonetheless, the comparisons in this section seem to indicate that losses scale linearly with output energy storage within a single package and losses appear to be dominated by the device itself, not the underlying packaging.

IV. HIGH $\mathbf{dV/dt}$ C_{OSS} LOSSES

Although large, the sine wave losses did not fully account for the magnitude of observed losses in the converters utilizing GaN devices from Section II. A sine wave has the lowest

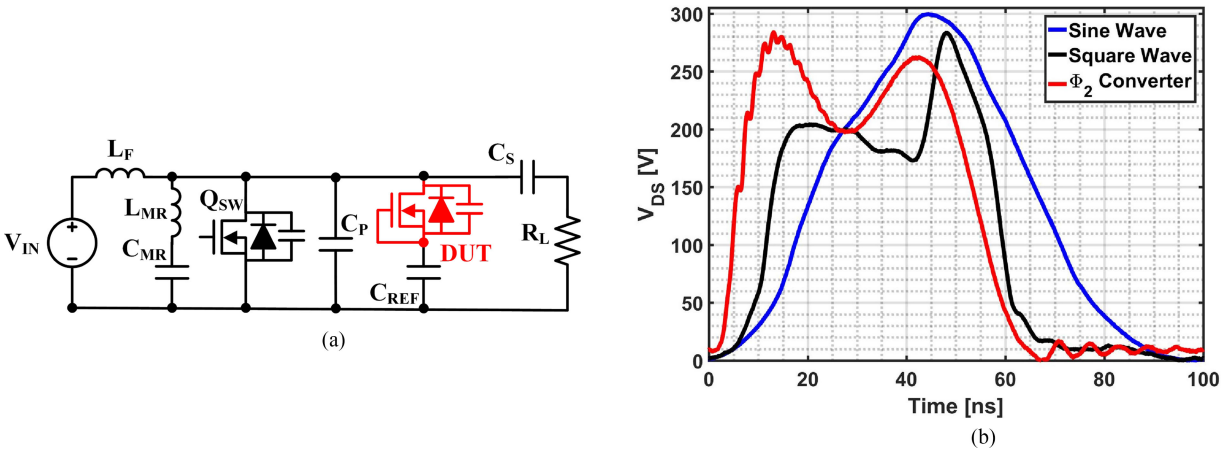


Fig. 13. (a) Schematic of the Class-Φ_2 waveshape generator to increase $\mathbf{dV/dt}$, with GaN HEMTs utilized as the switching device (Q_{SW}) and DUT. Gate drive circuitry not shown. (b) Waveforms injected across the device at 10 MHz with increasing $\mathbf{dV/dt}$. (a) Class-Φ_2 waveshape generator schematic. (b) Three measured V_{DS} waveshapes across the GS66504B at 10 MHz, with similar (~290 V) peak voltages.

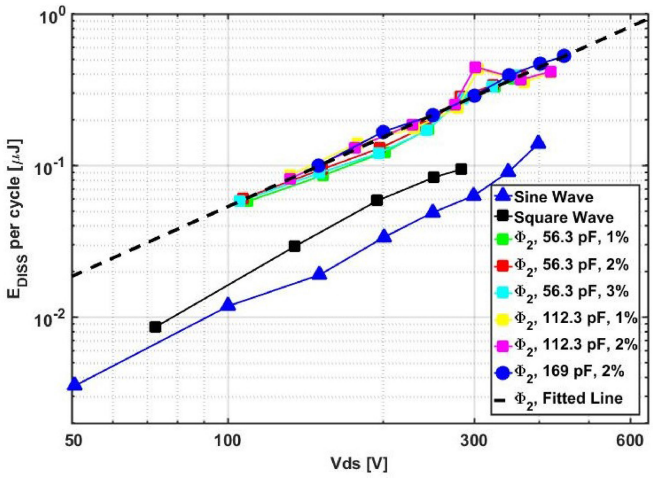


Fig. 14. Increasing $\mathbf{dV/dt}$ at 10 MHz (GS66504B). Legend values refer to C_{REF} and pulse width. Fit line uses (7), with $k = 3 \cdot 10^{-9}$, $\beta = 1.52$, $\alpha = 0.6$.

possible $\mathbf{dV/dt}$ for a given frequency and peak voltage, and we hypothesized that increasing $\mathbf{dV/dt}$ at a fixed frequency would result in a corresponding increase in E_{DISS}. This would also explain the frequency dependence measured in Section III-B.

To investigate, we fix the frequency and compare losses from three signals, the sine wave, a distorted square wave from the power amplifier, and a Class-Φ_2 waveform, measured by adding a Sawyer–Tower circuit in parallel with two operating converters at 10 and 30 MHz [see Fig. 13(a)]. At 10 MHz, this increases the peak slew rate from approximately 8 $\mathbf{V/ns}$ (sine) to 13 $\mathbf{V/ns}$ (square) to 70 $\mathbf{V/ns}$ (Φ_2). Applied waveforms at 10 MHz are shown in Fig. 13(b). At 30 MHz, the power amplifier cannot output a square wave, so only the sine (24 $\mathbf{V/ns}$) and Φ_2 (130 $\mathbf{V/ns}$) waveforms are compared. Φ_2 measurements include varying pulse rates and C_{REF} values to validate the measurements in lieu of a thermometric validation, which was not possible due to thermal cross coupling between the wave generator and the DUT.

Losses at 10 MHz for the GS66504B are shown in Fig. 14, with a clear increase in E_{DISS} between the sine, square, and Class-Φ_2 waveshapes. To separate increasing $\mathbf{dV/dt}$ from differences in waveshape, we introduce two normalizations. Fig. 15 plots loss per cycle against normalized $\mathbf{dV/dt}$ for all three devices, with the voltage slew normalized as (with β from Table V)

$$\left(\frac{dV}{dt}\right)_{\text{NORM}} = \left(\frac{dV}{dt}\right)_{\text{MEAS}} \left(\frac{V_{DS}}{V_{DS,MAX}}\right)^{\beta}. \tag{8}$$

This equation is proposed to eliminate voltage swing from the comparison to independently assess any $\mathbf{dV/dt}$ dependence.

Second, in Fig. 16, we plot the percentage of the stored energy that is dissipated (y-axis) versus the measured $\mathbf{dV/dt}$. Total stored energy is taken from the E_{OSS} plot in the respective datasheet (at the appropriate V_{DS}).

The e-mode devices exhibit exponentially increasing losses with $\mathbf{dV/dt}$. In each, we measure slightly lower losses than expected (based on $\mathbf{dV/dt}$ alone) with the Φ_2 waveshape, with a more pronounced decrease for the PGA26E19BA. This may be attributable to the asymmetry in the Class-Φ_2 waveform, where the charging $\mathbf{dV/dt}$ is much higher than the discharging $\mathbf{dV/dt}$. With a 650 V_{DS} swing and $\mathbf{dV/dt}$ of 50 $\mathbf{V/ns}$, the output capacitors in both devices dissipate over 0.5 μJ per cycle. Fig. 15 further confirms that the assumption of a fixed E_{OSS} percentage of dissipated energy [16] is not valid, as E_{OSS} is independent of $\mathbf{dV/dt}$ but the losses are highly dependent on this parameter.

As expected from the Steinmetz fitting, the TPH3202LS device has a bifurcated $\mathbf{dV/dt}$ relationship with the sine wave input. At low V_{DS}, the losses are less than the e-mode devices for a given normalized $\mathbf{dV/dt}$. For V_{DS} over 300 V, where E_{DISS} rises as V^4, the losses are much greater. As the $\mathbf{dV/dt}$ of the waveshape increases, however, the bifurcation becomes less apparent, and, for the Class-Φ_2 waveshapes, the low- and high-voltage results combine into a single curve when the Steinmetz β parameter is included in the normalization, as shown in Fig. 15. Fig. 16 does not account for the separate regions of voltage de-

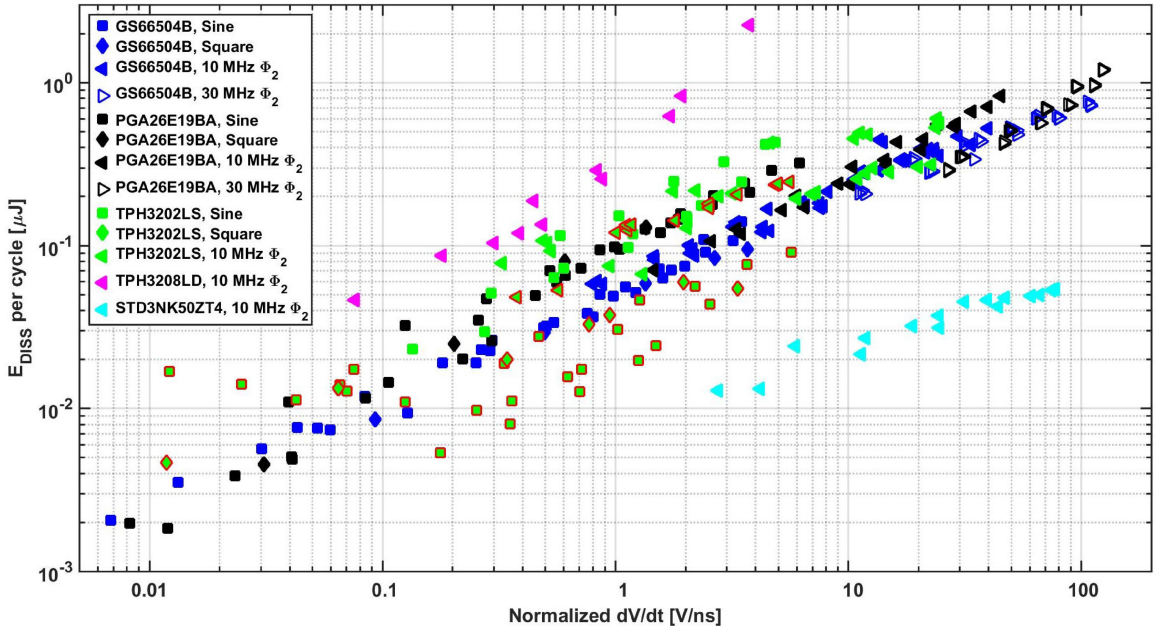


Fig. 15. Losses per cycle versus normalized, by (8), $\mathbf{dV/dt}$ for the three studied devices and two additional "extreme performance" devices. The red outline around the TPH3202LS results indicates applied voltages under 300 V and $\beta = 1.46$ in (8). All recorded measurements are included here. There are no measurements for the TPH3202LS 30 MHz Φ_2, as the Φ_2 wave generator could not be tuned to maintain ZVS with the TPH3202LS device and $\mathrm{C_{REF}}$ in parallel.

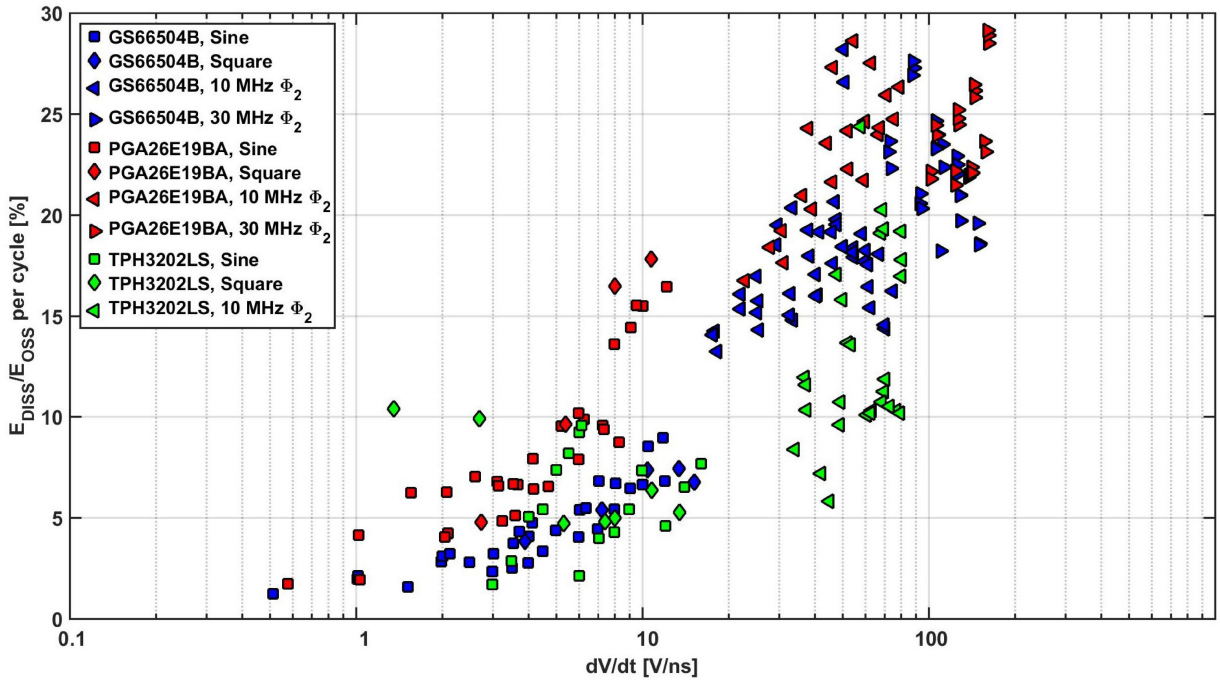


Fig. 16. Percent of stored energy that is dissipated each cycle versus measured $\mathbf{dV/dt}$ for the three studied devices. All recorded measurements are included here.

pendence in the cascode device, resulting in two groupings of data for this device at high $\mathbf{dV/dt}$ values. The lower group corresponds to high $\mathbf{dV/dt}$ but low overall voltage swing, where the cascode device outperforms the enhancement-mode devices.

Under extremely high $\mathbf{dV/dt}$, the three devices have similar measured losses. To verify that this convergence is not an artifact of the Class-Φ_2 measurement setup that generates the high $\mathbf{dV/dt}$ pulses, we tested two other devices with extreme expected $\mathrm{E_{DISS}}$, a 500 V Si device (ST Micro STD3NK50ZT4), which we expect to have much lower $\mathrm{E_{DISS}}$, and a larger device from the same family as TPH3202LS (TPH3208LD), which has an $\mathrm{E_{OSS}}$ around 2× larger than TPH3202LS and should, therefore, exhibit higher $\mathrm{E_{DISS}}$. We conservatively assume $\beta = 2$ for the Si device, and use $\beta = 1.46$ from TPH3202LS for the

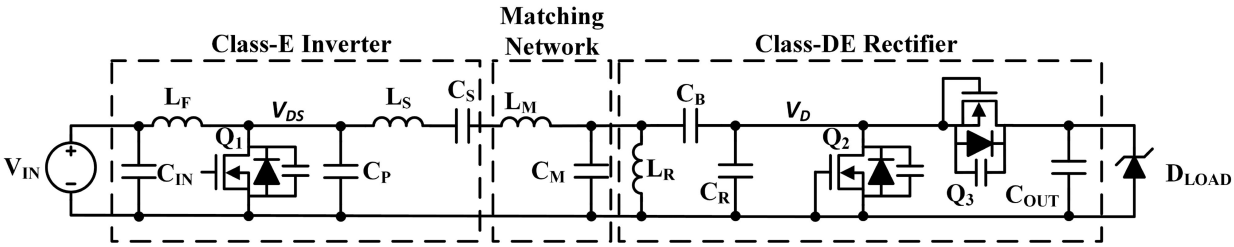


Fig. 17. DC–DC converter topology, with Q_1–Q_3 implemented as GaN HEMTs. Note that the converter could be further simplified by combining L_S and L_M and eliminating C_M, but the high component count is kept for modularity in testing.

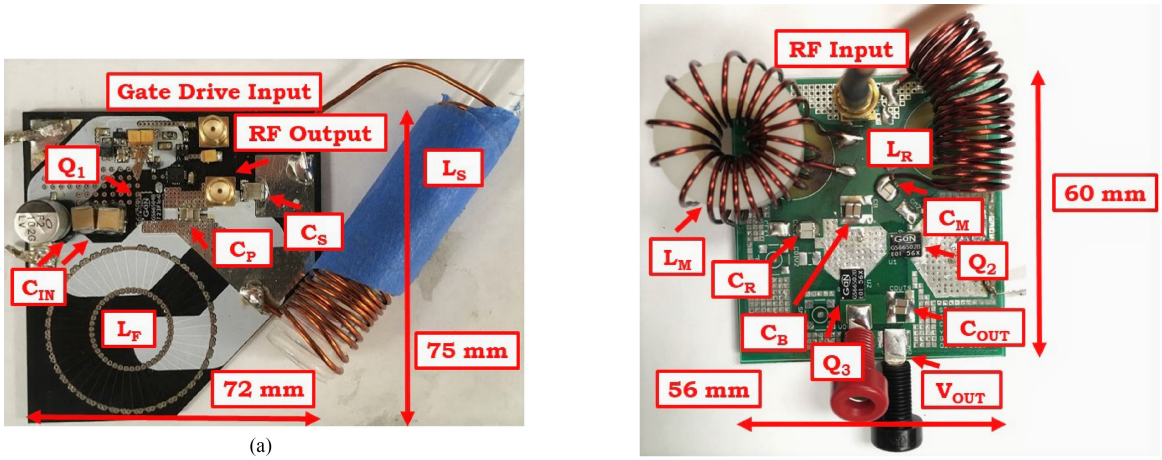


Fig. 18. Inverter and rectifier blocks for the implemented dc–dc converters. The matching network is included on the rectifier board. (a) Implemented GS66504B inverter. L_S is moved between the two boards to limit component variation. (b) Implemented GS66502B rectifier. The GS66504B rectifier is implemented on the same board with C_R removed and the devices replaced.

TPH3208LD. The results are as expected, and we conclude this convergence is not a relic of an invalid test setup.

Figs. 15 and 16 can be used to predict C_{OSS} losses in soft-switched converters using these GaN devices. From $\mathbf{dV/dt}$ and total voltage swing across the device, the reader can find the predicted E_{DISS} per cycle directly from either plot. The product of this value and the switching frequency is the predicted power dissipation from C_{OSS} losses. We demonstrate this method in a resonant dc–dc converter in Section V.

V. DC–DC Converter Demonstration

Generally, power converter efficiency is improved by increasing the size of the device, which lowers $R_{DS,ON}$ and thereby reduces conduction losses. In these soft-switched, HF/VHF converters, however, C_{OSS} losses may dominate over conduction losses, resulting in a *reduction* of overall converter efficiency with greater device area.

We demonstrate the importance and predictability of these losses *in situ* by fabricating two resonant dc–dc converters with a finite-choke Class E inverter [34], a matching network, and a Class-DE rectifier, as shown in Fig. 17. The Class E inverter is selected for the quasi-sinusoidal voltage applied across the inverter switching device, Q_1, which neatly approximates the Sawyer–Tower applied waveforms. The converters are designed to operate at 10 MHz switching frequency and deliver 200 W output power at 500 V_{OUT} and 125 V_{IN}. An array of zener diodes is used for the load to provide rapid clamping and a nearly fixed output voltage without closed-loop control. The converter could be further simplified (for example, by combining L_S and L_M and/or eliminating C_M), but modularity is maintained here so that we can swap the inverter and rectifier blocks separately.

The converters are first designed with GaN Systems GS66502B device as Q_1–Q_3, and we subsequently redesign the converter to utilize a lower $R_{DS,ON}$ device in the identical package, GaN Systems GS66504B, while maintaining similar output power, circulating currents, and drain-source voltage across the devices. In resonant converters, larger capacitances (including the device capacitance) may lower the impedance of the network and increase circulating currents, which can offset the gains achieved through reducing on-resistance [35]. Here, we fix the circulating currents by varying the values of C_P and C_R. This results in identical measured waveforms (see Fig. 19) and similar circulating currents (in simulation) in the two converters.

The top part of Table VII shows the key simulation parameters for each converter. As expected, moving from the GS66502B (nominal $R_{DS,ON}$: 200 mΩ) to the GS66504B (nominal $R_{DS,ON}$: 100 mΩ) device results in an increase in simulated efficiency and a reduction in conduction losses in the devices.

To include expected C_{OSS} losses, we use the normalized $\mathbf{dV/dt}$ in each device (using the simulated $\mathbf{dV/dt}$ and normalized using Equation (8) and find the intercept with the

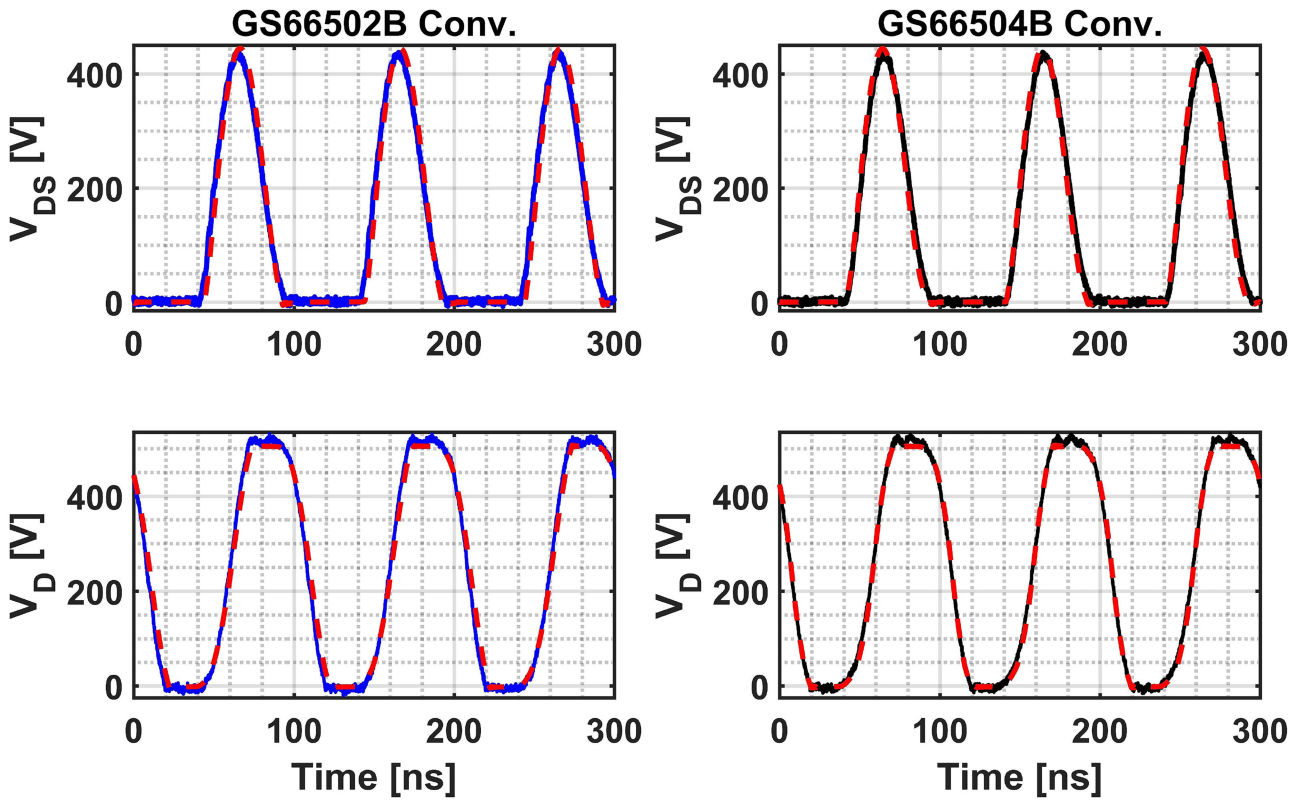


Fig. 19. Measured converter operation (solid lines) at 125 V_{IN}, with simulated results overlaid (red dashed lines). Simulation and measurement matching is good, and the key waveforms are nearly identical in both converters. Voltages refer to named nodes in Fig. 17.

TABLE VII
KEY SIMULATION PARAMETERS FOR THE FABRICATED CONVERTERS AT NOMINAL 125 V_{IN} AND 500 V_{OUT}

Parameter	GS66502B Conv.	GS66504B Conv.
Input power	186 W	185 W
Simulated η	88.1%	90.2%
Q_1 Sim. losses	1.9 W	0.9 W
$Q_{2,3}$ Sim. losses	0.8 W	0.8 W
Q_1 C_{OSS} losses	1.0 W	2.0 W
$Q_{2,3}$ C_{OSS} losses	1.8 W	3.5 W
Predicted η	85.6%	85.3%

$Q_{2,3}$ losses are given *per device*.

GS66504B results in Fig. 15. The two devices are packaged identically, and we therefore, can use the results from Fig. 11(a) to assume the C_{OSS} losses in the GS66502B (which were never measured in the Sawyer–Tower test setup) will be half the measured losses in the GS66504B. When the C_{OSS} losses are added to the simulated power dissipation in the remainder of the converter, as shown at the bottom of Table VII, the converter efficiency is predicted to decrease as the die size is increased.

These converters are subsequently fabricated, with the components detailed in Table VIII and the boards shown in Fig. 18. To eliminate component variation, the rectifiers use the same board, with the devices replaced and C_R varied, and L_S is transferred between two identical inverter boards (L_F does not vary significantly due to its implementation using PCB traces). The full converter implementation is shown in the center image of Fig. 21.

Fig. 19 shows the measured waveforms at the nominal 125 V_{IN} operating point for each converter. The simulation results, shown as red dashed lines, match the measured waveforms, shown as solid lines, in both the inverter and rectifier, and the rise time and peak voltages are nearly identical in the two converters. Q_1 achieves soft-switching in both implementations.

The input voltage is varied from 105 V, the minimum voltage that maintains conduction through the devices in the rectifier, to 130 V. The C_{OSS} losses in the rectifier are essentially fixed across this range, as those devices experience similar $\mathbf{dV/dt}$ independent of input voltage (due to the constant output voltage), while the inverter device (Q_1) has varying C_{OSS} losses with input voltage. DC–DC efficiency is measured at each operating point and compared with simulated efficiency and the predicted efficiency with C_{OSS} losses, as shown in Fig. 20. At all input voltages, the converter with larger devices, based on manufacturer-provided models, has higher simulated efficiency, but, when C_{OSS} losses are included, the converter with smaller devices achieves better performance. Measured efficiency approaches agreement with predicted efficiency only when C_{OSS} losses are considered.

Fig. 21, which shows steady-state thermal operation at 20% pulse rate and 125 V_{IN}, shows that the relative losses in the devices are correctly predicted by combining the C_{OSS} and simulated conduction losses. Namely, examining the summed device power dissipation in Table VII, we expect a negligible in-

TABLE VIII
CIRCUIT COMPONENTS IN RECTIFIER AND INVERTER, WITH REFERENCES FROM FIG. 17

Component	Design value	Implementation
C_{IN}	14 μF	10 μF Nichicon ULV2G100MNL1GS + 4 × 1 μF Knowles Syfer 2220Y5000105KXTWS2
L_F	580 nH	Toroidal PCB, Q = 125 at 10 MHz
L_S	4.7 μH	Solenoid Air-Core, Q = 350 at 10 MHz
C_S	60 pF	2 × 30 pF AVX 1808HA300KAT1A
C_P	GS66502B: 225 pF GS66504B: 200 pF	100 pF AVX 1206AA101JAT2A + (4 or 5) × 22 pF AVX 1206AA220KAT1A
L_M	1.98 μH	Toroidal Wirewound, Q = 198 at 10 MHz
C_M	78 pF	2 × 39 pF Murata GRM31A5C3A390JW01D
L_R	1.59 μH	Solenoid Air-Core, Q = 200 at 10 MHz
C_B	11.2 nF	2 × 5.6 nF Kemet C1206C562JBGACAUTO
C_R	GS66502B: 60 pF GS66504B: 0 pF	4 × 15 pF Yageo CC1206JKNPODBN150
C_{OUT}	11.2 nF	2 × 5.6 nF Kemet C1206C562JBGACAUTO
Z_{LOAD}	500 V Zener diodes	2 × 200 V NTE5296A + 100 V NTE5285A

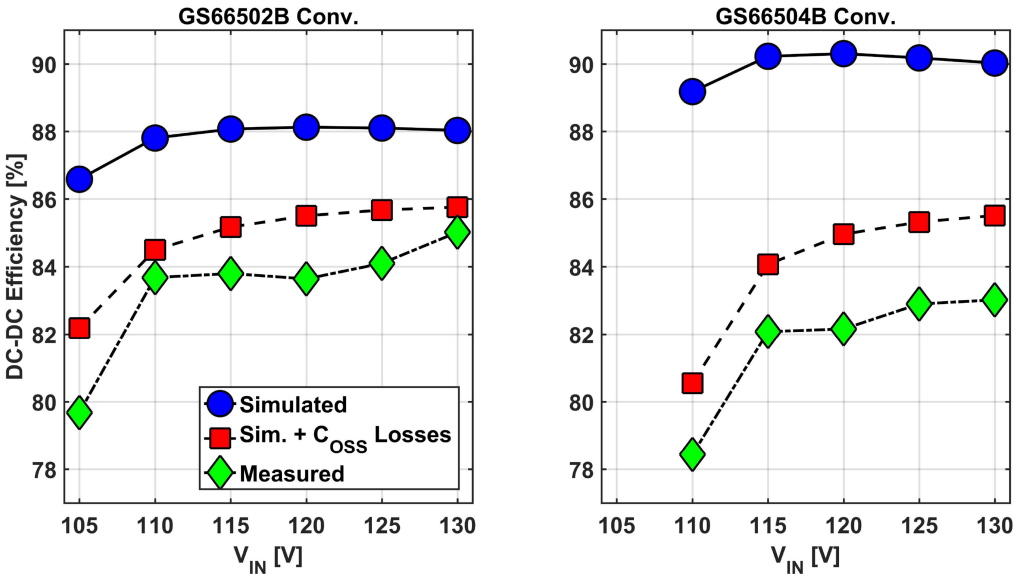


Fig. 20. Comparison between the GS66502B and GS66504B converters over the operating voltage range. At all operating points, the larger device (GS66504B) is simulated to have higher efficiency but measured efficiency is lower. At 105 V_{IN}, the GS66504B converter does not achieve turn-on of the devices in the rectifier, so, with the zener diode load, output power is zero. This point is excluded from the graph at right.

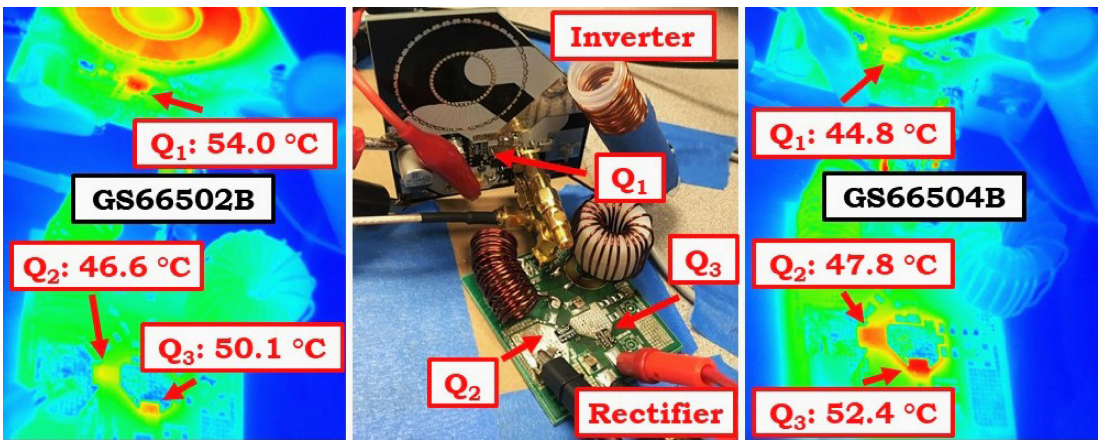


Fig. 21. Constructed full converter shown at middle. Thermal images of GS66502B operation (left) and GS66504B operation (right) at 20% duty cycle with 1 kHz pulse rate and 5-min. soak. The temperature of the rectifier devices rises in the GS66504B implementation due to much larger C_{OSS} losses in the larger devices.

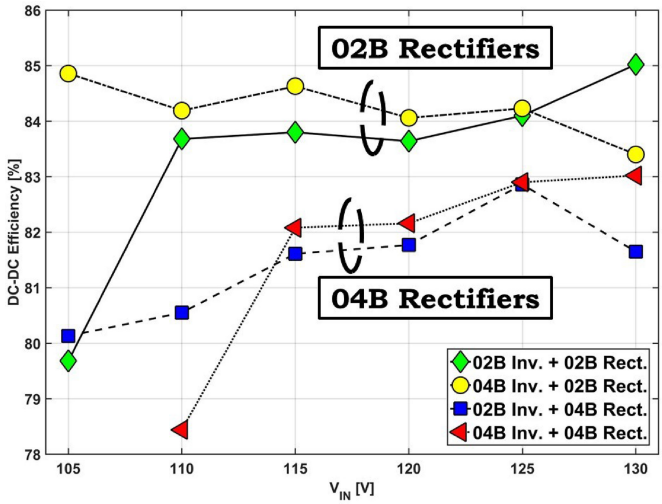


Fig. 22. Measured efficiency across the voltage input range for the various combinations of inverters and rectifiers. Legend terms refer to the GaN Systems GS6650xx device used for the power switches in each converter block. The choice of device in the rectifier has a significant effect on overall efficiency due to much higher C_{OSS} losses with the larger devices.

crease in inverter device (Q_1) power dissipation and a significant increase in rectifier device (Q_2 and Q_3) power dissipation. With lower thermal resistance in the GS66504B ($R_{JC} = 1$ K/W) relative to the GS66502B ($R_{JC} = 2$ K/W), this results in a lower Q_1 temperature (equal P_{DISS}, lower R_{JC}) and a higher Q_2 and Q_3 temperature ($1.7\times$ higher P_{DISS}, lower R_{JC}) on the GS66504B converter. Exact dissipation in each power device is difficult to determine due to coupling from neighboring dissipative components.

From these results, we see that, due to C_{OSS} losses, the advantage of switching to larger devices will depend on the application and specifically the device current, operating frequency, voltage swing, and C_{OSS} loss magnitude. In the converter demonstrated here, the larger device is slightly advantageous in the inverter, where similar dissipated power and the improved ability to remove heat result in improved performance (due to reduced device heating) over the smaller device, but extremely disadvantageous in the rectifier, where the larger voltage swing and lower conduction losses results in significantly worse performance with a larger device. These results are confirmed by combining inverters and rectifiers that utilize different devices, where we expect significantly worse performance with any configuration using the GS66504B devices in the rectifier and slight improvements when moving from the GS66502B device to the GS66504B device in the inverter. This hypothesis is confirmed through measured efficiency results with the various configurations, as shown in Fig. 22.

VI. Conclusion

We aimed to utilize GaN devices and air-core inductors from PCB traces to develop dc-RF converters using the Class-Φ_2 topology. After characterizing these converters, which operate at 1 kW output power and 10, 30, and 54.24 MHz switching frequencies, we found extremely high power dissipation in the GaN HEMTs. Prior art led us to investigate the output capacitance as the source of the unexpectedly high losses.

We report C_{OSS} losses in GaN devices with large, fast voltage swings at HF and VHF. In a sample from each manufacturer with commercially available 600 V_{DS} devices, we find significant losses that are either not included or poorly described in manufacturer-provided models. These losses, which are measured using standard and modified Sawyer–Tower circuits, correlate to higher-than-expected losses in operating soft-switched converters. Each of the devices, if exercised across its rated voltage at VHF, would dissipate too much heat *in* C_{OSS} *alone* to extract easily. For example, the best performing device here would dissipate over 20% of E_{OSS} in a 30 MHz Class-Φ_2 converter. Losses rise exponentially with $\mathbf{dV/dt}$, indicating that the loss mechanism is not only dependent on total charge storage, as described in the previous literature. Finally, we demonstrate the accurate prediction of total losses in 10 MHz, 200 W resonant converters utilizing GaN devices, including a device where the C_{OSS} losses were not directly measured and must be extrapolated from results in this paper. In these converters, we show that, due to these C_{OSS} losses, the overall performance is no longer improved by increasing the die area of the semiconductors. In application, C_{OSS} losses must be optimized with the conduction losses in the device, potentially resulting in limitations in operating frequency and voltage. C_{OSS} losses need to be added to manufacturer-provided datasheets and simulation models, and manufacturers must address these losses to utilize high-voltage GaN devices at high- and very-high-frequencies.

Acknowledgment

The authors would like to thank Dr. J. Plummer and Dr. J. Strydom for their insights and generosity of time.

References

[1] D. J. Perreault *et al.*, "Opportunities and challenges in very high frequency power conversion," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2009, pp. 1–14.
[2] N. O. Sokal, "Class-E RF power amplifiers," *QEX*, vol. 204, pp. 9–20, Jan./Feb. 2001.
[3] J. M. Rivas, Y. Han, O. Leitermann, A. Sagneri, and D. J. Perreault, "A high-frequency resonant inverter topology with low voltage stress," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 2705–2717.
[4] B. Ozpineci and L. Tolbert, "Comparison of wide-bandgap semiconductors for power electronics applications," United States Dept. Energy, Washington, DC, USA, Tech. Rep. ORNL/TM-2003/257, 2004.
[5] B. Lu, T. Palacios, D. Risbud, S. Bahl, and D. I. Anderson, "Extraction of dynamic on-resistance in GaN transistors: under soft-and hard-switching conditions," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, 2011, pp. 1–4.
[6] D. Jin and J. A. del Alamo, "Mechanisms responsible for dynamic on-resistance in GaN high-voltage HEMTs," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, 2012, pp. 333–336.
[7] O. C. Spro, D. Peftitsis, O. M. Midtgard, and T. Undeland, "Modelling and quantification of power losses due to dynamic on-state resistance of GaN E-mode HEMT," in *Proc. IEEE Control Model. Power Electron.*, 2017, pp. 1–6.
[8] Panasonic X-GAN Power Transistorsr, Panasonic, Kadoma, Japan. [Online]. Available: https://eu.industrial.panasonic.com/products/semiconductors/power/gan-power-transistors. Accessed on: Oct. 2017.
[9] K. Surakitbovorn and J. R. Davila, "Evaluation of GaN transistor losses at MHz frequencies in soft switching converters," in *Proc. IEEE Control Model. Power Electron.*, 2017, pp. 1–6.

[10] S. Park and J. R. Davila, "Power loss of GaN transistor reverse diodes in a high frequency high voltage resonant rectifier," in *Proc. IEEE Appl. Power Electron. Conf.*, 2017, pp. 1942–1945.

[11] J. Fedison, M. Fornage, M. J. Harrison, and D. R. Zimmanck, "C_{OSS} related energy loss in power MOSFETs used in zero-voltage-switched applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 2014, pp. 150–156.

[12] J. Fedison and M. Harrison, "C_{OSS} hysteresis in advanced superjunction MOSFETs," in *Proc. IEEE Power Electron. Conf.*, 2016, pp. 247–252.

[13] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and application of 600 V GaN HEMT in cascode structure," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2453–2461, May 2014.

[14] K. J. Chen *et al.*, "GaN-on-Si Power Technology: Devices and Applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, May 2017.

[15] R. Miftakhutdinov, "New ZVS analysis of PWM converters applied to super-junction, GaN and SiC power FETs," in *Proc. IEEE Appl. Power Electron. Conf.*, 2015, pp. 336–341.

[16] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.

[17] A. Sepahvand, Y. Zhang, and D. Maksimovic, "High efficiency 20–400 MHz PWM converters using air-core inductors and monolithic power stages in a normally-off GaN process," in *Proc. IEEE Appl. Power Electron. Conf.*, 2016, pp. 580–586.

[18] D. Kinzer, "GaN power IC technology: Past, present, and future," in *Proc. IEEE Int. Symp. Power Semicond. Dev. ICs*, 2017, pp. 19–24.

[19] W. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. Costinett, "Investigation of soft-switching behavior of 600 V cascode GaN HEMT," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 2865–2872.

[20] E. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.

[21] D. Reusch and J. Strydom, "Evaluation of gallium nitride transistors in high frequency resonant and soft-switching DC–DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5151–5158, Sep. 2015.

[22] C. B. Sawyer and C. Tower, "Rochelle salt as a dielectric," *Phys. Rev.*, vol. 35, no. 3, 1930, Art. no. 269.

[23] GS66504B Bottom-Side Cooled 650 V E-Mode GaN Transistor, GaN Systems, Ottawa, ON, Canada. [Online]. Available: www.gansystems.com/gs66504b.php. Accessed on: Oct. 2017.

[24] G. Zulauf, W. Liang, and J. Rivas-Davila, "A unified model for high-power, air-core toroidal PCB inductors," in *Proc. IEEE Control Model. Power Electron.*, 2017, pp. 1–8.

[25] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10 kV SiC MOSFETs and diodes," *IEEE Trans. Power Electron.*, to be published.

[26] J. T. Strydom, J. D. van Wyk, and J. A. Ferreira, "Capacitor measurements for power electronic applications," in *Proc. IEEE Ind. Appl. Conf.*, 1999, vol. 4, pp. 2435–2440.

[27] J. T. Strydom *et al.*, "Dielectric measurements for power electronic applications," *IEEE Trans. Ind. Appl.*, vol. 37, no. 3, pp. 829–839, 2001.

[28] R. Chen *et al.*, "Large signal dielectric characterization measurement for integrated passive devices," in *Proc. IEEE Appl. Power Electron. Conf.*, 2001, vol. 2, pp. 1203–1209.

[29] J. Prinsloo *et al.*, "Manufacture, behaviour and modelling of $BaTiO_3$ nonlinear ceramic disc capacitors for high-voltage applications," in *Proc. IEEE Electron. Compon. Technol. Conf.*, 1992, pp. 667–672.

[30] TPH3202L Series – 650V Cascode GaN FET, Transphorm, Goleta, CA, USA. [Online]. Available: http://www.transphormusa.com/document/600v-cascode-gan-fet-tph3202l/. Accessed on: Oct. 2017.

[31] Product Standards, PGA26E19BA, Panasonic, Kadoma, Japan. [Online]. Available: http://www.mouser.com/ds/2/315/pga26e19ba-product-standards-1112740.pdf. Accessed on: Oct. 2017.

[32] C. P. Steinmetz, "On the law of hysteresis," *IEEE Trans. Amer. Ins. Elect. Eng.*, vol. 9, no. 1, pp. 1–64, 1892.

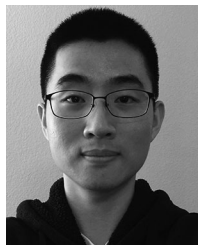
[33] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1977–1985, Apr. 2014.

[34] L. Roslaniec, A. S. Jurkov, A. Al Bastami, and D. J. Perreault, "Design of single-switch inverters for variable resistance/load modulation operation," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3200–3214, Jun. 2015.

[35] S. Sinha, B. Regensburger, K. Doubleday, A. Kumar, S. Pervaiz, and K. K. Afridi, "High-power-transfer-density capacitive wireless power transfer system for electric vehicle charging," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 967–974.

Grayson Zulauf (S'16) received the B.A. degree in engineering sciences in 2012 and the B.E. degree in electrical engineering with highest honors from the Thayer School of Engineering, Dartmouth College, Hanover, NH, USA, in 2013. He is currently working toward the Ph.D. degree in electrical engineering at the Stanford University Power Electronics Research Laboratory, Stanford University, Stanford, CA, USA, with research focused on extending high- and very-high-frequency resonant converters to electrified transportation applications.

His undergraduate research focused on reverse-engineering automotive CAN busses and the systemic delivery of magnetic nanoparticles for hyperthermia treatment. From 2013 to 2016, he was an Electrical Engineer and Product Manager with Motiv Power Systems, a company developing an all-electric powertrain for commercial vehicles.



Sanghyeon Park (S'16) was born in Seoul, South Korea, in 1991. He received the B.S. degree in electrical engineering from the Seoul National University, Seoul, South Korea, in 2015. He is currently working toward the Ph.D. degree in electrical engineering at the Stanford University, Stanford, CA, USA.

His research interest focuses on high-frequency power converters.

Wei Liang (S'12) received the B.Eng. degree from the Northwestern Polytechnical University, Xi'an, China, in 2011, the M.S.E. degree from the University of Michigan, Ann Arbor, MI, USA, in 2013, and the Ph.D. degree from Stanford University Power Electronics Research Laboratory, Stanford University, Stanford, CA, USA, in 2018, all in electrical engineering.

His research interests include high-/very-high-frequency power electronics and the air-core passive components design for HF/VHF power conversion.

Kawin North Surakitbovorn (S'15) was born in Bangkok, Thailand. He received the B.S. degree in physics and electrical science and engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2014. He is currently working toward the Ph.D. degree in electrical engineering from the Stanford University Power Electronics Research Laboratory, Stanford University, Stanford, CA, USA.

His current research interests include developing high efficient very high frequency power conversion system for wireless power transfer applications.

Juan Rivas-Davila (S'01–M'06–SM'17) was born in Mexico City, Mexico. He received the B.A.Sc. degree in electronics and communications engineering from the Monterrey Institute of Technology, Monterrey, Mexico, in 1998, and the S.M. and Sc.D. degrees in electrical engineering from the Laboratory of Electromagnetic and Electronic Systems, Massachusetts Institute of Technology, Cambridge, MA, USA, in 2003 and 2006, respectively.

From 2007 to 2011, he was a Power Electronics Engineer with the High-Frequency Power Electronics Group, General Electric Global Research Center, Niskayuna, NY, USA. From 2011 to 2013, he was an Assistant Professor with the University of Michigan, Ann Arbor, MI, USA. In 2014, he joined Stanford University, Stanford, CA, USA, as an Assistant Professor in the Electrical Engineering Department. His research interests include power electronics, RF power amplifiers, resonant converters, soft-switching topologies, and the design of air-core passive components for VHF power conversion.