CAD and Foundries for Microsystems

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Abstract

Besides foundry facilities, Computer-Aided Design (CAD) tools are also required to move microsystems from research prototypes to an industrial market. Currently available CAD tools need extensions before they can be used for the automated design of micromachined devices.
This paper presents a low cost access to microsystem technology (MST), applied by the CMP service, and based on the use of existing microelectronics production lines, with additional post-processing for microsystem specific 2D and 3D structures, and a global CAD approach for the design and simulation of microsystems applied to currently available commercial CAD tools, e.g. Mentor Framework, in order to ensure a continuous flow from the design to the manufacturing.

1. Introduction

Starting from the 70s, Microelectronics development has been made possible because of the use of CAD tools and because of the availability of foundries for Eduction/Research and for fabless companies, besides large IC manufacturers. Without such similar boosters, Microsystems might easily remain curiosities, top level prototypes manufactured by researchers, but they would not become industrial products.
Education and Research in Microelectronics had taken advantage of CAD tools developed in USA and in France: MAGIC in Berkeley, LUCIE in Grenoble. These tools were provided free of charge. Later, most Universities have been provided with commercial CAD tools. They had consequently the possibility to focus on the development of advanced CAD tools and on the design aspects rather than to spend time on CAD problems solved by commercial CAD tools.
Commercial CAD tools were initially basic layout editors. They became progressively frameworks allowing simulations, synthesis, schematics entry, etc. Design style has moved because of productivity needs required by the complexity provided by the technology. More and more, standard cells and, later, complex cores like microprocessors, caches, etc, have been used. The move is more recent for analog design, but it is emerging. From being an electronics engineer, the designer became a logic designer and next a system designer. But this is made possible because of the use of libraries, including layout and simulation models.
Considering the background on CAD for Microelectronics, a few principles should govern the development of CAD for Microsystems :

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• CAD for Microsystems should not be fully designed from scratch, but modules available for Microelectronics should be reused when existing ;
• CAD for Microsystems should look familiar to a user of CAD for Microelectronics ;
• the "system" user should be distinguished from the "library" designer : only the later one will use specific complex tools ;
• universities should be provided with the commercial tools developed for Microsystems.
Concerning the access to silicon, MOSIS in the US and CMP in France have provided in the early 80s facilities for integrated circuits manufacturing. These services have boosted Microelectronics since they allowed Students and Researchers to access professional facilities at a reasonable cost. Industry in turn received well educated Engineers, and make use actually of these services. Since 1981, CMP served 171 Institutions from 36 countries, about 1800 projects have been prototyped. When turning to Microsystems, the same approach to collectively manufacture microsystems at a low cost will boost Microsystems the same way as Microelectronics has been boosted in the past.
Considering the background on Microelectronics MPW, a few principles should govern the development of Microsystems MPW :
• Microsystems should be fabricated on industrial production lines, with an additional post-processing for microsystem specific structures. Moreover, it should be made use of production line already existing for Microelectronics, in order to take advantage of investments made in the past ;
• design kits to link CAD for Microsystems and MPW manufacturing have to be provided ;
• advanced microelectronics processes have to be accepted when IC-compatible microsystems are addressed, since CAD for Microelectronics come usually with (IC) libraries on advanced processes.
These principles for CAD and foundries for Microsystems govern the cooperative research on CAD done at TIMA in Grenoble in cooperation with Mentor Graphics, at TH Darmstadt and TU Budapest. The various modeling levels are addressed in the following : layout level, process level, device level, system level. An elementary design kit based on CADENCE has already been delivered to about 100 designers. An upgrated Engineering Kit based on MENTOR GRAPHICS is now available. Microsystem libraries and the electro-thermal simulator SISSSI, extended to microsystems, are also addressed.
The paper also addresses the manufacturing of Microsystems by CMP. The experience gained by CMP since 1981 with integrated circuits has been used to develop a service for providing microsystems. CMOS front-side silicon bulk micromachining as well as GaAs (HEMT and MESFET) compatible bulk micromachining are used to fabricate microsystems through the CMP service on a multi-project wafer using industrial production lines (e. g. ATMEL-ES2, PML, VITESSE, AMS), where the post-processing maskless

anisotropic etch is performed in central laboratories.
It is believed that the principles addressed for CAD and foundries for Microsytems will ensure that Microsystems will be only an **evolution** of Microelectronics, but Microsystems will ensure an industrial **revolution** by a massive pervasion of many application fields.

2. CAD overview

Most CAD tools for MEMS have been developped in the past to address specific needs like 3D analysis in OYSTER [Kop89] and MEMCAD [Sent92], etching in ASEP [Bus91], various characteristics of sensors in SENSIM [Lee82] and CAEMEMS [Zha90], or of actuators like micropumps [Zen93]. In addition, a few layout editors have been extended by defining additional layers. But all these tools are point tools ; they do not provide a complete CAD suite for the design of MEMS. The CAD situation can be compared to the IC CAD situation in the 70s when only point tools like those provided by CALMA, APPLICON, NCA or PDS were available. Later on, integrated tools from DAISY, MENTOR, VALID were available, and today Frameworks are available, from CADENCE, MENTOR, COMPASS, etc.. The issue today for the development of CAD tools for MEMS is to jump to a kind of framework, but based on existing IC frameworks.
The CAD environment considers both monolithic and hybrid solutions, answering the needs of both universities and companies as well as foundries. While the former considers the present state of the art and thus should be available , the monolithic approach aims at the co-fabrication of electronic and non-electronic functions: existing microelectronics production lines are being extended and adapted to allow MEMS production.
The environment allows a continuous design flow which can be seen or considered according to two points of view of a non-specialised *system-level designer* desiring to create a new microsystem with devices from at least two rather different areas, e.g. micro-mechanical and electronics, and the view of a device designer having expert knowledge on his domain of work, knowledge he would like to make available. Efforts to build more general simulation environments have been on going, e.g. to interface process simulators with FE tools, but these tools, besides having their own (non-standard) interface formats, require much expertise from the user, both in simulation and in device modeling. Our approach tends towards more flexibility and compatibility, and is intended for non-expert users as well as for expert users.

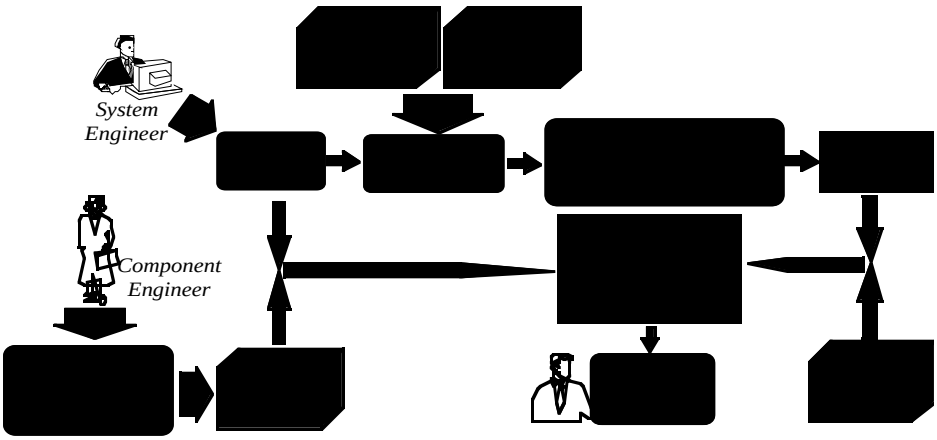

Fig. 1. The CAD structure

The environment hence contains elements for the device designer, enabling him to design modules, to simulate them, and finally to put the knowledge in the form of characterised standard cells in library.
The system level user takes profit of this standard cell library that contains multi-level information (e.g. layout information, behavioural models, FEM-models). He assembles the desired cells, and simulates them at system level. Then, the resulting assembly is handed over to a second set of tools, designed for chip level procedures. Once the final layout is produced, both the system level designer and the device level designer can intervene again to check the features of the resulting microsystem. The figure 1 shows the global CAD principle.

3. Tool adaptation and library development towards microsystem design environment

The work presented in this section targets mainly two axes: tool adaptations and library developments. In these directions, the following features have been made available:
• a continuous design flow achieved by the extension of the currently available IC design framework from Mentor, allowing:
- the layout generation of the whole microsystem (electronic and non-electronic parts) and a design rule verification. This is linked to the specific addressed technologies and can support both monolithic (one techology file) or hybrid (many technology files) solutions,
- layout generators for mechanical structures, such as bridges, cantilevers, membranes and application oriented structures, allowing the schematic driven layout feature,
- a parameter extraction tool from layout level to netlist level enabling post-layout back annotation which will consider the pakaging effect on the global system behaviour,
- full verification of the design functionality (ELDO / HDL-A),
- verification of the anisotropic etching procedure by the means of the anisotropic etching simulator, ACESIM, developed by CMP, and integrated within the Mentor environment,
- additional features, such as the cross-section viewer,
- a set of parametrized cells described at different levels (symbolic, system / behavioural, layout),

• device simulation capabilities enabling specific analyses for the component designer approach/needs (e. g. optic simulations),
• post-design verification, such as global electro-thermal

behaviour of the system.
The tools linked to the technology within the environment currently support the monolithic designs of microsystems. However, all the adaptation needed to address the hybrid solution are very close to be achieved. To understand the main difference between the design of monolithic and hybrid microsystems from the tools point of view, let's consider for example a hybrid microsystem composed of a microstructure manufactured on a production line A and the read-out or the drive electronics manufactured on a production line B. The design of this system does not differ from a monolithic one except at the layout level, since the multi-level, mixed-mode simulation is achieved by the means of a fully validated set of HDL-A behavioural library elements which are technology independent. These models are described by "grey boxes" having functional parameters as well as the technology parameters as inputs. However, when generating schematic driven layout, the structure generators must consider different technology files in only one session where for the monolithic systems or for microelectronics only one technology file is considered. In addition, when the structure and the electronic blocks are generated and routed simultaneously, a particular technology file is introduced related to the packaging and assembling of these two main blocks. When executing the design rules checking, the two blocks should be addressed respectively with their different corresponding rules, where the rules to assemble these blocks are mainly connectivity rules. An important point is the fact that when achieving the parameter extraction to insure the post layout simulation, the designer will be asked to specify the used packaging (flip chip, MCMs, etc.) to consider the related parameters (R, C, etc.).

3.1. MEMS Engineering Kit

The principles detailed above have been applied to extend the Mentor Framework to microsystem technology. The tool allows a continuous design flow enabling the generation of a schematic driven layout. It includes an extended schematic editor allowing the generation of an extended netlist, an extended DRC and an extended parameter extractor (from the layout level to netlist level) distinguishing electronic and non-electronic parts. An application oriented behavioural simulation can be achieved by the means of a comprehensive set of HDL-A microsystem library elements (pressure sensors, accelerometers, IR detectors, electro-thermal converters, ISFET, etc.). The schematic driven layout feature is achieved by the means of technology independent generators for structures, such as bridges, cantilevers, membrane or application oriented structures. Currently, both CMOS and GaAs compatible bulk micromachining technologies [Kar95, Kar96] are supported by the kit. The extension to other microsystem technologies is achieved on custom demand basis.

3.1.1. Extended Design Rules Checker

The design rules relative to microstructures have been elaborated in function of the results of the test structures manufactured through the CMP service, on the 1.0µ CMOS (from ATMEL-ES2 foundry), the 1.2µ CMOS (from AMS foundry) and the 0.2µ HEMT GaAs (from PML foundry) compatible bulk micromachining and have been implemented in the CAD environment. These design rules are imposed by the properties of the anisotropic etching. The rest of the design rules strictly concerning the conductive layers such as metal and polysilicon, has been kept unchanged for the simple reason that their electrical functionality is not altered even on suspended parts. Figure 2 shows a DRC example applied to a microsystem integrating microstructures as well as electronics.

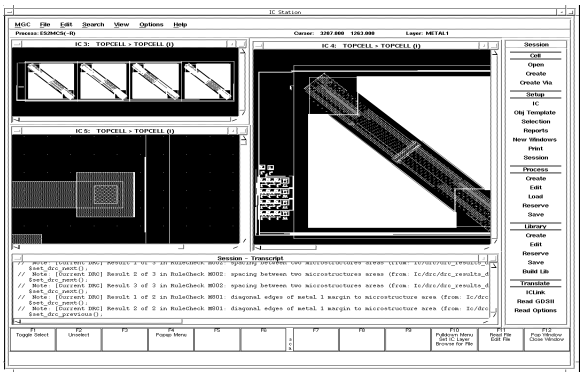

Fig. 2. Exemple of DRC execution: microsructure rules and electronic rules checked in the same time.

3.1.2. Parametrized Cell Library

A fully characterized set of HDL-A microsystem library elements has been developed. This library includes accelerometers (different types), temperature sensors, pressure sensors, IR detectors, electro-thermal converters, electro-thermo-pneumatic micro-pump, magnetic sensor (Hall effect) and gas flow sensor. Works towards new elements are in progress. These models are linked to technology independent structure generators insuring a schematic driven layout generation. Different kinds of generator exist for bridges, membranes, cantilevers and application oriented structures (fig. 3).

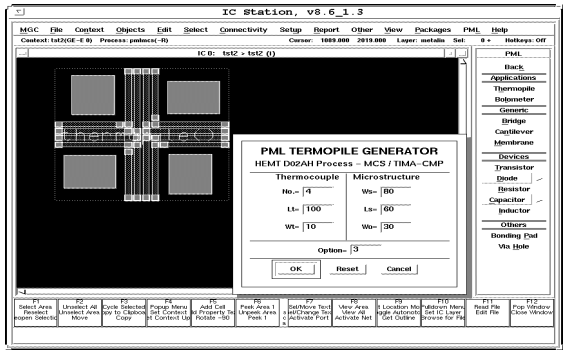

Fig. 3. Seebeck effect IR sensor structure generator

3.1.3. Cross-Section Viewer

Additional features, usefull for the microsystem engineers, have been added. One main function is the cross-section viewer allowing the visualization of the different layers according to a cut-line performed, in any direction, at the layout level. Figure 4 illustrates this function.

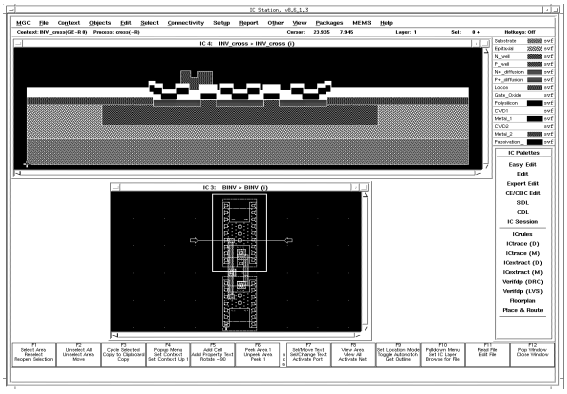

Fig. 4. The Cross-Section Viewer

3.2. Process level

Microsystems considered as an extension of microelectronics include all technological processes known from microelectronics, plus new processes which can in some cases be derived from microelectronics by adding post-processing steps. Among the new process steps, silicon bulk micromachining and surface micromachining are certainly the most important. More than fifty percent of all microsystems contain a device made by silicon bulk micromachining.

While the standard process steps (such as epitaxy, diffusion, etc.) can be modelled with existing tools like SUPREM IV the modelling of the new process steps introduced by the micromachining technologies is still not mature.

The ACESIM simulator developed at TIMA is based on a geometrical anisotropic etching model, in contrast with the complex atomistic models that require huge data space. The current version of this tool provides a two dimensional simulation. It has its main potential by the fact that it has been integrated within the Mentor MEMS Engineering Kit allowing an interactive design and dimensioning procedure of the microstructures considered as a post design rules checking operation. In addition, it's obvious that when targeting the monolithic solution where the structures are processed together with the electronics, one of the most important factors is the etching time necessary to liberate the suspended part, because the longer it is, the more the electronics parts can be damaged. This time mainly depends on the characteristics of the etchant, the shapes of the open areas constituting the microstructure and their relative positioning: these physical parameters determine the sequence of planes apparition within the silicon substrate, which is to be known in detail in order to predict the etching time.

Figure 5 shows an etching simulation performed by ACESIM within the Mentor MEMS Engineering kit. The etch rate diagram of EDP solution is also showed. It represents the etching speed of planes in mm /mn (indicated by graduations) as a function of their angle with the (100) plane.

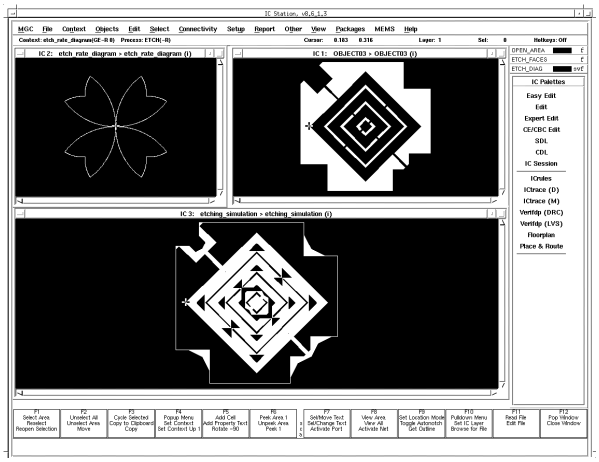

Fig. 5. Etching simulation performed by ACESIM within the Mentor Microsystem Engineering Kit. The etching diagram of EDP solution is also showed.

3.3. Device level

Device simulation is a key ingredient for the modelling of microsystems. Most existing simulation tools for microsystems concentrate on device simulations. They are mainly based on finite elements calculations and bond graph theory (especially for fluidic systems). The aim of a device simulation is to obtain the output characteristics of specific sensors as a function of the physical stimuli (pressure, temperature, humidity, magnetic field, etc.).

There are application fields which are not covered by the standard FEM simulations tools. A self consistent electro-thermal simulator, SISSSI, has been developed and extended to MST [Sze96]. SISSSI contains the following tools:

- μS-THERMANAL: an FFT-based, fast thermal simulation tool capable of performing thermal simulation of multilayered microelectronic and micromachined structures both for steady-state conditions and in frequency domain,
- THERMODEL: a dedicated tool which generates lumped element, compact thermal models of microelectronic or micromachined structures based on their frequency domain or time domain thermal response functions,
- TRANS-TRAN electro-thermal circuit simulation engine, which performs self-consistent electro-thermal simulation by means of the method of simultaneous iteration. This tool solves the coupled electrical and thermal problem described by an electro-thermal netlist. It provides steady-state, frequency domain and time domain solutions for the given electro-thermal simulation task.

The electrical netlist is extracted from the layout by conventinal means, while the thermal netlist extraction involves the following steps:

- the dissipating elements (MOS transistors) and the temperature sensitive elements (semiconductor devices, Si-Al contacts) are extracted and their layout is passed to the thermal simulator,
- by a set of thermal simulations the thermal behaviour of the chip is characterised (including its thermal environment, i.e. the encapsulation)
- based on the above thermal simulation results the compact thermal model generation tool (THERMODEL) generates the lumped element thermal model of the chip.

3.4. System level

Simulation of microsystems on the system level implies the simulation of the whole system and that of particular devices

with a special emphasis on certain properties or components. The difficulties that arise in this field are coming from the different signal abstractions (analog vs. digital) and the different underlying mathematics (algorithmic, algebrodifferential, partial differential equations). For all these domains there is a variety of tools that support modeling and simulation of a component, or to be more precise, the solution of a certain class of mathematical problem that is reflected by the model of the component. For heterogeneous systems with microsystems as an extreme example the problem of co-simulation of different mathematical based models on the system level exists. In principle, there are only two solutions to overcome this dilemma :

• interfacing two different simulators (e.g. analog/digital, structural (FEM) /behavioral etc.). This has the disadvantage of a very specialized software, problems with commercial software of different vendors and a long simulation time which is in general limited by the simulator handling the lower level of abstraction.

• model generation from the lower level of abstraction towards a system-simulation compatible hardware description language.

For different reasons we will focus on the latter choice :

• system simulation aims to identify structural lacks, i.e. problems arising from algorithms, choice of component parameters, software bugs etc. The different microsystem-components are needed on an accurate (but fast enough for efficient simulation) level in order to identify the lacks correctly. The problem of co-simulation of structural (FEM) models together with a hardware description language and software is that the model on the lowest level of abstraction very often determines the simulation time despite the fact that the simulation run does not intend to optimize this component.

• experiments and results from other projects show that interfacing commercial tools on a backplane requires excellent knowledge of the underlying software and creates a unwanted dependency on internal data-structures.

• very often the model on the lowest level of abstraction causes the most problems concerning stability and convergence.

We have to stress the fact that models that can be used for system simulation are far more complex than toy models that reflect only basic (linear) properties. Very often a realistic black-box view of a component is necessary for the design process of the adjacent modules or an estimation of system side-properties (heat flow, power consumption etc.).

The task of creating accurate models (including nonlinearities) had been focused in the past mainly by parameter extraction or parameter identification. This has the drawback that the nonlinearities must be known in order to identify them.

The developed tool allows the generation of accurate behavioral models in a analog hardware description language containing arbitrary nonlinearities which decouples the process of model creation from the understanding of the low level simulator. For space reasons we have to point to [Hof96] for a detailed description of the algorithms.

This CAD-tool will provide the following features :

• fixed interface for checking in Finite-Element-models to a CAD-library,

• check out of the FEM-models, alteration of the input stimuli and output-format according to the CAD-tools necessities, simulation of the FEM-models,

• supporting the reuse of already created behavioral models int the library, using the best-suited behavioral model as a beginning model,

• parameter-Optimization of the behavioral model (overcoming local minima),

• differential adaption of the behavioral model effects by comparing the waveforms of the FEM- and the behavioral model and concluding the insertion and deletion of certain (nonlinear) effects,

• support of model verification by using up to 10 different input stimuli,

• check in of the behavioral model in a format suitable to restart the model creation process,

• creation of a single HDL-A ARCHITECTURE/ENTITY-pair which is optimized with regard to the number of internal states needed for representing the specific model, and therefore optimized with regard to simulation speed.

The CAD-tool may be considered as a way of decoupling the creation of the behavioral model from the creation of the 2/3D-structural model. It is therefore a powerful tool for the usage within model-libraries containing components of different abstractions (e.g. structural<-> behavioral, transistor<->behavioral, pure-analog<->analog/digital). The application of this CAD-tool to several application-domains is currently in progress, but not yet finished.

4. Manufacturing

The experience gained by CMP since 1981 with integrated circuits has been recently used to develop a service for providing microsystems. CMP now supports micromachining technology to realize microsystems using the same principles applied to integrated circuits: to group projects together in order to fabricate them at a low cost [Kar 95].

There are two ways to manufacture microsystems : to develop processes specific to microsystems (hence these processes can address requirements specific to microsystems) or to use processes that have been developed for microelectronics. Among those later processes, some can be targeted to microsystems, again to address specific requirements, or it is possible to add special process steps to accomodate microsystems within integrated circuits. This later way will allow to collectively fabricate microsystems including the microelectronics part at a low-cost. This is the way addressed by the CMP Service and described in this paper [Kar95].

4.1. Silicon compatible micromachining

The fabrication of silicon compatible micromechanical structures involves the deposition, doping of the necessary material and the selective etching of the underlying support. Two main methods can be used; bulk micromachining where structures are etched in the substrate, and surface micromachining where the micromechanical layers are formed from layers deposited on the surface. Some advantages of these micromachining techniques include VLSI integration, low cost and rapid delivery.

Bulk micromachining is a process based on etching wells in the silicon substrate, leaving suspended structures. Two techniques can be used: etching from the front-side or etching from the back side.

Works at the CMP Service address mostly front-side bulk micromachining. In the back-side bulk micromachining the structures are usually large and alignment is difficult. If the bulk micromachining is performed from the front-side this alignment problem is immediately removed and dimensions can be reduced. The end result after CMOS fabrication is an open in the dioxide and nitride mixture passivation that exposes the bulk silicon surface (fig. 7). These chips are placed into an anisotropic etchant, such as EDP (ethylenediamine-pyrocathecol-water) or TMAH (tetramethylammonium hydroxide) or KOH (potassium hydroxide), and the exposed silicon is anisotropically etched.

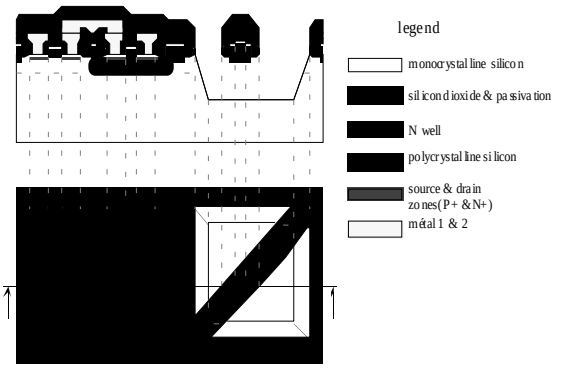

Fig. 7. Cross-sectional view of the microbridge with an inverter obtained by CMOS compatible front-side bulk micromachining

The 1.0µ CMOS (SLP / DLM, from ES2) compatible front-side bulk micromachining technique has been fully validated. Three Multi-Project-Wafer runs regrouping accelerometers, IR detectors, electro-thermal converters, micro-mirrors, pellestors, gas flow sensors, etc., has been manufactured for the first year. Figure 8 shows structures manufactured using this technology.

Another technology, the 1.2µ CMOS (DLP / DLM, from AMS) compatible front-side bulk micromachining technique has also been validated and characterized. This technology offers mixed electronics cell library requested by sensor and actuator interfaces. This technology is currently available through CMP.

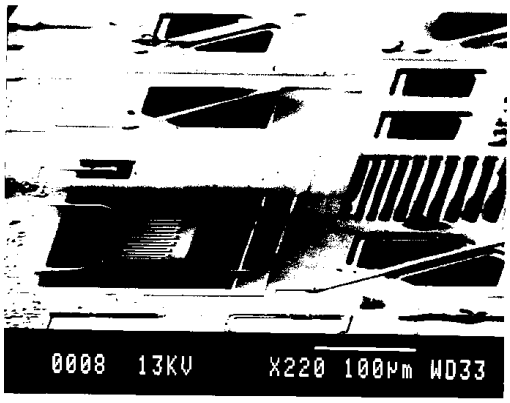

Fig. 8. SEM photograph of different structures fabricated monolithically with ICs using front-side CMOS bulk micromachining

4.2. Gallium arsenide micromachining

GaAs is for many people regarded as being too difficult and expensive for a sensor or actuator application. It is a fact that GaAs is not cheap in comparison with silicon and also cannot currently be produced with as high purity and few cristalline defects as Si. Therefore, it is preferable to use GaAs where and when one can take advantage of the good properties that it possesses. Possible applications could be where high-working temperature, high frequency, integrated optoelectronics or piezoelectricity are demanded.

As for silicon, Gallium arsenide based microsystems should be manufactured on industrial production lines, with an additional post-processing for microsystem specific structures [Kar96]. Thus, the CMP Service investigates micromachining techniques using the Philips Microwave Limeil (PML) HEMT (High Elecron Mobility Transistor) and the Vitesse MESFET (MEtal Schottky Field Effect Transistor) foundry processes. The results show that both processes can be used to implement front-side bulk micromachining. This can be achieved through an additional post-process etching without modifying the conventional IC fabrication procedure and with no influence on the electronic part behaviour (fig. 9). For that, both isotropic and anisotropic wet etching have been applied successfully, resulting in different structures in respect to the remaining bulk material.

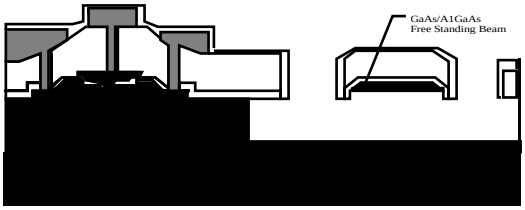

Fig. 9. Cross-sectional view of a free standing beam using a PML HEMT process

Fig. 10. Structure manufactured using 0.2µ GaAs HEMT compatible front-side bulk micromachining

5. Conclusions

In this paper, a general CAD structure for MEMS is described. Such a general structure based on a commercial IC design framework is the first to be offered to MEMS designers. Also CMP is the only service offering, in addition to the MEMS manufacturing facilities, CAD tools including design rules and anisotropic etching verification, parameter extraction, system level simulation, and schematic driven layout generation, allowing to design MEMS ready to go to fab, exactly as IC designers can design ICs ready to go to fab if they are provided with appropriate design kits bridging the CAD tools and the targeted foundry. It is expected that providing such facilities will help to massively move MEMS from research to commercial products.

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