

Cad of masks and wiring

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C.A.D. OF MASKS AND WIRING

by

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and

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INTRODUCTION

This report emanates from a seminar of the group EEC, held in spring 1972, and it reflects our knowledge in the field of automatic wiring design, built up during the first months of that year. At the second session the participants discussed the schematic overview of page 2. The framed subjects in this scheme were pointed out as topics of the sessions to follow. In the seminar the simultaneous "placement-and-routing"-part was emphasized, so that only the Lee-Akers-algorithm was presented (by Prof. Jess at the third session), since it was the most representative and general of all routing algorithms. A flaw was elicited during this session and a correction seemed to be difficult. Our ideas about this algorithm are more mature now and that is why the treatment of the subject is different in this report. Starting from a simple "minimum-distance" algorithm we generalize as far as possible ending up with an abstract model.

Next in this report we have a short introduction to notions in graph theory, although this was a subject of the fourth session. This reordering was necessary, because of the final description of routing algorithms and problem formulations in which some of the notions are employed.

The mathematical formulation is published as an article in the "International Journal of Circuit Theory and Applications"^{*}. The fourth and the fifth constraint were presented in the formulation for the whirl problem, but the solutions given during the session were basically wrong. We added some directives for technological modifications.

Four planarity tests were given then

1. CEL-algorithm: preceded by the treatment of "drain functions" and "deltas and their formulas";
2. pseudo-hamiltonian method;
3. methods using matrices;
4. whirl method.

The last session was concerned with planarization of networks. It concludes also this report.

^{*}M.C.van Lier, R.H.J.M. Otten, "On the mathematical formulation of the wiring problem ", Int.Journ. of Circuit Theory and Applications, Vol.1,137-147, March, 1973.

WIRING-PROBLEM

separate placement and routing

simultaneous placement and path-routing

off-line

on-line

ACCEL (Automated Circuit Card etching layout)
 1. placement-algorithm, using a concept of forces;
 2. routing by a mixture of the LEE-AKERS-algorithm and a topographic simulation.

CADIC (Computer-Aided Design of Integrated Circuits) with a graphical display; placement by hand and routing with the LEE-algorithm.

construction of the potential-graph from the circuit with or without certain constraints

planarity-test on the total graph

planarity-test by checking the planarity of certain subgraphs

matrix
DAMBIT
DUNN & CHAN

constructive
WEINBERG

denumeration
CEDERBAUM
EVEN
LEMPER

elementary
windows
YOSHIDA & OHTA

cut-sets
CHUNG & ROE

circuits and bridges
AUSLANDER & PARTER
DEMOUCRON
BADER
FISHER & WING
HOTZ

modifications

Planar drawing taking the dimensions into account

I. GRAPH-THEORETICAL NOTIONS

We start from a non-empty set G , the so-called set of vertices. On this set we define a binary relation: $\Gamma \subseteq G \times G$. The elements of Γ are called arcs. Our notation of an arc will be $[x,y>$ with x and y as terminal-vertices. In the following the set of arcs will be designated by V .

The pair consisting of G and V is called a digraph, and is denoted by (G,V) . We assume the relation Γ to be antireflexive (this means $[x,x> \notin \Gamma$). A digraph is finite, when G is finite. We will restrict ourselves to finite digraphs. If the relation Γ is symmetric ($[x,y> \in \Gamma \leftrightarrow [y,x> \in \Gamma$), we speak of a graph, here denoted by (G,U) with $U = \{[x,y] \mid [x,y> \in \Gamma\}$. U is a set of non-ordered pairs of vertices, called edges. We speak of a multigraph, when U is a family.

The relation Γ can be treated as any other binary relation:

We write $y \in \Gamma(x)$, when $[x,y> \in \Gamma$.

The inverse of Γ is denoted by Γ^{-1} , and is defined by $\Gamma^{-1}(y) = \{x \mid y \in \Gamma(x)\}$.

We define the powers of Γ in the following way:

$$\Gamma^0(x) = \{x\}$$

$$\Gamma^1(x) = \Gamma(x)$$

$$\Gamma^i(x) = \Gamma(\Gamma^{i-1}(x)) \quad (i \text{ is a non-negative integer})$$

$$\Gamma^{-i}(x) = (\Gamma^{-1})^i(x)$$

The transitive closure $\hat{\Gamma}$ of Γ is defined by $\hat{\Gamma}(x) = \{x\} \cup \Gamma(x) \cup \Gamma^2(x) \cup \Gamma^3(x) \dots$

For digraphs we have also the following notions:

$|\Gamma(x)|$ is called the out-degree of x and is denoted by $\gamma^+(x)$.

$|\Gamma^{-1}(x)|$ is called the in-degree of x and is denoted by $\gamma^-(x)$.

$\gamma(x) = \gamma^+(x) + \gamma^-(x)$ is the degree of x .

$x \in G$ is a source, when $\Gamma^{-1}(x) = \emptyset$ or equivalently $\gamma^-(x) = 0$

$x \in G$ is a sink, when $\Gamma(x) = \emptyset$ or equivalently $\gamma^+(x) = 0$

For graphs we have only the degree of $x \in G$: $\gamma(x) = |\{y \mid [x,y] \in U\}|$.

Suppose we have two digraphs (G_1, V_1) and (G_2, V_2) , and a bijective mapping ϕ from G_1 into G_2 . Then ϕ is called an isomorphic mapping (or an isomorphism), if

$$[x,y> \in V_1 \leftrightarrow [\phi(x), \phi(y)> \in V_2.$$

If such a mapping exists, then (G_1, V_1) and (G_2, V_2) are called isomorphic. For graphs we have a similar definition.

A graph (G, U) is called topological if:

1. G is a set of points in a topological space R , and U is a set of open Jordancurves in R ,
2. the terminalpoints of an edge of U are in G ,
3. the edges of U have no other points in common than terminalpoints.

In the case of digraphs we give the Jordancurve $[x, y]$ an orientation in the direction of y .

(G', U') is a topological representation of (G, U) , if (G, U) and (G', U') are isomorphic and (G', U') is a topological graph.

A graph is called planar, when it has a topological representation in a plane.

The graph (G', U') is a subgraph of (G, U) , when $G' \subset G$ and $\forall_{u \in U'} [u \in U]$.

The name chain is given to a sequence v_1, v_2, \dots, v_k of arcs of (G, V) such that, if $v_i = [x_i, y_i]$, then $y_i = x_{i+1}$ for $i = 1, 2, \dots, k-1$. A chain is simple, if no arc occurs twice in the sequence. It is called elementary, if it does not contain a vertex twice. We denote a chain by $C[x_1, y_k]$.

A cycle is a chain in which $x_1 = y_k$. A cycle is elementary if, apart from x_1 and y_k , every vertex in it is distinct from the others.

A digraph is called acyclic, when it has no cycles. The length of a chain is the number of its arcs.

A path is a sequence u_1, u_2, \dots, u_k of edges of a graph (G, U) in which we have with $u_i = [x_i, y_i]$, that $y_i = x_{i+1}$ and $y_{i-1} = x_i$ for $i = 2, 3, \dots, k-1$. A path is simple, when all its edges are different, and elementary, when every vertex in it appears only once. A path is denoted by $P[x_1, y_k]$. A circuit is a path with $x_1 = y_k$, and it is called elementary, when all its vertices x_1, x_2, \dots, x_k are distinct.

A graph (G,U) is connected, if for every pair of vertices in G there is a path between them. A component of (G,U) is a maximal connected subgraph of (G,U) . A vertex x of G is an articulation point of (G,U) , if the number of components of the subgraph obtained by deleting x and all the edges incident to x is one higher than in (G,U) .

T h e o r e m 1: A vertex a is an articulation point of a connected graph, if and only if there exist two vertices x and y such that every path joining x and y contains a . ($x \neq a \neq y$).

The proof of this theorem is trivial.

A graph (G,U) is said to be biconnected, if it is connected, and it contains more than one edge and no points of articulation.

T h e o r e m 2: Given any elementary path $P[a_0, a_1, \dots, a_k]$ joining two distinct vertices a_0 and a_k of a biconnected graph (G,U) , we can associate with it two elementary paths P' and P'' such that:

1. P' and P'' join both a_0 and a_k ,
2. a_0 and a_k are the only vertices which P' and P'' have in common,
3. if P' or P'' is followed from a_0 to a_k , the indices of the vertices of P encountered on route are in increasing order.

Proof: The theorem is trivially true, when P has length 1 ($P = [a_0, a_1]$), for U contains at least two edges, and neither a_0 nor a_1 can be an articulation point.

Let us assume the theorem to be true for all elementary paths of length k , and deduce from this that it is also true for the elementary path

$$P[a_0, a_{k+1}] = [a_0, a_1, \dots, a_k, a_{k+1}].$$

By hypothesis there exist two disjoint paths P'_0 and P''_0 joining a_0 and a_k , and satisfying the conditions of the theorem. We now have to show the existence of two paths P' and P'' between a_0 and a_{k+1} with analogous properties.

From theorem 1 we know that there is a path $Q[a_0, a_{k+1}]$, which does not contain a_k . Let us denote by q the vertex of $Q[a_0, a_{k+1}]$ nearest to a_{k+1} , and which is also in $P[a_0, a_k]$ or $P'_0[a_0, a_k]$ or $P''_0[a_0, a_k]$.

We distinguish four cases:

I. $q = a_0$:

This case is simple: $P'[a_0, a_{k+1}] = P[a_0, a_{k+1}]$

$$P''[a_0, a_{k+1}] = Q[a_0, a_{k+1}]$$

II. $q = a_{k+1}$:

This means that $q \notin P[a_0, a_k]$. This leaves two analogous cases:

$q \in P'_0[a_0, a_k]$ or $q \in P''_0[a_0, a_k]$. Take for example $q \in P'_0[a_0, a_k]$, then

$$P'[a_0, a_{k+1}] = P'_0[a_0, q]$$

$$P''[a_0, a_{k+1}] = P''_0[a_0, a_k] + [a_k, a_{k+1}]$$

III. $q \notin P[a_0, a_{k+1}]$:

This means that either $q \in P'_0[a_0, a_k]$ or $q \in P''_0[a_0, a_k]$. In the latter case (the former is analogous), we take

$$P'[a_0, a_{k+1}] = P'_0[a_0, a_k] + [a_k, a_{k+1}]$$

$$P''[a_0, a_{k+1}] = P''_0[a_0, q] + Q[q, a_{k+1}]$$

IV. $q \in P[a_1, a_k]$:

Then we can write $q = a_m$ with $m < k$. Let p be the highest index with $a_p \in P[a_0, a_{k+1}]$, $a_p \in P''_0[a_0, a_{k+1}]$ ($a_p \in P'_0[a_0, a_k]$ is analogous) and $p < m$.

In such a case we take

$$P'[a_0, a_{k+1}] = P'_0[a_0, a_k] + [a_k, a_{k+1}]$$

$$P''[a_0, a_{k+1}] = P''_0[a_0, a_p] + P[a_p, a_m] + Q[a_m, a_{k+1}]$$

Theorem 3: Given two arbitrary edges u_1 and u_2 of a connected graph, we can construct an elementary path, which starts with u_1 and finishes with u_2 .

Proof: If $u_1 = [a, x]$ and $u_2 = [b, y]$, then since the graph is connected, the vertices a and b can be joined by an elementary path $P[a, b] = [a, a_1, a_2, \dots, a_k = b]$.

Again four cases (the required path is denoted by P_0):

I. $x \notin P[a, b], y \notin P[a, b]$:

$$P_0 = [x, a] + P[a, b] + [b, y]$$

II. $x \notin P[a, b], y \in P[a, b]$:

$$P_0 = [x, a] + P[a, y] + [y, b]$$

III. $x \in P[a, b], y \notin P[a, b]$:

$$P_0 = [a, x] + P[x, b] + [b, y]$$

IV. $x \in P[a, b], y \in P[a, b]$:

$$P_0 = [a, x] + P[x, y] + [y, b]$$

Theorem 4: Given two arbitrary edges u_1 and u_2 of a biconnected graph, an elementary circuit exists which contains u_1 and u_2 both.

Proof: $P[a_0, a_k]$ is an elementary path with $u_1 = [a_0, a_1]$ and $u_2 = [a_{k-1}, a_k]$. Such a path exists, as is said by theorem 3. From theorem 2 we know that in such a case there exist two disjoint paths $P'[a_0, a_k]$ and $P''[a_0, a_k]$ with the properties advertised there.

Let us denote by p the first vertex of $P[a_0, a_k]$ after a_0 , which is also in $P'[a_0, a_k]$ or in $P''[a_0, a_k]$ and by q the last vertex before a_k with the same properties.

We have three cases this time:

I. $p = a_k$:

Necessarily $q = a_0$ then. The required circuit is

$$P[a_0, a_k] + P'[a_k, a_0]$$

II. $p \neq a_k$ and thus $q \neq a_0$; further $p \in P'[a_0, a_k]$ and $q \in P'[a_0, a_k]$.
 (The case $p \in P''[a_0, a_k]$ and $q \in P''[a_0, a_k]$ is analogous). Now we take

$$P[a_0, p] + P'[p, q] + P[q, a_k] + P''[a_k, a_0]$$

III. Again $p \neq a_k$ and $q \neq a_0$, but now $p \in P''[a_0, a_k]$ and $q \in P''[a_0, a_k]$.
 (The case $p \in P'[a_0, a_k]$ and $q \in P'[a_0, a_k]$ is analogous).

$$P[a_0, p] + P'[p, a_k] + P[a_k, q] + P''[q, a_0]$$

We have a biconnected graph (G, U) . Let H be a subset with $|H| \geq 2$. We suppose that (G, U) has the following property:

(G, U) has a topological representation (G', U') in a plane such that H is completely contained in a circuit C' that (of course) divides the rest of the plane into two connected open domains and one of these domains contains no edge of U' .

Such a graph is called H -accessible and the representation (G', U') is called an H -periphery representation. Two elements h_1 and h_2 of H are said to be G' -adjacent, if there is a path $P[h'_1, h'_2]$ between h'_1 and h'_2 which is on the periphery C' of (G', U') and which contains no vertex of $H \setminus \{h'_1, h'_2\}$.

Theorem 5: If (G', U') and (G'', U'') are both H -periphery representations of an H -accessible graph (G, U) , then every G' -adjacent pair is also a G'' -adjacent pair.

Proof: If $|H| \leq 3$, then there is nothing to prove. Thus, suppose $|H| > 3$ and that h_1 and h_2 (both elements of H) are G' -adjacent and not G'' -adjacent. This means that there is a path $P'[h'_1, h'_2]$ on C' in which no element of $H \setminus \{h'_1, h'_2\}$ appears. $P''[h''_1, h''_2]$ is the corresponding path in (G'', U'') and this path contains at least one edge which is not on C'' .

Let $P''_a[h''_1, h''_2]$ and $P''_b[h''_1, h''_2]$ be two disjoint paths, together covering the whole C'' . On $P''_a[h''_1, h''_2]$ there must be an h''_a not equal to h''_1 or h''_2 . On $P''_b[h''_1, h''_2]$ there must be an h''_b , which is also unequal to h''_1 or h''_2 . From the Jordancurves-theorem we know that there is no path from h''_a to h''_b not containing a vertex of $P''[h''_1, h''_2]$ in (G'', U'') . In (G', U') however, there is clearly a path from h'_a to h'_b which contains no vertex of $P'[h'_1, h'_2]$. This is a contradiction.

REFERENCES

- [1] C.Berge, "Théorie des graphes et ses applications", Paris, Dunod, 1966.

II. ROUTING ALGORITHMS

1. SIMPLE CONNECTION ALGORITHM ON A GRID

Consider two sets of natural numbers: $R = \{n | n \in \mathbb{N} \wedge (0 < n \leq r)\}$

$K = \{n | n \in \mathbb{N} \wedge (0 < n \leq k)\}$

We define the set C as being $R \times K$ and we call its elements "cells". On this set we define a relation $\eta \subset C \times C$ in the following way:

$$\forall_{c_i \in C} \forall_{c_j \in C} [(c_i, c_j) \in \eta \leftrightarrow (|r_i - r_j| + |k_i - k_j| = 1)]$$

where $c_i = (r_i, k_i)$ and $c_j = (r_j, k_j)$. By $c_i \eta$ we mean $\{c | (c_i, c) \in \eta\}$. Clearly, η is symmetric, and it is easy to see that

$$\forall_{c_i \in C} [2 \leq |c_i \eta| \leq 4]$$

At the initialization of the so-called "connection"-procedure, we suppose that C is partitioned into two subsets A and B. A is called the set of admissible cells, while B consists of these cells which are "prohibited". Further two elements of A are pointed out: one as being the origin c^* , the other as the target c^{**} .

The procedure is a search routine followed by a trace-routine: in the first routine we split A in three sets: P, Q and $A \setminus (P \cup Q)$; in the second step we select a sequence S of elements of P and Q which are added to B. This sequence is called "the shortest path from c^* to c^{**} ".

The procedure is built in such a way that

1. $S \subset A$
2. $S = (c_1, c_2, \dots, c_m) \rightarrow (c_1 = c^* \wedge c_m = c^{**} \wedge \forall_{c_i \in S} [(c_i, c_{i+1}) \in \eta])$
3. For every sequence S' that satisfies 1. and 2., we have $|S'| \geq |S|$

We must emphasize that the solution need not be unique. In the blocks marked by an asterisk the determination of the new \bar{c} may give some difficulties. We can meet here two situations:

1. $|P \cap \bar{c} \eta| = 1$
 $|Q \cap \bar{c} \eta| = 1$: the procedure can proceed in a unique way.
2. $|P \cap \bar{c} \eta| \geq 2$
 $|Q \cap \bar{c} \eta| \geq 2$: the procedure needs a rule to decide which cell will be the next \bar{c} .

For the missing rule in the second case one may take the following one:
 if possible, do not change the coordinate that was changed in the preceding step;

if possible, make the coordinate that must be changed as low as possible.

The procedure gets stuck in the block marked by two asterisks when this set is empty: this means that no solution exists. (Fig.2.)

As an application of the described procedure we consider the rectangular grid of fig. 1a. The cells are here the little squares of the grid determined by the coordinates at the top and at the left side. The cells belonging to B are shaded.

Let the origin be (1,6) and the target (7,5).

After the first part of the procedure the partition gives the result as given in fig. 1b. The set P consists of the cells containing the character "p" and the set Q is the set of all cells containing the "q".

During the "trace-routine", the second step, we meet only the situation $|P \cap \bar{c} \cap n| = 1$ or $|Q \cap \bar{c} \cap n| = 1$, and thus, the solution is unique.

However, when we choose (1,3) instead of (1,6) as the origin, a rule like the one given above is necessary to obtain a unique solution. The results are depicted in fig. 1c.

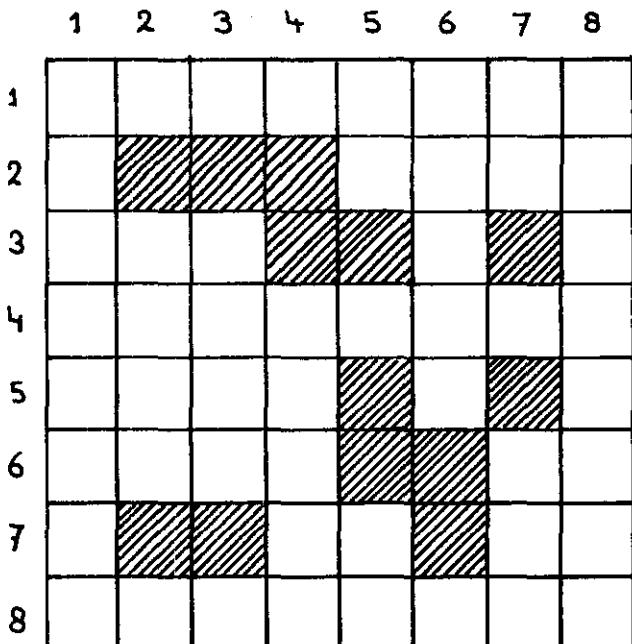


fig. 1a

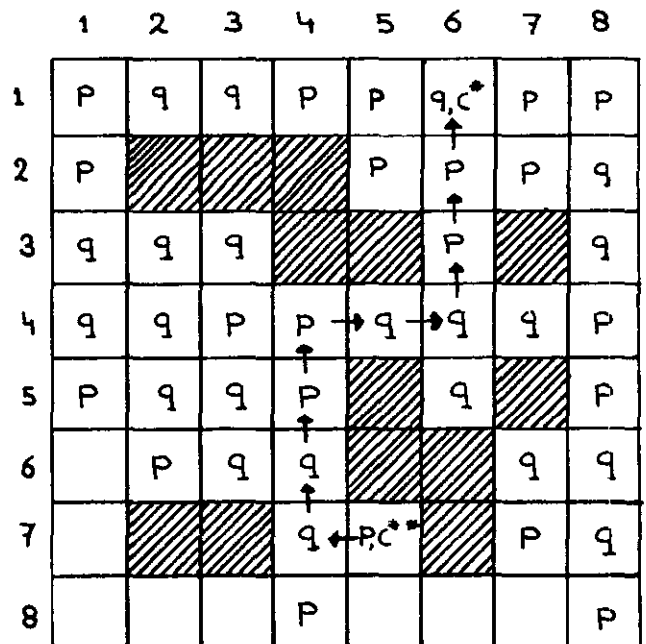


fig 1b

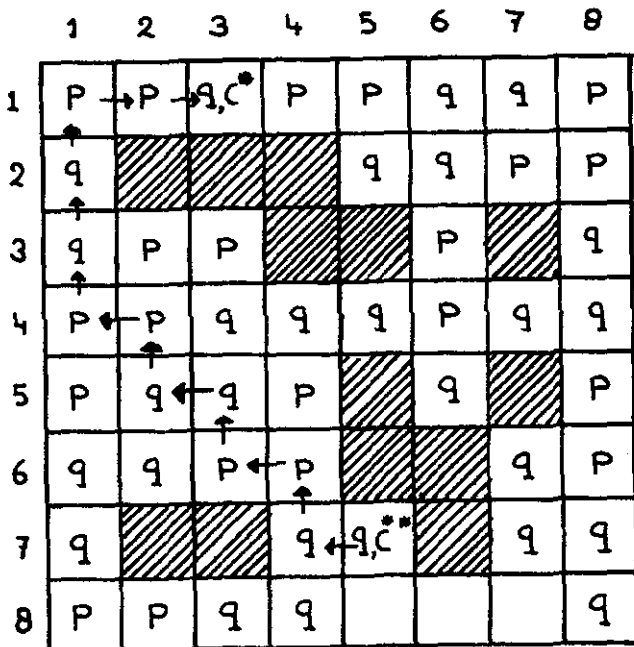


fig. 1^c

Fig.1: Example of a routing algorithm on a grid.

2. SIMPLE CONNECTION ALGORITHM ON A GRAPH

The connection algorithm on a graph has a more general nature and the procedure described in the preceding section, must be modified. The main principle, however, is still the same.

The set C is now equal to the set of vertices G, while the relation η is now the same as the relation Γ . Again, C is partitioned into two sets A and B, and an origin and a target are pointed out.

However, the first step splits A in four sets: P, Q, R and $A \setminus (P \cup Q \cup R)$.

Again, the blocks marked by an asterisk make uniqueness uncertain. One has to add a "decision-rule" to eliminate this flaw, e.g. when the vertices are labeled with different integers one may demand that the vertex with the lowest label of all possible vertices is taken. But when the labels were not assigned in a special way, this will be an arbitrary choice.

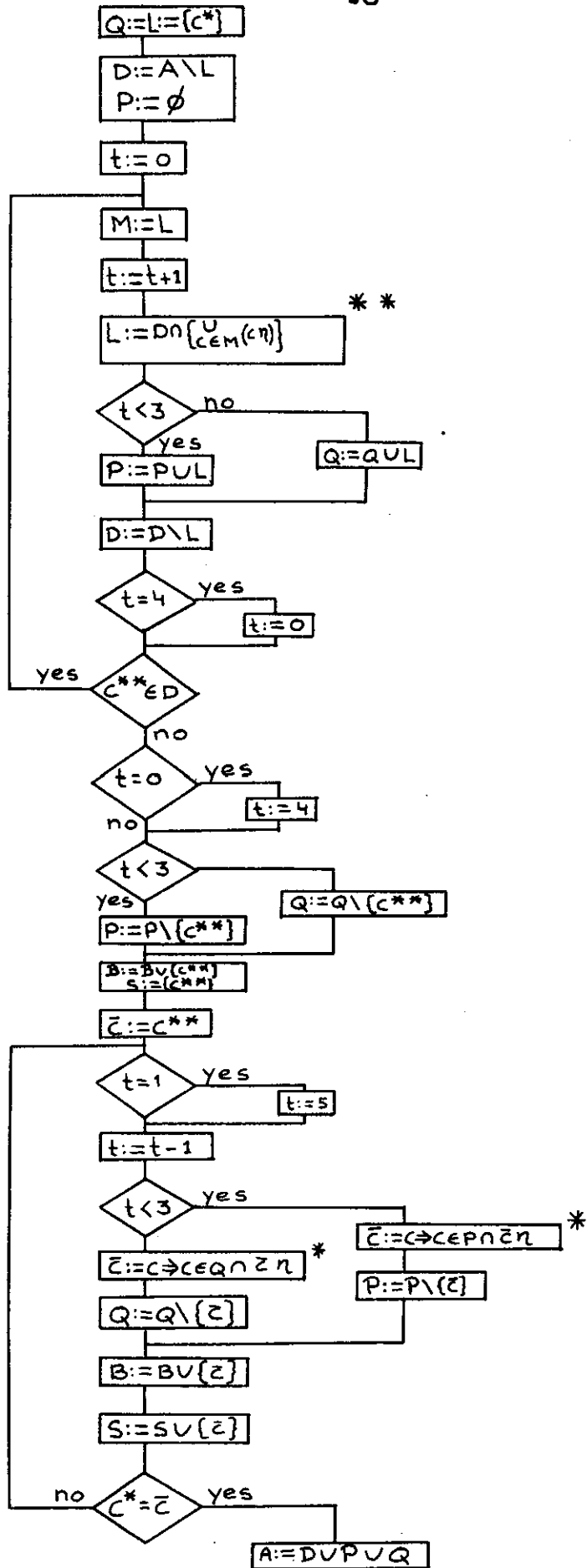


Fig.2

Connection procedure for the grid problem

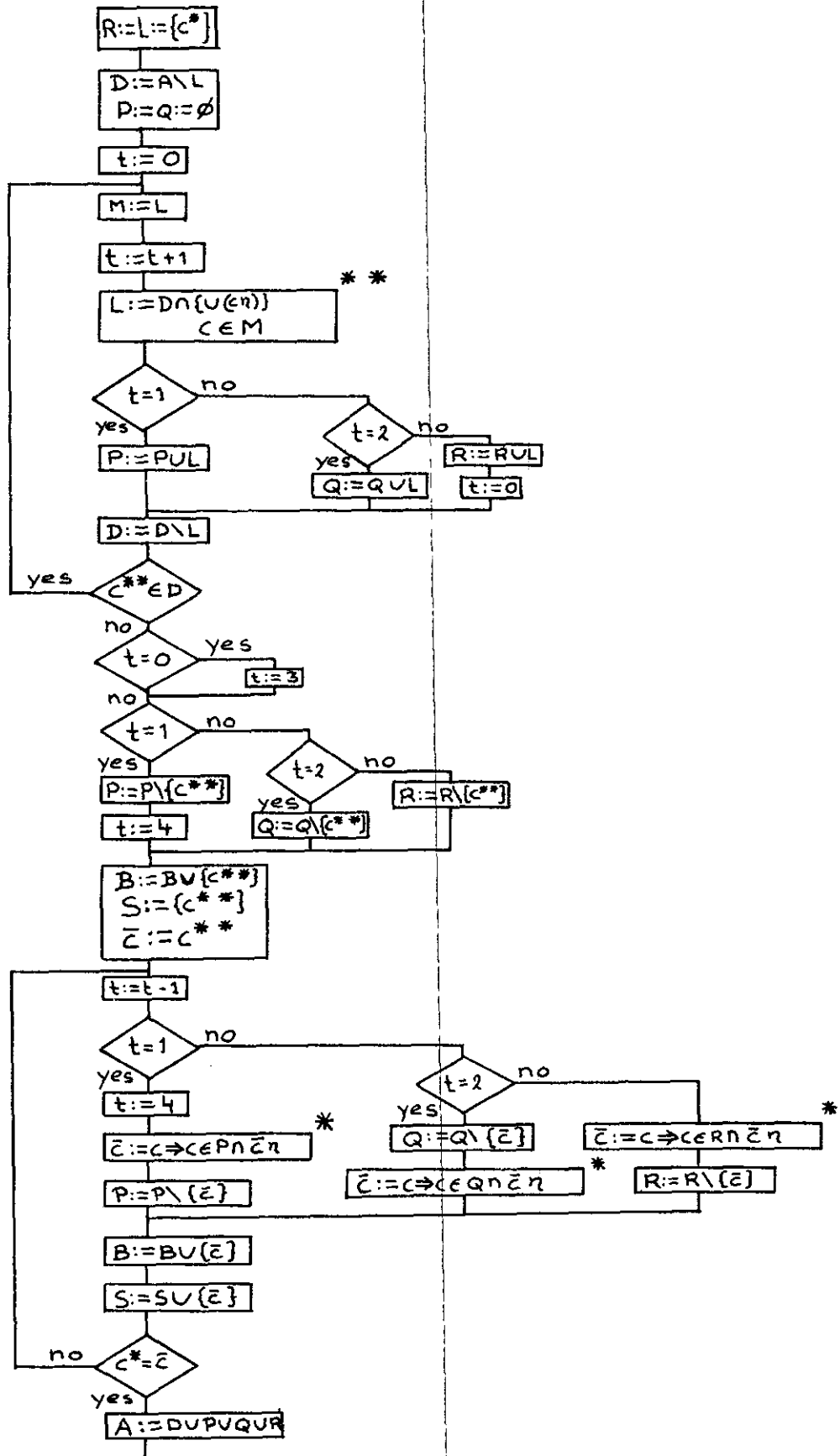


Fig. 3

Connection procedure for the graph problem

3. SIMPLE MULTILAYER CONNECTION ALGORITHM

In the preceding section we generalized the algorithm of section 1 by admitting an arbitrary relation η . In this section we want to generalize not on the relation η , but on the number of "layers". Every layer has the same "grid structure". In every layer we have a partition of C into two sets: for layer i f.e. A_i and B_i . Again, we have in C an origin and a target. The procedure consists also of a search routine and a trace routine. In the first one C is partitioned into four sets P , Q , R and T and in the second part the sequence S is selected where $S \subset C \times L$ (L is the set of "layers", $|L| = \ell$).

In the description of the algorithm the following arrays are used to store the sets:

$F[1:r, 1:k, 1:\ell]$ is an array which is not changed during the connection procedure. It is only changed after such a procedure to add the cells of S to the proper B_i 's. During the procedure the array F is as follows:

$$F[i, j, h] = \chi_{A_h}((i, j)) \quad d w z \quad \begin{aligned} F[i, j, h] = 1 &\leftrightarrow (i, j) \in A_h \\ F[i, j, h] = 0 &\leftrightarrow (i, j) \in B_h \end{aligned}$$

The array $E[1:r, 1:k]$ keeps track of the partition of C into P , Q , R and T

$$\begin{aligned} E[i, j] = 0 &\leftrightarrow (i, j) \in T \\ E[i, j] = 1 &\leftrightarrow (i, j) \in P \\ E[i, j] = 2 &\leftrightarrow (i, j) \in Q \\ E[i, j] = 3 &\leftrightarrow (i, j) \in R \end{aligned}$$

At the initialization of the procedure all cells are in T and thus all $E[i, j]$ are zero.

t is an variable, which can take the values 1, 2 and 3.

$$\begin{aligned} \text{Further we have two "projection" functions: } \pi_1(c) = i &\leftrightarrow \exists_{j \in K} [c = (i, j)] \\ \pi_2(c) = j &\leftrightarrow \exists_{i \in R} [c = (i, j)] \end{aligned}$$

The search procedure can be described as follows:

$$\text{Step 1: } D := \{c^*\}, E[\pi_1(c^*), \pi_2(c^*)] := 3; t := 3$$

$$\text{Step 2: } t := t+1 \pmod{3}$$

$$\text{Step 3: } DD := \bigcup_{c \in D} \{c\eta\}$$

Step 4: For every c in the set DD we determine whether $E[\pi_1(c), \pi_2(c)] = 0$ and whether there is an h such that

$$F[\pi_1(c), \pi_2(c), h] = 1 \wedge \exists_{c' \in c\eta} [F[\pi_1(c'), \pi_2(c'), h] = 1 \wedge E[\pi_1(c'), \pi_2(c')] \neq 0]$$

If both conditions are satisfied, then $E[\pi_1(c), \pi_2(c)] := t$
else $DD := DD \setminus \{c\}$

Step 5: $D := DD$

Step 6: If $c^{**} \in D$ then the search routine is completed, else go back to step 2.

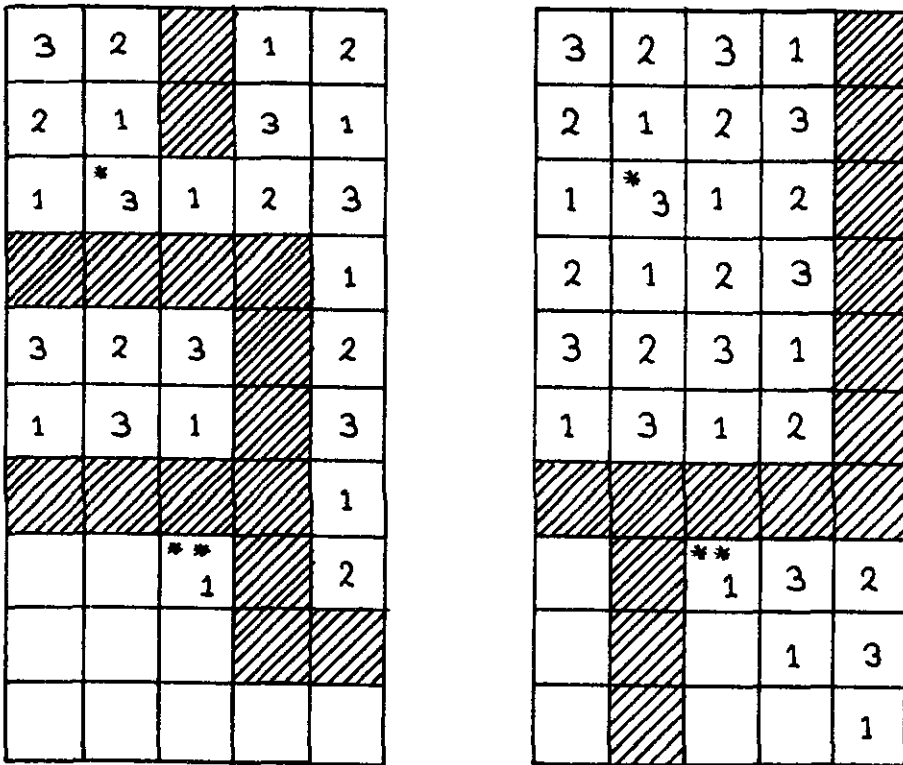
After the search routine we have some data for the trace routine available, i.e. t , F and E . With these data we can determine the sequence S , but in general this sequence will not be uniquely determined, so that additional decision rules have to be applied.

An example of this procedure is given in fig. 4.

The array E does not supply all the information necessary for the trace routine. Suppose we have reached cell c and $E[\pi_1(c), \pi_2(c)] = t$.

The next cell c' must be chosen such that

1. $c' \in c\eta$
2. $E[\pi_1(c'), \pi_2(c')] = t - 1 \pmod{3}$
3. $\exists_{h \in L} [F[\pi_1(c), \pi_2(c), h] = 1 \wedge F[\pi_1(c'), \pi_2(c'), h] = 1]$



	1			2			3			4			5		
	F ₁	F ₂	E	F ₁	F ₂	E	F ₁	F ₂	E	F ₁	F ₂	E	F ₁	F ₂	E
1	1	1	3	1	1	2	0	1	3	1	1	1	1	0	2
2	1	1	2	1	1	1	0	1	2	1	1	3	1	0	1
3	1	1	1	1	1	0	1	1	1	1	1	2	1	0	3
4	0	1	2	0	1	1	0	1	2	0	1	3	1	0	1
5	1	1	3	1	1	2	1	1	3	0	1	1	1	0	2
6	1	1	1	1	1	3	1	1	1	0	1	2	1	0	3
7	0	0		0	0		0	0		0	0		1	0	1
8	1	1		1	0		1	1	1	0	1	3	1	1	2
9	1	1		1	0		1	1		0	1	1	0	1	3
10	1	1		1	0		1	1		1	1		1	1	1

Fig.4: Example of a multilayer problem.

4. GENERALIZATIONS

In the two preceding sections we have generalized the procedure of section 1 in two different ways. In section 2 the η -relation became unrestricted (except for finiteness, of course); in section 3 we introduced a multilayer procedure. Another possibility is to allow for a more complex optimality criterion. The criterion was up to now "the shortest path between the origin and the target", where "shortest" meant: "passing through a minimum number of cells". One could solve the problem also by assigning "cell masses" instead of partitioning into sets P, Q, (R) and D. The "cell mass" of c is in such a case the smallest number of cells one has to pass through before reaching c started in c^* . By allowing a more "general cell mass" one may think to have improved the procedure greatly. One can take for example as a "cell mass" a weighed sum of penalties:

$$f(c) = \sum_{i=1}^n \alpha_i f_i(c)$$

$f_i(c)$ are the penalty functions, f.e. the number of cells one has to pass through to reach c from c^* , the number of crossings one has met, etc.. Two complications are then introduced. Firstly, our strategy has to be changed (one must assign "cell masses" only to those cells that obtain the lowest possible mass, which means that one has to remember all neighbour cells which didn't get a mass) and secondly, the penalty function has to satisfy special conditions (the minimum corner problem is not solvable by this algorithm). We will give the description of the algorithm, and then these difficulties will be apparent.

The model

- b b is a symbol, the so-called prohibition symbol
- R_+ R_+ is the set of non-negative real numbers
- C C is a finite set of "cells"
- S' S' is a finite set, the so-called cell alphabet
 $C \cap S' = \emptyset$
 $b \in S'$
- S $S = S' \setminus \{b\}$
- η $\eta \subset C \times C \wedge \forall_{c \in C} \forall_{c' \in C} [(c, c') \in \eta \wedge ((c, c') \in \eta \leftrightarrow (c', c) \in \eta)]$
 η is called the neighbour relation
- σ $\sigma \subset C \times S' \wedge \forall_{c \in C} \exists!_{s \in S'} [(c, s) \in \sigma]$
 σ is called the labeling relation
- μ $\mu \subset R_+ \times S \times R_+$
 $\forall_{(n, s) \in R_+ \times S} \exists!_{m \in R_+} [(n, s, m) \in \mu]$
 $\forall_{n \in R_+} \forall_{s \in S} \forall_{m \in R_+} [(n, s, m) \in \mu \rightarrow n \leq m]$
 $\forall_{n \in R_+} \forall_{n' \in R_+} \forall_{s \in S} [n \leq n' \rightarrow (n, s) \mu \leq (n', s) \mu]$
 μ is called the weighing relation

Auxiliary entities

- A $A \subset C \wedge \forall_{c \in C} [c \in A \leftrightarrow (c, b) \notin \sigma]$
A is the set of admissible cells
- P^* $P^* = \{(c_1, c_2, \dots, c_n) \mid (c_1, c_2, \dots, c_n) \in \bigcup_{i=1}^{|C|} A^i \wedge$
 $\wedge \forall_{1 \leq i < n} [(c_i, c_{i+1}) \in \eta \wedge \forall_{i < j \leq n} [i \neq j \leftrightarrow c_i \neq c_j]]\}$
- P^* is the set of paths
- δ $\delta \subset P^* \times R_+$
 $\forall_{c \in A} \forall_{n \in R_+} [(c, n) \in \delta \rightarrow n = 0]$
 $\forall_{(c_1, c_2, \dots, c_n) \in P^*} [(c_1, c_2, \dots, c_n), m) \in \delta \leftrightarrow ((c_1, c_2, \dots, c_{n-1}) \delta, c_n \sigma, m) \in \mu]$
 δ is called the cellmass relation
- $P_c^{c'}$ $P_c^{c'} = \{(c_1, c_2, \dots, c_n) \mid (c_1, c_2, \dots, c_n) \in P^* \wedge c_1 = c \wedge c_n = c'\}$
- τ $\tau \subset A \times P^* \times P^*$
 $(p \in P^* \wedge p = (c_1, c_2, \dots, c_n) \wedge c \notin p \wedge c \in c_1 \eta) \rightarrow (c, p) \tau = (c, c_1, c_2, \dots, c_n)$

The problem

Find a path p such that:

$$p \in P_c^{c^{**}} \wedge \forall p' \in P_c^{c^{**}} [((p, m_0) \in \delta \wedge (p', m) \in \delta) \rightarrow m_0 \leq m]$$

The algorithm

1. $L := \{c^*\}, L' := L'' := I := \emptyset, f(c^*) := \mathcal{L}(c^*) := 0, \forall c \in C \setminus \{c^*\} [f(c) := \mathcal{L}(c) := \infty], \mathcal{L} := 0$
2. $I := \emptyset, \mathcal{L} := \mathcal{L} + 1$
3. $\forall_{c \in L} [\forall_{c' \in c\eta \cap A} [f(c') = \infty \rightarrow (c' \in L' \wedge (f(c), c'\sigma)\mu \in I)]]$
4. $m_0 := \rightarrow (m_0 \in I \wedge \neg \exists_{m \in I} [m < m_0])$
5. $\forall_{c \in L'} [\exists_{c' \in c\eta \cap L} [(f(c'), c\sigma, m_0) \in \mu] \rightarrow (f(c) := m_0 \wedge c \in L'' \wedge \mathcal{L}(c) := \mathcal{L})]$
6. $L := (L \cup L'') \setminus \{c \mid c \in A \wedge \forall_{c' \in c\eta} [f(c') \neq \infty \vee c'\sigma = b]\}$
7. $L = \emptyset \rightarrow P_c^{c^{**}} = \emptyset$ (no solution)
8. $f(c^{**}) = \infty \rightarrow r.2$
9. $p := (c^{**}), \tilde{c} := c^{**}$
10. $\bar{c} := \rightarrow ((\tilde{c}, \bar{c}) \in \eta \wedge \forall_{c \in c\eta} [\mathcal{L}(c) \geq \mathcal{L}(\bar{c})])$
11. $p := (\bar{c}, p)\tau$
12. $\tilde{c} := \bar{c}$
13. $\tilde{c} \neq c^* \rightarrow r.10$

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III. THE MATHEMATICAL FORMULATION OF THE WIRING PROBLEM

1. INTRODUCTION

The wiring problem which occurs in the design of printed boards and integrated circuits, arises from the restriction of the number of wiring layers. In many cases this number will be one. The problem is usually translated into a graph-theoretical formulation [1, 2, 3] in such a way that a certain graph has to be tested for planarity. When the result of such a test is negative, technical modifications should be applied in order to obtain a planar graph.

Besides the one layer constraint there are other requirements. They are listed below.

C_1 : *The terminals of the circuit are to be placed on the periphery of the chip or the board.*

The connection of the printed board with the other parts of the system is simplified by satisfying this requirement. In the case of circuit integration the same applies for the bondation of the circuit to its package, but here we have the additional advantage of keeping the bonding pads out of the region in which the elements are placed (thermal effects).

C_2 : *The terminals are to be positioned on the periphery in a previously specified sequence.*

This constraint is dictated by standardization rules and the desire to avoid special precautions for isolation.

With C_1 and C_2 a practical layout algorithm for integrated circuits is possible. The formulation for printed boards, however, is not complete. It should be extended by the following three constraints (C_3 , C_4 , C_5).

C_3 : *The contacts of a certain component must appear in a given sequence.*

As to its treatment this constraint is equivalent to a combination of C_1 and C_2 . Components with more than three pins in a fixed order make the implementation of C_3 necessary. However, in order to match the pins of the components to the contacts on the board, the sequence of the contacts has to have a specific orientation, namely clockwise or counterclockwise. Therefore we introduce the following constraint.

C_4 : *The orientation of the contacts on the board must be the same for all the components with more than two pins in a fixed order.*

The last requirement makes an a priori choice of the side on which the components are to be placed, possible:

C_5 : *The orientation of the components described in C_4 is defined with respect to the orientation of the terminal sequence at the periphery.*

In order to adapt our notions to those in literature we will start section 2 with some definitions and statements whose proofs are either trivial or to be found in books on graph theory and analytic topology [4, 5, 6]. Section 2 ends with the statement and the proofs of the five crucial theorems necessary for the justification of the mathematical formulation of the problem with the above-mentioned five constraints. This formulation is described in section 3, and in section 4 an example is presented for printed board layout. The last section contains some concluding remarks.

2. THE GRAPHTHEORETICAL BASE

A graph (G, U) consists of a finite set of vertices G and a finite family of edges U such that $G \cap U = \emptyset$. G and U define an incidence relation which associates with each edge $[x, y]$ two vertices, x and y , called its ends. Parallel edges are associated with the same pair of vertices. A loop is an edge of which the associated vertices are not distinct. The number of edges incident with vertex x is called the degree $\gamma(x)$ of x . We call a graph simple, when there are no vertices of degree less than 3, no parallel edges and no loops. With every graph we associate a simple graph by applying the following rules as many times as possible:

1. Delete a loop
2. Delete a vertex of degree 1 with its incident edge
3. Replace two parallel edges by one edge in such a way that every pair of vertices which was associated with an edge remains so
4. Replace a vertex of degree 2 and the two edges incident with it by one edge in such a way that the degree of the other vertices is not changed.

A path $P[x_1, y_k]$ is a sequence $[x_1, y_1], [x_2, y_2], \dots, [x_k, y_k]$ of edges in which we have

$$\forall_{1 \leq i < k} \forall_{1 < j \leq k} [(x_i = x_j \leftrightarrow i = j) \wedge (y_i = x_{i+1}) \wedge (x_j \neq y_k)]$$

A circuit is a path with $x_1 = y_k$. A graph is called connected, when there is a path between every pair of vertices. The maximal connected subgraphs of a graph are called components. The intersection of two graphs consists of all the edges they have in common and their associated vertices. The union of two graphs is the graph consisting of all the edges and vertices of the original graphs. Two graphs are said to meet each other, if they have an edge in common. Otherwise they are called disjoint. The complement of a subgraph (H, V) in the graph (G, U) is the graph consisting of all the edges in $U \setminus V$ and all their associated vertices, denoted by $G \setminus H$. The set $H \cap (G \setminus H)$ is called the attachment set of (H, V) . The number of elements in this set is called the attachment number.

Let (C, W) be a circuit of (G, U) . We call a subgraph (H, V) of $(G \setminus C, U \setminus W)$ C -bounded, when all its vertices of attachment are vertices of C . It is clear that $(G \setminus C, U \setminus W)$, the complement of any C -bounded subgraph in $(G \setminus C, U \setminus W)$, and the intersection of any two C -bounded subgraphs, are all C -bounded. A C -bounded subgraph of $(G \setminus C, U \setminus W)$ is called a bridge of (C, W) if none of the subgraphs of this graph is C -bounded. In other words a bridge of (C, W) is a minimal C -bounded subgraph of $(G \setminus C, U \setminus W)$. When $[x, y] \in U \setminus W$, then the intersection of all the C -bounded subgraphs of $(G \setminus C, U \setminus W)$ containing $[x, y]$, is a bridge. $(G \setminus C, U \setminus W)$ is thus the union of all the bridges of (C, W) . Clearly, a bridge is connected, because it is minimal [7].

A graph is called n -separable, where n is a non-negative integer, when it can be partitioned into two disjoint subgraphs, each having at least one vertex which is not a vertex of the other, such that the attachment number is not more than n . A graph is properly n -separable, when its simple graph is n -separable. The graph is n -connected when it is not properly m -separable for any $m < n$. An articulation set is a set of n vertices being the vertices of attachment of a subgraph of an n -separable and n -connected graph. In a 2-connected graph a circuit can be found such that it contains an arbitrary edge (or vertex) [7, 8, 9].

A graph is called planar, when it has a topological representation in a plane (or equivalently on a sphere). This definition is the link between graph theory and analytic topology. For the details we refer to the literature [4, 5, 6].

Here we confine ourselves to some facts from these areas.

A graph is planar if and only if its simple graph is planar. Further, every subgraph of a planar graph is planar. The most famous criterion for the planarity of a graph is due to Kuratowski [10]: A graph is planar if and only if it has no subgraphs whose simple graphs are isomorphic to $(\{x_i | 1 \leq i \leq 5\}, \{[x_i, x_j] | 1 \leq i < j \leq 5\})$ or $(\{x_i | 1 \leq i \leq 6\}, \{[x_i, x_j] | 1 \leq i \leq 3 \wedge 4 \leq j \leq 6\})$.

A planar 2-connected graph (G, U) is called H -accessible where $H \subset G$, when there exists a circuit (C, W) in (G, U) such that $H \subset C$ and there is a planar representation (G', U') of (G, U) in which every point of $C' \cup W'$ can be connected with a point $x \notin G' \cup U'$ by disjoint Jordan curves without intersecting $G' \cup U'$. (G', U') is called an H -periphère representation of (G, U) . It is clear that one of the regions in which $C' \cup W'$ divides the plane, contains no edges of U' . We call this region a face in this particular representation. The circuit $C' \cup W'$ forms the boundary of this face. Two elements h_1 and h_2 of H are called G' -adjacent in H when they can be connected by a Jordan curve in this face without intersecting other Jordan curves in this face connecting two elements of H . The notation for this relation will be: $h_1 \sim h_2$. Every planar representation automatically defines an adjacency relation on H , when it is H -periphère. In a planar representation every vertex and every edge is on the boundary of some face. The whole graph is contained in the interior region of one of the boundaries. This boundary is called the outer boundary. For every face there can be found a planar representation on a plane such that its boundary is the outer boundary. Suppose namely that the graph is mapped onto the surface of a sphere. Call an arbitrary point of the face in question the north pole P . Stereographic projection from P on the tangent plane through the south pole will project the north pole on the infinite of the plane and the projection of the face concerned will form the outer region of the plane.

Suppose we have a simple closed Jordan curve C (dividing the plane into two regions; Jordan curve theorem) on which two pairs of distinct points C_1, C_2 and C_3, C_4 are selected ($C_1 \neq C_2$ and $C_3 \neq C_4$). These pairs are said to alternate when there is no section of C connecting C_1 with C_2 without containing C_3 or C_4 . It is possible to connect C_1 with C_2 and C_3 with C_4 by disjoint Jordan curves in one region if and only if (C_1, C_2) and (C_3, C_4) do not alternate [6]. An equivalent definition of G' -adjacent in H is now: two vertices h_1 and h_2 of H are G' -adjacent in H if they do not alternate with any other pair of vertices of H on $C' \cup W'$.

From now on in this section (G, U) is a 2-connected graph. In the case of 1-connectedness the according statements are easy to derive from the results below. Only theorem 3 undergoes a slight modification.

Theorem 1: $H_i \subset G, x_i \notin G' \cup U'$

(G, U) has a planar representation (G', U') that is H_i -periphere for $1 \leq i \leq m$ if and only if the graph

$$(K, V) = (G \cup (\bigcup_{i=1}^m \{x_i\}), U \cup (\bigcup_{i=1}^m \{[x_i, h^i] | h^i \in H_i\}))$$

is planar for some $\{x_1, x_2, \dots, x_m\}$

Proof: Suppose (K, V) is planar, then it has a planar representation (K', V')

We consider a face with x_i on its boundary. Since x_i is only connected with elements of H_i , h_1^i and h_2^i must also be on this boundary. Thus the boundary consists of $[h_2^i, x_i]$, $[x_i, h_1^i]$ and $P_1[h_1^i, h_2^i]$. None of the pairs (x_i, y) where $y \in P_1[h_1^i, h_2^i]$, are mutually alternating, so every point of $P_1[h_1^i, h_2^i]$ can be connected with x_i by a Jordan curve in the face without meeting one of the other connecting curves. The same applies for the points of $P_2[h_2^i, h_3^i]$, $P_3[h_3^i, h_4^i]$, etc. The curves connecting the points of $P_j[h_j^i, h_{j+1}^i]$ with x_i are in another face as the curves belonging to $P_k[h_k^i, h_{k+1}^i]$ ($k \neq j$). The Jordan curves $[h_j^i, x_i]$ are disjoint from each other because (K', V') is a planar representation, and disjoint from the constructed curves, because they are on the boundary of the faces.

So we conclude that every point of the circuit $P_1[h_1^i, h_2^i] \cup P_2[h_2^i, h_3^i] \cup \dots \cup P_k[h_k^i, h_{k+1}^i] \cup H_i$ can be connected with the point x_i by disjoint Jordan curves. This means that

$(K' \setminus (\bigcup_{i=1}^m \{x_i\}), V' \setminus (\bigcup_{i=1}^m \{[x_i, h^i] | h^i \in H_i\}))$ is a H_i -periphere representation of (G, U) for all $1 \leq i \leq m$.

Conversely, when (G, U) has a planar representation which is H_i -periphere for $1 \leq i \leq m$, then every $h^i \in H_i$ can be connected to an x_i with mutually disjoint Jordan curves, and without intersecting any edge. We only have to consider the points x_i as new vertices, and the connecting Jordan curves as new edges, and we have a planar representation of

$$(G \cup (\bigcup_{i=1}^m \{x_i\}), U \cup (\bigcup_{i=1}^m \{[x_i, h^i] | h^i \in H_i\}))$$

Theorem 2: $H \subset G, x \notin G \quad H = \{h_1, h_2 \dots h_k\}$

(G, U) has an H -periphère representation (G', U') with the property

$$\forall_{1 \leq i < k} [h_i \cup h_{i+1}]$$

if and only if

$(K, V) = (G \cup \{x\}, U \cup \{[x, h] \mid h \in H\} \cup \{[h_1, h_k]\} \cup \{[h_i, h_{i+1}] \mid 1 \leq i < k\})$ is planar.

Proof: For $|H| \leq 3$ the theorem reduces to theorem 1. So we suppose $|H| \geq 4$.

For the first part of the proof we start from the planar H -periphère representation (G', U') with the proposed properties. We can connect h_i with h_{i+1} and h_1 with h_k by disjoint Jordan curves in the face with H on its boundary. The new edges form together a circuit containing H completely and being the boundary of a new face. The new represented graph is thus H -periphère. From theorem 1 we know that the graph (K, V) is planar.

Now we suppose we have an H -periphère representation (G', U') but with a wrong adjacency relation on H . This means that there is a subset $\{h_a, h_b, h_c, h_d\}$ of H with $a < b < c < d$ and $h_a \cup h_c$ and $h_b \cup h_d$ in $\{h_a, h_b, h_c, h_d\}$. Further, we suppose that (K, V) is planar, and thus we have a planar representation of

$$(M, W) = (G, U \cup \{[h_1, h_k]\} \cup \{[h_i, h_{i+1}] \mid 1 \leq i < k\})$$

since this is a subgraph of (K', V') . From the first part of this proof we also know that this representation is still H -periphère with the same adjacency relation.

From theorem 1 and the first part of this proof we conclude that the graph $(MU\{x\}, WU\{[h_a, h_c], [h_b, h_d], [h_a, x], [h_b, x], [h_c, x], [h_d, x]\})$ must also be planar.

However this graph contains the subgraph

$$(HU\{x\}, \{[h_a, x], [h_b, x], [h_c, x], [h_d, x], [h_a, h_c], [h_b, h_d], [h_1, h_k]\} \cup \{[h_i, h_{i+1}] \mid 1 \leq i < k\})$$

whose simple graph is isomorphic to one of the graphs in the theorem of Kuratowski. So (K, V) cannot be planar, which implies a contradiction.

Theorem 3: When a graph (G, U) is H -accessible, there is only one adjacency relation on H possible.

Proof: Again we suppose that $|H| \geq 4$.

Since (G, U) is H -accessible it has an H -periphery representation (G', U') . Suppose it has another H -periphery representation (G'', U'') such that there is a pair h_1, h_2 in H , which is G' -adjacent and not G'' -adjacent. This means there is a path $P'[h_1, h_2]$ in (C', W') in which there is no element of $H \setminus \{h_1, h_2\}$. $P''[h_1, h_2]$ is the corresponding path in (G'', U'') , and this path contains at least one edge not in (C'', W'') . Let $P''_a[h_1, h_2]$ and $P''_b[h_1, h_2]$ be two disjoint paths, together covering the whole (C'', W'') . On $P''_a[h_1, h_2]$ there must be an $h_a \in H$ and not equal to h_1 or h_2 , and on $P''_b[h_1, h_2]$ there must be an $h_b \in H$, not equal to h_1 or h_2 . In (G', U') we can easily find a path $P'[h_a, h_b]$ not containing a vertex of $P'[h_1, h_2]$ (for example in $(C' \cup W') \setminus P'[h_1, h_2]$). However, in (G'', U'') there is not such a path, since h_a, h_b and h_1, h_2 are alternating on $C'' \cup W''$.

Theorem 4: A planar graph (G, U) is properly 2-separable if and only if there is at least one face boundary in an arbitrary planar representation of its simple graph which has more than one bridge.

Proof: There is a planar representation of the simple graph of (G, U) . Suppose one of the face boundaries has more than one bridge. Bridges are connected, thus attachment vertices of a bridge B cannot alternate with vertices of attachment of another bridge B' . So all the vertices of attachment of B are on a path $P[c_1, c_2]$ of the boundary and none of the attachment vertices of B' is. Then the graph is separated by c_1 and c_2 .
Conversely let the planar graph (G, U) be properly 2-separable with articulation set $\{c_1, c_2\}$. Then separate the graph at c_1 and c_2 . We have now two components: (H'_1, U'_1) and (H'_2, U'_2) . Since c_1 and c_2 are connected in (H'_2, U'_2) , (H'_1, U'_1) must be $\{c_1, c_2\}$ -periphery (apply theorem 1 after choosing an arbitrary point on a path $P_2[c_1, c_2]$ in (H'_2, U'_2)), so we can connect c_1 and c_2 by a Jordan curve in the new face. The same is possible in (H'_2, U'_2) . After identifying $[c_1, c_2]$ in both components we have a Jordan curve between c_1 and c_2 in (G', U') and from theorem 1 we know that c_1 and c_2 must be on the same boundary (C', W') . (This fact is obvious from a picture, but as many theorems of analytical topology hard to prove).

The theorem is usually referred to as the Jordan-Schönflies theorem [6]) Since the graph (G, U) was properly 2-separable, there must be a vertex not in C in H_1 as well in H_2 . This means that $(H_1 \cap C, U_1 \setminus W)$ and $(H_2 \cap C, U_2 \setminus W)$ contain each at least one bridge of (C, W) , since they are not empty.

Theorem 5: A graph (G, U) has a unique planar representation (i.e. the boundaries of the faces consist of the same edges for every planar representation of (G, U)) if and only if (G, U) is planar and not properly 2-separable ([11, 12]).

Proof: The necessity is easy to see., for one can, without spoiling the planarity, obtain the mirror-image of every subgraph with attachment number two, by twisting it around its attachment vertices.

The sufficiency follows from theorem 4:

Suppose we have two planar representations (G', U') and (G'', U'') of (G, U) . (C', W') is the boundary of a face in (G', U') and (C'', W'') , the corresponding circuit in (G'', U'') , is not the boundary of a face. In (G'', U'') , (C'', W'') must contain inner and outer bridges, so at least two bridges. Thus the corresponding circuit in (G', U') , (C', W') must also have at least two bridges. Since (C', W') was the boundary of a face. The graph (G, U) must be properly 2-separable.

3. THE MATHEMATICAL FORMULATION

In this section we want to construct a graph from a given network and some additional design data (constraints) such that it is suitable for a number of tests which are necessary and sufficient to yield C_1 to C_5 , and a practical implementation on a computer is possible. In the case of integrated circuits where C_4 and C_5 have lost their relevance a planarity test proves to be efficient. However, with printed board layout we have chosen for a combination of two tests, a planarity test followed by a connectivity test. Of course it will be advantageous that the output of the first test is adapted to the other. We will come back to these subjects in section 5.

The starting point is the schematic diagram of the network consisting of components and conductive interconnections. In the set of components we distinguish between components that can be crossed by wires and those that cannot be crossed. Resistors on a printed board are usually big enough to allow for one or more crossings. In IC-technology a diffusion resistor of more than $1\text{ k}\Omega$ can also be crossed without difficulty. These components belong to the first set. A transistor is an example of the second kind of components. Its contacts are too close to each other to permit a crossing (In IC-technology the distance between the contacts is sometimes big enough, but here we want to avoid crossings too, since parasitic capacitors are introduced then). With every component of the second kind we associate a vertex in the graph to be constructed. We refer to such a vertex as a c-vertex. The conductive interconnections in the diagram form a set of "trees". These trees can never be crossed without special measures ("jumpers" for printed boards, "cross-under resistors" for IC's). With every conductive tree we associate a vertex, called a t-vertex. Whenever a component belonging to a c-vertex c of the graph has one of its contacts on a conductive tree associated with t-vertex t we connect c with t by an edge $[c,t]$. Note that the graph so constructed is bipartite. This means that the set of vertices can be partitioned into two subsets, such that every edge of the graph connects a vertex of one subset with a vertex of the other.

Remark: Some components with a special shape (f.e. IC with a "dual in line"-package) should be implemented in a special way.

The graph generated by the described procedure is called the potential graph. We assert that, when the potential graph is planar, then there exists a planar wiring and a non-overlapping component placement. It is easy to get a layout with these properties by "growing" the c-vertices until they have reached the size of their components. The wiring between the components is (for example) the rest of the graph. Of course this is not a practical layout. In one of the subsequent stages of the program one has to minimize the chip area or to place everything on a board (mostly with standardized dimensions). These procedures are not the subject of this paper.

After the construction of the potential graph we have to implement C_1 to C_5 . The treatment of the first constraint is immediately clear from theorem 1. There are several conductive trees which contain terminals. The set of vertices H is the set of their t-vertices. What in fact we want to know now is whether the graph is H -accessible. We therefore connect every vertex in H with a new vertex x . (The graph is still bipartite; we consider the vertex x as a c-vertex). Planarity of the graph thus obtained is necessary and sufficient for the H -accessibility.

The introduction of C_2 seems to be obvious from theorem 2. Acting in the sense of this theorem we connect every pair of "adjacent" terminals by a new "adjacency edge" (bipartiteness is preserved by laying a vertex on every new edge; these vertices can be considered as c-vertices). The potential graph is now extended by a so-called wheel (the "terminal wheel" in this particular case): the adjacency edges form together the "rim" of the wheel, x is called the "hub" and the edges incident with x are called the "spokes". Planarity of the obtained graph is necessary and sufficient for a planar potential graph constrained by C_1 and C_2 . However, theorem 3 makes the usefulness of the implementation of C_2 questionable. (We will explain this in section 5). Nevertheless we maintain the addition of the adjacency edges, because most planarity tests yield directives as to the set of edges whose deletion planarizes the graph and then the adjacency edges may be useful. Besides the implementation of C_4 becomes easier as we will see later in this section.

C_3 is treated in an analogous manner. Here the hub is the c-vertex associated with the respective component. The set H is formed by the t-vertices directly connected with the hub. We only have to add new edges between adjacent contacts, and again a complete wheel is introduced. We can make the same remarks on the introduction of C_3 as we did with C_2 . The graph so obtained is called the extended potential graph.

The question now is, whether this graph is planar or not. In case of planarity a layout constrained by C_1 , C_2 and (eventually) C_3 exists. Otherwise the graph should be modified by using possibilities given by the technology until planarity is obtained. The problem which is left now can be formulated as: "Does a planar representation of the (eventually modified) graph exist in which C_4 and C_5 are satisfied?". This is very unlikely to occur, and thus in most cases modifications should be carried out. It is immediately clear that methods searching all planar representations (f.e. by applying the theory described in [12], [16] or [17]) are not recommendable. Firstly because of the computational effort involved, and secondly because we don't obtain any indication for executing the necessary modifications. The next thought can be to invalidate these objections by using a "constructive" planarity test. By constructive we mean that the starting point is a planar subgraph which is extended until the graph at hand is obtained. The extension-steps consist of transformations, which do not spoil the planarity and take the orientations into account. Nevertheless we prefer a connectivity test (subsequent to the planarity test) on a planar representation of the (eventually modified) extended potential graph which accounts for C_4 and C_5 . The reason for this choice will be given in section 5. The connectivity test implies a partitioning of the graph into maximal not properly 2-separable subgraphs. Before executing the test we add the three adjacency edges of each component with three pins whose orientation has to be considered. They may not

have been inserted into the extended potential graph, since they are not essential for the sequence of the contacts (it always is the same in the case of three contacts) and they may complicate the modification steps.

Yet, in the connectivity test, these edges are important, because the graph has to be subjected to a simplification procedure in which a c-vertex associated with an orientated three-pin-component may disappear.

Furthermore, wheels are clearly not properly 2-separable. This means that its hub cannot be in an articulation set with less than three elements. Thus wheels will not be split apart by the connectivity test procedure.

According to theorem 5 the subgraphs generated by the test have unique planar representations. So the orientations of the components in such a subgraph are fixed with respect to each other. Consequently, a necessary condition for satisfying C_4 is that the orientations of the components in such a subgraph are all clockwise or all counterclockwise. This is also sufficient, because some subgraph with all its wheels oriented in the same way may be adjusted with respect to the orientation in another subgraph by twisting it around its articulation points.

The orientation of the "terminal wheel" referred to in constraint C_5 , can easily be incorporated into the procedure to check C_4 .

4. EXAMPLE

In this section the described method is demonstrated with a printed board layout design.

The circuit diagram is given in figure 1 (voltage stabilizer). The components are numbered (1) up to (12) inclusively, and the conductive trees 13 up to 23 inclusively. The constraints are specified as follows:

- C_1 : The terminals 13, 14, 15 and 16 are to be placed on the periphery of the board.
- C_2 : The following sequential position of the terminals around the periphery is required: 13, 14, 15, 16.
- C_3 : The contacts of component (1) (the operational amplifier) must appear in the following sequence: 16, 19, 13, 21, 20, 14.
- C_4 : The orientation of the components (1), (3), (4) and (9) has to be the same: when walking along the rim of the respective wheels in clockwise direction the hub has to be in the region at the right. The t-vertices on the rims

then have to occur in the following sequence:

a) for the operational amplifier ((1)):

16, 19, 13, 21, 20, 14

b) for the transistors ((3) respectively (4))

(3): 15, 23, 16 (emitter-base-collector)

(4): 16, 20, 23 (idem)

c) for the potentiometer ((9)):

17, 18, 19

C_5 : When walking along the rim of the "terminal wheel" in the sequence 13, 16, 15, 14, the hub has to be at the right.

The potential graph can easily be constructed by connecting the c-vertices ((1)-(12)) with the t-vertices (13-23) according to the schematic diagram of figure 1. For the moment we consider all the components to be non-crossable. If necessary all the components may be crossed except the transistors, operational amplifier, and the potentiometer. (The op-amp has a TO-5-TYPE package; see bottomview).

We take care of constraint C_1 and C_2 by adding a new vertex ((24); c-vertex) and adding the edges [24, 13], [24, 14], [24, 15], [24, 16] and the edges [13, 14], [14, 15], [15, 16], [16, 13].

The treatment of C_3 requires the addition of the edges [16, 19], [19, 13], [13, 21], [21, 20], [20, 14], [14, 16]. The graph obtained now, is the extended potential graph and has to be tested on planarity. The test discloses the extended potential graph to be non-planar. Planarity can be obtained by deleting two edges. A possible choice can be:

- a) edge [4, 20] (the base of transistor (4)); Technologically this connection can be established as a "jumper".
- b) One of the edges [14, 10] and [10, 18]; In this case, the modification is simple, since vertex (10) is associated with a component (resistor) that may be crossed.

Since the planar representation in figure 2 does not satisfy the constraints C_4 and C_5 , the connectivity test has to be executed.

The starting point for this test is the extended potential graph (figure 2, without dotted lines) with addition of all the "adjacency edges" of each 3-pin-component whose orientation has to be considered. The first thing to do is simplifying this graph. The result is depicted in figure 3.

Theorem 4 indicates that we have to determine which faces of this graph have more

than one bridge. The following faces (shaded in figure 3) have this property:

- 1 - 19 - 13
- 17 - 13 - 19 articulation points 13 and 19
- 16 - 13 - 18 - 19

- 16 - 14 - 15 - 23
- 16 - 3 - 15 articulation points 15 and 16
- 16 - 15 - 24

Faces with two vertices in common are grouped together and enclose a maximal subgraph of the simple graph, that is not properly 2-separable. The orientations of the components that are placed in the same subgraph, are fixed. If these relative orientations are not according to the constraints C_4 and C_5 , some additional modifications have to be carried out to satisfy the constraints. If the (relative) orientations of the components in distinct subgraphs are not according to the constraints, then the orientations in some subgraph may be changed by twisting the subgraph around its eventual articulation points. In our case we have 3 maximal subgraphs that are not properly 2-separable:

- a) ($\{13, 17, 19, 18, 9\}$, $\{[13, 17], [17, 19], [18, 19], [13, 18], [9, 17], [9, 18], [9, 19]\}$).
This subgraph contains the wheel associated with the potentiometer (9).
- b) ($\{16, 23, 15, 3\}$, $\{[16, 23], [23, 15], [3, 15], [3, 23]\}$).
This subgraph contains the wheel associated with transistor (3).
- c) The subgraph containing all the edges of the graph in question except those edges that are contained in the graphs a) and b).
This subgraph contains two wheels, namely the terminal-wheel (hub 24) and the wheel associated with the operational amplifier (1).

The orientation of transistor (4) is of course always ensured since one of its pins is connected with a jumper. The relative orientation of the two wheels in c) is according to the constraints, so no additional modifications have to be carried out. The subgraphs a) and b) have to be rotated to get the planar representation of the graph as given in figure 4. From this graph it is easy to construct the planar representation of the modified potential graph that satisfies the given constraints.

5. CONCLUDING REMARKS

In the preceding sections we have shown how the wiring problem in a general form (taking into account the five design requirements C_1 tot C_5) can be formulated in a graph theoretical way such that implementation on a computer is possible.

The construction of the potential graph as described here is in fact the same as in [13], but we do not want to adopt the cumbersome notion of the generalised graph [14], which is only a bipartite graph from the topological point of view. Of the five constraints the first two did appear in literature before [15, 16, 13, 1]. The step to C_3 is then evident. In [13, 1] the implementation was also the same as described here but the actual content of theorem 3 is not noted. From this theorem it is tempting to conclude that the adjacency edges are superfluous, and indeed, in the planarity test they are. The planarity test on the graph extended with adjacency edges even yields less information than the test on the graph that does not contain these edges. However, when the graph turns out to be non-planar modifications have to be applied. The importance of the adjacency edges at this stage depends on how these modifications are carried out. Of course the potential graph need not be biconnected, but separability only has influence on the preceding when an articulation point is in one of the sets H_1 . In practice this case will not occur; besides this influence can easily be seen from the planar representation.

In the construction we indicated how to preserve the bipartiteness of the graph. This only is advantageous when this property is used in the operations carried out on this graph, for example in the planarity test.

After the planarity test a connectivity test is necessary for treating the orientations of the components as fixed in C_4 and C_5 . In the case that such a test has to be carried out it is recommendable to apply a planarity test that gives adequate output for the connectivity test. We have at our disposal a planarity test that yields the planar representation in a face-oriented way. After the planarisation a check on the orientations can be executed very easily. Another advantage is that the terminal wheel need not be added since C_1 and C_2 can be taken care of by starting the procedure with a face that contains the terminals in the required sequence.

More facts about splitting a graph in not properly 2-separable subgraphs are given in [17]. This paper, however, does not contain an algorithm for the splitting procedure in spite of Weinbergs statement [16] that it does.

In section 3 we mentioned as a thought that a constructive searching for a planar representation could solve the problem. Then, one can investigate the graph upon the requirements C_1 to C_5 by one test. However the problem remains to find a practical implementation. Weinbergs algorithm [16] for example can be altered easily for this purpose, but is as planarity test already difficult to implement. Several other "constructive" algorithms have a simpler implementation, but the required alterations are complicated. This is the reason of preferring the method presented in section 3.

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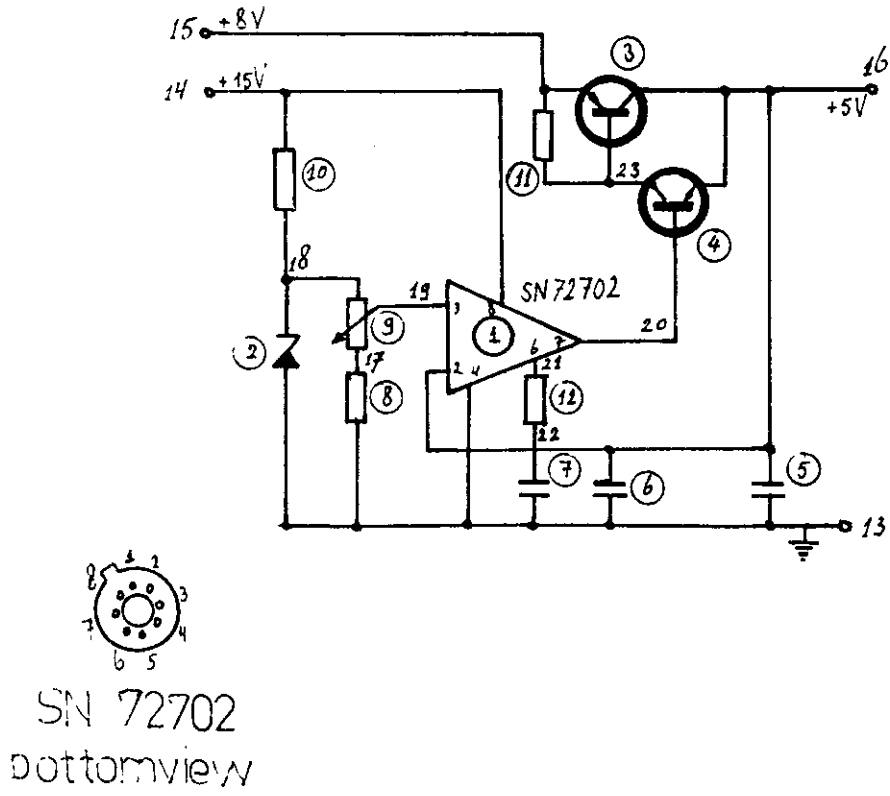


fig. 1

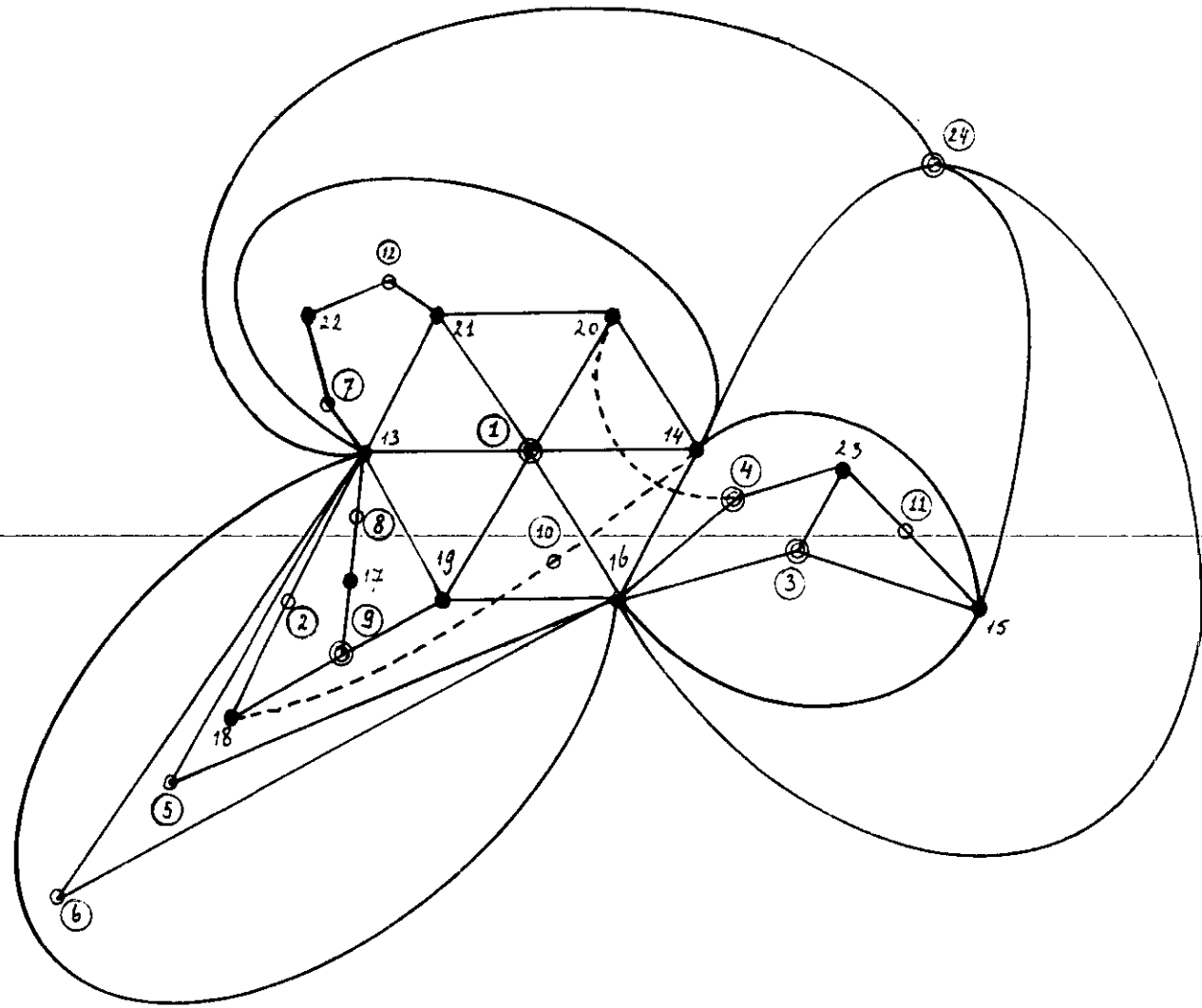


fig 2

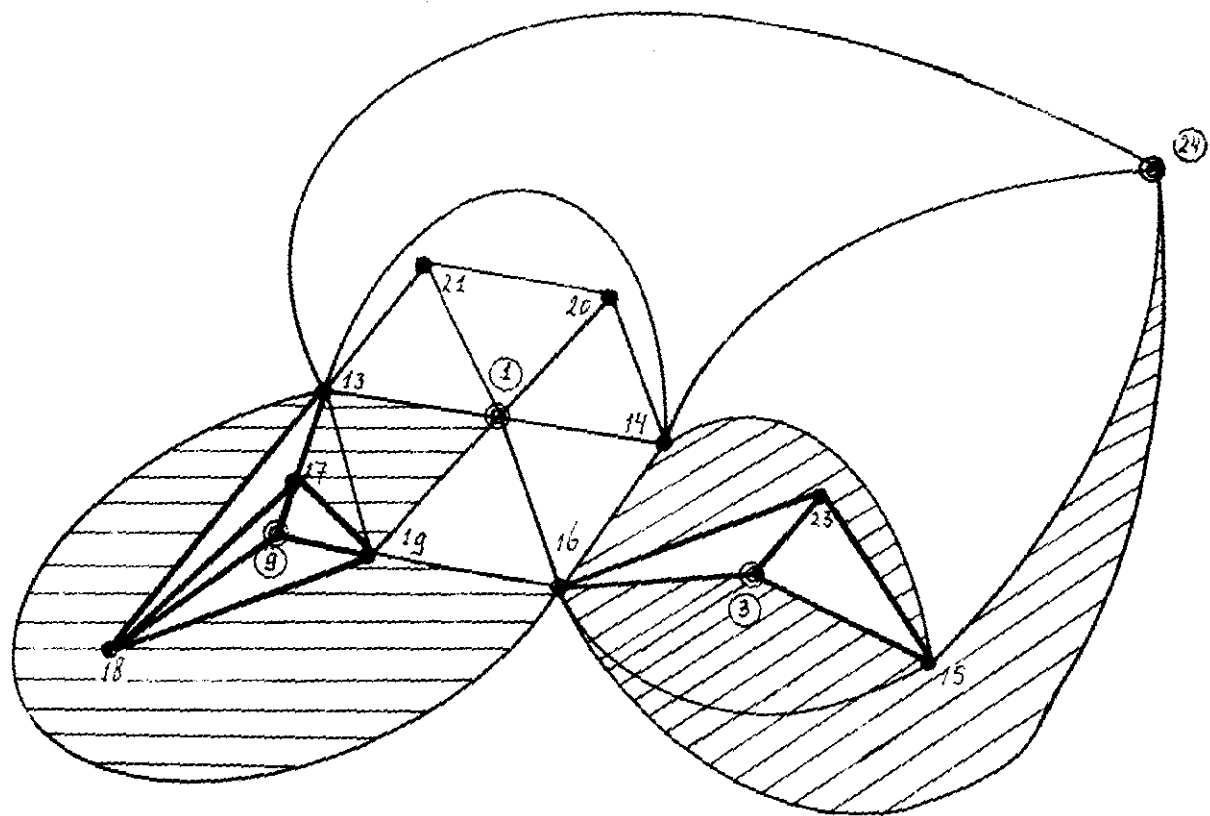


fig. 3

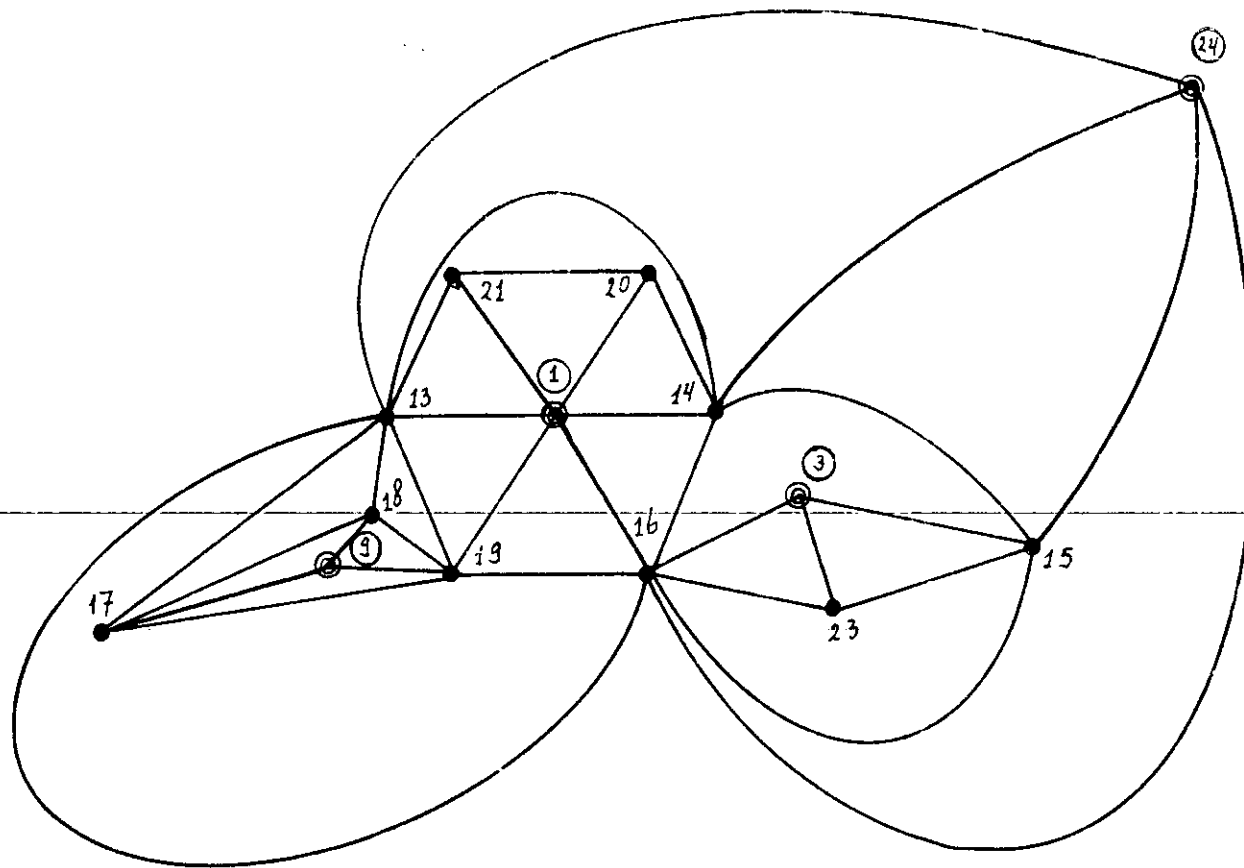


fig 4

IV. MODIFICATIONS FOR MONOLITHIC IC'S

From the modifications we demand that

- a. they do not increase the number of masks
- b. they do planarize the extended potential graph.

The following modifications are used to obtain the modified potential graph of fig. 3 from the extended potentialgraph of fig. 2:

M1: When the collectors of some npn-transistors are connected with the same "potential tree" they may be placed in the same isolated region. This means that we need only one contact between this region and the conductive interconnection. In the graph this is reflected by a possible deletion of all the corresponding edges except one (arbitrary chosen) edge.

The disadvantages of this modification are not very important:

- restriction of the "layout-freedom"
- parasitic capacitance between the isolators and connections crossing the region
- field effects (when there is no buried layer, the expected decrease of the collector resistance is often held off because of these effects.

In the example the deletion of [45,7] is necessary for planarization, but also [43,12] and [44,8] are deleted.

M2: For pnp-transistors the same possibility occurs, when their bases are connected with the same potential tree. In the graph all the corresponding edges except one arbitrary edge can be deleted. In the example no pnp-base-contacts are connected with each other, so in this case M2 cannot be applied.

M3: The "lateral" realization of a pnp-transistor is the most common and better one, but in case the collector is connected with the lowest potential in the circuit one may choose for the substrate-pnp-transistor, since the substrate is always on the lowest potential. However, there are severe objections against this modification, which causes a deletion of the corresponding edge in the graph. Normally the p-diffusion is so undeeep that the current gain is too low. Making the diffusion deeper causes many other components to have a parasitic pnp-transistor which is almost always disadvantageous. Besides the depth of the diffusion is difficult to handle.

Using this modification, [51,4] is deleted in fig. 3.

Fig.1 Schematic diagram.

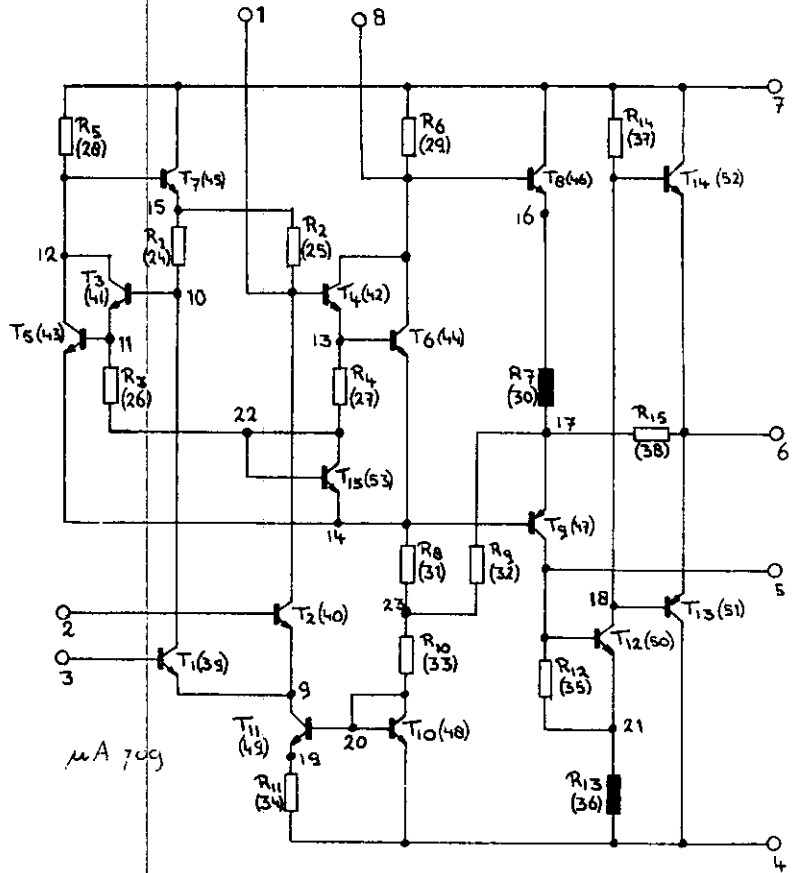
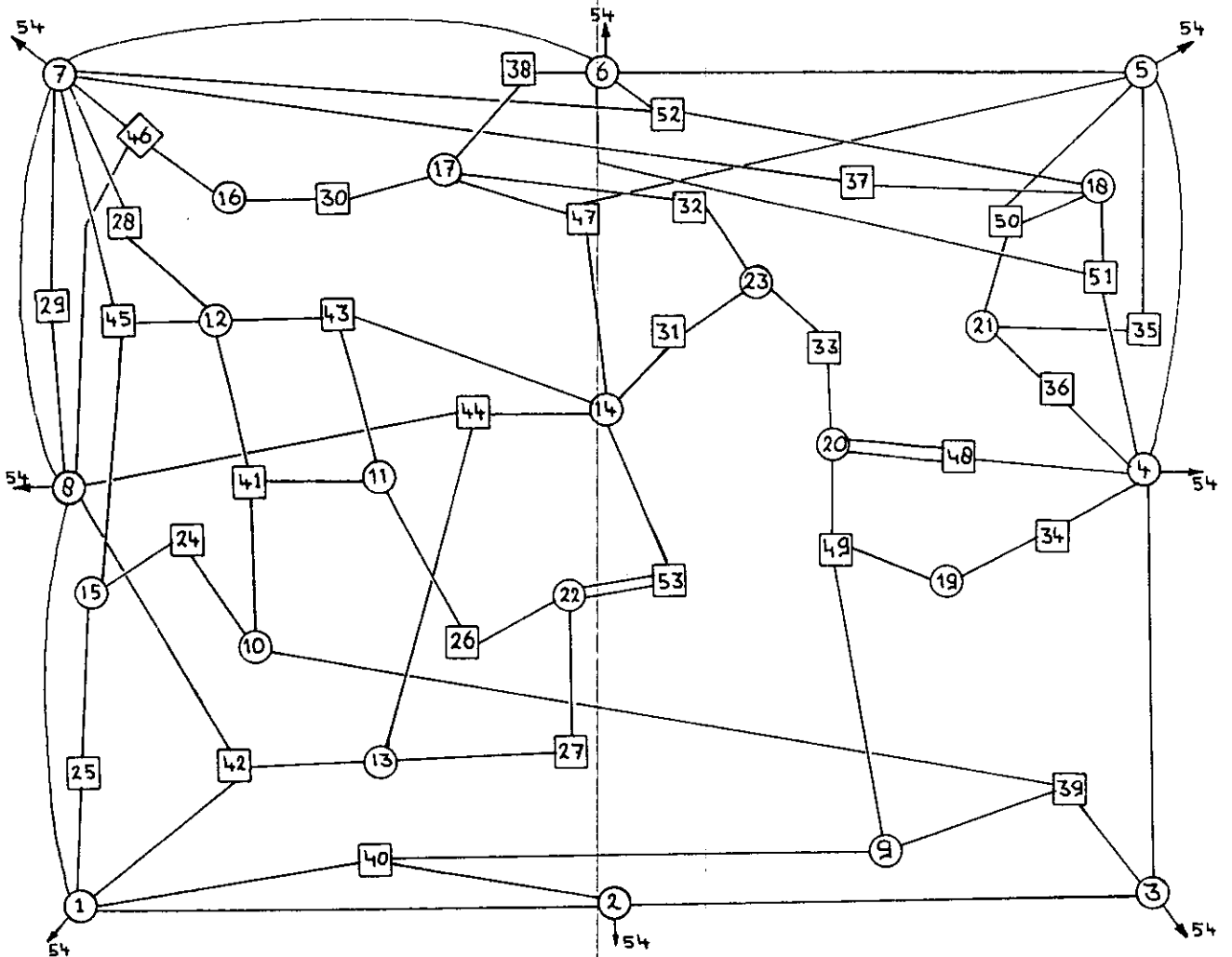


Fig.2 Extended potential graph (constructed from fig.1 by the method of Chapter III).



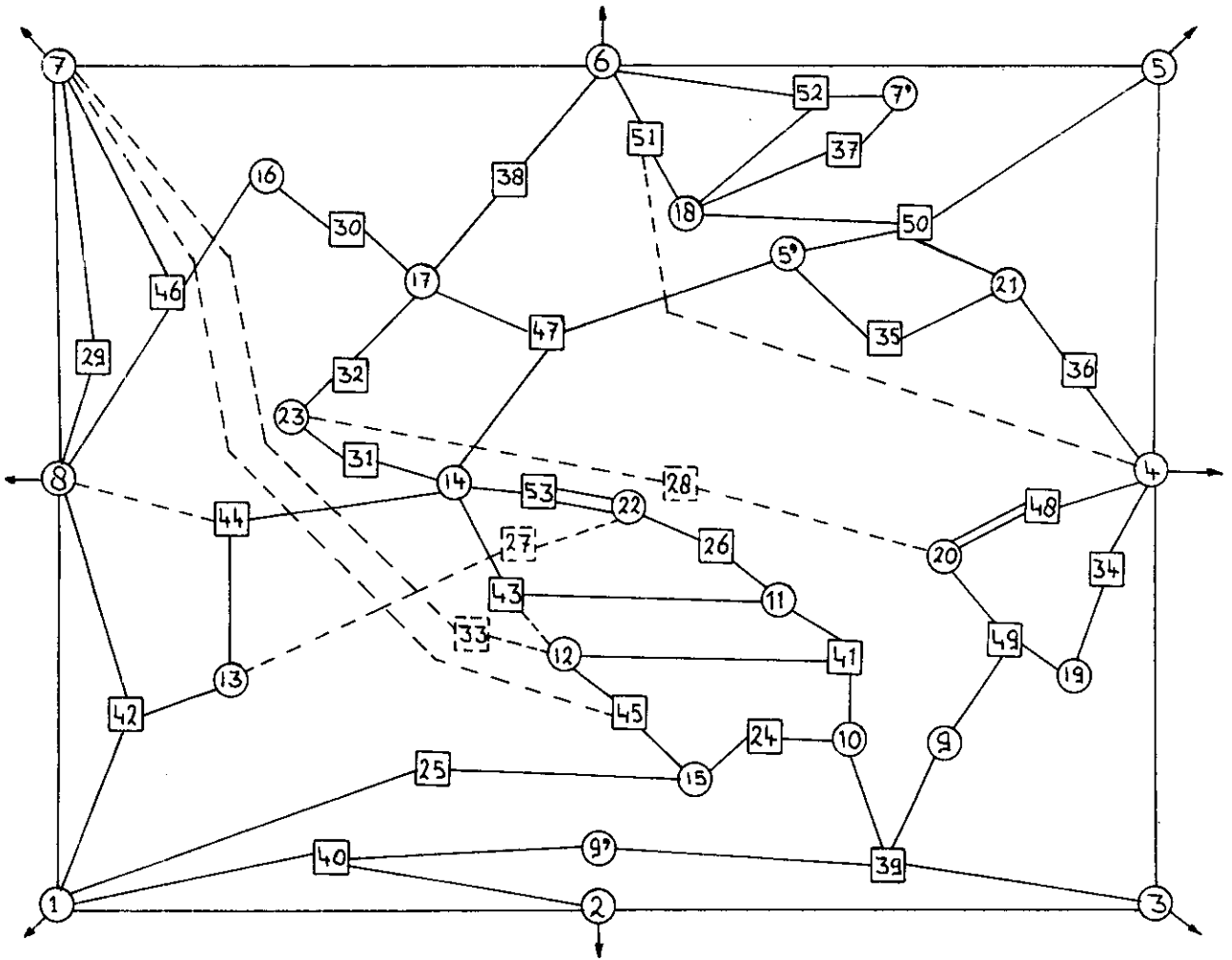


Fig.3 Modified extended potential graph.

Ad fig.3:

The following modifications have been applied:

- M1: 7,45 , 8,44 , and 12,43 are deleted;
- M3: 4,51 is deleted;
- M4: 27, 28, and 33 are deleted;
- M5: 7 is doubled;
- M6: emitter contact (9) of T1 (39) is doubled;
base contact (5) of T12 (50) is doubled.

M4: The greater the resistance, the larger is the possible distance between its contacts. When this resistorlength is large enough conductive interconnections may cross the resistor between its contacts. Their number is limited by the distance of the contacts. In this stage of the design, however, we make this number unlimited for resistors with a value greater than five times the "square resistance". In a later stage we incorporate the resistors taking into account their length and other criteria using the algorithm of Chapter II section 4. (When problems arise by the number of crossing connections, this can always be solved by a n^+ -diffusion series resistor (ca. 10Ω)). In the graph the modification is effected by deleting the corresponding vertex and its associated edges. The only objection is the restriction of the "layout-freedom". In fig. 3 the vertices 27, 28 and 33 with their associated edges are deleted. In fig. 4 they are introduced again. The same modification is possible in case of capacitors, but the series resistance of a SiO_2 -capacitor will increase.

M5: Beside deleting edges a graph may be planarised by increasing the number of vertices by doubling: this means replacing a t-vertex by two new vertices t_1 and t_2 such that:

$$\{c|[c, t_1] \in U'\} \cup \{c|[c, t_2] \in U'\} = \{c|[c, t] \in U\}$$

and

$$\{c|[c, t_1] \in U'\} \cap \{c|[c, t_2] \in U'\} = \emptyset$$

The number of "potential trees" is increased, but both new "trees" should have the same potential. Therefore they are connected by a crossunder resistor (which is an as small as possible n^+ -diffusion resistor permitting a crossing) or by a connection with the same isolated region. Of the last kind is the modification to obtain a doubling of vertex 7 in fig. 3. The n^+ diffusion resistor must be applied only when it is absolutely necessary, because:

- its value is not always neglectible (ca. 10Ω) and depends on the potential difference
- parasitic capacitance is introduced and we have field effects that may increase the resistance
- a separate isolated region may be necessary.

M6: Another is the doubling of a transistor contact. In the graph this is a doubling of a t-vertex as described above. Both new vertices, however must be connected with the c-vertex corresponding with the transistor. When a contact of a transistor is doubled no other contact of the same transistor can be doubled. Transistor T_{12} of fig. 1 has got a double base contact and transistor T_1 a double emitter contact, which means a doubling of vertex 5 and vertex 9.

A disadvantage is the increase of the capacitance between the base- or emitter lead and the collector region and - in the latter case - the base region.

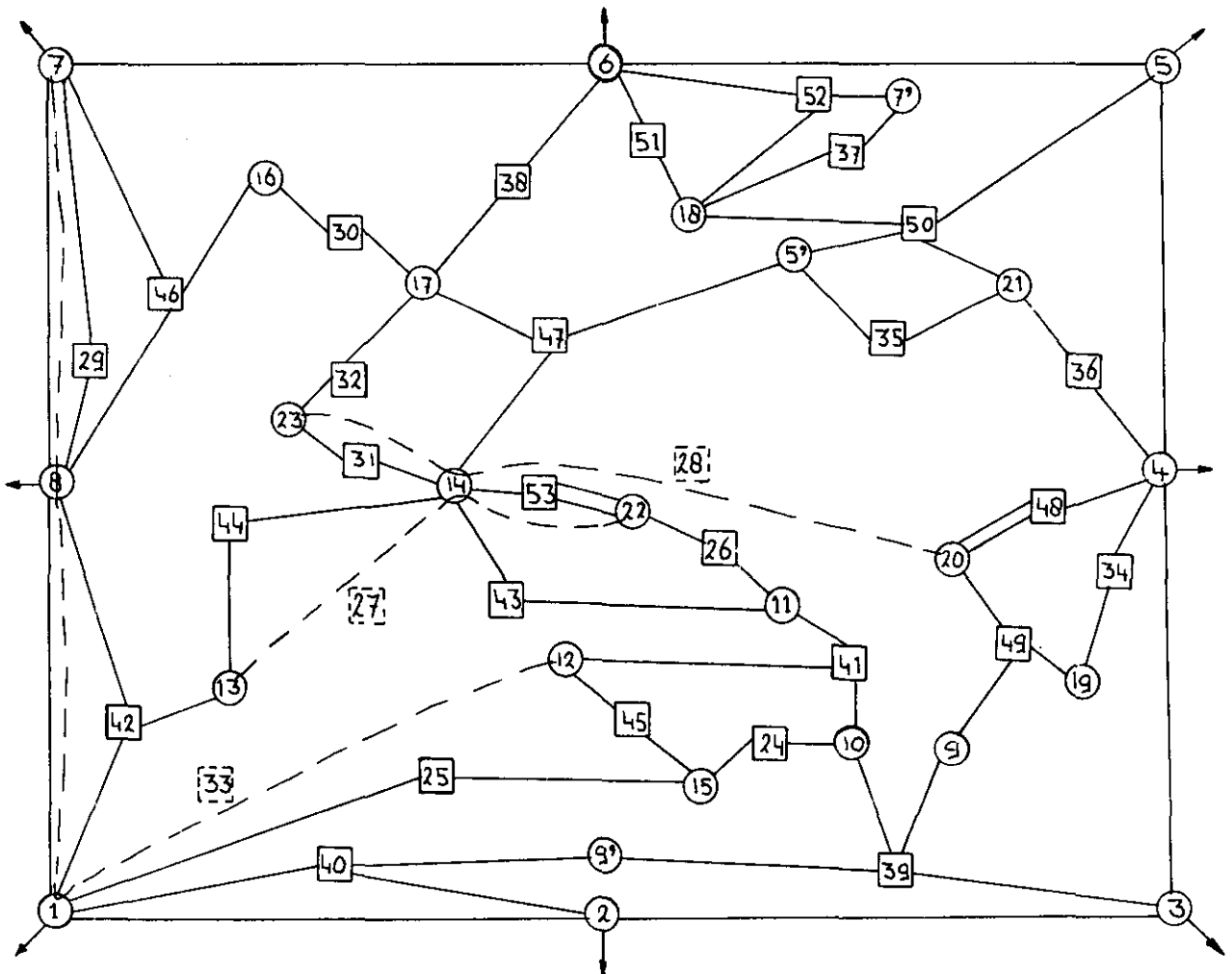


Fig.4 Embedding of the resistors.

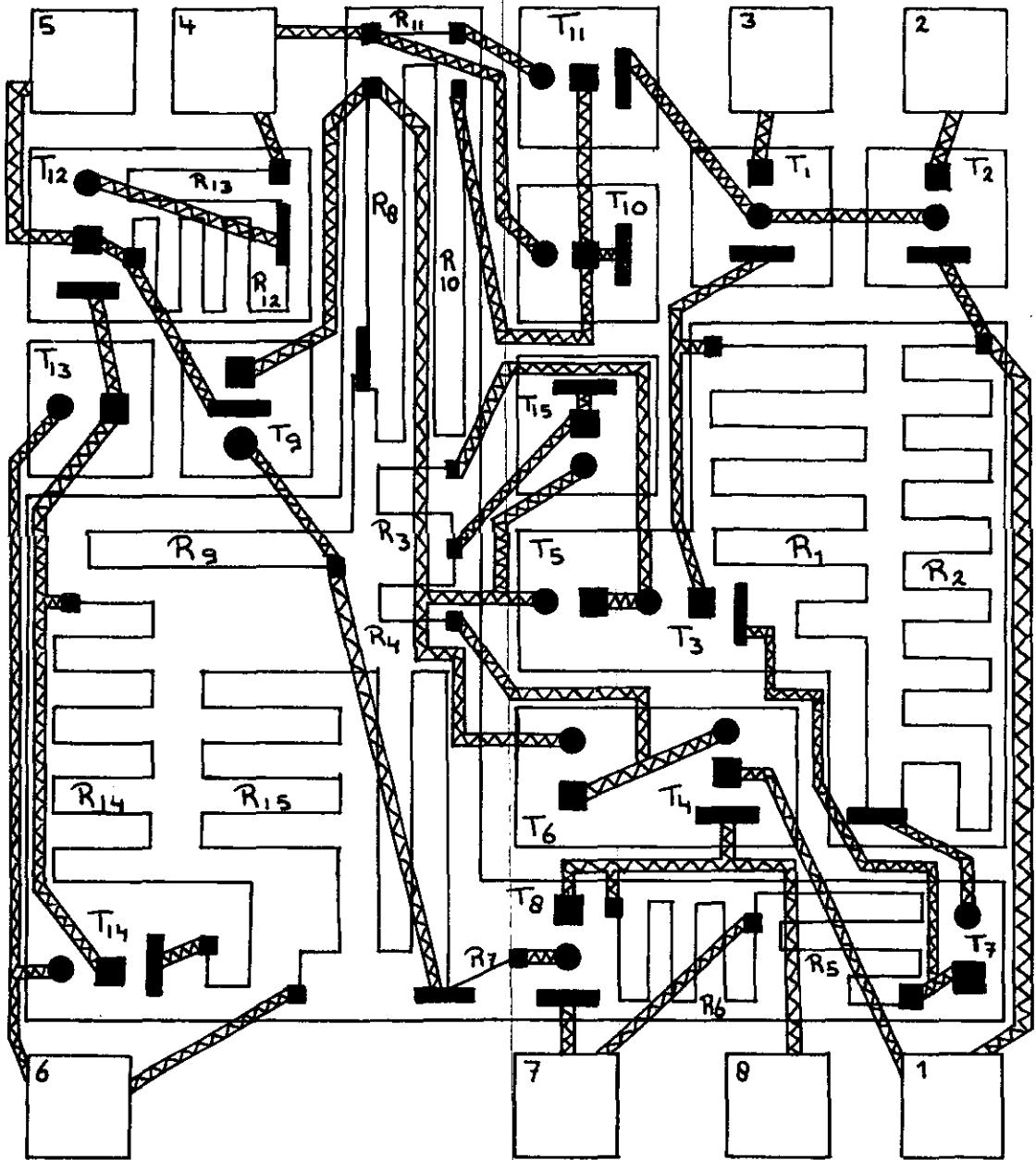


Fig.5 Symbolic layout.

Ad fig.4 and fig.5:

In fig.4 one can see which potentials cross the deleted resistors. The resistor are embedded such that they only cross t-vertices taking into account optimization criteria e.g. the least possible number. In fig.5 a symbolic layout of the schematic diagram of fig.1 is depicted in correspondence with the modifications of fig.3.

V. THE "CEL"-PLANARITY ALGORITHM

1. Assigning a drain function to a graph

We have a graph (G,U) with n vertices ($|G| = n$). Of course we can define a bijective mapping f from G into the set $\{1, 2, 3, \dots, n\}$. This means that every vertex $x \in G$ is associated with an integer $f(x)$. We can use this fact in giving the edges of (G,U) an orientation. The result is a digraph (G,V) , called the f -oriented digraph of (G,U) and defined by

$$\forall_{x \in G} \forall_{y \in G} [[x,y] \in V \leftrightarrow [x,y] \in U \wedge f(x) < f(y)]$$

Every function f which is conform the description above, points out one vertex $s \in G$ with $f(s) = 1$ and one vertex $t \in G$ with $f(t) = n$. A function f is called a drain function of (G,U) when it possesses the additional property

$$\forall_{x \in G} [[x \neq s \wedge x \neq t] \leftrightarrow \exists_{[x,y] \in U} \exists_{[x,z] \in U} [f(y) > f(x) > f(z)]]$$

A digraph (G,V) is called a drain if it is acyclic and it contains exactly one source and exactly one sink.

Theorem 1: Every f -oriented digraph (G,V) for which f is a drain function, is a drain.

Proof: First suppose that (G,V) possesses a cycle. $C[a_0, a_1, a_2, \dots, a_k]$ with $a_0 = a_k$. From the definition of f -oriented we conclude

$$f(a_0) < f(a_1) < f(a_2) < \dots < f(a_k) \rightarrow f(a_0) < f(a_k)$$

This is contradictory, since f is bijective and thus $a_0 = a_k \rightarrow f(a_0) = f(a_k)$

1 is the smallest number in the range of f . The graph is f -oriented thus s must be a source. n is the highest number in the range of f , and so t is a sink.

There are no other sources, because for every $x \neq s$ there is a $y \in G$ with $f(y) < f(x)$. (f is a drain function !)

Analogously, t is the only sink.

Now we have a drain (G, V) . Let U be the set $\{[x, y] \mid [x, y] \in V \vee [y, x] \in V\}$. Suppose that f is such a drain function of (G, U) , that the associated f -oriented digraph of (G, U) is equal to (G, V) . Then we call f a natural drain function of (G, V) .

Theorem 2: With every drain (G, V) there is at least one natural drain function associated.

Proof: We have a drain (G, V) with the source s , and the sink t .

Let us construct the following subdigraph of (G, V) :

$$\begin{aligned} (G_{n-1}, V_{n-1}): \quad G_{n-1} &= G \setminus \{t\} \\ V_{n-1} &= V \setminus V'_{n-1} \\ V'_{n-1} &= \{[x, t] \mid [x, t] \in V\} \end{aligned}$$

By deleting arcs we cannot get extra cycles so (G_{n-1}, V_{n-1}) is also acyclic.

Clearly, every source of (G, V) is a source in (G_{n-1}, V_{n-1}) . Furthermore, G_{n-1} does not contain more sources, since Γ only changes for vertices in the set $G'_{n-1} = \{x \mid [x, t] \in V\}$. If such a vertex x is a source of (G_{n-1}, V_{n-1}) then $\Gamma_{n-1}^{-1}(x) = \emptyset$. Since $t \notin \Gamma^{-1}(x)$ for every x in G , $\Gamma^{-1}(x) = \emptyset$, and x would be a source of (G, V) .

We conclude thus that (G_{n-1}, V_{n-1}) has also one unique source. We now state that (G_{n-1}, V_{n-1}) is connected, in other words, t is not an articulation point of (G, V) . We prove this statement by reducing its negation to an absurdity.

When (G_{n-1}, V_{n-1}) is not connected, it consists of more than one component. We consider one of these components (G', V') of (G_{n-1}, V_{n-1}) and prove that it must contain at least one source. Since (G_{n-1}, V_{n-1}) has only one source, it can have at most one component, which means that it is connected.

The outline of this part of the proof is:

- we prove that $\hat{\Gamma}$ is a partial ordering for G'
- every chain has an upper bound
- according to Zorn's lemma we conclude that there is a minimal element which is a source in our case.

$\hat{\Gamma}$ is reflexive, because $(x,x) \in \hat{\Gamma} \rightarrow x \in \hat{\Gamma}(x)$

$\hat{\Gamma}$ is transitive: $(x,y) \in \hat{\Gamma} \rightarrow y \in \hat{\Gamma}(x) \rightarrow \exists_{i \in \mathbb{N}} [y \in \Gamma^i(x)]$
 $(y,z) \in \hat{\Gamma} \rightarrow z \in \hat{\Gamma}(y) \rightarrow \exists_{j \in \mathbb{N}} [z \in \Gamma^j(y)]$ } $\rightarrow z \in \Gamma^{i+j}(x) \rightarrow$
 $\rightarrow z \in \hat{\Gamma}(x) \rightarrow (x,z) \in \hat{\Gamma}$

$\hat{\Gamma}$ is antisymmetric: $(x,y) \in \hat{\Gamma} \rightarrow y \in \hat{\Gamma}(x) \rightarrow \exists_{i \in \mathbb{N}} [y \in \Gamma^i(x)]$
 $(y,x) \in \hat{\Gamma} \rightarrow x \in \hat{\Gamma}(y) \rightarrow \exists_{j \in \mathbb{N}} [x \in \Gamma^j(y)]$ } $\rightarrow x \in \Gamma^{i+j}(x)$

This means that there is a chain $C'[x,y>$ and there is a chain $C''[y,x>$, which form together a cycle. However (G',V') is acyclic, thus $i = j = 0$ or $x = y$.

These three properties of $\hat{\Gamma}$ make it a partial ordering.

For every chain C in (G',V') we have $\forall_{x \in C} \forall_{y \in C} [(x,y) \in \hat{\Gamma} \vee (y,x) \in \hat{\Gamma}]$.
 which means that C is a linearly ordered subset of G' .

Every chain in (G',V') has a lower bound $g \in G'$: for take g in the following way

$$g \in C \wedge \neg \exists_{y \in C} [(y,g) \in \hat{\Gamma} \wedge y \neq g]$$

then

$$\forall_{c \in C} [(g,c) \in \hat{\Gamma}]$$

Finally, a minimal element in G' is an element s_0 , such that

$$\forall_{x \in G'} [(x,s_0) \in \hat{\Gamma} \rightarrow s_0 = x]$$

or in our terminology: s_0 is a source (for $\Gamma^{-1}(s_0) = \emptyset$)

We use now the famous lemma of Zorn:

Every partially ordered set in which every chain has a lower bound, has a minimal element.

From this lemma we conclude that every component of (G_{n-1}, V_{n-1}) contains a source, and since there is only one source in G_{n-1} , (G_{n-1}, V_{n-1}) must consist of only one component, which means that (G_{n-1}, V_{n-1}) is connected.

Analogously, we can find upper bounds for chains and then, again according to Zorn's lemma, there exists a maximal element, for us a sink.

We delete one of these sinks, say t_{n-1} , and all the arcs incident to it. So we get (G_{n-2}, V_{n-2}) , and the whole process is repeated. We proceed in this way until we have $G_1 = \{s\}$.

The drain function becomes $f(t_k) = k$, $1 \leq k \leq n$ with $s = t_1$ and $t = t_n$.

Theorem 3: We have a biconnected graph (G, U) and a subset G_1 of G with $|G_1| \geq 2$. There exists a path $P[x, y] = [x, I, y]$ in (G, U) with $x \in G_1$, $y \in G_1$ and $I \cap G_1 = \emptyset$. When $G_1 \subset G$, then $I \neq \emptyset$.

Proof: In a biconnected graph there exists an elementary circuit which contains two given edges. Because (G, U) is biconnected we can find two edges $[x, z]$ and $[x', z']$ with x and x' in G_1 and z and z' in $G \setminus G_1$. C is a circuit containing these two edges. We consider the path $P'[x, x']$ on C consisting of x, I' and x' , while I' has z as its first vertex. Let y be the first vertex next to z in $P'[x, x']$ which belongs to G_1 . $P'[x, y]$ is the required path. $I \neq \emptyset$, because $z \in I$.

We call a graph (G, U) x - y -biconnected, when $x \in G$, $y \in G$ and $(G, U \cup \{[x, y]\})$ is biconnected.

Theorem 4: A connected graph (G, U) possesses a drain function with $f(s) = 1$ and $f(t) = n$ for given s and t , if and only if (G, U) is s - t -biconnected.

Proof: Assume that (G, U) is not s - t -biconnected. This means that $(G, U \cup \{[s, t]\})$ contains an articulation point a . If there exists a drain function for (G, U) , then this function will also be a drain function for $(G, U \cup \{[s, t]\})$.

I. $a = s$:

$$G_1 = \{x \mid \forall_{P[x,t]} [a \in P[x,t]]\}$$

$$\exists!_{y \in G_1} [\forall_{x \in G_1} [f(y) \geq f(x)]]$$

It is certain that $G_1 \neq \emptyset$, $s \neq y$ and $t \notin G_1$. Further, every vertex adjacent to y is an element of G_1 , thus

$$\neg \exists_{z \in G} [[y,z] \in U \wedge (f(z) > f(y))]$$

But then f is not a drain function

II. $a \neq s$:

$$G_1 = \{x \mid \forall_{P[x,s]} [a \in P[x,s]]\}$$

$$\exists_{x \in G_1} \exists_{y \in G_1} \forall_{w \in G_1} [f(x) \leq f(w) \wedge f(y) \geq f(w)]$$

Now $G_1 \neq \emptyset$ and $s \notin G_1$.

$$x = a \rightarrow \neg \exists_{z \in G} [[y,z] \in U \wedge f(z) > f(y)]$$

$$x \neq a \rightarrow \neg \exists_{z \in G} [[x,z] \in U \wedge f(z) < f(x)]$$

Again f is not a drain function.

The second half of the proof is by construction:

Find a path $P_0[s,t] = [s, I_0, t]$
in $(G, U \cup \{[s,t]\})$

$G_1 := \{s\} \cup I_0 \cup \{t\}$
 $m := |G_1|$

$f_1(s) := 1$
 $x := s$

$y :=$
 $y \in I_0 \wedge [x,y] \in P_0[s,t]$

$f_1(y) := f_1(x) + 1$

Decision: $f_1(y) = m - 1$
0 (No) / 1 (Yes)

$f_1(t) := m$

Decision: $m = n$
0 (No) / 1 (Yes)

$k := 1$

Find a path $P_k[x_k, y_k] = [x_k, I_k, y_k]$
with $x_k, y_k \in G_k \wedge f_k(x_k) < f_k(y_k) \wedge I_k \cap G_k = \emptyset$

$m := |I_k|$
 $G_{k+1} := G_k \cup I_k$

$f_{k+1}(x) := f_k(x)$ for $x \in G_k \wedge f_k(x) < f_k(y_k)$
 $f_{k+1}(x) := f_k(x) + m$ for $x \in G_k \wedge f_k(x) \geq f_k(y_k)$

$z := y_k$
 $y := y_k$

$x :=$
 $[x,y] \in P_k[x_k, y_k] \wedge x \neq z$

$f_{k+1}(x) := f_{k+1}(y) - 1$
 $z := y$

$y := x$

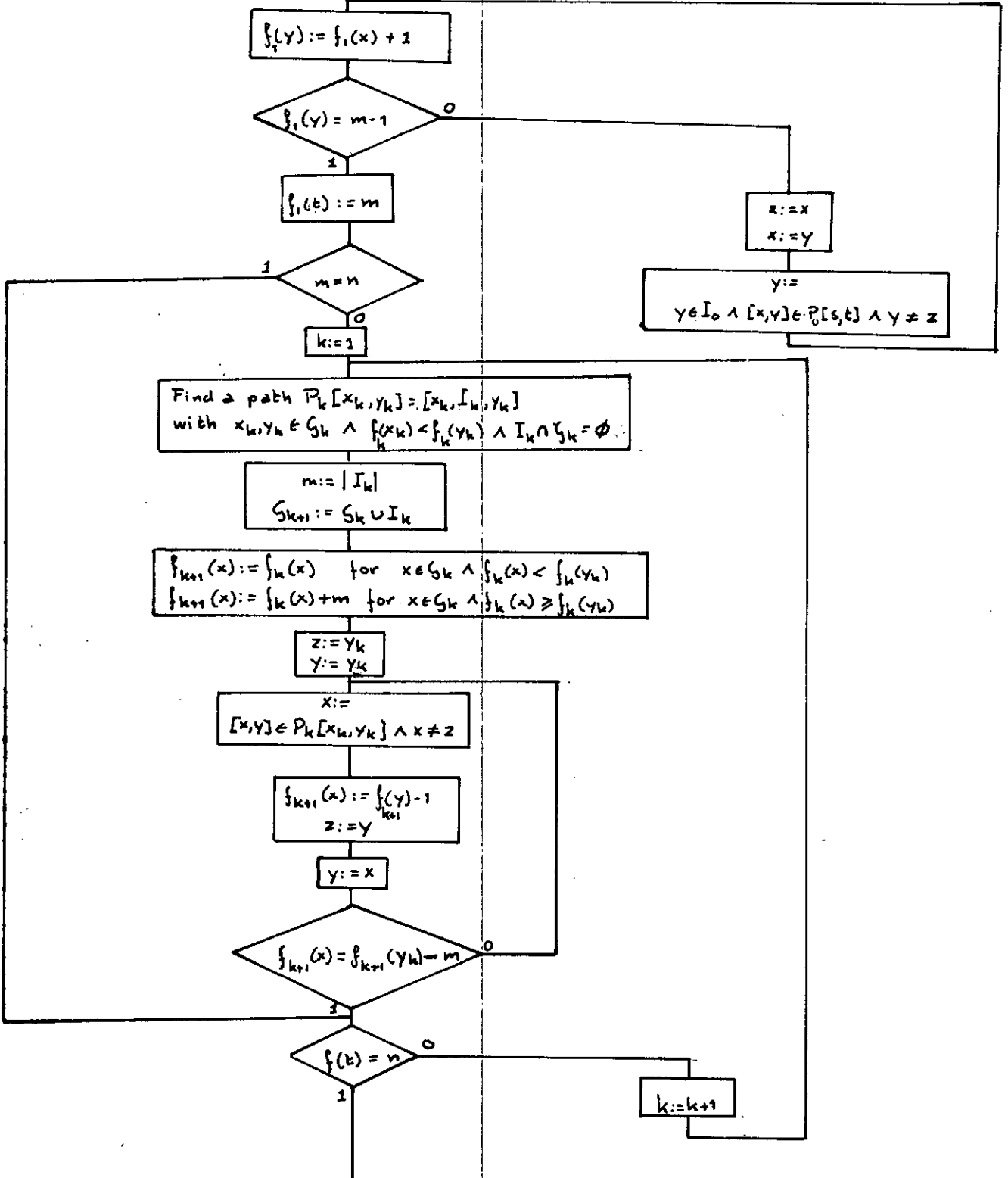
Decision: $f_{k+1}(x) = f_{k+1}(y_k) - m$
0 (No) / 1 (Yes)

Decision: $f(t) = n$
0 (No) / 1 (Yes)

$z := x$
 $x := y$

$y :=$
 $y \in I_0 \wedge [x,y] \in P_0[s,t] \wedge y \neq z$

$k := k + 1$



2. Deltas and their formulas

A digraph (G, V) is called a delta D , if it satisfies the following conditions:

1. (G, V) is acyclic,
2. $\exists!_{s \in G} [\Gamma^{-1}(s_\Delta) = \emptyset]$
3. $\forall_{t \in G} [\Gamma(t) = \emptyset \leftrightarrow |\Gamma^{-1}(t)| = 1]$
4. (G, V) has a topological representation in a plane conform the following description: α is a given straight line in that plane, all the vertices of G are on one side of α , $d(\alpha, x)$ is a distance between a vertex $x \in G$ and the line α ,
 $\forall_{x \in G} \forall_{y \in G} [[x, y] \in V \rightarrow d(\alpha, x) < d(\alpha, y)]$
 $\forall_{t \in G} \forall_{z \in G} [\Gamma(t) = \emptyset \rightarrow d(\alpha, t) \geq d(\alpha, z)]$

In the described representation we can take:

$$\forall_{t_1 \in G} \forall_{t_2 \in G} [(\Gamma(t_1) = \emptyset) \wedge (\Gamma(t_2) = \emptyset) \leftrightarrow d(\alpha, t_1) = d(\alpha, t_2)]$$

All sinks are then on a line σ parallel to the line α . σ is called the sink line. $d(\alpha, \sigma)$ is the distance between α and σ .

A connected graph is called separable, when it has at least one articulation point.

The definitions relating to connectivity are given only in the case of graphs. With respect to digraphs we use these words, when the graph which is left after replacing every arc by an edge, possesses the corresponding properties.

A section is a maximal subdigraph of a delta which contains the source s_Δ , in such a way that s_Δ is not an articulation point. Clearly, a section is a delta.

The maximal non-separable subdigraph S_c of a section S containing the source, is called the core of S . A maximal connected subdigraph of the digraph obtained by deleting all the arcs of S_c and the isolated vertices formed thereby, is called a shell of S .

Of course, every section with more than one edge has at least one shell and every shell is a delta.

Having a plane representation as described in condition 4., we can give the sections of a delta an ordering according to the incidence at s_Δ (f.e. from the left to the right): $[S^1 * S^2 * \dots * S^p]$. A similar ordering for the shells of a section, taking into account the shell-at-core incidence order, is possible: $[T^1 T^2 \dots T^q]$.

Two deltas are called similar, if they are isomorphic and if for every pair of corresponding subdeltas the same orderings have been taken. A permutation of a delta is a transformation into an isomorphic delta under preservation of the similarity of the corresponding sections. A reflection of a section is a transformation which is not trivial and results with an isomorphic section under preservation of the similarity of corresponding shells.

Theorem 1: The reflection of a section $[T^1 T^2 \dots T^q]$ is given by $[T^q T^{q-1} \dots T^1]$.

Proof: Let S be a section and S_c its core. H is a subset of the set of vertices in S such that: $H = \{s, h_1, h_2, \dots, h_q\}$ with s as the source of S , h_i as the source of T^i . Clearly S_c is H -accessible. The plane representations of S_c satisfying condition 4. must be H -periphere. Theorem 5 in "Graphtheoretical notions" gives directly the rest of the proof.

From now on in this paper we assume that with every vertex x there is associated a label $\ell(x)$. The mapping ℓ from G in some label alphabet L is not injective; this means that the labels of distinct vertices can be the same. Two digraphs are called L -isomorphic, if they are isomorphic and the corresponding vertices possess the same labels. In our case we take for the elements of L positive integers.

The sinks of a delta possessing the lowest label are called index sinks. Their labels are called index labels. A delta D is called normalisable, if it may be transformed into an L -isomorphic delta D' such that all the index sinks are together on the sink line without another sink in between. D' is called the normal form of D .

Theorem 2: Every normalisable delta may be normalised by a successive application of permutations and reflections.

Proof: When D is a normalisable delta, then there exists a delta D' which is L-isomorphic to D and which is in normal form. Consider any pair of corresponding sections, and if the shell ordering is not the same, then make it so by reflection (theorem 5 in "Graphtheoretical notions"). Next consider any pair of corresponding subdeltas, and if the section ordering is not the same, then make it so by permutation. After noting that the transformations do not impair each other, the theorem will be clear.

Consider now a delta which is in normal form. On this delta we perform the following reductions:

1. identify all index sinks with one new vertex r for which $d(\alpha, r) < d(\alpha, \sigma)$, without introducing crossings,
2. add a new vertex t' to the delta on the sink line in such a way that not-neighbour-sinks in the original delta are not neighbours after adding t'.
3. adjoin a new arc [r, t'] between the new vertices,
4. assign the index label of the original delta to r and to t'.

The obtained digraph is again a delta, and it is called the reduced form of the original delta.

Elements of L, parentheses and asterisks are the symbols in the formula ϕ of a delta which can be defined recursively:

1. the formula of a section consisting of one arc is equal to the label of the sink:

$$S = (\{x, y\}, \{[x, y]\}) \rightarrow \phi = \mathcal{L}(y)$$

2. the formula of a delta with p sections is as follows

$$D = [S^1 * S^2 * \dots * S^p] \rightarrow \phi = (\phi^1) * (\phi^2) * \dots * (\phi^p)$$

where ϕ^i is the formula of S^i . ϕ is called the product of $\phi^1, \phi^2, \dots, \phi^p$. (ϕ^i) is called a factor of ϕ .

3. the formula of a section with q shells is as follows

$$S = [T^1 T^2 \dots T^q] \rightarrow \phi = (\phi^1) (\phi^2) \dots (\phi^q)$$

and now ϕ^i is the formula of T^i . ϕ is called the concatenation of $\phi^1, \phi^2, \dots, \phi^q$.
(ϕ^i) is called a component in ϕ .

Remark: It is obvious that only sink labels enter the formula, and that they appear in the same order as the corresponding sinks on the sink line.

Sometimes (not always) we can drop some of the parentheses in a formula without losing information:

1. $((\phi))$ can be replaced by (ϕ) ,
2. (ϕ) where ϕ is a single label, can be replaced by ϕ ,
3. (ϕ) where (ϕ) is a factor in a product, and ϕ is a concatenation, can be replaced by ϕ .

The meaning of the transformations permutation and reflection for the formula is clear. Permutation is effected through a permutation of the factors in some product. Reflection is effected through a reversing of the order of the components in a concatenation which is either a factor in some product or a single component in some other concatenation.

A formula is in normal form, if all of its index labels are together only interlaced with asterisks and parentheses. It is easy to see that the formula of a delta is in normal form if and only if the delta is in normal form (see the remark at the end of the definition of a formula).

A formula is called normalisable, if it may be transformed into a normal form by a successive application of permutations and reflections. Knowing the effect of the transformations on formulas and deltas it is also clear, that a delta is normalisable if and only if its formula is normalisable.

We now want to define the reduction of a formula in normal form in such a way that for any delta in normal form the reduced form of its formula is equal to the formula of its reduced form. This means that we have to translate the identification of the index sinks in a proper way. First we give a gradation to the parentheses of a formula.

A parenthesis is called weak, if it is placed between two index labels (ignoring asterisks and other parentheses). A weak parenthesis which is not enclosed by a pair of parentheses of which one parenthesis at least is weak, is called a main weak parenthesis.

The reduction rules become:

1. If ϕ_i contains an index label, and it is the first or the last factor of a product bordered by a pair of parentheses, at least one of which is a main weak one (marked by an apostrophe), then

$$(\dots * \phi_i)' \rightarrow (\dots) \phi_i$$

$$'(\phi_i * \dots) \rightarrow \phi_i(\dots)$$

2. if ϕ_i contains an index label and it is a concatenation bordered by a pair of parentheses, at least one of which is a main weak one (marked by an apostrophe), then

$$'(\phi_i)' \rightarrow \phi_i$$

$$(\phi_i)' \rightarrow \phi_i$$

$$'(\phi_i) \rightarrow \phi_i$$

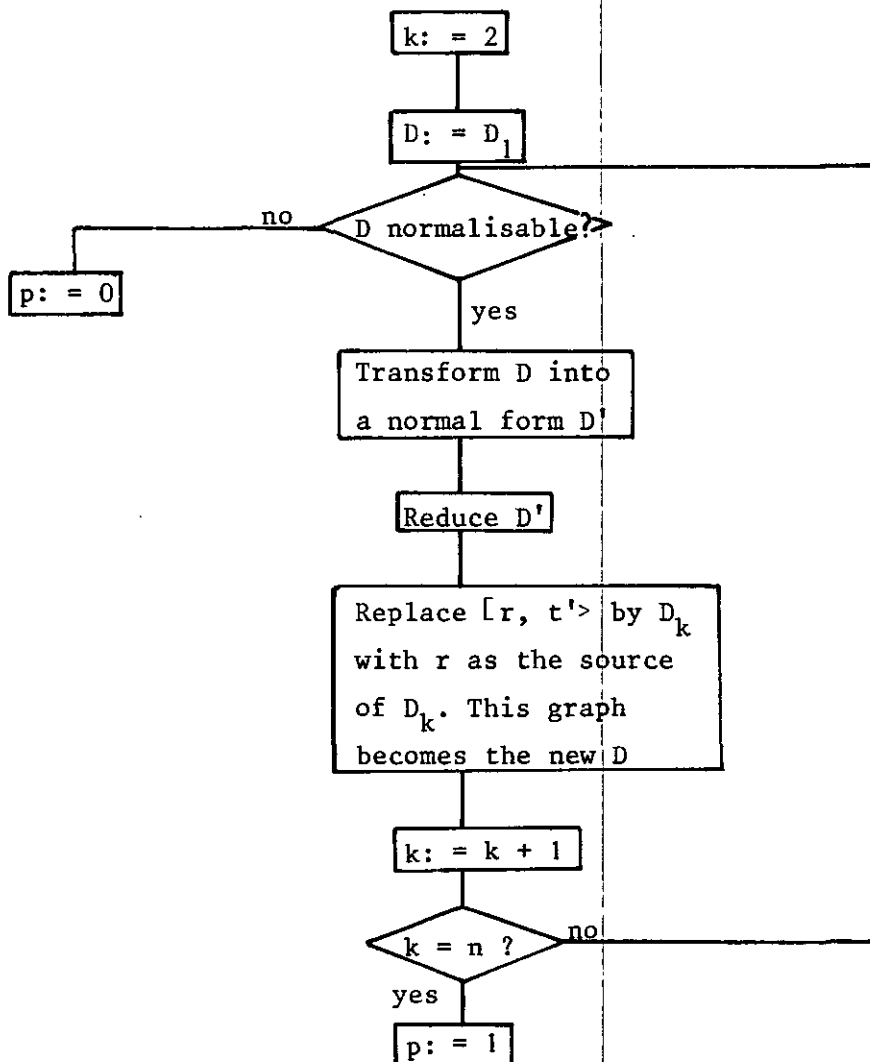
3. apply 1. and 2. recursively until all index labels are no longer interlaced with parentheses,
4. replace all the index labels by one single index label. The resultant formula is the reduced form of the original normal form.

3. The CEL-algorithm

From theorem 4 in "Assigning a drain function to a graph" we know that it is no restriction on the generality, when we assume that a biconnected graph which is to be tested for planarity, is a drain with the source and the sink connected by an arc. In such a graph we define a basic set of $(n - 1)$ deltas:

$$D_k = (\{Z^{-1}(k)\} \cup \Gamma(Z^{-1}(k)), \{[Z^{-1}(k), x] \mid x \in \Gamma(Z^{-1}(k))\}) \text{ for } 1 \leq k < n$$

With the following rules we generate from the basic set a set of deltas, and we give the so-called planarity-bit p a value 0 or 1:



Since we are dealing with deltas, the described procedure must have an analogue for formulas. First the basic set of formulas:

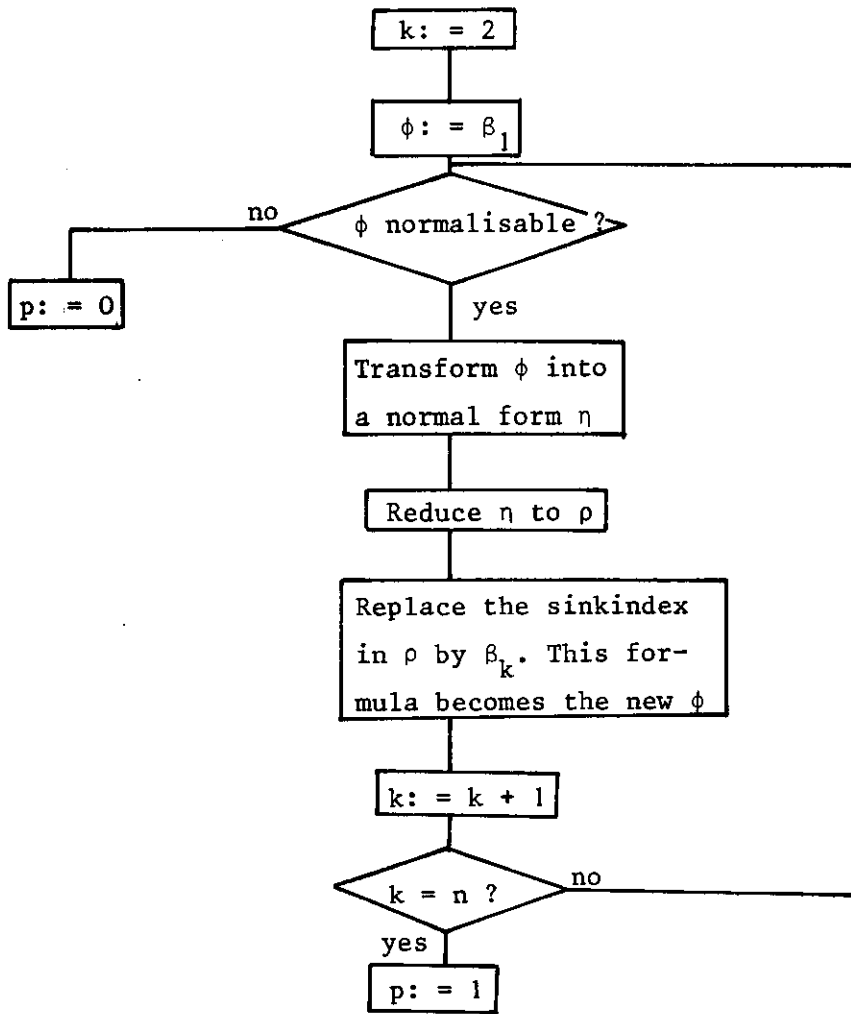
$$\beta_k = \mathcal{L}(x_1) * \mathcal{L}(x_2) * \dots * \mathcal{L}(x_m) \text{ with } x_i \in \Gamma(\mathcal{L}^{-1}(k))$$

$$i \neq j \rightarrow x_i \neq x_j$$

$$m = |\Gamma(\mathcal{L}^{-1}(k))|$$

for $1 \leq k < n$

The generation of the formulas declines as follows



At this point we emphasise the fact that the generation procedure for a given drain is not unique, simply because the normalisation need not be unique. A delta may possess several normal forms. The following theorem states that, no matter how the normalisation is done, this will have no influence on the value of p at the end of the generation.

Theorem 1: Given an arbitrary drain, then every generation gives the same value to the planarity-bit.

Proof: Suppose that there is a generation R' which gives p the value 0 and there is a generation R , which gives p the value 1, both belonging to the same drain. This means that we meet in the procedure R' a non-normalisable formula ϕ' and a corresponding non-normalisable delta D' . There must be an L -isomorphic delta D in the generation R with its formula ϕ . These are however normalisable, since the procedure R ends with $p = 1$. This is a contradiction.

Finally we have to give a proper interpretation of the planarity-bit. Doing this the next lemma turns out to be helpful.

Consider a planar drain $D = (G, V)$, D' is a planar representation of D ; $D'(k) = (G'_k, V'_k)$ is defined by:

$$D'(k) = (\{x \mid x \in G' \wedge l(x) \leq k\}, \{[x, y] \mid [x, y] \in V' \wedge l(x) \leq k \wedge l(y) \leq k\})$$

By a face of a planar representation of a graph we mean a set of points in the plane that can be connected to each other by a Jordancurve, disjoint from the graph.

Theorem 2: For any plane representation D' of a planar drain D , and every $0 < k \leq n$, all vertices belonging to $G' \setminus G'_k$ are contained in the same face of $D'(k)$.

Proof: The theorem is trivial for $k \leq 2$ and $k \geq n - 1$. Suppose the theorem is not true for some k $2 < k < n - 1$. This means that the sink t of the drain is in one face and there are other vertices in $G' \setminus G'_k$ in another face. Among these there has to be a vertex with a maximal label, and this vertex has to be a sink. Since there is only one sink in a drain, our assumption must be false.

Theorem 3: Given a drain D , then this drain is planar, if and only if there is a generation R for D which gives the planarity-bit the value 1.

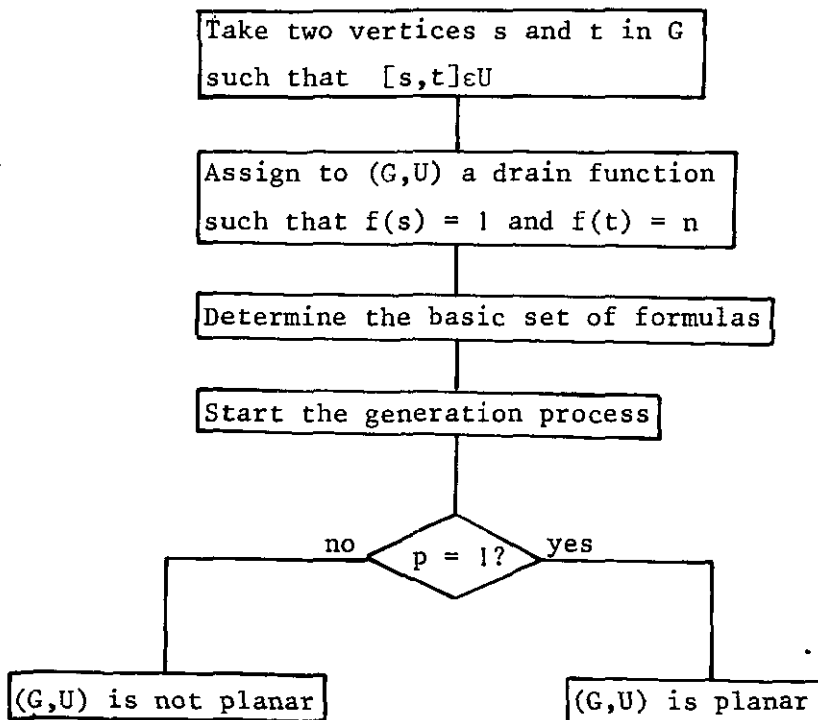
Proof: That D is planar when $p = 1$, is clear from the generation, for the last generated delta is equal to the given drain, when we remove the last formed arc $[r, t']$.

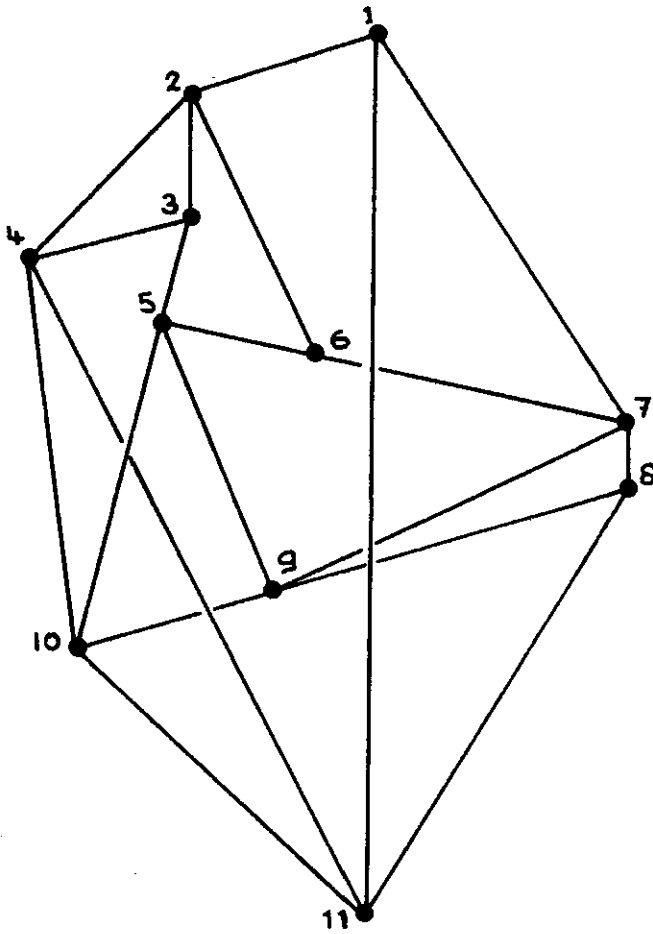
Now suppose that D is planar and D' is a planar representation of it such that $[s, t]$ is on the boundary of the outer face. We assume that

$$\forall x \in D' \setminus \{s, t\} [d(\alpha, t) > d(\alpha, x) \wedge d(\alpha, s) < d(\alpha, x)]$$

According to theorem 2 all vertices of $G' \setminus G'_k$ are lying in the outer face of $D'(k)$. Under this condition all the successive $D'(k)$ in the generation can be drawn on the plane in a way that condition 4 of the delta definition is fulfilled. They form the whole set of deltas of the generation procedure, so the theorem follows.

The CEL-algorithm can be given in the following schematic way:





$$\beta_1 = 2 * 7 * 11$$

$$\beta_2 = 3 * 4 * 6$$

$$\beta_3 = 4 * 5$$

$$\beta_4 = 10 * 11$$

$$\beta_5 = 6 * 9 * 10$$

$$\beta_6 = 7$$

$$\beta_7 = 8 * 9$$

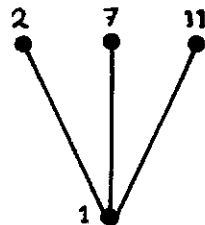
$$\beta_8 = 9 * 11$$

$$\beta_9 = 10$$

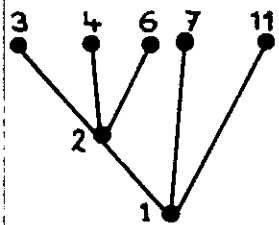
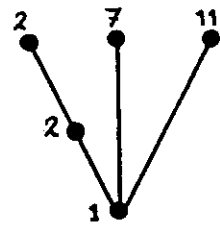
$$\beta_{10} = 11$$

4. Two examples

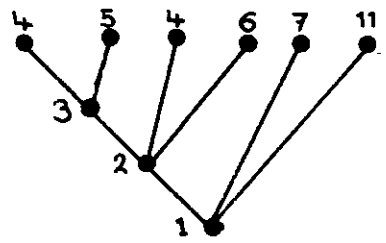
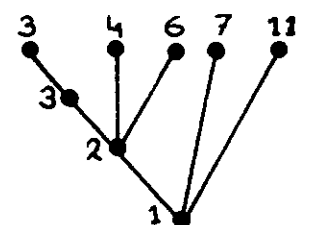
In this section we give two examples, one planar graph and one non-planar graph.



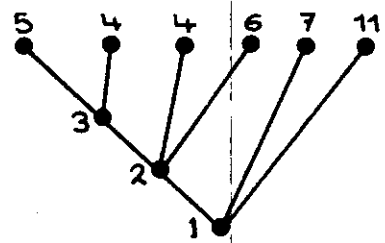
$$\beta_1 = \mathcal{S}_2 = 2 * 7 * 11 = \eta_2 = \mathcal{S}_2$$



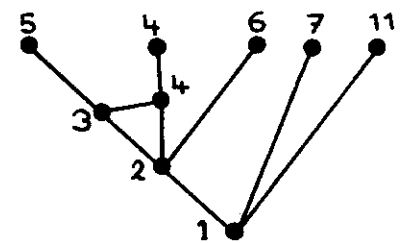
$$\mathcal{S}_3 = (3 * 4 * 6) * 7 * 11 = \eta_3 = \mathcal{S}_3$$



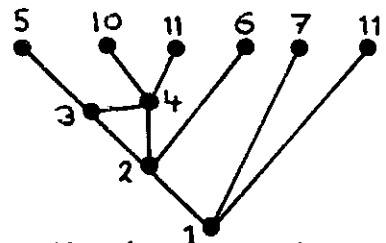
$$\mathcal{S}_4 = ((4 * 5) * 4 * 6) * 7 * 11$$



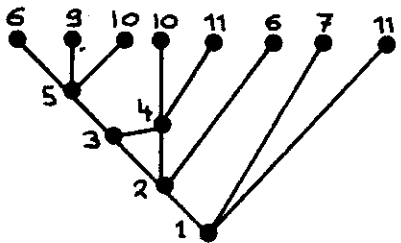
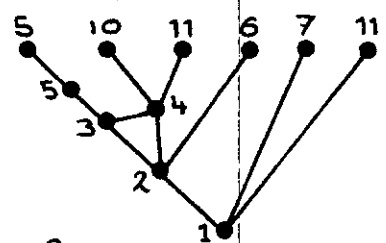
$$\eta_4 = ((5 * 4) * 4 * 6) * 7 * 11$$



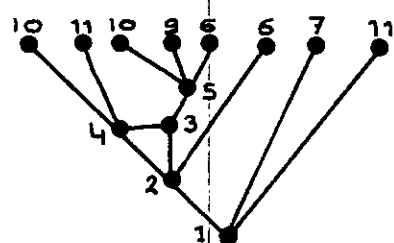
$$\mathcal{S}_4 = (5 * 4 * 6) * 7 * 11$$



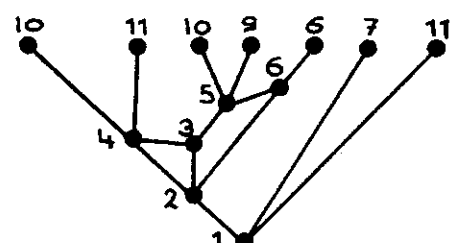
$$\mathcal{S}_5 = (5(10 * 11) * 6) * 7 * 11 = \eta_5 = \mathcal{S}_5$$



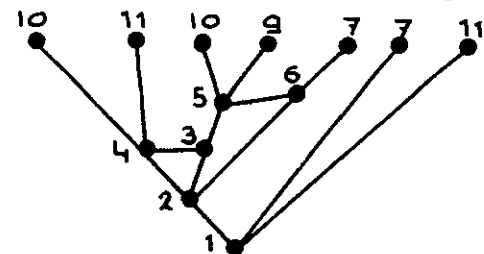
$$\mathcal{S}_6 = ((6 * 9 * 10)(10 * 11) * 6) * 7 * 11$$



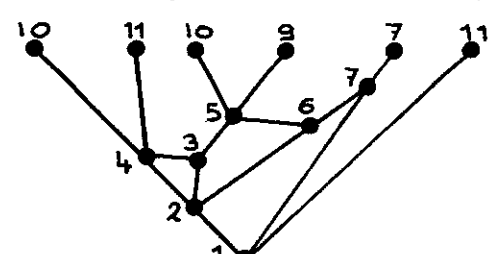
$$\eta_6 = ((10 * 11)(10 * 9 * 6) * 6) * 7 * 11$$



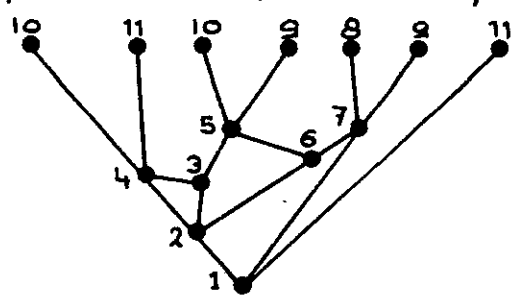
$$\mathcal{S}_6 = ((10 * 11)(10 * 9) 6) * 7 * 11$$



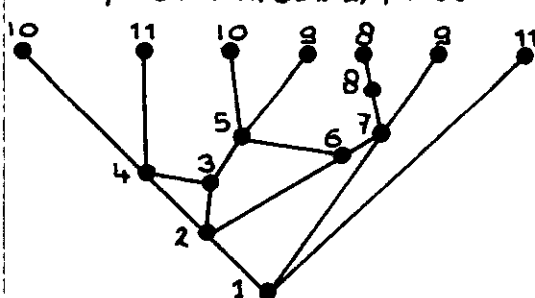
$$\mathcal{S}_7 = ((10 * 11)(10 * 9) 7) * 7 * 11 = \eta_7$$

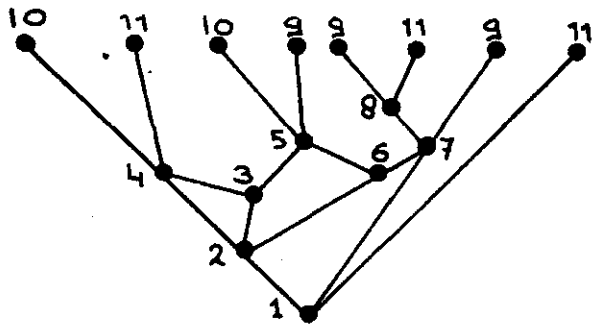


$$\mathcal{S}_7 = (10 * 11)(10 * 9) 7 * 11$$

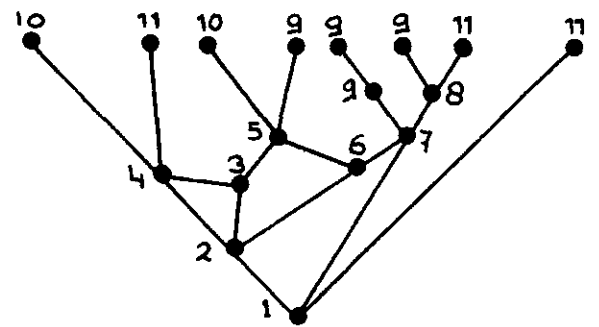


$$\mathcal{S}_8 = (10 * 11)(10 * 9)(8 * 9) * 11 = \eta_8 = \mathcal{S}_8$$

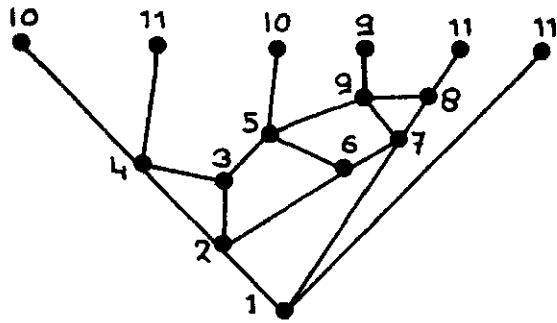




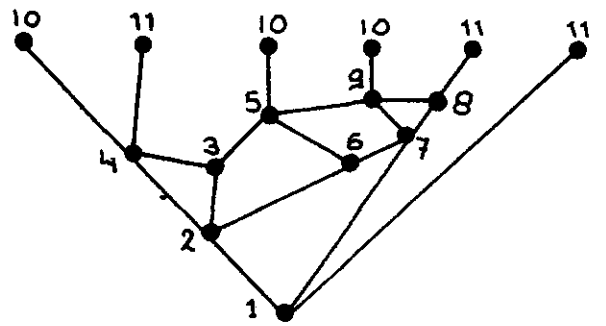
$$\mathcal{S}_9 = (10 * 11)(10 * 9)(9 * 11) * 9 * 11$$



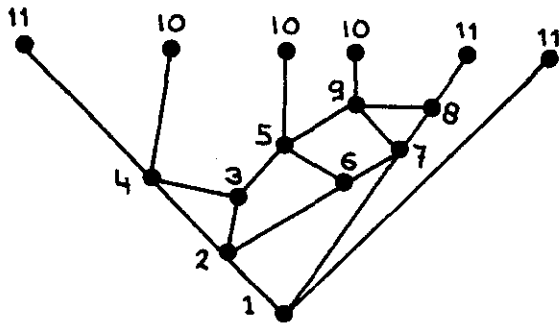
$$\eta_9 = (10 * 11)(10 * 9)(9 * (9 * 11)) * 11$$



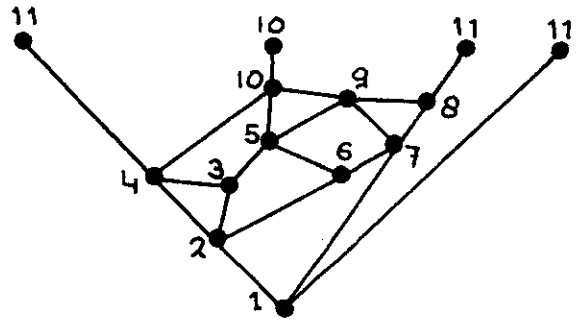
$$\mathcal{S}_9 = (10 * 11) 10 9 11 * 11$$



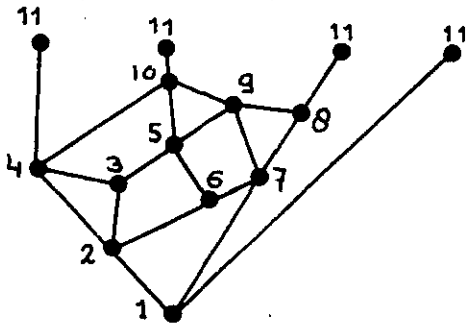
$$\mathcal{S}_{10} = (10 * 11) 10 10 11 * 11$$



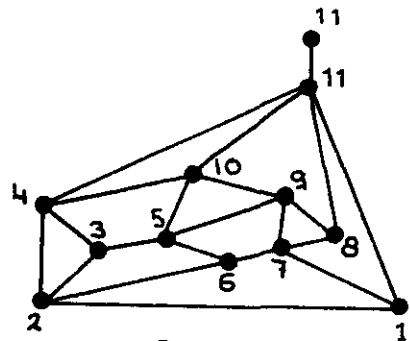
$$\eta_{10} = (11 * 10) 10 10 11 * 11$$



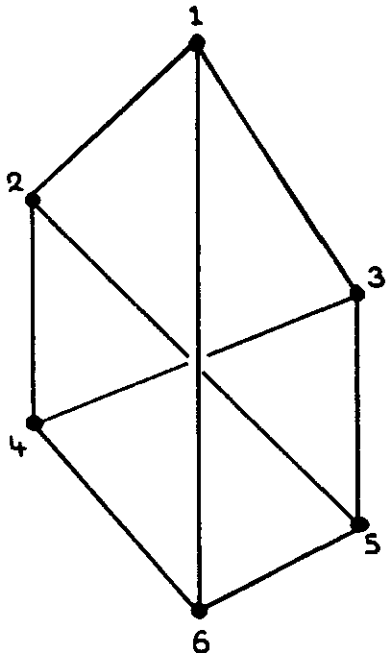
$$\mathcal{S}_{10} = 11 10 11 * 11$$



$$\mathcal{S}_{11} = 11 11 11 * 11 = \eta_{11}$$



$$\mathcal{S}_{11} = 11$$



$$\beta_1 = 2 * 3 * 6$$

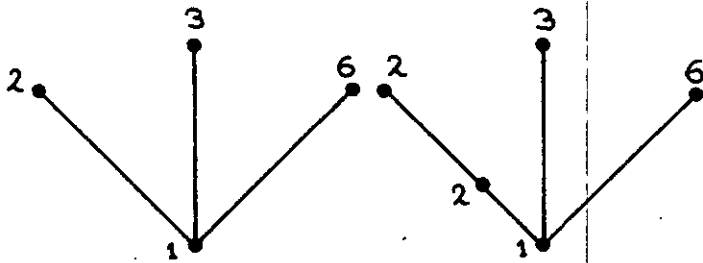
$$\beta_2 = 4 * 5$$

$$\beta_3 = 4 * 5$$

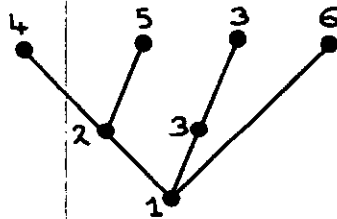
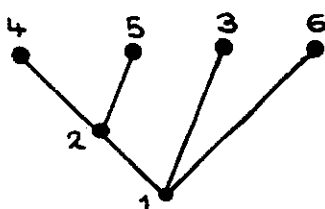
$$\beta_4 = 6$$

$$\beta_5 = 6$$

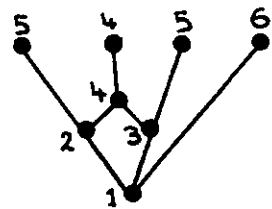
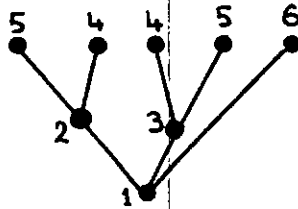
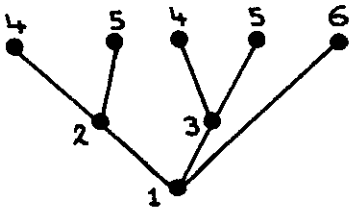
The non-planar example



$$\beta_1 = \beta_2 = 2 * 3 * 6 = \beta_2$$



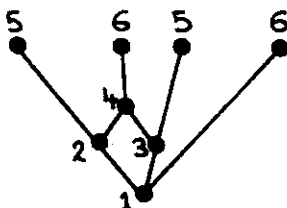
$$\beta_3 = (4 * 5) * 3 * 6 = \eta_3 = \beta_3$$



$$\beta_4 = (4 * 5) * (4 * 5) * 6$$

$$\eta_4 = (5 * 4) * (4 * 5) * 6$$

$$\beta_4 = 5 * 4 * 5 * 6$$



$$\beta_5 = 5 * 6 * 5 * 6$$

REFERENCES

- [1] Lempel, A., Even, S., Cederbaum, J., "An algorithm for planarity testing of graphs", Theory of Graphs, Intern. Symposium, pp.215-232, Rome, 1966

VI. OTHER PLANARITY ALGORITHMS

1. A planarity-test based on an iterative decomposition method ("pseudo-Hamiltonian method").

Our starting point is the (connected and) nonseparable graph (G, U) .

$S \subseteq U$ is a segregate set, which divides G into two disjoint proper subsets G_I and G_{II} . $\{S_i\}$ is a set of disjoint cutsets such that $S_1 \cup S_2 \cup \dots \cup S_n = S$

The subgraph (G_I, U_I) exists such that: $\forall_{x \in G_I} \forall_{y \in G_I} [x, y] \in U_I \rightarrow [x, y] \in U$

Define a set of subgraphs (G_i, U_i) of (G, U) such that:

- 1) $G_{II} = G_1 \cup G_2 \cup \dots \cup G_n$; $G_i \cap G_j = \emptyset$
- 2) $U = U_I \cup D \cup S \cup U_1 \cup U_2 \cup \dots \cup U_n$; $U_i \cap U_j = \emptyset$; $U_i \cap S = \emptyset$; $U_i \cap U_I = \emptyset$; $U_I \cap S = \emptyset$; $U_i \cap D = \emptyset$
 $\forall_{x \in G_I} \forall_{y \in G_I} [x, y] \in U \wedge [x, y] \notin U_I \leftrightarrow [x, y] \in D$
- 3) $\forall_{x \in G_i} \forall_{y \in G_i} [x, y] \in U \rightarrow [x, y] \in U_i$
- 4) $\forall_{[x, y] \in S_i} [x \in G_i \vee y \in G_i]$
- 5) (G_i, U_i) is connected.

The subgraphs (G_i, U_i) can be constructed by deleting all the vertices G_I and all the edges which are incident to these vertices.

Let (G, U) and (H, C) be graphs and let ϕ be a mapping from G onto H : ϕ is called a homomorphic mapping or a homomorphism if:

- 1) $\forall_{h_i \in H} [(\phi^{-1}(h_i), \{[x, y] \mid x \in \phi^{-1}(h_i) \wedge y \in \phi^{-1}(h_i) \wedge [x, y] \in U\})$ is connected]
- 2) $[h_i, h_j] \in C \leftrightarrow \exists_{x \in \phi^{-1}(h_i)} \exists_{y \in \phi^{-1}(h_j)} [x, y] \in U$

" (G, U) is homomorphic to (H, C) " if there exists a homomorphism from G onto H .

Notation: $(G, U) \succ (H, C)$

For example (H, C) can be created by "contraction" of some subgraphs (G_i, U_i) of the original graph (G, U) !

Consider the homomorphic mapping from $(G_I \cup G_{II})$ onto $(G_I \cup H)$:

$$(G, U) \succ (G_I \cup H, U_I \cup S \cup D)$$

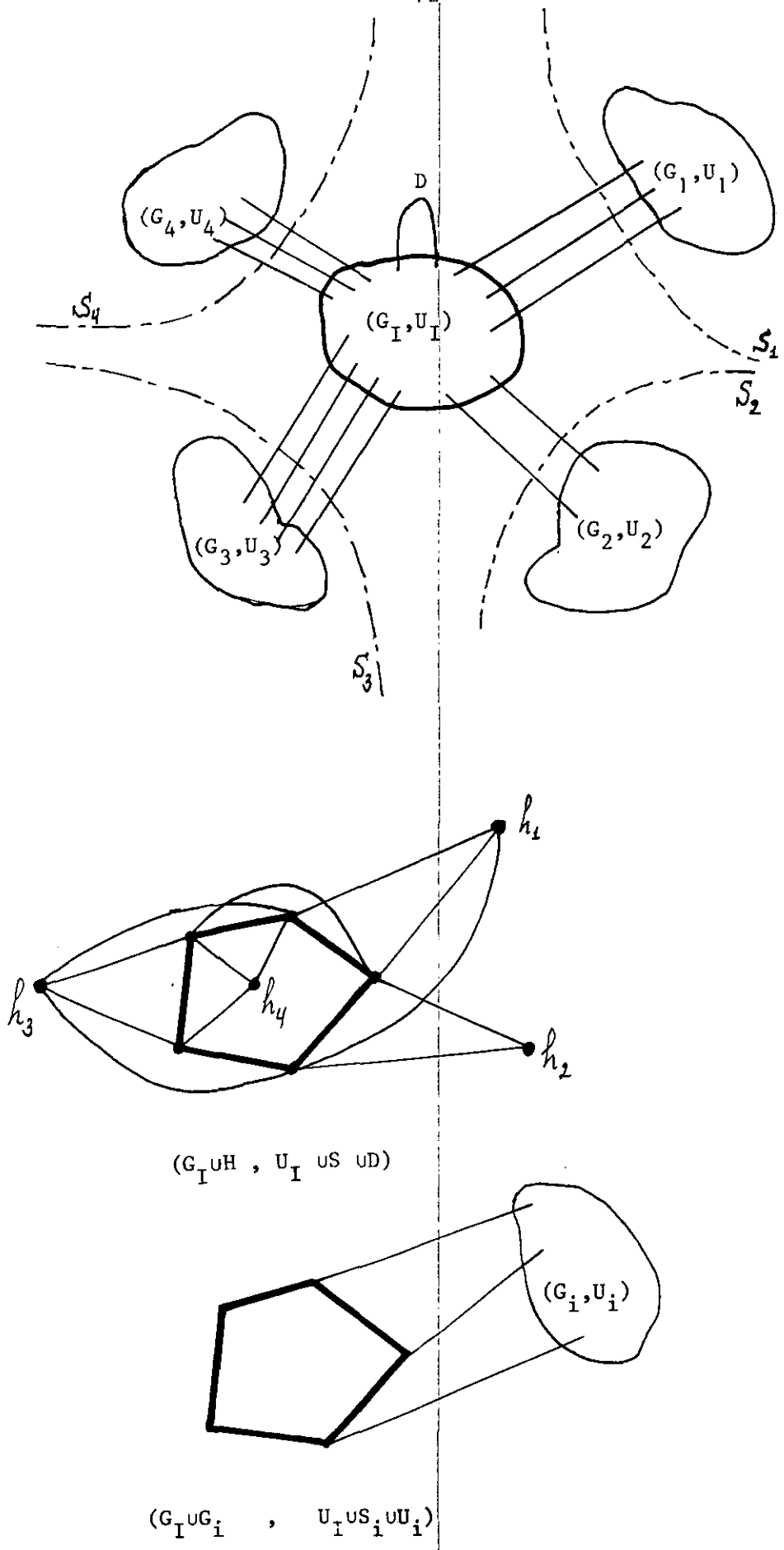
Theorem 1:

In a connected nonseparable graph (G, U) let a segregate set S and two associated subsets of G , G_I and G_{II} , be chosen such that (G_I, U_I) defined above, is a (chordless) circuit, C . Then, necessary and sufficient conditions for (G, U) to be planar are that $(G_I \cup H, U_I \cup S \cup D)$ and $\{(G_I \cup G_i, U_I \cup S_i \cup U_i)\}$ are planar.

Proof: 1) Assume (G, U) is planar. Then all its subgraphs are planar. Thus $(H \cup G_I, S \cup U_I \cup D)$ and $\{(G_I \cup G_i, U_I \cup S_i \cup U_i)\}$, which are subgraphs of (G, U) are planar.

2) Assume that $(H \cup G_I, S \cup U_I \cup D)$ and $\{(G_I \cup G_i, U_I \cup S_i \cup U_i)\}$ are planar (Note that from the definition each $(G_I \cup G_i, U_I \cup S_i \cup U_i)$ and each (G_i, U_i) is connected). Since all (G_i, U_i) have no edges incident to each other, the addition to the planar graph $(H \cup G_I, S \cup U_I \cup D)$ of each (G_i, U_i) will remain planar if each $(G_I \cup G_i, U_I \cup S_i \cup U_i)$ is planar. The latter is one of our starting points. Therefore (G, U) is planar.

In the literature the graph $(H \cup G_I, S \cup U_I \cup D)$ is often called "pseudo-Hamiltonian graph" and each $(G_I \cup G_i, U_I \cup S_i \cup U_i)$ "decomposed subgraph" of (G, U) . Deleting the set of edges U_I decomposes the graph (G, U) into a union of edge-disjoint subgraphs, denoted as the "bridges" of C in (G, U) . The above-mentioned (decomposition) theorem suggests an iterative algorithm for testing whether a graph is planar or not. Given a graph (G, U) , we find a circuit C , form the corresponding pseudo-Hamiltonian graph and test the planarity of the latter graph. The planarity of each decomposed subgraph ($i = 1, 2, \dots, n$) is then tested by the decomposition theorem in a subsequent iteration (see fig.2).



$(G_I \cup H, U_I \cup S \cup D)$

$(G_I \cup G_i, U_I \cup S_i \cup U_i)$

Fig. 1. Partitioning according to theorem 1.

Planarity-test by iterative decomposition:

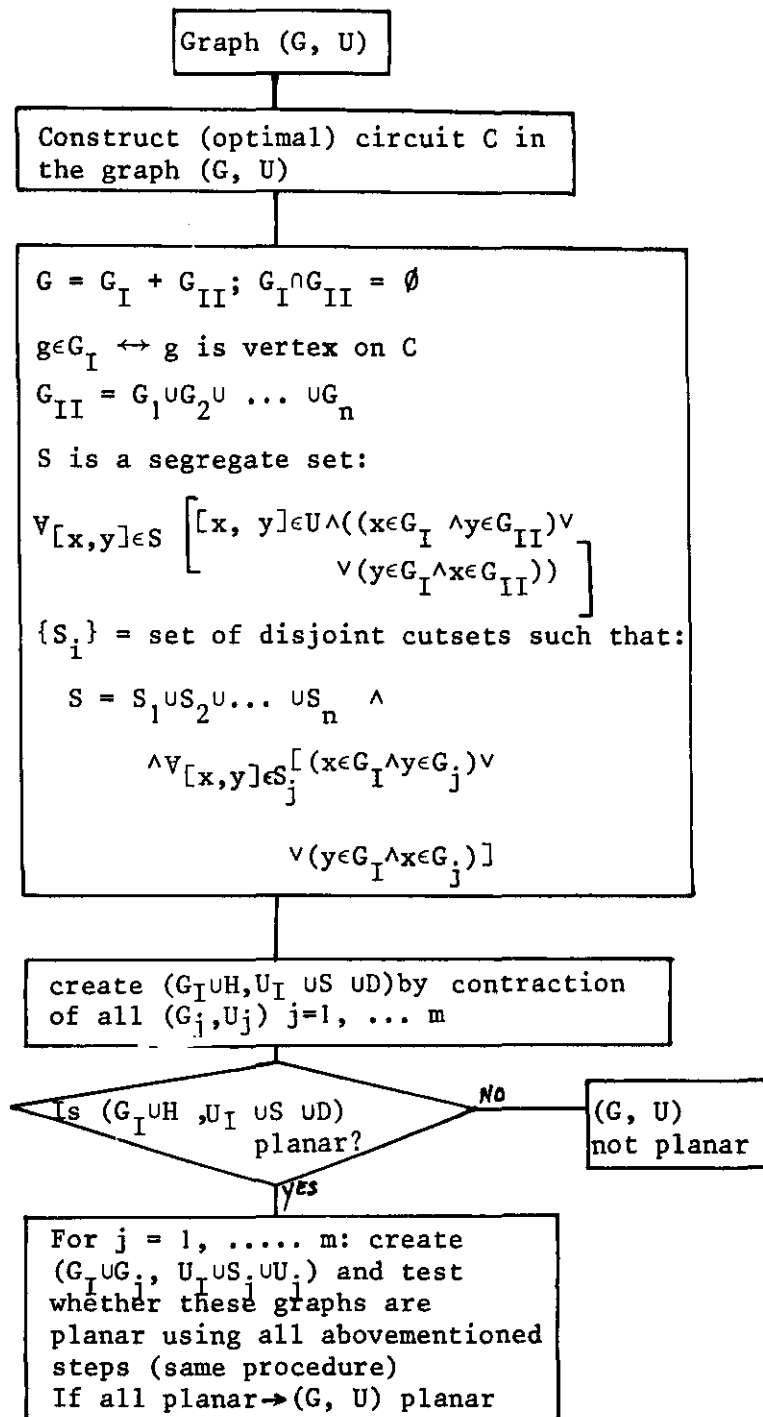


Fig. 2.

Thus the problem of testing the planarity of an arbitrary graph can be reduced essentially to the problem of testing the planarity of a pseudo-Hamiltonian graph. The requirements that the latter graph is planar, is equivalent to the requirement that its bridges can be mapped on the inside and the outside of C in such a manner that no two edges on the same side cross. The vertices of a bridge which are common to C will be called "vertices of attachment" of the bridge. Assume that there are at least two such vertices (otherwise the bridge can be separated from C) and that they are ordered in a clockwise sense on C . The successive vertices in this ordering divide C into a set of edge-disjoint paths. We say that bridge b' does not alternate with bridge b , if all the vertices of attachment of b' lie on a path defined by two successive vertices attachment of b . Otherwise, we say that b' alternates with b . Notice that in a planar graph, the bridges which alternate must be mapped on opposite sides of C . On the other hand, bridges which do not alternate are not so constrained and may be mapped on either the same or on opposite sides of C . From this knowledge the following theorem is clear.

Theorem 2:

A pseudo-Hamiltonian graph is planar if and only if its bridges can be associated with two disjoint classes I and O , such that no two bridges in the same class alternate.

This theorem expresses the condition that the pseudo-Hamiltonian graph be planar in terms of the symmetric binary relation, "alternation", which is defined on the set B of bridges. To examine this relation we form an (undirected) alternation graph (G_a, U_a) , such that:

- 1) For every element in B there corresponds a vertex in G_a
- 2) b_i alternates with $b_j \leftrightarrow [g_i, g_j] \in U_a$

It is clear that for every pseudo-Hamiltonian graph, there is a unique alternation graph (relative to the circuit C). In general, the alternation graph will consist of several connected components.

Def. A bipartite graph is a graph in which the vertex set G decomposes into two disjoint sets G_1 and G_2 such that each edge connects an element of G_1 with an element of G_2 .

Theorem 3:

The necessary and sufficient condition that the pseudo-Hamiltonian graph be planar is that its alternation graph is bipartite.

The proof follows directly from theorem 2.

The following procedure may be used to determine whether a graph is bipartite or not. Construct a spanning forest of the alternation graph. Assign to an arbitrary vertex of the tree the plussign. The vertices which are connected with the plussign via one edge obtain a minus-sign (and vice versa). In this way the sign of each vertex of the alternation graph is uniquely fixed. The graph is bipartite if and only if all remaining edges are incident to two vertices with opposite sign.

Another procedure is the following: Choose a vertex of the alternation graph and assign to this vertex the plussign. Assign this minussign to each vertex which is connected to the plussign via one edge. If there exists an edge between any two elements of this set of minussign-vertices, then the graph is not bipartite. If this is not the case, then choose one of the last set of assigned vertices and assign the opposite sign to the vertices which are connected with the chosen vertex via one edge. If there exists an edge between any of these vertices (the last set of assigned vertices) and any other vertex with the same sign, then the graph is not bipartite. The procedure is going on until all vertices have a sign. It is possible that in a particular step, there are no other edges going out from any vertex of the last set of assigned vertices. Then the procedure is started again for the vertices which are left (which have no sign).

The property of alternation also makes it possible to implement the decomposition on the computer using matrix notation. To illustrate this let us consider the incidence matrix A of the pseudo-Hamiltonian graph. Arrange the rows and columns of this matrix A in such a manner that the property of alternation can be determined by inspection. The leading rows and columns correspond to the vertices and edges of C in a natural sequence. The edges of attachment of each bridge are grouped together and placed next (ending with the bridges consisting of only one edge, namely the edge between two vertices of C).

To determine whether two bridges alternate. We examine the submatrix of A whose rows correspond to the vertices of C, and whose columns correspond to the bridges. This matrix is called the attachmentmatrix H, and can be divided into submatrices A_i of H which correspond to the bridges b_i :

$$H = [A_1 A_2 A_3 \dots A_n]$$

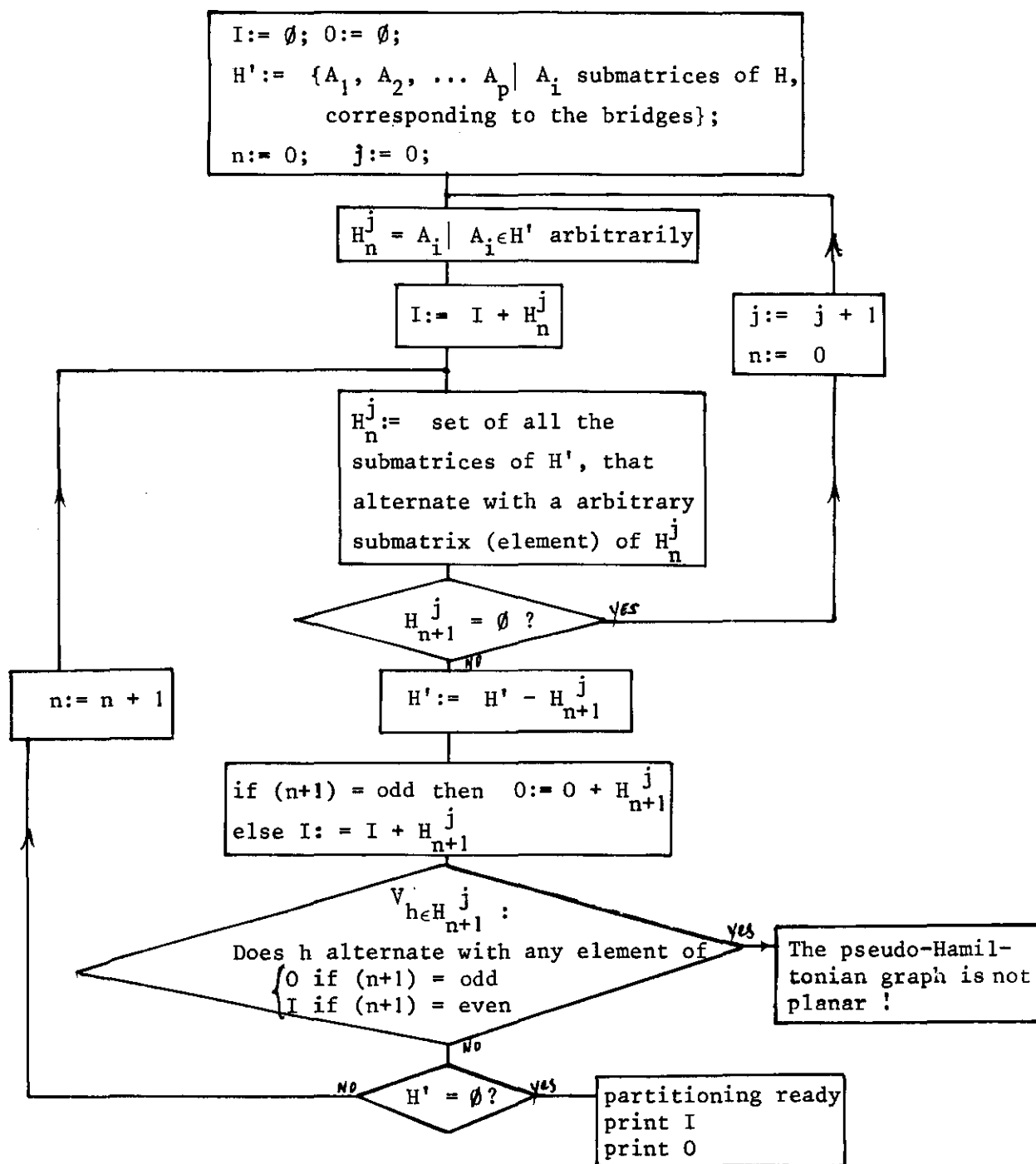
Let A_i and A_j be two distinct submatrices of H. Then, A_i does not alternate with A_j , if all of the nonzero rows of A_i are bounded by the same two successive nonzero rows of A_j . From the above-mentioned theorem 2 we now can state:

The pseudo-Hamiltonian graph is planar if its attachmentmatrix can be partitioned $H = [I:O]$, where no two submatrices A_i, A_j in a partition I of O alternate.

A partitioning-algorithm of the attachment matrix is given below.

Partitioning-algorithm of the attachment matrix H of a pseudo-Hamiltonian graph

(Note that this algorithm is like the second procedure which tests the bipartiteness of the alternation graph).



The above-described partitioning of H takes the form

$$H = [H_0^0 H_1^0 \dots H_k^0 H_1^1 \dots H_p^1 H_0^2 \dots]$$

2. Planarity-tests based on matrix methods

A; Some graph-theoretical notions

Before defining the "dual graph", let us define some other notions and properties of these notions.

Nullity (cyclomatic number):

The nullity of a graph with m edges, n vertices and p components is $\mu = m - n + p$.

Rank: The rank of a graph with m edges, n vertices and p components is $n - p$.

Theorem 1: The nullity of a graph is equal to the maximum number of independent circuits.

Proof: Let us build up the graph edge by edge, starting with a graph consisting of the vertices of the graph, isolated one from the other. Adding a new edge connecting two vertices a and b of the graph which are connected by a path in the graph, will increase the nullity by one (the nullity will not alter in other cases $a \neq b$), and the addition closes new circuits. Suppose that before adding the edge e_k we had obtained a fundamental basis containing the circuits C_1, C_2, \dots ; and that after the edge e_k has been added we have formed the new circuits: C'_1, C'_2, \dots . Clearly C'_1 cannot be expressed linearly in terms of the C_i (since it contains an edge which is not contained in the C_i); on the other hand C'_2, C'_3, \dots can be expressed linearly in terms of the C_i and C'_1 . So, each time the nullity is increased by one the maximum number of linear independent circuits increases by one.

Corollary 1: A graph contains no circuits if and only if its nullity is zero.

Corollary 2: A graph possesses a unique circuit if and only if its nullity is one.

Cut-set:

A cut-set is a set of edges of a connected graph (G, U) such that the removal of these edges from (G, U) reduces the rank of (G, U) by one, provided that no proper subset of this set reduces the rank of (G, U) by one when it is removed from (G, U) .

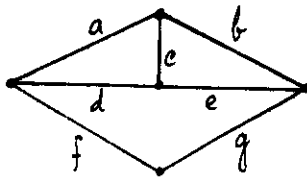
Dual graphs:

(G_2, U_2) is a dual of (G_1, U_1) if there is one-to-one correspondence between the edges of the two graphs, such that if (H_1, E_1) is any subgraph of (G_1, U_1) and (H_2^*, E_2^*) is the complement of the corresponding subgraph of (G_2, U_2) , then

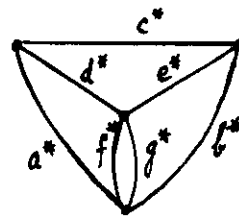
$$r_2 = R_2 - \mu_1$$

where r_2 and R_2 are ranks of (H_2^*, E_2^*) and (G_2, U_2) , respectively, and μ_1 is the nullity of (H_1, E_1)

Example of a dual graph:

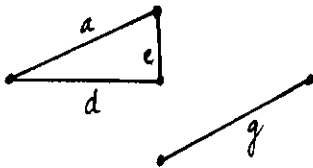


(G_1, U_1)

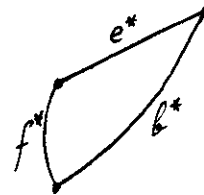


(G_2, U_2)

$$\begin{aligned} r_2 &= 2 \\ R_2 &= 3 \\ n_1 &= 1 \end{aligned}$$



(H_1, E_1)



(H_2^*, E_2^*)

Theorem 2: If (G_1, U_1) and (G_2, U_2) are dual graphs, circuits in either graph correspond one-to-one with cut-sets in the other.

Proof: Assume C to be a circuit in (G_1, U_1) . Consider this circuit as the subgraph (H_1, E_1) in the definition of a dual graph. Since the nullity of a circuit is one (theorem 1), the rank of the complement of the corresponding subgraph is exactly one less than the rank of graph (G_2, U_2) . Since no proper subset of a circuit is a circuit, no proper subset of the corresponding set of edges of the circuit reduces the rank of (G_2, U_2) with one by removing these edges.

So the set of edges of the circuit is a cut-set.

Assume a set of edges to be a cut-set of (G_2, U_2) . Removal of this set of edges reduces the rank of (G_2, U_2) with one. The corresponding subgraph in (G_1, U_1) will have nullity one (according to the definition of a dual graph). Since a cut-set is a minimal set, the corresponding subgraph in (G_1, U_1) which contains a circuit (Cor. 2) contains no subgraph containing a circuit. Hence this subgraph is a circuit itself. Since the edges of this circuit are uniquely determined by the edges of the cut-set, this circuit is uniquely determined.

B. Planarity-tests (for relatively small graphs)

Let us start from a connected graph (G, U) with the following properties

1. the relation Γ is antireflexive (no loops);
2. U is a set of non-ordered pairs of vertices, called edges, (so the graph is not a multigraph).

a. We first of all give a planarity-test which is based on the theorem of Whitney: A graph is planar if and only if it has a dual.

Write $U = T \cup L$ in which $T =$ set of edges which form a spanning tree
 $|G| = n; |T \cup L| = m$ $L =$ set of edges which are the links

The nodal incidence matrix can be given in the following form:

$$A = (a_{ij}) = \begin{pmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{pmatrix} \begin{matrix} i = 1, 2, \dots, n \\ j = 1, 2, \dots, m \end{matrix}$$

in which the edges which belong to the columns of the matrix A_{12} form a spanning tree. This means that matrix A_{12} is non-singular, so its inverse exists. The edges which belong to the columns of matrix A_{11} form the set L of links.

Reduced form of the nodal incidence matrix (deletion of one row):

$$A = (a_{ij}) = (A_{11} \ A_{12}) \quad i = 1, 2, \dots, n-1 \quad j = 1, 2, \dots, m.$$

Each of the $(m-n+1)$ links of the tree defines a loop of the graph, called fundamental loop of the graph. The fundamental loops define a $(m-n+1) \times m$ matrix B_f ; if the edges of the graph are numbered so that the links of the tree form the first $(m-n+1)$ edges, and if the fundamental loops are numbered corresponding, B_f will be of the form:

$$B_f = \begin{pmatrix} I_{m-n+1} & F \end{pmatrix} \quad T = \text{transposing} \\ \text{in which } F = -A_{11}^T \cdot (A_{12}^{-1})^T \quad \text{Additions modulo 2.}$$

Each edge of a spanning tree of a connected graph segregates the vertices into two sets; the corresponding cut of the graph consists of that particular tree-edge together with certain links of the tree. The set of $(n-1)$ cuts obtained in this way from a tree is called the fundamental set of cuts and define a $(n-1) \times m$ matrix C_f ; if the edges of the graph are numbered so that the last $(n-1)$ columns correspond to the tree, and if the cuts are numbered correspondingly, then C_f will be of the form:

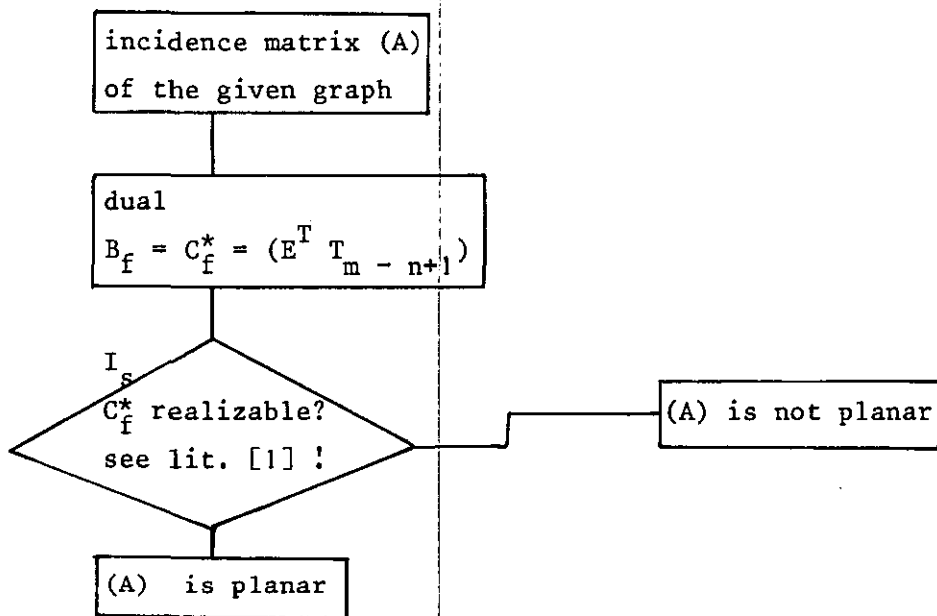
$$C_f = \begin{pmatrix} E & I_{n-1} \end{pmatrix} \\ \text{in which } E = -F^T = A_{12}^{-1} \cdot A_{11}$$

The planar graph (G, U) has a fundamental cut-matrix C_f and a fundamental loop-matrix B_f . The dual graph (G^*, U^*) has a fundamental cut-matrix C_f^* and a fundamental loop-matrix B_f^* .

From the duality of circuit and cut-set it now is clear that:

There exists a one-one-corresponding mapping of the edges of the graphs (G, U) and (G^, U^*) such that $C_f = B_f^*$ and $B_f = C_f^*$*

The algorithm now is of the following form:



lit [1] : Tutte, W.T.,
From matrices to graphs,
Can. J of Math., vol. 16, pp. 108-127 (1964).

- b. The following planarity-test is based on the theorem of McLane:
Given a nonseparable connected graph (G, U) of m edges and n vertices having circuit matrix B . A necessary and sufficient condition for the graph to be planar is that it have a circuit-basis together with one additional circuit (together forming submatrix B_m) such that this collection of circuits contains each edge of the graph exactly twice.
Testing the rows of the circuit matrix of the graph, taking $m-n+2$ rows

at a time involves a too big amount of labor. Let us therefore use two basic topological properties:

1. each row of B_m (circuit set) corresponds to the set of edges that comprise the boundary of a region produced when the planar graph is mapped on the sphere;
2. (based on intuition). If all the circuit sets of a planar graph are considered, the circuit sets that bound the regions will predominately have fewer edges than those circuit sets whose edges do not together bound a single region. Consequently one can test the rows of the circuit matrix of a planar graph, giving preference to circuit sets having a small number of edges, and thereby realize more quickly the submatrix B_m .

Let us introduce the following definitions

Def. 1: Edge Ordered Circuit Matrix B_e : A circuit matrix of a graph is edge ordered when a given row has at least as many 1's as the preceding row.

Def. 2: Edge Set Vector E : An edge set vector E of an edge ordered circuit matrix B_e of N rows is a column matrix having N elements with its k th element corresponding to the k th row of B_e , and having numerical value equal to the number of 1's in that row of B_e (Each k th entry of E is the number of edges in the k th circuit set of B_e).

Def. 3: Circuit Combination Vector C_k : Consider a graph of m edges and n vertices, which has an edge ordered circuit matrix B_e of N rows. A circuit combination vector of B_e is a row vector of N elements of which $m-n+2$ elements have value 1 while the remaining elements have value 0.

Def. 4: Primitive Circuit Combination Vector C_p : A primitive circuit combination vector is a circuit combination vector in which there is no more than one 0 between the first and last 1 entry in the vector.

Each row of B_e represents a circuit set having as many edges as, or fewer edges than, the circuit set represented by any subsequent row. We are interested in evaluating rows of B_e , $m-n+2$ at a time. Consequently a set of rows under consideration can be represented by the circuit combination vector C_k .

All possible combinations of rows of a circuit matrix taken $m-n+2$ at a time can be represented by a systematic listing of M circuit combination vectors (f.e. reading columnwise from top to bottom).

Note that: $C_k E =$ total number of edges (including repeated edges) in the circuit sets of B_e represented by C_k .

For a planar graph we know that a submatrix B_m exists having exactly two 1's per column (thus m columns gives a total of $2m$ edges) (McLane).

Lemma 1:

Given a nonseperable connected graph (G, U) having m edges and edge set vector E . Then (G, U) is planar only if there exists a circuit combination vector C_j such that:

$$C_j E = 2m$$

If we identify any primitive circuit combination vector in the systematic listing of all circuit combination vectors, we observe that each given 1 element in all the vectors following the primitive vector is either in the same position or moved to the right of the position it occupied in the primitive primitive vector.

Lemma 2:

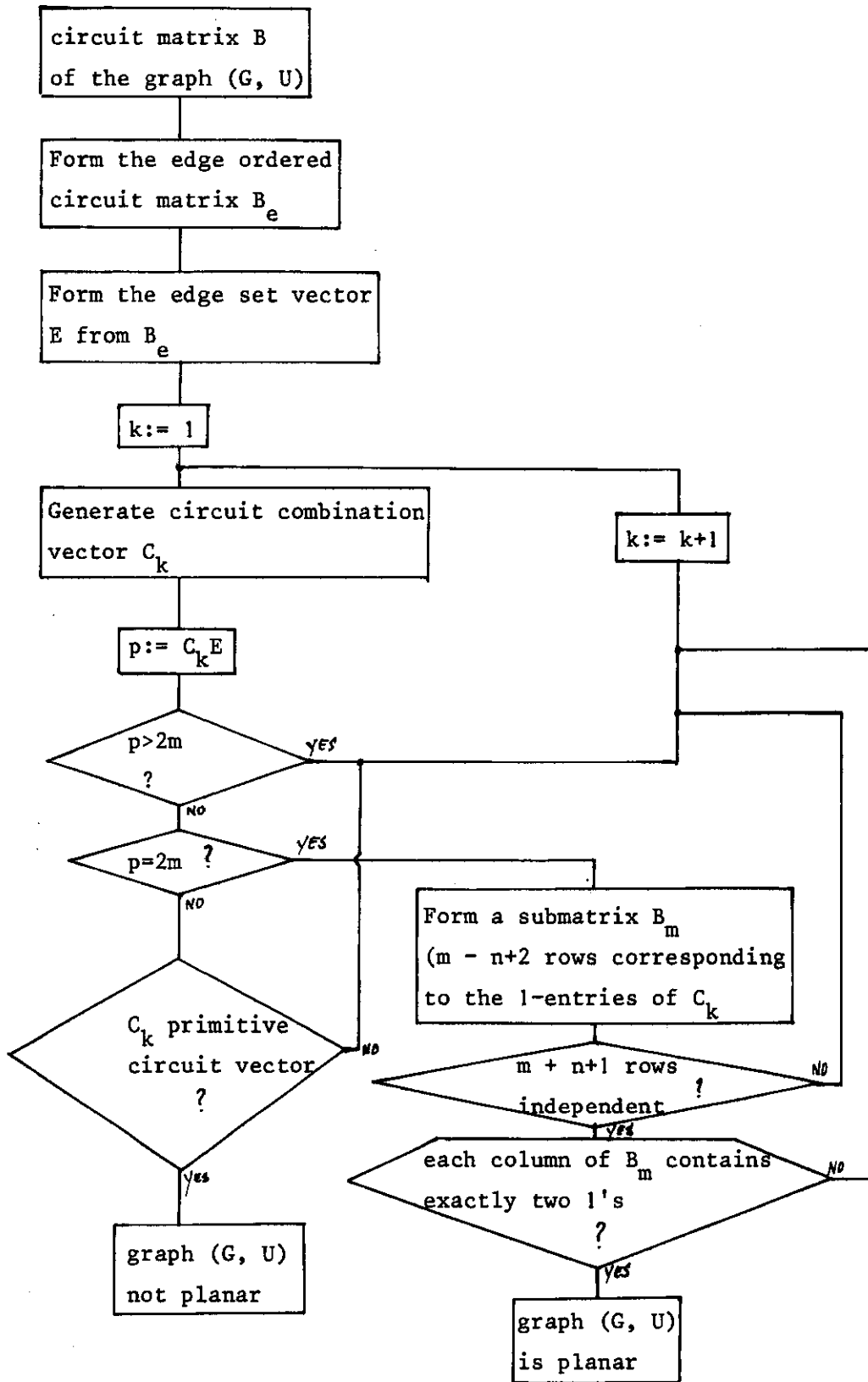
Given edge set vector E a primitive circuit combination vector C_p and any subsequent circuit combination vector C_q (i.e. $q > p$). If $C_p E = m$ and $C_q E = n$, then $n > m$ (m and n being pos. integers).

Lemma 3:

Given a nonseperable, connected graph (G, U) , having m edges and edge set vector E . Consider systematically listed circuit combination vectors $C_1, C_2, \dots, C_{p-1}, C_p$, where C_p is a primitive circuit combination vector. (G, U) is nonplanar when a) C_1, C_2, \dots, C_{p-1} does not satisfy the above-mentioned theorem of McLane, and b) $C_p E > 2m$.

Proof: for a) The theorem includes necessary conditions for a planar graph for b) We note from Lemma 2, all C_{p+r} listed subsequent to C_p will have a product greater than $2m$. Hence Lemma 1 is not satisfied. Since neither a) nor b) satisfy necessary conditions for a planar graph, the graph must be nonplanar.

Using above-mentioned Lemmas, the planarity-test-algorithm must have the following form:



3. The whirl method

In the mathematical formulation of the problem we introduced a method of taking care of the following constraints:

1. certain terminals must be at the periphery of the graph;
2. these terminals have to appear in a previously specified order.

We will now translate the problem including these requirements into a graph like problem, ending up with a structure which is called a "whirl" i.e. a set of vertices, a set of arcs, and a set of edges.

1. Construct the potential graph in the usual way (thus without the extensions to examine the constraints).
2. Determine the simple graph of the obtained graph. This will be the graph to test on planarity, since we may conclude from the result whether the potential graph is planar.
3. Take now the - let us say t - terminals that should be at the periphery in a specified sequence, and number them in such a way that terminal i should be a neighbour of $i-1$ and $i+1 \pmod{t}$.
4. If terminal i is connected with terminal $i+1$ by an edge, then replace this edge by an arc from terminal i to terminal $i+1$, else add an arc from terminal i to terminal $i+1 \pmod{t}$.

We assume that the constructed "whirl" is biconnected (this is not a restriction, if we are able to treat the components not containing arcs in the same way. We will see that this is true).

The planarity test is an iterative one, i.e. the test is a special partitioning of the whirl in "sub-whirls" which must be partitioned in the same way, until only digraphs with vertices of indegree 1 are left. If the partitioning of one of the "whirls" appears to be impossible the original whirl is not planar. The partitioning should decline according to the following eight rules:

1. Search for a path $P[x,y]$ where x and y are the only "periphery" terminals. x and y divide the set of arcs into two chains C_1 and C_2 . The vertices are numbered from x to y by "path-indices".
2. Now we have to consider the sub whirls and subgraphs that are obtained by applying the following operations:

- Remove the edges that have only path vertices as terminal vertices, and that are not from $P[x,y]$.

They are a first set of subgraphs (each consisting of one edge).

- Next remove all edges of $P[x,y]$. This may give several components. For each component we examine whether a subset of the vertices of $P[x,y]$ is an articulation set for this component. If so then separate this component on these vertices, and consider the connected subgraphs as a second set.

3. The whirl is not planar, if now C_1 and C_2 are still in one component.
4. We'll call the whirl containing C_1 S_1 and the one containing C_2 S_2 . The other are numbered S_3, S_4, \dots, S_p .
5. Assign to each subgraph S_i an array L_i of the indices of the path-vertices contained in S_i ; $l_i = \min \{L_i\}$ $m_i = \max \{L_i\}$

6. Construct an auxiliary graph (H, U') :

$$H = \{S_1, S_2, \dots, S_p\}; [S_i, S_j] \in U' \leftrightarrow \exists_{(\alpha, \beta) \in L_i \times L_j} [(l_i < \beta < m_i) \wedge (l_j < \alpha < m_j)]$$

7. Test whether (H, U') is bipartite, and if so divide H into two sets H_1 and H_2 such that

$$[a, b] \in U' \leftrightarrow ((a \in H_1 \wedge b \in H_2) \vee (a \in H_2 \wedge b \in H_1))$$

else the whirl is not planar.

8. Split the whirl into two whirls by

1. replacing all edges of $P[x,y]$ by two parallel arcs with opposite orientations.
2. Separate the whirl now on the vertices of $P[x,y]$ (this is an articulation set) in such a way that each whirl contains a cycle and one whirl contains all $S_i \in H_1$ and the other all $S_i \in H_2$.

We end this description by adding two remarks:

- the big advantage of this method is that it gives as a result a face-oriented representation of the graph, but it is a relatively slow test, since it always consists of a number of partitions that is equal to the number of edges minus the number of vertices;
- if one wants to test a graph instead of a whirl, this is possible by starting with replacing an arbitrary edge by two parallel arcs with opposite orientations.

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VII. THE PLANARISATION OF NONPLANAR NETWORKS

1. TERMINALVALUES

A convenient way of describing an n-terminal-network is by the n x n-resistance- or n x n-conductance-matrix. For some reason the latter is chosen, and it will be called the S-matrix.

$$\begin{bmatrix} i_1(t) \\ i_2(t) \\ \vdots \\ i_n(t) \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \dots & S_{1n} \\ S_{21} & S_{22} & \dots & S_{2n} \\ \vdots & \vdots & & \vdots \\ S_{n1} & S_{n2} & \dots & S_{nn} \end{bmatrix} \begin{bmatrix} v_1(t) \\ v_2(t) \\ \vdots \\ v_n(t) \end{bmatrix} \quad \text{or } I = S V \quad (1)$$

In these equations the current entering the network via terminal p is denoted by $i_p(t)$, while $v_q(t)$ is the voltage between terminal q and some freely chosen reference.

Two n-terminal-networks are called equivalent if and only if their S-matrices are identical.

The S-matrix always enjoys two properties which are direct consequences of the Kirchhoff-laws:

- The Kirchhoff-current-law says that, irrespective of the terminal-voltages, the sum of all entering currents is 0. This means for a voltage-vector $(0, 0, \dots, v_j, \dots, 0)$, that we have:

$$\sum_{i=1}^n i_i(t) = \sum_{i=1}^n \{s_{ij}\} v_j = 0 \rightarrow \sum_{i=1}^n s_{ij} = 0 \quad (2)$$

- Since the choice of the reference-voltage has no influence on the currents, we can write for arbitrary a

$$\begin{aligned} i_i(t) &= \sum_{j=1}^n \{s_{ij} \cdot v_j(t)\} = \sum_{j=1}^n \{s_{ij} (v_j(t) + a)\} = \\ &= \sum_{j=1}^n \{s_{ij} \cdot v_j(t)\} + a \sum_{j=1}^n s_{ij} \end{aligned}$$

and conclude

$$\sum_{j=1}^n s_{ij} = 0 \tag{3}$$

We now direct our attention to special classes of n-terminal-networks. The star connected-R-networks represent one of these classes.

A star connected-R-network, for short a "star", is an n-terminal-network, consisting of n conductances and one node which is not available as a terminal and with which every terminal is connected by means of one conductance. The conductance between terminal i and the "inner node" is denoted by G_i .

Let the auxiliary entity G be defined by

$$G = \sum_{i=1}^n G_i \tag{4}$$

The entries of the S-matrix of such a network are:

$$\left. \begin{aligned} s_{ij} &= -\frac{G_i G_j}{G} \text{ for } i \neq j \\ s_{ij} &= G_i - \frac{G_i^2}{G} \text{ for } i = j \end{aligned} \right\} \tag{5}$$

Note that, if the network structure is a star, the correspondence between the network and its S-matrix is one-one [5].

At this moment we fulfil the first part of our promise and define the terminalvalue ϕ_i for stars:

$$\phi_i = \frac{G_i}{\sqrt{G}} \tag{6}$$

Using (6) and (2) or (3) we can rewrite (5) as:

$$\left. \begin{aligned}
 s_{ij} &= -\phi_i \phi_j && \text{for } i \neq j \\
 s_{ij} &= \phi_i \sum_{\substack{p=1 \\ p \neq i}}^n \phi_p && \text{for } i=j
 \end{aligned} \right\} \quad (7)$$

So far our discussion of star-networks. We now proceed with the polygon-connected-R-networks, here called "polygons". This is an n-terminal-network without "inner nodes" in which each terminal is connected with every other terminal by one conductance. The number of conductances is equal to $\frac{1}{2}n(n-1)$. We write $G_{i,j}$ for the conductance between the terminal i and j.

Again we express the matrix-entries in the conductancevalues:

$$\left. \begin{aligned}
 s_{ij} &= -G_{i,j} && \text{for } i \neq j \\
 s_{ij} &= \sum_{\substack{p=1 \\ p \neq i}}^n G_{i,p} && \text{for } i=j
 \end{aligned} \right\} \quad (8)$$

It is also true, that in case we are dealing with polygon-networks the the correspondence between the network and its S-matrix is one-one.

At this point let us agree upon the following convention:

- We consider the indices as residue-classes (mod n); this means that we make no difference between p and q, when $p - q = k.n$ for some integer k. We write $p \equiv q$.

Consider now polygons that satisfy the following conditions:

- The value of

$$\frac{G_{i,x} G_{i,y}}{G_{x,y}} \quad (9)$$

is independent of the choice of x and y . Of course cases with $x \equiv i$, $y \equiv i$ and $x \equiv y$ are excluded, since $G_{i,i}$ does not have a meaning. We will refer to this kind of polygons as T-polygons.

The set of conditions (9) is highly redundant. In the appendix we will give an equivalent system of mutually independent equations.

The special property (9) of a T-polygon makes it possible to associate with every terminal i a value: the terminal-value ψ_i

$$\psi_i = \frac{\sqrt{G_{i,x}} \sqrt{G_{i,y}}}{\sqrt{G_{x,y}}} \tag{10}$$

The importance of this definition becomes clear when we look at the identity:

$$\psi_i \psi_j = \frac{\sqrt{G_{i,j}} \sqrt{G_{i,p}}}{\sqrt{G_{j,p}}} \cdot \frac{\sqrt{G_{i,j}} \sqrt{G_{j,p}}}{\sqrt{G_{i,p}}} = (\sqrt{G_{i,j}})^2 = G_{i,j}$$

With this equation and (2) or (3), we have for T-polygons:

$$\left. \begin{aligned} s_{ij} &= -\psi_i \psi_j && \text{for } i \neq j \\ s_{ij} &= \psi_i \sum_{\substack{p=1 \\ p \neq i}}^n \psi_p && \text{for } i=j \end{aligned} \right\} \tag{11}$$

Comparing (7) and (11) with each other we come to the conclusion that every star is transformable into a T-polygon, and conversely that every T-polygon is transformable into a star. In both cases we only have to take the terminalvalues of corresponding terminals identical.

Now the question arises: "Are there polygon-networks, having an equivalent star without being a T-polygon?" The answer will be clear from the following reasoning:

Suppose there is such a polygon, then find its equivalent star. Since every star can be transformed into an equivalent T-polygon, it is possible to give a T-polygon equivalent to the original polygon which was not a T-polygon.

This contradicts with the one-one-correspondence between polygons and their S-matrices.

The main theorem is proved now:

EVERY STAR IS TRANSFORMABLE INTO A POLYGON AND A POLYGON IS TRANSFORMABLE INTO A STAR IF AND ONLY IF THE POLYGON IS A T-POLYGON.

The transformation formulas are:

Star-into-polygon-transformation

$$\sum_{i=1}^n G_i = G; \phi_i = \frac{G_i}{\sqrt{G}}; G_{i,j} = \phi_i \phi_j \quad (12)$$

T-polygon-into-star-transformation

$$\psi_i = \frac{\sqrt{G_{i,x}} \sqrt{G_{i,y}}}{\sqrt{G_{x,y}}}; \sum_{i=1}^n \psi_i = \Psi; G_i = \psi_i \Psi = \sum_{\substack{j=1 \\ j \neq i}}^n G_{i,j} + \psi_i^2 \quad (13)$$

The last formula will be clear after noting that $\sum_{i=1}^n \psi_i = \sqrt{G}$

Sometimes it will be profitable to permit negative conductances.

In case $G_{i,j} < 0$ we write

$$G_{i,j} = \sqrt{-1} \sqrt{-G_{i,j}}$$

At the end of a procedure like (13) the exponent of -1 will be even. If it is quadruple, we replace it by a plus-sign and otherwise by a minus-sign. However, it is possible that the situation with $G = 0$ occurs. Since the S-matrix is not properly defined then, the presented approach is not adequate. For T-polygons the corresponding case is $\Psi = 0$. This condition is equivalent to:

$$\sum_{i=2}^n \frac{G_{i,p}}{G_{1,p}} \neq -1$$

Every star with $G \neq 0$ is transformable into a polygon and a polygon is transformable into a star if and only if the polygon is a T-polygon with

$$\sum_{i=2}^n \frac{G_{i,p}}{G_{1,p}} \neq -1$$

2. PLANAR EQUIVALENTS OF POLYGONS

It is sometimes desirable to have a planar equivalent for a certain non-planar network. In this section we will search for such equivalents in case the original network is an n-polygon. Using the concept of terminal-values one can find them, when $n \leq 7$. The cases $n = 4$ and $n = 5$ were already known [1,2]. A solution for $n = 6$ was communicated to us by S. Tirtoprodjo.

The case $n = 7$ is rather complicated for a one-colour-figure. This is the reason for not presenting it here. After seeing how the procedure works for $n = 4, 5$ and 6, $n = 7$ will give no extra difficulties. The structure of the resulting planar equivalent is shown in fig. 4.

$$\boxed{n = 4}$$

The arbitrary 4-polygon of fig. 1a will not be in general a T-polygon. Nevertheless we will give it terminal-values derived from only four of the six conductances e.g. $G_{1,3}$, $G_{1,4}$, $G_{3,4}$ and $G_{2,4}$:

$$\psi_1 = \frac{\sqrt{G_{1,3}} \sqrt{G_{1,4}}}{\sqrt{G_{3,4}}}$$

$$\psi_3 = \frac{G_{1,3}}{\psi_1}$$

$$\psi_4 = \frac{G_{1,4}}{\psi_1}$$

$$\psi_2 = \frac{G_{2,4}}{\psi_4}$$

$$\Psi = \psi_1 + \psi_2 + \psi_3 + \psi_4$$

We replace the two other conductances $G_{1,2}$ and $G_{2,3}$ by parallel-circuits (fig. 1b) in such a way that we are left with a T-polygon and two parallel-conductances. After transforming the T-polygon into a star, we have the planar network of fig. 1c, which is equivalent to the original 4-polygon.

$n = 5$

Now we derive the terminal-values from five of the ten conductances (fig. 2a). We choose the inner conductances $G_{1,3}$, $G_{1,4}$, $G_{2,4}$, $G_{2,5}$ and $G_{3,5}$, for then the parallel circuits will form the periphery of the network:

$$\psi_1 = \frac{\sqrt{G_{1,3}} \sqrt{G_{2,5}} \sqrt{G_{1,4}}}{\sqrt{G_{3,5}} \sqrt{G_{2,4}}}$$

$$\psi_2 = \frac{G_{2,4}}{G_{1,4}} \psi_1$$

$$\psi_3 = \frac{G_{3,5}}{G_{2,5}} \psi_2$$

$$\psi_5 = \frac{G_{3,5}}{G_{1,3}} \psi_1$$

$$\psi_4 = \frac{G_{2,4}}{G_{2,5}} \psi_5$$

$$\Psi = \psi_1 + \psi_2 + \psi_3 + \psi_4 + \psi_5$$

Again we replace the other conductances in the same way as before ($G_{i,j}$ by $(G_{i,j} - \psi_i \psi_j) // \psi_i \psi_j$) (fig. 2b) and we obtain a T-polygon with five additional conductances. After transforming the T-polygon, the planar network of fig. 2c is left.

$n = 6$

This case is more complicated because we need six conductances to determine six terminal-values. This leaves nine conductances to be replaced by parallel circuits. It is impossible to keep the extra conductances at the periphery of the network. Therefore we choose our six in such a way that we can follow the same procedure in the resulting network:

Fig. 3a gives the original configuration. We derive the terminalvalues from: $G_{1,3}$, $G_{1,5}$, $G_{3,5}$, $G_{1,4}$, $G_{3,6}$ and $G_{2,5}$ in the usual way. This gives the T-polygon drawn with full lines ($\psi_i \psi_j$) in fig 3b.

To obtain equivalence to fig. 3a, we have to add the conductances indicated by the dotted lines ($G_{i,j} = \psi_i \psi_j$). In fig. 3c we have transformed the T-polygon into a star and now we can treat the 4-polygons 1 - 2 - S - 6, 3 - 4 - S - 2 and 5 - 6 - S - 4 as we did above ($n = 4$). Fig. 3d gives the configuration of the resulting planar network.

3 . CONCLUDING REMARKS

The introduction of terminal-values has made it possible to prove the main theorem in an easier way as with the existing methods [3, 4, 5, 6] and gives practical formulas to perform the star-polygon-transformation. But it has other advantages. One of these is presented in section 2 where planar equivalents for polygons are given. This way of searching planar equivalents is not restricted to polygons. Both elementary Kuratowsky-graphs [7] , for example, can be transformed in planar networks. To conclude from the famous theorem in this paper [7] that every RLC-network has a planar equivalent appears to be wrong after careful examination, but the restrictions are not very strong.

In applications, for example in energy-distributions, it often occurs that the conductance values in a polygon are not all different from each other. Let us take an n -gon with only two different conductance values G_1 and G_2 . With the concept of terminal values in mind, we know that this polygon is transformable into a star if and only if $(n-1)$ conductances with value G_1 come together in one node and all the other conductances have the value G_2 . This structure is easy to recognise in a polygon-network.

It will be easy to find other examples of the application of terminal values, but we hope that the above is sufficient to convince the reader of the power of this concept.

APPENDIX

In fact we did prove in section I that a polygon is transformable into a star if and only if

$$\frac{G_{i,x} G_{i,y}}{G_{x,y}} = \frac{G_{i,v} G_{i,u}}{G_{v,u}} \quad (A)$$

for all i, x, y, u and v with $i \neq x, i \neq v, i \neq y, i \neq u, x \neq y$ and $v \neq u \pmod{n}$.

The set of conditions (A) is equivalent to

$$\frac{G_{i,k}}{G_{j,k}} = \frac{G_{i,l}}{G_{j,l}} \quad (B)$$

for all i, j, k and l with $i \neq k, j \neq k, i \neq l$ and $j \neq l \pmod{n}$.

Proof:

From (A) follows (B), for

$$\frac{G_{i,k} G_{i,j}}{G_{j,k}} = \frac{G_{i,l} G_{i,j}}{G_{j,l}} \rightarrow \frac{G_{i,k}}{G_{j,k}} = \frac{G_{i,l}}{G_{j,l}}$$

(A) is also consequence of (B):

$$\frac{G_{i,x}}{G_{u,x}} = \frac{G_{i,y}}{G_{u,y}} \rightarrow \frac{G_{i,x}}{G_{u,x}} \frac{G_{i,y}}{G_{x,y}} \frac{G_{i,u}}{G_{u,v}} G_{i,v} = \frac{G_{i,y}}{G_{u,y}} \frac{G_{i,y}}{G_{x,y}} \frac{G_{i,u}}{G_{u,v}} G_{i,v} \rightarrow$$

$$\left. \begin{aligned} &\rightarrow \frac{G_{i,v}}{G_{u,v}} \frac{G_{i,u}}{G_{x,u}} \frac{G_{i,x} G_{i,y}}{G_{x,y}} = \frac{G_{i,y}}{G_{u,y}} \frac{G_{i,y}}{G_{x,y}} \frac{G_{i,u} G_{i,v}}{G_{u,v}} \\ &\frac{G_{i,v}}{G_{u,v}} = \frac{G_{i,y}}{G_{u,y}} \\ &\frac{G_{i,u}}{G_{x,u}} = \frac{G_{i,y}}{G_{x,y}} \end{aligned} \right\} \frac{G_{i,x} G_{i,y}}{G_{x,y}} = \frac{G_{i,v} G_{i,u}}{G_{u,v}}$$

Hence, the set (B) is also sufficient for the transformability, but the conditions in (B) are not independent. In the following two steps we will come to a set with a minimal number of conditions. Since every $Y - \Delta$ - transformation is always possible in both directions, we take $n > 3$.

The set (B) is equivalent to

$$\frac{G_{i,j}}{G_{i+1,j}} = \frac{G_{i,j+1}}{G_{i+1,j+1}} \quad (C)$$

for all i and j with $j \neq i-1$, $j \neq i$ and $j \neq i+1 \pmod n$

Proof: The derivation of (C) from (B) is simple, but we have also to prove that (C) implies (B):

$$\begin{aligned} (C) \rightarrow \frac{G_{i,i+2}}{G_{i+1,i+2}} &= \frac{G_{i,i+3}}{G_{i+1,i+3}} = \frac{G_{i,i+4}}{G_{i+1,i+4}} = \dots = \frac{G_{i,i+n-2}}{G_{i+1,i+n-2}} \\ \rightarrow \frac{G_{i,p}}{G_{i+1,p}} &= \frac{G_{i,r}}{G_{i+1,r}} \text{ or } \frac{G_{i,r}}{G_{i,p}} = \frac{G_{i+1,r}}{G_{i+1,p}} \text{ for } p \neq i, r \neq i \\ & \qquad \qquad \qquad p \neq i+1, \text{ and } r \neq i+1 \pmod n \end{aligned} \quad (1')$$

Be $r > p$ (this is no restriction!), then

$$\frac{G_{r,r+1}}{G_{p,r+1}} = \frac{G_{r,r+2}}{G_{p,r+2}} = \frac{G_{r,r+3}}{G_{p,r+3}} = \dots = \frac{G_{r,p-1}}{G_{p,p-1}} \quad (2')$$

From (1') we also get:

$$\left. \begin{aligned} \frac{G_{p-1,r}}{G_{p,r}} &= \frac{G_{p-1,p+1}}{G_{p,p+1}} \\ \frac{G_{p,r}}{G_{p+1,r}} &= \frac{G_{p,p-1}}{G_{p+1,p-1}} \end{aligned} \right\} G_{p,r} \quad G_{p+1,p-1} = G_{p,p-1} \quad G_{p+1,r} = \\ = G_{p,p+1} \quad G_{p-1,r}$$

Dividing the last two members of this equation by $G_{p,p+1} G_{p,p-1}$ gives:

$$\frac{G_{p,p-1} G_{p+1,r}}{G_{p,p-1} G_{p,p+1}} = \frac{G_{p,p+1} G_{p-1,r}}{G_{p,p+1} G_{p,p-1}} \rightarrow \frac{G_{r,p+1}}{G_{p,p+1}} = \frac{G_{r,p-1}}{G_{p,p-1}} \quad (3')$$

We are now able to continue the sequence (2'):

$$\begin{aligned} \frac{G_{r,r+1}}{G_{p,r+1}} &= \frac{G_{r,r+2}}{G_{p,r+2}} = \dots = \frac{G_{r,p-1}}{G_{p,p-1}} = \frac{G_{r,p+1}}{G_{p,p+1}} = \frac{G_{r,p+2}}{G_{p,p+2}} = \\ &= \dots = \frac{G_{r,r-1}}{G_{p,r-1}} \end{aligned}$$

This completes the proof because this sequence contains all the equations of (B).

We can write the set (C) also in the following way:

$$\begin{array}{cccc} C_{1,1} & C_{1,2} & \dots & C_{1,n-3} \\ C_{2,1} & C_{2,2} & \dots & C_{2,n-3} \\ \vdots & \vdots & & \vdots \\ C_{n,1} & C_{n,2} & \dots & C_{n,n-3} \end{array}$$

where $C_{i,j}$ stands for the equation

$$\frac{G_{i,i+j+1}}{G_{i+1,i+j+1}} = \frac{G_{i,i+j+2}}{G_{i+1,i+j+2}}$$

We allege now that every equation occurs twice in the set (C)

Proof:

$$\begin{aligned} C_{n-j+q,j} &\rightarrow \frac{G_{n-j+q,n-j+q+j+1}}{G_{n-j+q+1,n-j+q+j+1}} = \frac{G_{n-j+q,n-j+q+j+2}}{G_{n-j+q+1,n-j+q+j+2}} \rightarrow \\ &\rightarrow \frac{G_{n-j+q,n+q+1}}{G_{n-j+q+1,n+q+1}} = \frac{G_{n-j+q,n+q+2}}{G_{n-j+q+1,n+q+2}} \rightarrow \\ &\rightarrow \frac{G_{n+q+1,n-j+q}}{G_{n+q+2,n-j+q}} = \frac{G_{n+q+1,n-j+q+1}}{G_{n+q+2,n-j+q+1}} \rightarrow \\ &\rightarrow \frac{G_{q+1,n+q-j}}{G_{q+2,n+q-j}} = \frac{G_{q+1,n-j+q+1}}{G_{q+2,n-j+q+1}} \end{aligned}$$

$$\rightarrow \frac{G_{q+1,q+1+n-j-2+1}}{G_{q+2,q+1+n-j-2+1}} = \frac{G_{q+1,q+1+n-j-2+2}}{G_{q+2,q+1+n-j-2+2}}$$

This last equation is precisely $C_{q+1,n-j-2}$

Thus, it is enough to check the equations contained in the following tables:

in case n is odd:

$C_{1,1}$	$C_{1,2}$	$C_{1,\frac{n-3}{2}}$	
$C_{2,1}$	$C_{2,2}$	$C_{2,\frac{n-3}{2}}$	
⋮	⋮	⋮	⋮	
$C_{n,1}$	$C_{n,2}$	$C_{n,\frac{n-3}{2}}$	(B)

in case n is even:

$C_{1,1}$	$C_{1,2}$	$C_{1,\frac{n-4}{2}}$	$C_{1,\frac{n-2}{2}}$	
$C_{2,1}$	$C_{2,2}$	$C_{2,\frac{n-4}{2}}$	$C_{2,\frac{n-2}{2}}$	
⋮	⋮	⋮	⋮	⋮	
$C_{\frac{n}{2},1}$	$C_{\frac{n}{2},2}$	$C_{\frac{n}{2},\frac{n-4}{2}}$	$C_{\frac{n}{2},\frac{n-2}{2}}$	(D)
⋮	⋮	⋮	⋮	⋮	
$C_{n,1}$	$C_{n,2}$	$C_{n,\frac{n-4}{2}}$		

The conditions in these tables are independent, for, if one reads the equations column after column, and each column downward, then we meet in every equation a conductance which did not appear before, namely $G_{i,i+j+2}$. The total number of equations in (D) is $\frac{1}{2}n(n-3)$, and this number does not surprise us:

- a polygon is determined by its $\frac{1}{2}n(n-1)$ conductances: $\frac{1}{2}n(n-1)$ degrees of freedom
- a star is determined by its n conductances: n degrees of freedom
- a T-polygon is equivalent to a star, and cannot have more than n degrees of freedom.

This means that the minimal set of conditions must contain $\frac{1}{2}n(n-1) - n = \frac{1}{2}n(n-3)$ independent equations.

The set (D) is also easily found by inspection:

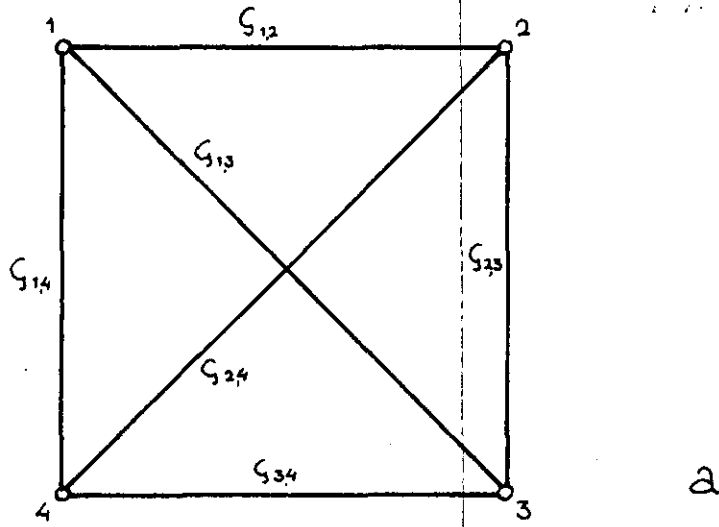
We write the equations

$$G_{p,q} G_{p-1,q+1} = G_{p-1,q} G_{p,q+1} ,$$

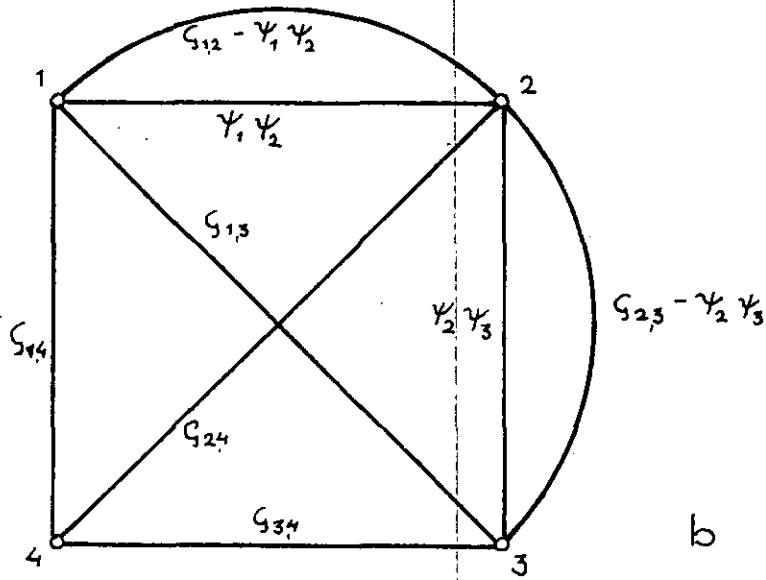
choosing for q first p+1, while p runs from 1 to n. Then we take for q p+2 and again p runs from 1 to n. We continue in this way until we have $\frac{1}{2}n(n-3)$ equations (fig. 5) [2] .

CAPTIONS OF FIGURES

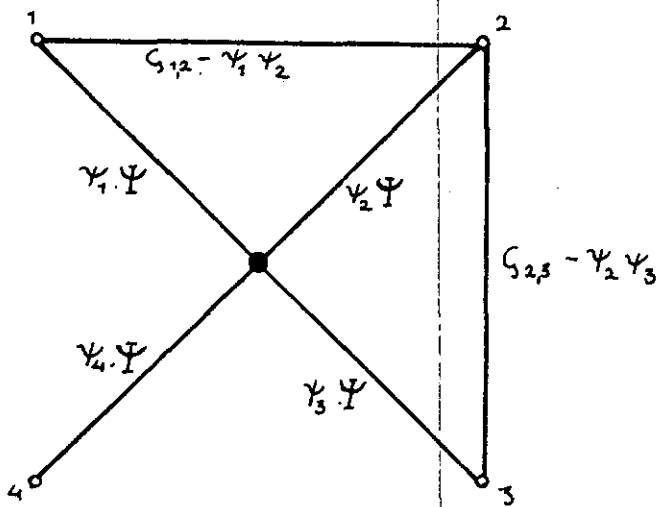
- Fig. 1 : A planar transformation of a 4-gon
- Fig. 1a : A general 4-gon
- Fig. 1b : Splitting of the 4-gon in a T-4-gon and residual conductances
- Fig. 1c : The planar equivalent of a 4-gon
- Fig. 2 : A planar transformation of a 5-gon
- Fig. 2a : A general 5-gon
- Fig. 2b : Splitting of the 5-gon in a T-5-gon and residual conductances
- Fig. 2c : The planar equivalent of a 5-gon
- Fig. 3 : A planar transformation of a 6-gon
- Fig. 3a : A general 6-gon
- Fig. 3b : Splitting of the 6-gon in a T-6-gon (full lines) and residual conductances (dotted lines)
- Fig. 3c : The network after transformation of the T-6-gon
- Fig. 3d : The planar equivalent of a 6-gon
- Fig. 4 : The structure of a planar equivalent of a general T-7-gon
- Fig. 5 : A sub-network of a T-polygon.



a

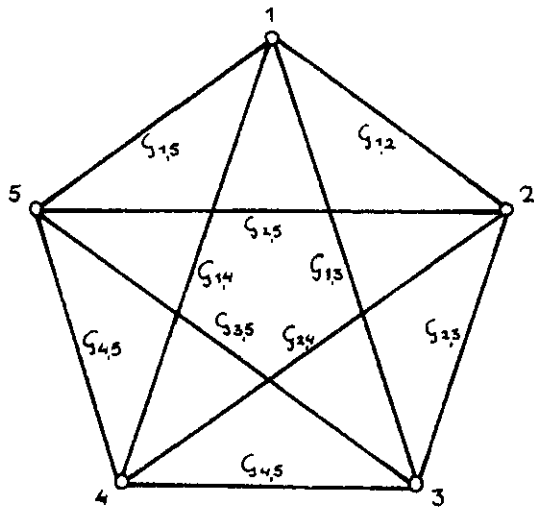


b

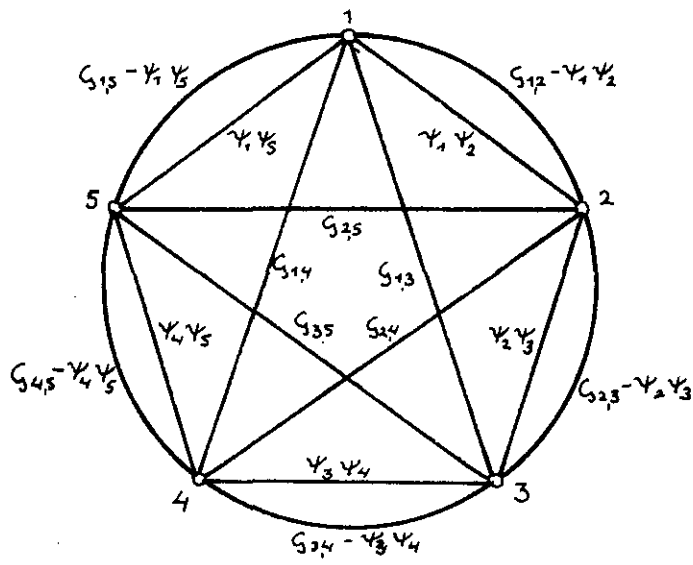


c

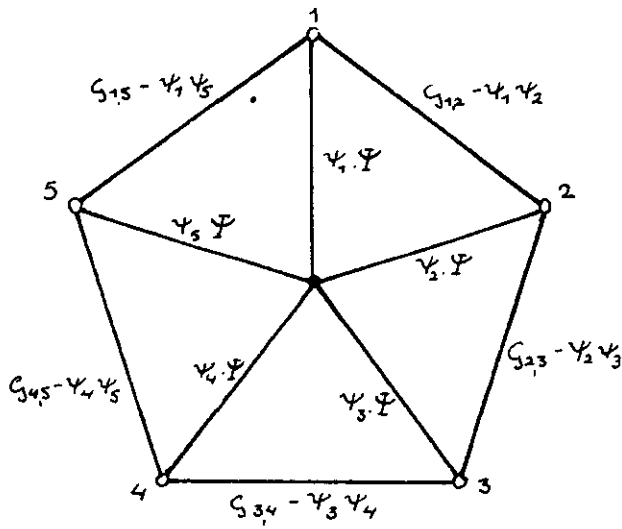
FIG. 1



a



b



c

FIG. 2

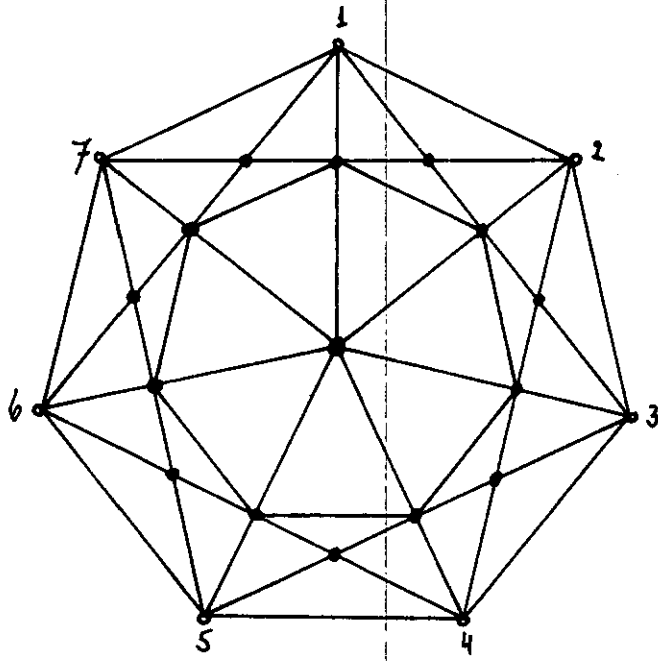


FIG. 4

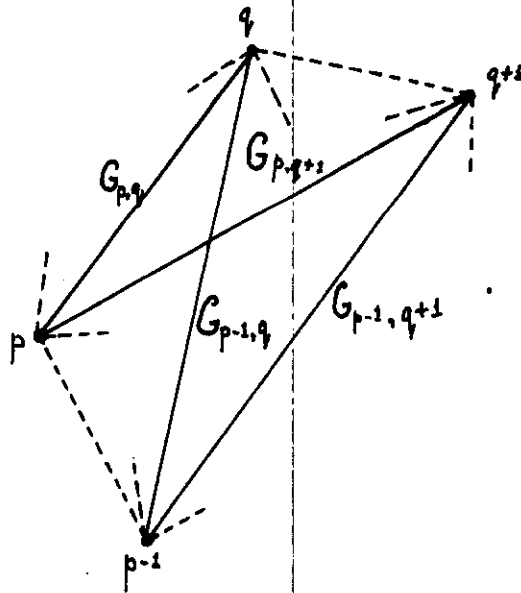


FIG. 5

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