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Calculation of Planar Transformer Capacitance Based on the Applied Terminal Voltages

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***Abstract*—In order to calculate the parasitic capacitors of a transformer, it is important to apply the correct transformer terminal voltages such that only the desired lumped capacitors are charged. This paper shows the correct transformer terminal voltages that match measurement scenarios that are widely used to extract lumped capacitor values. The parasitic capacitors are calculated based on the stored energy in the transformer windings for different measurement scenarios. A 5kW heavily interleaved high turns-ratio planar transformer is constructed, and its parasitic capacitance is measured. Lumped capacitor simulations are performed using Ansys Maxwell 3D. The simulations are verified through comparison with the measurements and the difference from the measurements is between 1.55-3.76%. The calculation method has a difference of 9.92-10.38% compared to the simulated model, which primarily is caused by an assumption of overlapping turns which is different from the simulated model.**

***Index Terms*—FEM simulation, Capacitor calculation, Parasitic capacitance, Equivalent circuits, Transformers, Modeling, Impedance measurement**

I. Introduction

Optimization of transformers are essential in any isolated switch mode power supply (SMPS), since they often are the bulkiest and biggest component [1]–[3]. Knowledge of the operation and lumped circuit parameters is crucial to ensure a successful and optimal SMPS design. As the switching frequency increases, the parasitic impedance has an increasing impact on the transformer performance. This is especially true for the capacitance of the transformer, which directly influences the capacitive power loss and noise emission [4], [5].

Planar transformers are becoming more commonly used in SMPS due to their large power density [6]. It is important to understand the parasitic components of the planar transformers, especially for the high turns-ratio high power designs. Increasing the turns-ratio and power of a planar transformer complicates the calculation of the lumped capacitors. A common method for calculating the parasitic capacitance of the transformer is to derive the total stored energy in the electric field surrounding the windings, from which lumped capacitance values can be derived [6], [7]. However depending on the equivalent circuit model, matching the measured and calculated capacitance values is not always possible, as it becomes difficult to apply the desired voltages at the transformer terminals that correspond to the theoretical model.

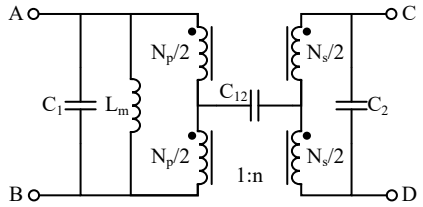
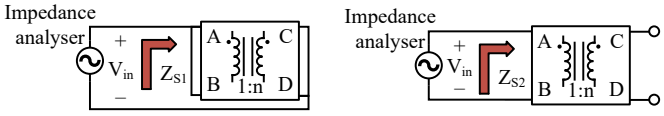


Fig. 1. The symmetrical transformer model



(a) Scenario 1 (b) Scenario 2

Fig. 2. Measurement of (a) inter-winding capacitance and (b) self-capacitance

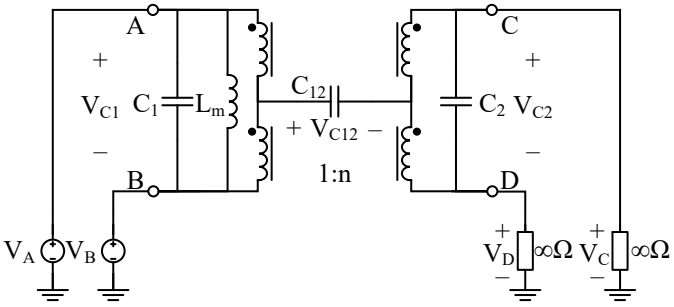


Fig. 3. Illustration of transformer terminal voltages

Another method to obtain the parasitic capacitance of a transformer is by simulating the stored energy by use of finite element method (FEM). FEM simulations of parasitic capacitance is presented in [8], while the impact of interleaving on the parasitic capacitance is simulated in [9] on planar transformers. However, neither presents validations of the accuracy in the form of comparisons with the calculation or measurement. [10] presents calculations, simulations and measurements of parasitic capacitance in high voltage high turns-ratio wire-wound transformers. Different winding architectures are investigated, ranging from non-interleaved scenarios to highly interleaved scenarios. Great accuracy is obtained in the non-interleaved scenarios, whereas up to 7.7% error is obtained between the calculation and measurement in the highly

interleaved scenario. The error between the simulation and measurement is 67% in the highly interleaved scenario. The literature presents many attempts at simulating the parasitic capacitance of a transformer, however either the accuracy of the simulations are not validated, or the simulations are error-prone.

This paper utilizes the well known stored energy method for accurately calculating the parasitic capacitance. The voltages differences in the calculation are however altered as to be a function of the applied transformer terminal voltages. The method furthermore allows for direct comparison with measurements and allows for easy and direct split of which lumped capacitors is charged during capacitor measurements. Ansys Maxwell 3D simulations are performed using the same principle with the transformer terminal voltages, resulting in excellent accuracy. A planar transformer with high-turns ratio for high power application is presented, and the calculations and simulations are validated through capacitance measurements on the transformer.

II. The Transformer Terminal Signal Potential for Parasitic Capacitor Calculation

Many different equivalent circuit models exist in the literature which represent the parasitic capacitance of a transformer [11], [12]. A simple three capacitor model that clearly separate the influence of the respective lumped capacitors, is the symmetrical transformer model [13], [14]. The symmetrical transformer model is shown on Fig. 1, where the leakage inductance and winding resistance have been excluded for the sake of simplicity. The model includes three lumped capacitors, namely the inter-winding capacitance (C_{12}) and two self-capacitors (C_1 and C_2). The measurement scenario for extracting the lumped capacitors are shown on Fig. 2, where scenario 1 measures the inter-winding capacitance and scenario 2 measures the total self-capacitance. The impedance of the symmetrical model in the two scenarios are shown, below where L_m is the magnetizing inductance of the transformer.

$$Z_{s1} = \frac{1}{sC_{12}} \tag{1}$$

$$Z_{s2} = \frac{sL_m}{s^2L_m\left(C_1 + n^2C_2\right) + 1} \tag{2}$$

A lumped capacitor is only measurable when it is affected by a signal. The signal level are therefore equal to zero for non-affected lumped capacitors. Fig. 3 shows the symmetrical transformer model where signals are applied to each primary terminal (V_A and V_B). The secondary terminals are each loaded with infinite impedance and have the terminal signals V_C and V_D. The voltage across the lumped capacitors are given by the equations below, where n is the transformer turns-ratio.

$$V_{C1} = V_A - V_B \tag{3}$$

$$V_{C2} = n\,V_{C1} = V_C - V_D \tag{4}$$

$$V_{C12} = (V_A + V_B)/2 - (V_C + V_D)/2 \tag{5}$$

It is clear from inspection of the impedance in (1) that only C_{12} is measured in scenario 1, meaning that $V_{C1} = V_{C2} = 0$.

TABLE I
Required Terminal Voltages in the Two Measurement Scenarios

	V_A	V_B	V_C	V_D
Scenario 1	V_{in}	V_{in}	0	0
Scenario 2	$V_{in}/2$	$-V_{in}/2$	$n\,V_{in}/2$	$-n\,V_{in}/2$

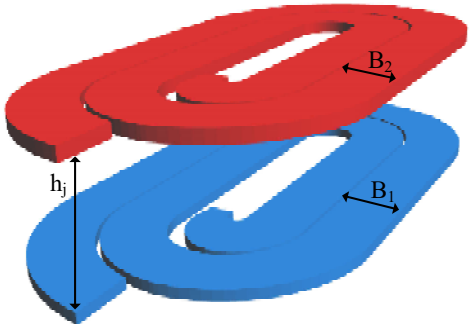


Fig. 4. Illustration of two transformer layers in 3D

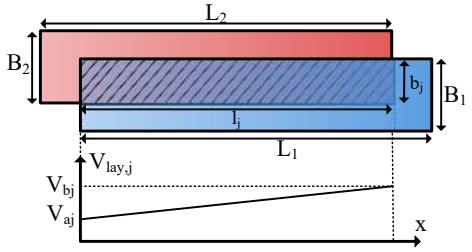


Fig. 5. Illustration of overlapping area between two transformer layers and voltage difference between them

In scenario 2 however, it is clear from the impedance in (2) that only the total self-capacitance ($C_1 + n^2C_2$) is measured, meaning that $V_{C12} = 0$. The required terminal signals to only measure the affected capacitors in the respective scenarios, are deduced from (1), (2), (3), (4) and (5). The deduced voltage signals are listed in Table I, where the applied voltage signal from the impedance analyzer is denoted as V_{in}.

III. Energy Stored Between Two Layers

The equivalent lumped capacitance between two layers of a transformer is found from the stored electrical energy (E_j) as shown below. The voltage potential between the layers are denoted as $V_{lay,j}$ and ϵ_j is the permittivity of the insulation material.

$$E_j = \int\int\int_{vol} \frac{1}{2}\,\epsilon_j(x,y,z)\,\left(V_{lay,j}(x,y,z)\right)^2\,dx\,dy\,dz \tag{6}$$

Assuming that ϵ_j is constant in all dimensions and that the voltage is constant in the z dimension, allows for the following simplification, where h_j is the distance between the layers.

$$E_j = \frac{\epsilon_j}{2\,h_j}\int\int_A \left(V_{lay,j}(x,y)\right)^2\,dx\,dy \tag{7}$$

An illustration of two layers of a planar transformer is shown on Fig. 4. The width of each winding are B_1 and B_2 respectively, while the length of each winding are L_1 and

TABLE II
HEIGHT OF INDIVIDUAL INSULATION LAYERS IN STACK-UP

	Insulation layer no.								
j	1	2	3	4	5	6	7	8	9
h_j	286μm	200μm	218μm	296μm	100μm	296μm	218μm	200μm	286μm

Fig. 6. Constructed 32:4 planar transformer

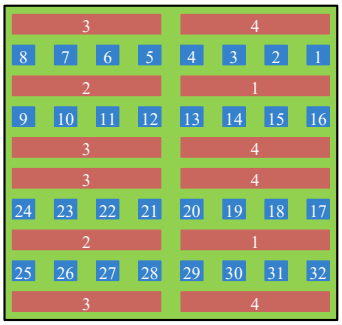


Fig. 7. Stack-up of a single PCB in the planar transformer

L_2 respectively. Fig. 5 shows the two windings from Fig. 4 stretched along their length, with the purpose of illustrating their overlapping area. The width and length of the overlapping area are b_j and l_j respectively.

Assuming the voltage is increasing linearly along the length of the turns and is constant along their width, then $V_{lay,j}$ can be expressed as shown on Fig. 5. Using (7), the energy stored in the electric field between the two layers simplifies to

$$E_j = \frac{\epsilon_j\ b_j}{2\ h_j} \int_0^{l_j} \left(\frac{V_{b,j} - V_{a,j}}{l_j} \cdot l + V_{a,j} \right)^2 dl = \frac{\epsilon_j\ b_j\ l_j}{6\ h_j} \left(V_{a,j}^2 + V_{a,j}\ V_{b,j} + V_{b,j}^2 \right) \quad (8)$$

IV. HIGH-POWER HIGH TURNS-RATIO PLANAR TRANSFORMER

A planar transformer with 32 primary turns (N_p) and 4 secondary turns (N_s) are constructed as shown on Fig. 6, with the intent of validating the capacitance calculation provided at the end of this section. The transformer core consist of two E58/11/38-3C95 cores from Ferroxcube. The transformer is highly interleaved to reduce the AC resistance and leakage inductance. The transformer windings consist of three identical PCB placed in parallel. The stack-up of a single PCB is shown on Fig. 7, where the blue squares are the primary-turns and the red rectangles are the secondary-turns. The numbers indicate the respective turn-number in the windings, where numbers in ascending order are series connected. Turns of the same color and same number are parallel connected. All the primary layers are identical with 8 turns $(N_{p,l})$ but mirrored as to properly connect between the layers. The same is true for the secondary layers which has 2 turns per layer $(N_{s,l})$. The height of the individual insulation layers (h_j) of a single PCB are listed in Table II.

The width of the constructed transformer's primary and secondary turns are changing slightly throughout the length of the windings. The width is especially larger at the interconnection of layers. The average turn width of the primary and secondary windings are 2mm and 9.5mm (b_{wp} and b_{ws}) respectively, and their average length are 1.42m and 0.37m (L_p and L_s) respectively.

TABLE III
VOLTAGE AT THE BEGINNING AND END OF THE LAYERS IN THE STACK-UP

Layer no.	Scenario 1		Scenario 2	
j	$V_{start,j}$	$V_{end,j}$	$V_{start,j}$	$V_{end,j}$
1	0	0	$-\frac{1}{2}V_{in}\,n$	0
2	V_{in}	V_{in}	$\frac{1}{2}V_{in}$	$\left(\frac{1}{2} - \frac{N_{p,l}}{N_p}\right)V_{in}$
3	0	0	$\frac{1}{2}V_{in}\,n$	0
4	V_{in}	V_{in}	0	$\left(\frac{1}{2} - \frac{N_{p,l}}{N_p}\right)V_{in}$
5	0	0	$-\frac{1}{2}V_{in}\,n$	0
6	0	0	$-\frac{1}{2}V_{in}\,n$	0
7	V_{in}	V_{in}	0	$\left(\frac{1}{2} - 3\frac{N_{p,l}}{N_p}\right)V_{in}$
8	0	0	$\frac{1}{2}V_{in}\,n$	0
9	V_{in}	V_{in}	$-\frac{1}{2}V_{in}$	$\left(\frac{1}{2} - 3\frac{N_{p,l}}{N_p}\right)V_{in}$
10	0	0	$-\frac{1}{2}V_{in}\,n$	0

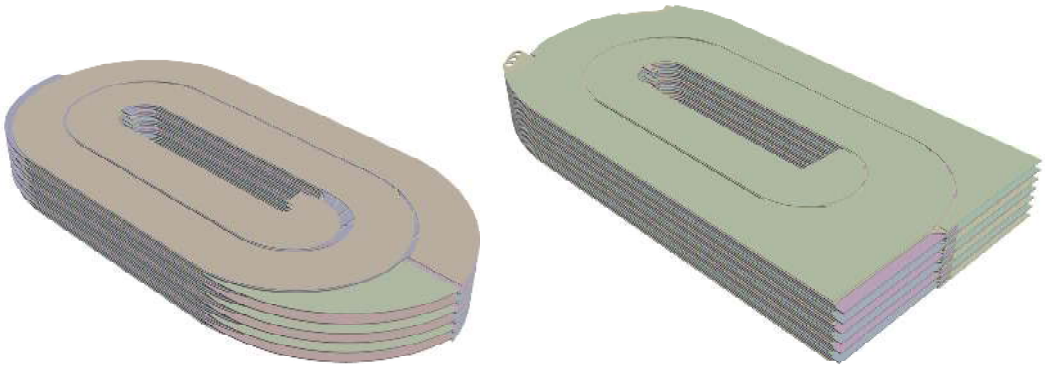
The equivalent lumped capacitor (C_x) of the transformer are quantified by calculating the stored energy (E_{tot}) in the entire stack-up for the specific scenario.

$$E_{tot} = N_{PCB} \sum_{j=1}^{N} E_j \quad (9)$$

where N is the number of insulation layers in one PCB and N_{PCB} is the number of parallel PCB. By inserting (8) into (9), can E_{tot} be expressed as

$$E_{tot} = N_{PCB} \sum_{j=1}^{N} \frac{\epsilon_j\ b_j\ l_j}{6\ h_j} \left(V_{a,j}^2 + V_{a,j}\ V_{b,j} + V_{b,j}^2 \right) \quad (10)$$

The secondary winding almost completely covers the primary winding, from which it is assumed that the overlapping



(a) Constant width transformer (b) Constructed transformer

Fig. 8. 3D models of the two transformers

area equals the length times the width of the primary winding. The equivalent lumped capacitor is then calculated from (10) by using the following relation.

$$C_x = \frac{2\,E_{tot}}{V_{in}^2} = \frac{\epsilon\ N_{PCB}\ b_{wp}\ L_p}{3\ V_{in}^2} \sum_{j=1}^{N} \frac{V_{a,j}^2 + V_{a,j}\ V_{b,j} + V_{b,j}^2}{h_j} \quad (11)$$

The voltage potential between the layers depend on the scenario and stack-up. The voltages of the stack-up layers shown on Fig. 7 are found for the two measurement scenarios with the signals from Table I, by assuming a linear change in voltage across the winding length as shown on Fig. 5. The voltage at the beginning and at the end of each layer ($V_{start,j}$ and $V_{end,j}$) are derived and listed in Table III. These voltages are used to determine the voltage difference at the beginning and at the end of the overlapping area across the insulation layers ($V_{a,j}$ and $V_{b,j}$), as shown below.

$$V_{a,j} = V_{start,j} - V_{start,j+1} \quad (12)$$

$$V_{b,j} = V_{end,j} - V_{end,j+1} \quad (13)$$

It follows from Table III, that $V_{start,j}$ and $V_{end,j}$ of each insulation layer is constant in measurement scenario 1 where the inter-winding capacitance (C_{inter}) is calculated. In measurement scenario 2 where the total self-capacitance $(C_1 + n^2 C_2)$ is calculated, the voltage changes from layer to layer, thereby giving rise to two different lumped capacitors values when using the same calculation method.

V. Ansys Simulation of the Lumped Capacitors

In the former section it was explained that the width is assumed constant along the length of the windings when calculating the lumped capacitors. The width of the windings in the constructed transformer is however not constant, and is primarily larger close to interconnections of the PCBs. For this reason, it is chosen to analyze on two different transformers. One of the transformers is a model mimicking the constructed transformer, whereas the other is a model that closely mimicks the assumption of constant width along the transformer windings. 3D models of the two transformers are shown on Fig. 8, which clearly illustrates the difference in width in one of the secondary layers.

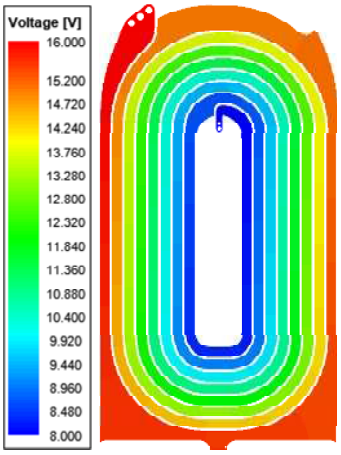
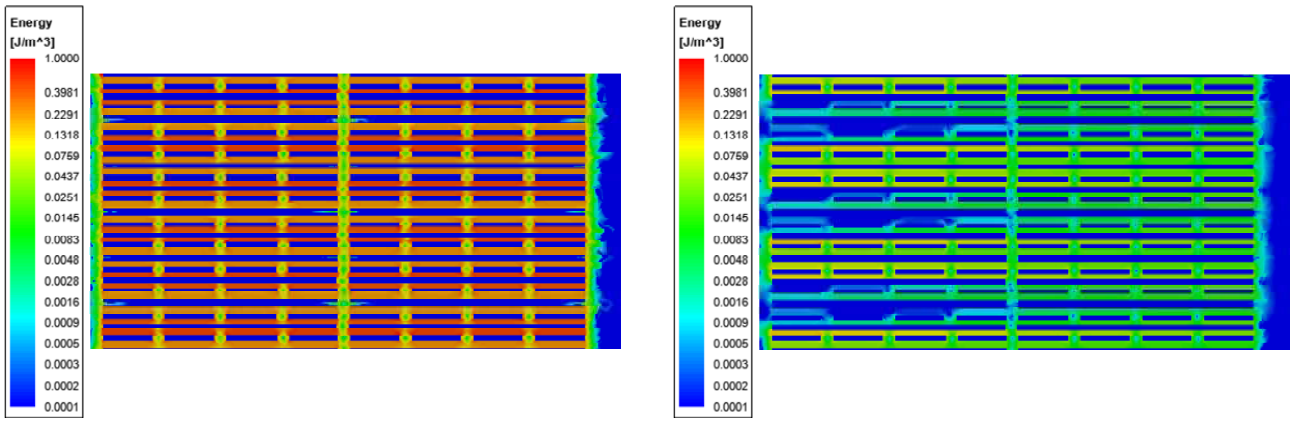


Fig. 9. Illustration of how the voltage unfolds in one of the primary layers

The two transformers are simulated with Ansys Maxwell 3D. The accuracy of the simulation is tested by comparing the measurement and simulation in the case with the constructed transformer. Once the simulation accuracy is determined, are the calculated capacitance compared with the simulation in the case with the constant width transformer. All of these validations are performed in the next section with the experimental results.

The simulations are performed with the layer voltages from Table III, thereby mimicking the two measurement scenarios. In Fig. 9 is the voltage of a primary layer shown for scenario 2, where it clearly shows that the voltage is changing linearly along the length of the winding.

A cross-sectional cut of the layers energy density of the constructed transformer is shown on Fig. 10 in the two measurement scenarios. The two simulations of energy density are scaled the same way, from which it is determined that much more energy is stored in scenario 1 compared to scenario



(a) Scenario 1 (b) Scenario 2

Fig. 10. Stored energy in the constructed transformer in the measurement scenarios of Fig. 2

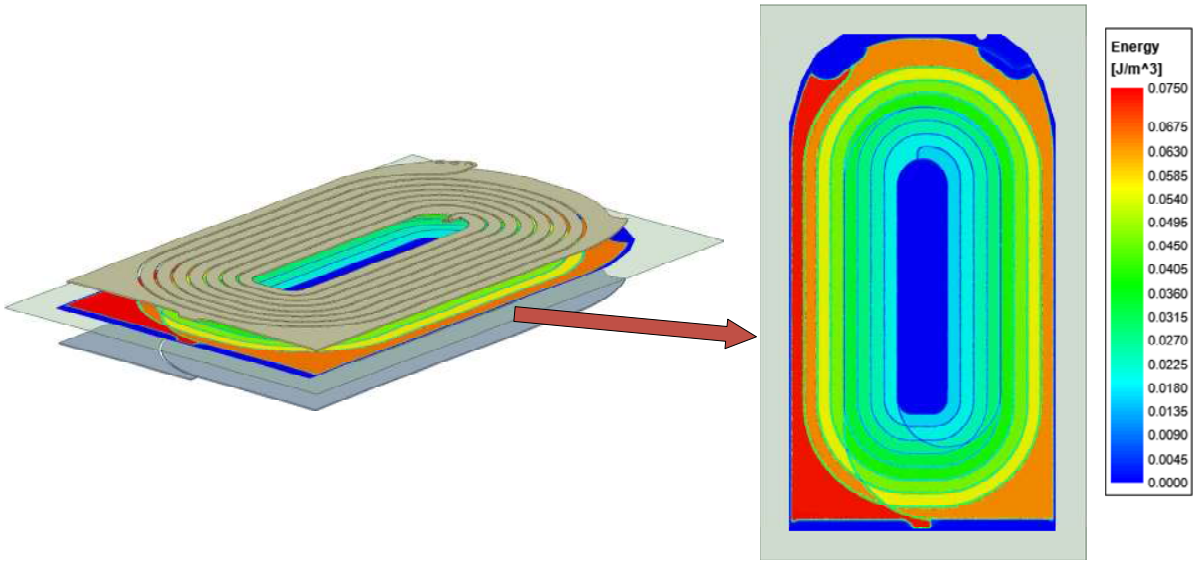


Fig. 11. Stored energy in the insulation layer between layer 9 and 10 of the constructed transformer in scenario 2

2. The Fig. 10a clearly shows that the energy is constant throughout the insulation layers between a primary and secondary layer. Also, the highest energy density is at the smallest height difference between the primary and secondary layers. The reason why the energy is constant throughout the layers are that the voltage difference across the insulation layers are constant in scenario 1, as is listed in Table III.

In scenario 2 however, the voltage difference varies along the layers, which clearly is reflected in the stored energy density shown on Fig. 10b. The plot shows that the stored energy is concentrated at turns corresponding to places where large voltage differences are predicted when using Table III along with equations (12) and (13).

Another way of representing the simulated energy density of scenario 2 is shown on Fig. 11, where the stored energy of the insulation layer between layer 9 and 10 is shown. The figure clearly shows that the energy density is largest where the highest voltage difference can be predicted. The figure furthermore illustrates that areas with large turn-width are placed in positions with large voltage, which derives to a high energy density. These large widths adds a lot of stored energy to the design compared to the transformer with constant width. This fact is proved in the following section.

VI. Experimental results

The equivalent lumped circuit parameters of the constructed transformer is measured using a Keysight 4294A Presion Impedance Analyzer. The inter-winding capacitance (C_{12}) is determined from the measured impedance on Fig. 12a, which up to the first resonance frequency are described using (1).

The magnetizing inductance (L_m) and the total self-capacitance ($C_1 + n^2\ C_2$) is measured using measurement scenario 2 of Fig. 2b, see Fig. 12b for the measurement. The impedance is described using (2), and it is dominated by L_m before the resonance frequency (f_{res}). The numerical value of L_m is extracted one decade before f_{res} to attain the

TABLE IV
EQUIVALENT CIRCUIT PARAMETERS OF THE TRANSFORMER REFERRED TO THE PRIMARY SIDE

Parameter	Symbol	Value
Magnetizing inductance	L_m	9.3 mH
Leakage inductance @ 200kHz	L_{lk}	283 nH
AC resistance @ 200kHz	R_{AC}	187 mΩ

TABLE V
CALCULATED, SIMULATED AND MEASURED CAPACITANCE OF THE PLANAR TRANSFORMER

		C_{12}	$C_1 + n^2\ C_2$
Constant width transformer	Calculated	10.9 nF	0.95 nF
	Simulated	12.1 nF	1.06 nF
Constructed transformer	Simulated	13.8 nF	1.27 nF
	Measured	13.3 nF	1.29 nF

biggest accuracy, by assuming $Z_{s2} = sL_m$. Afterwards, the self-capacitance is determined at f_{res} as shown below.

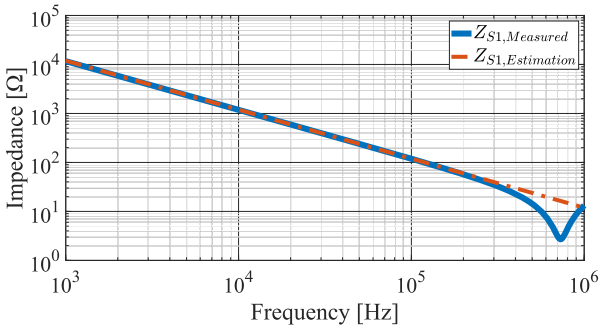
$$C_1 + n^2\ C_2 = \frac{1}{(2\ \pi\ f_{res})^2\ L_m} \tag{14}$$

The AC resistance (R_{AC}) and leakage inductance (L_{lk}) is measured using a short circuit measurement. The extracted L_m, L_{lk} and R_{AC} is listed in Table IV, where the parameters are referred to the primary side of the transformer. The extracted lumped capacitors are listed in Table V, along with the calculated and simulated values.

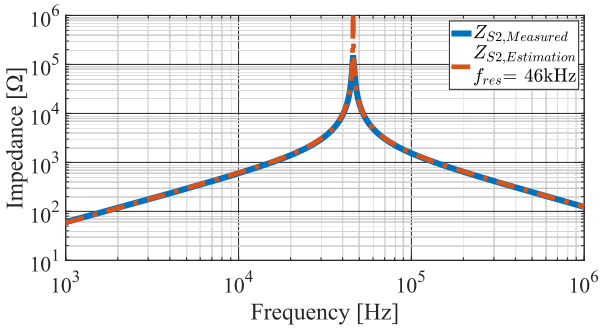
The measured and simulated lumped capacitors of the constructed transformer are compared as to validate the accuracy of the simulations. There is great coherence between the measured and simulated lumped capacitors, with very small differences between 1.55-3.76%. This clearly validates the accuracy of the simulation method for determining the lumped capacitor values.

The calculated and simulated lumped capacitors are compared in the constant width transformer shown on Fig. 8a, with the purpose of validating the calculation method. The results are listed in Table V. It follows that there are differences of 9.92-10.38% between the simulated and calculated lumped capacitors. The difference is primarily caused by the assumption of zero fringing flux in the electric field and the assumption of complete overlap in the layers of the stack-up. In the simulation of the constant width transformer, the ascending turns changes direction throughout the stack-up. This causes the overlap to change compared to the assumptions used in the calculated case.

When comparing the calculated lumped capacitors in the fixed width transformer with the measured lumped capacitors in the constructed transformer, it follows that the measured capacitors are numerically larger in value. This is caused by the difference in width of the windings. The positions with large width is also positions with big voltage difference between the layers. Large amounts of energy is therefore stored at those positions, as shown on Fig. 11. When the total



(a) Scenario 1



(b) Scenario 2

Fig. 12. Impedance measurement on the planar transformer of the two scenarios from Fig. 2

stored energy increases, so does the equivalent capacitance value, which explains the difference between the measured and calculated lumped capacitors.

VII. CONCLUSION

Two widely used measurement methods for extracting the inter-winding and self-capacitance of a transformer has been presented and explained. A method for calculating these two capacitances has been presented, and it is stated that the correct voltage signals must be applied to the transformer terminals to accurately calculate the two capacitances.

Ansys Maxwell 3D simulations were used as an intermediate to verify the accuracy of the calculation method. This was done by analyzing the lumped capacitance of two transformers in the two measurement scenarios. One of the transformers had a constant winding width along their respective length. The other is a constructed 5kW highly interleaved 32:4 planar transformer whose winding width varies along their respective length. Stored energy simulations corresponding to the inter-winding capacitance has been performed on the constructed transformer, which showed that the energy stored in an insulation layer is even along the layer. Simulations of the self-capacitance were widely spread with most stored energy at areas where the voltage difference are largest. It is furthermore shown that much energy is stored in parts of the windings where the constructed transformer windings are widest.

Lumped capacitor measurements on the constructed transformer verified the accuracy of the simulations with only 1.55-3.76% difference. Simulations of the constant width

transformer verified the accuracy of the calculations with only 9.92-10.38% difference. The biggest reason for the difference is assumed due to differences in how the windings overlay each other in the stack-up, along with an assumption of zero fringing flux in the electric field.

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