Calibration Techniques of Active BiCMOS Mixers

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***Abstract*—This paper describes calibration techniques for downconversion mixers used in integrated direct-conversion receivers. A method of achieving a high even-order intermodulation rejection is presented. Using the method presented, the receiver second-order input intercept point (IIP2) can always be improved by more than 20 dB. The minimum achieved receiver IIP2 after calibration is +38 dBm. A technique to enhance the I/Q-amplitude balance between the quadrature channels is also introduced. A single-balanced adjustable mixer is implemented as a part of a prototype direct-conversion receiver. The receiver chip consists of a low-noise amplifier, mixers and calibration circuitry, a divide-by-two circuit, local oscillator (LO) buffers for LO generation, and active baseband filters. The chip is fabricated using a 0.35-μm SiGe BiCMOS process and is characterized at 900 MHz.**

***Index Terms*—BiCMOS analog integrated circuits, calibration, dc offset, direct conversion, IIP2, mixers, radio receivers.**

I. Introduction

MUCH attention has been paid to the investigation and development of integrated direct-conversion receivers (DCR) for wireless cellular radios during recent years. While many of the well-known direct-conversion design issues [1], [2] have existing solutions that are sufficient for most cellular standards, the even-order intermodulation still remains without a complete solution. Many cellular systems require a high second-order input intercept point (IIP2) if direct-conversion or low-IF receiver architecture is used. In wideband code division multiple access (WCDMA), for example, several code channels compose a wideband signal that can have a high crest factor. The high crest factor results in large envelope variations in the signal. On the other hand, in time division multiple access (TDMA) systems, as in GSM, the ramping power at the beginning of the TDMA burst will cause a large amplitude modulation (AM) component although the modulation has a constant envelope. These envelope variations are detected by the second-order nonlinearities of the receiver causing in-band interference. Guidelines to estimating the specification for radio systems are discussed, for example, in [3]. Recently, some technical papers have been published which not only discuss the problems caused by the second-order distortion, but also provide analysis and propose solutions for the problems [3]–[6]. Another problem in demodulating receivers is the imbalance between the I and Q channels. Although these errors are usually corrected in the digital back end of the receiver, as in [7], we present a simple analog method to improve the receiver I/Q-channel amplitude balance by a mixer biasing arrangement.

This paper describes an implemented DCR, and more particularly, its downconversion stage including circuits to improve the even-order linearity and I/Q-amplitude balance. Section II presents the receiver topology as well the basic mixer structure. In Section III, the IIP2 canceling technique is introduced. The work is based on a theoretical study of the IIP2 and mismatches in transconductance mixers [8]. The I/Q-balancing circuit is discussed in Section IV, and Section V summarizes the work.

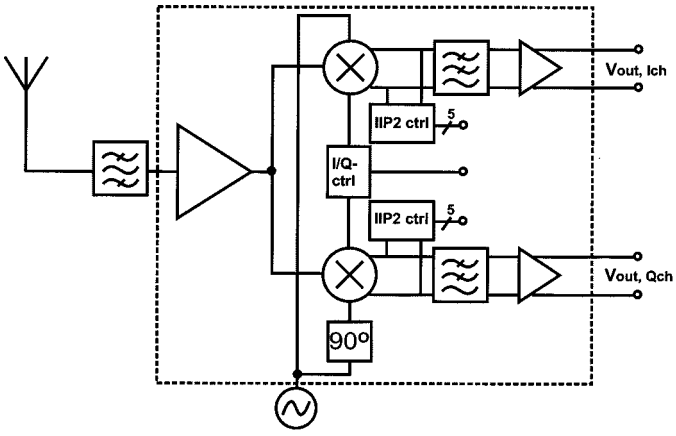

Fig. 1. Block diagram of implemented direct-conversion receiver.

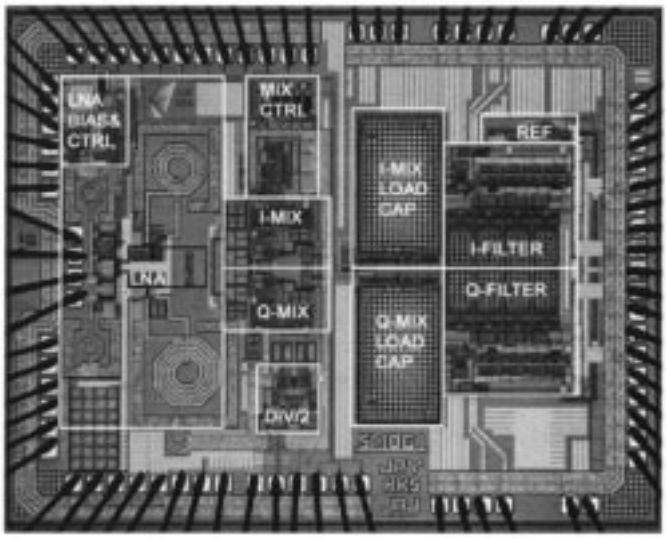

Fig. 2. Chip microphotograph.

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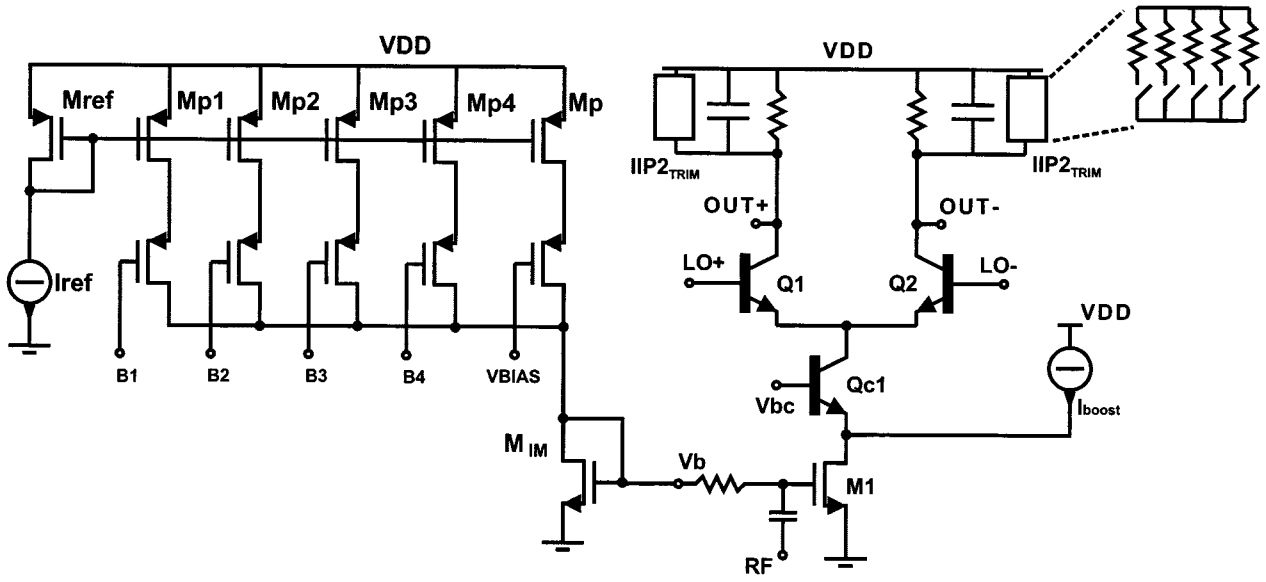


Fig. 3. Schematic of implemented mixer with tunable V-I stage and load resistors.

TABLE I
MEASURED RECEIVER PERFORMANCE AT 900 MHZ

Supply voltage	2.7 V
Current consumption	14.8 mA
Voltage gain	75.8 dB
NF (DSB)	4.6 dB
IIP3	-17 dBm
LO-to-RF isolation	> 65 dB
I/Q amplitude match (nom)	0.2 dB
I/Q phase match (nom)	3.5°

TABLE II
MEASURED PERFORMANCE OF SEVERAL RECEIVER SAMPLES

Sample	IIP2(nom) [dBm]	IIP2(trimmed) [dBm]	Improvement [dB]	ΔR(nom) [%]
S1	18	43	25	0.24
S2	13	38	25	0.12
S3	21	46	25	0.12
S4	16	42	26	0.12
S5	21	45	24	0.24
S6	16	39	23	0.23

II. RECEIVER ARCHITECTURE

A. Receiver Topology

The block diagram of the implemented direct-conversion receiver is shown in Fig. 1. The receiver consists of a low-noise amplifier (LNA), quadrature mixers, second-order intermodulation (IMD2) cancelers, local oscillator (LO) generation circuitry, an I/Q-balancing circuit, and a baseband circuit including channel selection filters. Thus, proper interfaces with the neighboring blocks of the mixer have been provided for reliable characterization. The measured receiver performance is given in Table I. The receiver uses a 2.7-V supply, and is characterized at 900-MHz frequency. The 75-dB receiver gain is divided by 25, 13.5, and 36.5 dB between LNA, mixer, and baseband, respectively. The microphotograph of the 7.2 mm^2 chip is shown in Fig. 2.

B. Mixer Topology

The single-balanced transconductance mixer is shown in Fig. 3. The nMOS V–I converter (M1) is isolated by means of a bipolar cascode transistor (Qc1) from the bipolar LO switching pair (Q1, Q2). Additional current to the input device is fed through a small-sized long-channel pMOS current source $I_{\rm boost}$. The current boosting technique is discussed in [9] and [10]. The positive and negative *RC* loads include digitally controllable resistors to implement second-order linearization described in Section III. The biasing of the transconductance stages in I and Q channels is tunable to allow gain balancing between quadrature channels. A single mixer consumes 2.2 mA.

III. IIP2 TRIMMING

Ideally, the even-order distortion would not exist in balanced circuits. In practical applications, however, it appears due to any asymmetry that causes nonideal cancellation of common-mode signals generated by even-order distortion. In the single-balanced mixer, the nonlinearity comes mainly from the input g_m device. The dominant asymmetries in the single-balanced mixer are the load resistor mismatch and the LO-signal duty-cycle deviation from the nominal (50%). These mismatches can be minimized by proper circuit design and layout techniques; however, unfortunately, the asymmetry is finally limited by the processing tolerances of the IC technology used. In Table II, the IIP2s and corresponding mixer load resistor mismatches are shown for several measured samples. Although the resistor mismatches are very small, relatively low IIP2s are observed. So, the effects of even-order distortion in symmetrically realized structures cannot be neglected, and the load resistor mismatch alone does not explain the deterioration of the IIP2 performance. It should be noticed that the IIP2 values are referred to the LNA

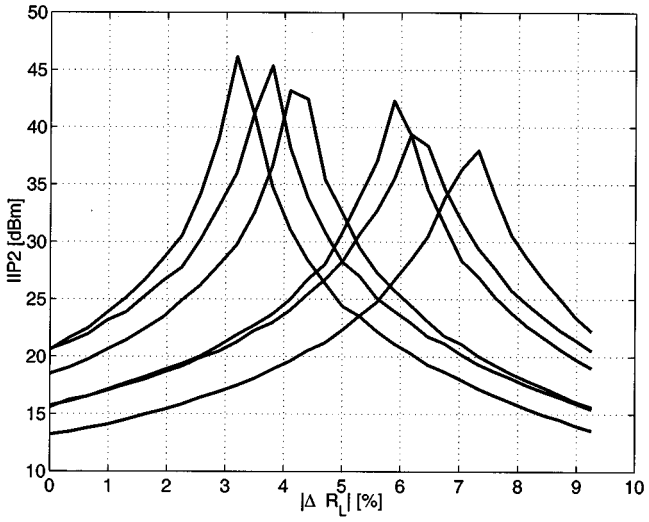
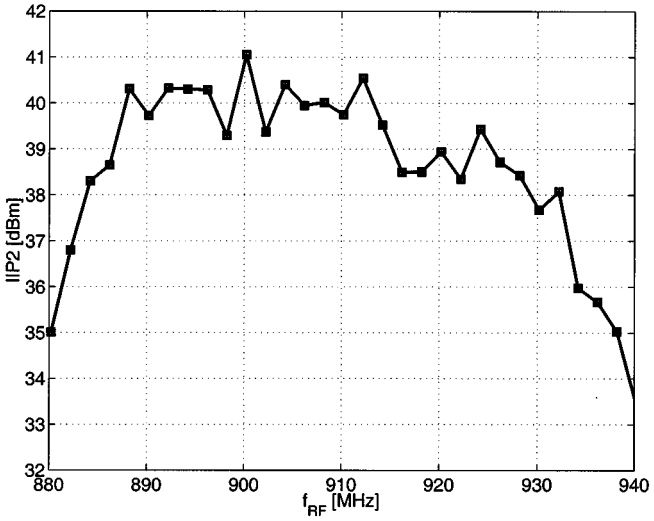


Fig. 4. Improved receiver IIP2 of six samples versus tuning range.

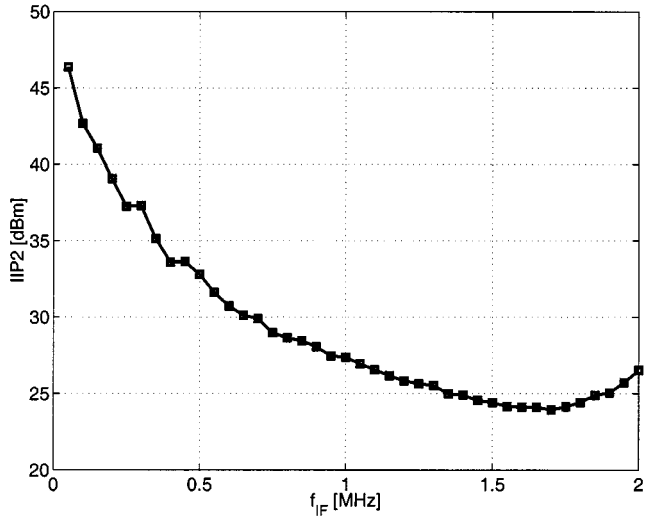
input and that the corresponding mixer performance is achieved by adding the LNA gain to the given values.

The realized IMD2 cancelers consist of binary-weighted multiples of equal-sized unit resistors, which have the same size as the actual load devices. The control of these additional loads is 5 bit. The switched resistors are placed in parallel to both mixer loads and are respectively different in I and Q channels, as these exhibit different IIP2 characteristics and should be calibrated separately. Fig. 4 illustrates the measured IIP2 of six receiver samples as a function of the controlled imbalance in the mixer load resistors. The tuning range is $\pm 10\%$ from the nominal mixer load resistance values. The tuning range and resolution were determined by simulations and known process tolerances and cover all the measured samples. The same method can be used in double-balanced mixers as well [8]. After the tuning, a mixer IIP2 of over $+60$ dBm can be observed for all samples. The mixer is preceded by an LNA having 25 dB of voltage gain, which has been extracted from the results. The ΔR that is needed to create a proper amount of imbalance to balance the circuit by the means of even-order nonlinearity is so small that it has a negligible effect on the other performance parameters such as gain, noise, or IIP3. Contrary to the general opinion, the mixer IIP2 can be maximized even if the circuit exhibits some amount of dc imbalance [8]. The direct tuning typically increases the dc offset at the mixer output. Nevertheless, the natural device mismatching always generates some amount of dc offset that must be removed in a DCR. The options available for removing the dc offset in DCRs depend on the system specifications, for example, bandwidth and modulation. In some cases, a high-pass filtering, which can be implemented by ac coupling or a servo feedback loop, may be suitable [11]. The linearizing devices can also be ac coupled to the mixer outputs, in which case the extraneous imbalance will not contribute more dc offset to the mixer output.

Fig. 5(a) illustrates the RF bandwidth of the IIP2 trimming. The two-tone test signals and LO signal are swept from 880 to 940 MHz, keeping the frequency of the IMD2 tone fixed. A substantially large bandwidth is needed in radio systems tuned to a wide range of RF carriers. The IIP2 of the uncalibrated receiver



(a)



(b)

Fig. 5. (a) Measured sensitivity of improved IIP2 as a function of Rx channel handover. (b) Measured downconversion channel response of trimmed IIP2.

shown is $+16$ dBm, having the improved value of $+39$ dBm. It may be seen that, as the tuning has been carried out at the 910-MHz frequency, the IIP2 remains over $+38$ dBm over the ± 20-MHz band. This band is sufficient directly for 900-MHz GSM band if the trimming is performed in the middle channels.

Another important aspect is the in-band dispersion of calibration along the frequency. While the calibration has been made at a fixed downconversion test frequency, it must be preserved over the entire modulation bandwidth. Fig. 5(b) illustrates the variation in IIP2 along the downconverted channel once the mixer has been trimmed. The IMD2 frequency has been changed by sweeping another input frequency in the two-tone test to produce the IF response of the IIP2. It may be seen that the IIP2 drops immediately after the frequency at which it has been trimmed (200 kHz). The *RC* load at the mixer output constitutes a first-order low-pass pole. The mixer load trimming significantly affects the output pole if it is located close to the channel corner frequency. Therefore, it shifts the pole frequency of the trimmed branch in the channel. This can be compensated capacitively to keep the pole frequencies approximately equal in

both branches during the trimming and in the entire downconversion band. If different cellular standards are considered, the compensation must be carried out at least in wide-band reception, e.g., in WCDMA. However, in narrow-band systems such as GSM, the tuning is adequate without frequency compensation. In addition, the IIP2 of the mixer is quite sensitive to the LO signal power. This sensitivity is avoided by proper on-chip LO generation and buffering. Also, the variations in the supply voltage and temperature can influence the calibration. These are all important design factors in determining how an automatic receiver calibration sequence can be implemented, and when the calibration should be performed. One example of a possible calibration procedure is given in [12].

IV. I/Q-Gain Balancing

Another essential problem in all quadrature-demodulating receivers is the channel imbalance. Although the DCR does not suffer from image frequency, the errors in channel amplitudes and phases affect the receiver bit-error rate. In a DCR, the amplitude equalization of the downconversion channels can be done at RF frequencies immediately after the received signal is fed into the I and Q mixers. The imbalance in I/Q amplitudes is corrected by adjusting the drain currents through the mixer transconductance elements. The mixer conversion gains can then be either increased or decreased using a 4-bit digitally controlled bias arrangement. The mixer g_m-stage bias arrangement shown in Fig. 3 is illustrated by means of a basic pMOS cascode current mirror. The pMOS transistors (M1–M4) are binary weighted and consist of unit transistors (Mref). Nominally the transconductor bias current is provided through the transistor (Mp) and half of the tuning range provided by the M1–M4. The realized tuning range is 1.5 dB with a maximum step of 0.13 dB and a minimum step of 0.09 dB. The tuning is monotonic but not linear as the g_m of the MOS transistor is changed. This method has only a moderate effect on the channel phase balance. The typical I/Q-phase deviation is 3.5° in the tuning range. Nominally, the measured I/Q-gain errors ranged from 0.1 to 0.2 dB, and after reduction, to less than 0.05 dB. The gain equalization has a small effect on the channel noise figure. However, this may be essential in receivers with a very low noise figure [13], if the mixer and following baseband stages have a high noise contribution to the receiver noise performance.

V. Conclusion

This paper presents an RF downconverter for a direct-conversion receiver. The presented mixer includes tunable resistive loads to improve the IIP2 performance. The achieved improvement in the receiver IIP2 is over 20 dB. The lowest calibrated receiver IIP2 was +38 dBm after trimming, thus becoming a mixer IIP2 of more than +63 dBm. The method used is simple and thus practical to adopt. It is applicable for double-balanced structures as well. In addition, it does not degrade the other receiver performance parameters such as noise or IIP3. It has a relatively wide band and so is insensitive to the RF frequency handovers. A simple mixer-biasing method is adopted in order to equalize the signal amplitudes in the quadrature downconversion channels and thus improve the I/Q-gain balance.

Acknowledgment

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