Cancellation of Load-Regulation in Low Drop-Out Regulators

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A method for canceling load-regulation, based on level shifting the reference, is proposed. In this architecture, the load current is monitored, sensed, and used to dynamically adapt the effective value of the reference voltage. The proposed architecture reduced a 2.5% load-regulation droop to a mere 0.2%, without compromising system stability.

Introduction: Modern state-of-the-art technologies require higher accuracy performance from voltage regulators. With load-regulation performance being a significant factor, special attention is warranted in reducing its negative effects. In typical low drop-out (LDO) topologies, dc open-loop gain is severely restricted because of stringent stability requirements. Process variations in the output and the vast load current range of the circuit impose severe challenges on frequency compensation, thereby allowing only low-gain circuits to be reliably stable [1].

Load regulation is defined as the output voltage variation resulting from a unit load current change, which is equivalent to describing the output resistance of the regulator, as is clear from equation (1), given a simple feedback circuit as illustrated in Fig.3(a),

$$R_{Load-reg} = \frac{\Delta V_{Out}}{\Delta I_{Load}} = \frac{R_{O-pass}}{1 + A_{OL}\beta}, \quad (1)$$

or, equivalently,

$$V_{Out} = V_{Ideal} - I_{Load} \cdot R_{Load-reg}, \quad (2)$$

where resistor $R_{O\text{-}pass}$ is the output resistance of the pass device, A_{OL} is the open-loop gain of the control circuit, and β is the feedback factor. As shown, load-regulation is inversely proportional to open-loop gain; but, as stated earlier, the gain cannot be high. The unity-gain frequency (UGF) is limited by the parasitic poles of the system and correspondingly restricts the bandwidth of the circuit. Load-regulation performance, as a result, is fundamentally poor.

Background: A couple of techniques have been proposed to tackle the load-regulation issue without excessively compromising stability. The first technique directly alters the Bode-plot performance of the circuit, while the later two adaptively optimize either the open-loop gain or the pole placement in the buffer stage.

1. ***Pole-zero generation*:** In this technique, the dc open-loop gain is augmented by adding a pole-zero pair in the transfer function. For a given UGF, dc open-loop gain is increased by increasing the gain-drop rate in the frequency response, as is shown in Trace-B of Fig.1. In essence, the gain drops faster with increasing frequencies, thereby allowing larger dc gains with equal bandwidths. Consequently, regulation performance is improved while maintaining a stable condition. The design location of the added pole and zero determine the maximum dc open-loop gain possible, given output filter requirements. The circuit can be realized, generally, in one of several ways, two of which are by the use of parallel amplifiers [2] and by a feed-forward capacitor [3], as shown in Fig.2 (a) and (b). The basic idea is to feed-forward the ac signal through a bypass path, constituted by either a low gain amplifier or by a capacitor. The amplifier is

unaffected by the feed-forward capacitor at low frequencies, and thus gives a high overall dc gain. At higher frequencies, the capacitor provides a parallel short circuit path, thereby giving rise to a lower high-frequency gain [3].

2. ***Load-Adaptive Techniques:*** In typical LDO architectures, the frequency response itself varies with load current; thus, to have good phase-margin, even in worst-case conditions, some trade-offs between gain and stability are necessary. Dynamically adapting the open-loop gain with load current helps in having a better phase-margin and a higher overall open-loop dc gain. To ensure that, in this architecture, the regulator uses a non-inverting, variable gain amplifier stage. In specific, the load current is sensed and used to modulate the output impedance of the second gain stage to keep the output pole beyond the UGF [4]. Thus, phase-margin performance is maximized, keeping the open-loop dc gain high and consequently load-regulation effects low.

   To similarly optimize the buffer, a load-dependent feedback signal may be used to modulate its conductance [5], [6]. As with the previous topology, the load current is sensed but a fraction of it is now fed back to a source-follower buffer stage. A positive feedback loop results but its gain is low and its signal is further attenuated with an RC filter, thereby not interfering with the negative feedback of the overall circuit [6].

Proposed Technique – Floating Reference LDO: The techniques described above either alter the frequency response or directly change the circuit, thereby compromising system stability. Ideally, an enhancing technique should cancel any load-regulation effects without altering the frequency response, or any other aspect, of the circuit, including

parametric performance. The proposed circuit architecture does just that while enjoying the luxury of simplicity.

As with the other techniques, the load current is sensed and fed back but it is only used to level-shift the reference in a benign fashion, as it relates to stability and circuit operation. Only the effective ground current of the control circuit is affected –it increases– but that too at a significantly reduced rate. Simply inserting a resistor in its path, between ground and the reference, produces a voltage drop that increases linearly with the load current, exactly the opposite effect of load-regulation. The mirroring of the current does not deteriorate current efficiency, as at zero-load current the mirrored current is also zero. Further, there is no change in the dc open-loop gain and hence the UGF is kept constant, thereby not compromising stability in the least. Overall, this topology is capable of completely canceling all load-regulation effects by appropriately choosing a resistor, as is clear from equation (3),

$$V_{Out} = V_{Ideal} - \left(\frac{R_{O-pass}}{1 + A_{OL}\beta} - \frac{R_{Low}}{C} \right) \cdot I_{Load}, \tag{3}$$

where R_{Low} is the resistance, through which, the mirrored current is passed to level shift the reference and C is the factor by which the load current is reduced in the mirror (e.g., for A_{OL} = 100, β = 1, $R_{O\text{-}pass}$= 10 Ω, and C = 1000, R_{Low} = 100 Ω yields zero load-regulation effects).

Results: The design was fabricated and tested with provisions to adjust resistor R_{Low}. Near zero load-regulation effects were observed; higher resolution of R_{Low} could have given still better results. As is obvious from the test results, shown in Fig.4 (b), the proposed architecture reduced a 60 mV load-regulation droop, which is prevalent in most widely stable LDO regulators, to a mere 5 mV, without sacrificing stability or affecting

any other aspect of the circuit. The fact that stability is intact is shown through simulations by the open-loop frequency response (Fig.4 (a)), phase and gain margin are unaffected by adding the resistor. With frequency response unchanged, the method is relatively easy to apply to most LDO topologies and, consequently, nearly cancel all load-regulation effects.

Conclusion: From a design perspective, the proposed architecture is simple and benign, and effectively cancels all load-regulation effects. Other topologies directly alter either the circuit and/or the gain and hence the frequency response, more than likely compromising stability. For optimal performance (complete cancellation), the value of R_{Low} can be easily trimmed during wafer testing, requiring only a few bits (e.g. three bits for roughly 3-4 mV resolution) [7].

References:

[1] Goodenough, F.: 'Low Dropout Linear Regulators', *Electronic Design,* pp. 65-77, May 13, 1996.

[2] Rincón-Mora, G.A.: 'Optimized frequency shaping circuit topologies for LDOs' *United States Patent No*.5,982,226*,* November 1999.

[3] Rincón-Mora, G.A., and Allen, P.E.: 'Optimized Frequency Shaping Circuit Topologies for LDOs'*, IEEE Transactions on Circuits and Systems II, pp. 703-708,* June 1998.

[4] Xi, Xiaoyu: 'PMOS low drop-out voltage regulator using non-inverting variable gain stage', *United States Patent No*. 6,246,221, September 2000.

[5] Rincón-Mora, G.A., and Allen, P.E.: 'A Low Voltage, Low Quiescent Current, Low Drop-out Regulator', *IEEE Journal of Solid-State Circuits*, pp. 36-44, January 1998.

[6] Rincón-Mora, G.A.: 'Low-dropout voltage regulator incorporating a current efficient transient response boost circuit', *United States Patent No.* 6,046,577, April 2000.

[7] Rincón-Mora, G.A.: 'Voltage Reference- from Diodes to Precision High-Order Bandgap Circuits', *IEEE Press, Wiley Interscience*, pp. 126-130, 2002.

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Figure Captions:

Fig.1: Bode plot.

Fig.2: (a) Parallel Amplifier and (b) Feed-Forward Capacitor.

Fig.3: (a) Basic Architecture (b) Proposed Architecture.

.***Fig.4:*** (a) Bode plot and (b) Load Regulation.

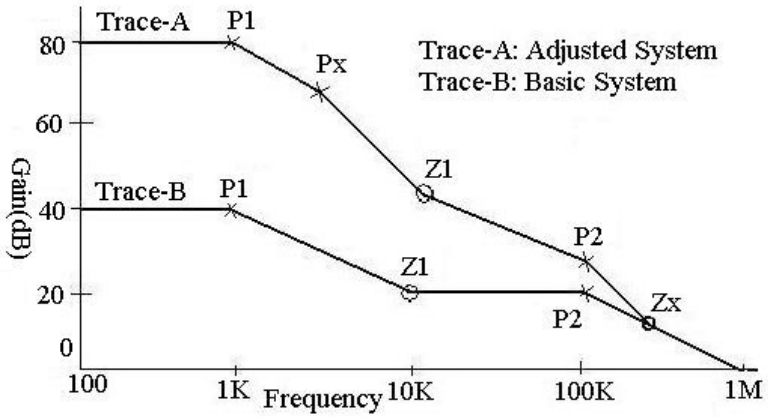

Fig.1: Bode plot.

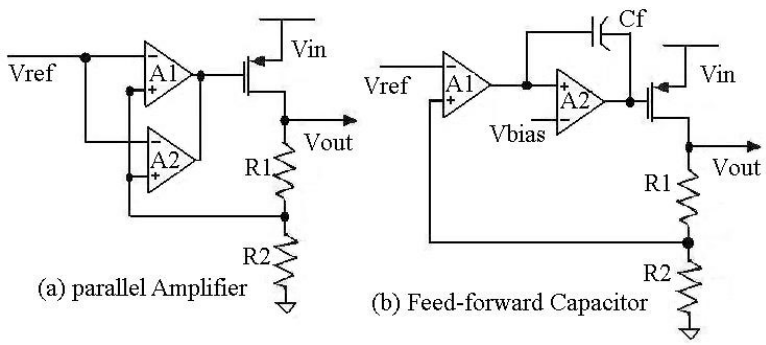

Fig.2: (a) Parallel Amplifier and (b) Feed-forward Capacitor.

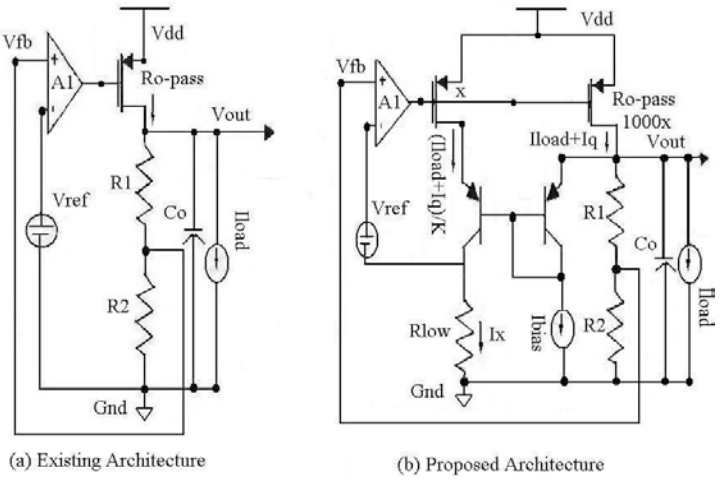

Fig.3: (a) Basic Architecture and (b) Proposed Architecture.

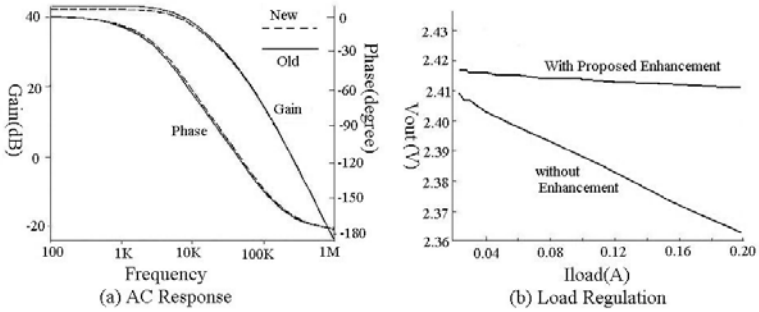

Fig.4: (a) Bode plot and (b) Load Regulation.