Capacitance modeling of laterally non-uniform MOS devices

A.C.T. Aarts, R. van der Hout[+], J.C.J. Paasschens, A.J. Scholten, M. Willemsen, and D.B.M. Klaassen

Philips Research Laboratories, Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands

[+]also at: School of Engineering and Science, International University Bremen, Postfach 750561, D-28725 Bremen, Germany

Phone: +31-40-2742418; Fax: +31-40-2744113; E-mail: annemarie.aarts@philips.com

Abstract

In compact transistor modeling for circuit simulation, the capacitances of conventional MOS devices are commonly determined as the derivatives of terminal charges, which on their turn are obtained from the so-called Ward-Dutton charge partitioning scheme [1]. For devices with a laterally non-uniform channel doping profile, however, it is shown in this paper that 1) *no* terminal charges exist for the description of capacitances. Instead, 2) a model is presented for the capacitances of such devices, including numerical results for a MOS transistor with a laterally diffused channel doping profile. Finally, 3) a method is given to incorporate such a capacitance model in circuit simulators which are traditionally based on terminal charge models.

Introduction

LDMOS devices are well-known examples of MOS devices with a laterally non-uniform channel doping profile. Accurate modeling of capacitances in high-voltage LDMOS devices is a prerequisite for integrated RF-design of, for instance, switch-mode power supplies and power amplifiers. For high-voltage devices often the sub-circuit model approach is followed, but the effect of the lateral non-uniformity in the channel is usually neglected [2-6]. Efforts have been taken to incorporate the lateral channel non-uniformity in a terminal charge model [7-9]. However, we will show that incorporation of a lateral channel non-uniformity via a terminal charge model is incorrect.

LDMOS devices

The channel doping N_A of an LDMOS device decreases from source to drain; see Fig. 2a. The n^--drift region is needed to withstand high voltages. In Fig. 2b a typical capacitance measurement on an LDMOS device is shown, together with the simulation result of a sub-circuit model comprising MOS Model 11 (MM11; [10]) for the channel region and MOS Model 31 (MM31; [10]) for the drift region. The discrepancy between measurements and modeling results triggered device simulations of a MOSFET with the same non-uniform channel doping profile, but without a drift region; see Fig. 2c. This last figure shows that the non-uniform channel doping profile causes a peak in the capacitance behavior, which is accurately described by a segmentation approach [11] using 20 segments each modeled by MM11 with parameters varying according to the doping profile.

Laterally uniform MOSFETs

Before turning to laterally non-uniform MOSFETs, we recall the charge and capacitance modeling of uniform MOSFETs. As shown by [1], charges can be assigned to each terminal, where the source- and drain charge are obtained from the inversion charge using the well-known Ward-Dutton charge partioning scheme. From these terminal charges Q_i the capacitances $C_{ij} = (2 \cdot \delta_{ij} - 1) \cdot \partial Q_i / \partial V_j$ follow (i and j = S, G, D or B; see also [12]). The existence of a terminal charge Q_i implies **1)** $(2 \cdot \delta_{ij} - 1) \cdot \partial C_{ij} / \partial V_k = (2 \cdot \delta_{ik} - 1) \cdot \partial C_{ik} / \partial V_j$, and **2)** the integral $q_{c,\,i}$ of the charging current through terminal i for a closed voltage cycle in time equals zero, i.e. $q_{c,i} \equiv \oint [I_i(t) - I_T(t)]\,\mathrm{d}t = 0$, where I_i is the total current through terminal i and I_T is the transport current. The fact that $q_{c,i} = 0$ can be understood from $I_i(t) - I_T(t) = \mathrm{d}Q_i/\mathrm{d}t$, with Q_i varying with the terminal voltages V_j.

Laterally non-uniform MOSFETs

We have tested both implications —noted **1)** and **2)** above— of the existence of terminal charges for a laterally non-uniform MOSFET using device simulations as well as circuit simulations with the segmentation approach mentioned above (see Fig. 3). From these tests we have found that for laterally non-uniform MOSFETs, charges can be attributed to the gate and bulk terminal (see Fig. 3b and Fig. 3c), but **not** to the source and drain terminal (see Fig. 3a and Fig. 3c). This is in line with the general observations on non-linear dissipative systems [13] and with the terminal charge conservation constraints in [14]. Consequently, for the compact modeling of laterally non-uniform MOSFETs expressions for the source and drain related capacitances have to be derived directly.

New capacitance model for laterally non-uniform devices

We consider the current I through the device, given by (1); see Fig. 1. For simplicity we assume a constant electron mobility, but this is not a fundamental limitation and the approach can be extended to include mobility degradation and velocity saturation. By a perturbation of the voltages according to (2) around its dc-solution (3), the imaginary parts of the small-signal drain and source currents, under quasi-static operation, are given by (4). Since the variation ΔQ_{inv} of inversion charge with time is due to a perturbation of, e.g., the gate voltage, these small-signal currents can be written according to (5). Notice that for a uniform MOSFET, the second term at the right-hand side of (5)

0-7803-8684-1/04/$20.00

equals zero since $\partial Q_{\rm inv}/\partial x = 0$, and consequently the Ward-Dutton charge partioning scheme is obtained. With the small-signal solution given by (6), we determine the capacitances $C_{{\rm D}j} = (2\delta_{{\rm D}j} - 1) \cdot i_2(L)$ and $C_{{\rm S}j} = -(2\delta_{{\rm S}j} - 1) \cdot i_2(0)$. In Fig. 4 and Fig. 5 the capacitances, calculated from these equations elaborated in the surface-potential formalism, compare very well to the ones obtained from 2D-device simulation (MEDICI) as well as from the segmentation model mentioned above.

Incorporation of capacitance model into circuit simulators

Conventional circuit simulators are based on terminal charges. We have developed a method to implement capacitances directly into these circuit simulators. This method is illustrated in Fig. 6a. In Fig. 6b the total charging currents through the terminals for a closed voltage cycle in time (see also Fig. 3c) are shown for the segmentation approach and for a capacitance model for a laterally non-uniform MOSFET developed along the formulas of Fig. 1. Clearly, both implementations yield the same results, demonstrating that such capacitance-based models can be implemented in conventional circuit simulators.

Conclusions

In this paper, we have shown that (i) laterally non-uniform channel doping profiles in, for instance, LDMOS devices and conventional MOS devices with heavy pocket implantations, lead to a capacitance behavior that is fundamentally different from that of MOSFETs with uniform channels. Furthermore, we have demonstrated that (ii) for these devices as a consequence of these laterally non-uniform channel doping profiles, no source and drain charges exist. Finally, we have (iii) derived a capacitance model for MOS devices with a laterally non-uniform channel doping profile and (iv) presented a method to implement such a capacitance-based model into standard charge-based circuit simulators.

References

[1] D.E. Ward, Charge-Based modeling of capacitance in MOS transistors, Ph.D. Thesis, Stanford University (1981).

[2] Y. Subramanian *et al.*, MSM 1999, pp.284-288.

[3] S.F. Frere *et al.*, ESSDERC 2001, pp.219-222.

[4] J. Jang *et al.*, MTT-S 2001, pp.967-970.

[5] C. Liu and J.B. Kuo, Trans. Electron Devices **44**, pp.1117-1123 (1997).

[6] J. Victory *et al.*, SISPAD 1998, pp.271-274.

[7] N. D'Halleweyn *et al.*, ISPSD 2001, pp.291-294.

[8] Y. Kim *et al.*, Trans. Electron Devices **38**, pp.1641-1649 (1991).

[9] Y. Chung, Circuits Devices Syst. **147**, pp.219-227 (2000).

[10] MM11 & MM31: www.semiconductors.philips.com/Philips_Models.

[11] A.J. Scholten, IEDM 1999, pp. 163-166.

[12] Y. Tsividis, Operation and Modeling of the MOS Transistor, McGraw-Hill (1987).

[13] H.K. Dirks, Kapazitätskoeffizienten nichtlinearer dissipativer Systeme, Habilitationsschrift, Aachen University of Technology (1988).

[14] D.E. Root, MWSCAS 2001, pp. 768-772.

Channel current: $I = W \cdot \mu \cdot (-Q_{\rm inv}) \cdot \frac{\partial V}{\partial x}, \qquad \frac{\partial I}{\partial x} = W \cdot \frac{{\rm d}Q_{\rm inv}}{{\rm d}t}, \qquad Q_{\rm inv} = Q_{\rm inv}\left(V, V_{\rm GB}, x\right).$ (1)

Small-signal analysis: $V_{\rm GB}(t) = \overline{V}_{\rm GB} + \overline{v}_{\rm GB} \cdot {\rm e}^{j\cdot\omega\cdot t} \qquad V_{\rm DB}(t) = \overline{V}_{\rm DB} + \overline{v}_{\rm DB} \cdot {\rm e}^{j\cdot\omega\cdot t}, \qquad V_{\rm SB}(t) = \overline{V}_{\rm SB} + \overline{v}_{\rm SB} \cdot {\rm e}^{j\cdot\omega\cdot t},$

$$I(x,t) = \overline{I}(x) + (i_1(x) + j\cdot\omega\cdot i_2(x)) \cdot {\rm e}^{j\cdot\omega\cdot t}, \qquad V(x,t) = \overline{V}(x) + (v_1(x) + j\cdot\omega\cdot v_2(x)) \cdot {\rm e}^{j\cdot\omega\cdot t}. \quad (2)$$

Dc-current: $\overline{I}(x) = -W \cdot \mu \cdot Q_{\rm inv}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right) \cdot \frac{{\rm d}\overline{V}(x)}{{\rm d}x}, \qquad \frac{{\rm d}\overline{I}(x)}{{\rm d}x} = 0.$ (3)

Small-signal current: $i_2(L) = W \cdot \int_0^L \Delta Q_{\rm inv}(x) \cdot \frac{x}{L}\,{\rm d}x + \frac{W\cdot\mu}{L} \cdot \int_0^L \frac{\partial Q_{\rm inv}}{\partial x}(\overline{V}(x), \overline{V}_{\rm GB}, x) \cdot v_2(x)\,{\rm d}x,$

$$i_2(0) = -W \cdot \int_0^L \Delta Q_{\rm inv}(x) \cdot \left(1 - \frac{x}{L}\right){\rm d}x + \frac{W\cdot\mu}{L} \cdot \int_0^L \frac{\partial Q_{\rm inv}}{\partial x}(\overline{V}(x), \overline{V}_{\rm GB}, x) \cdot v_2(x)\,{\rm d}x,$$

where $\Delta Q_{\rm inv}(x) = \frac{\partial Q_{\rm inv}}{\partial V}(\overline{V}(x), \overline{V}_{\rm GB}, x) \cdot v_1(x) + \frac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}(\overline{V}(x), \overline{V}_{\rm GB}, x) \cdot \overline{v}_{\rm GB}.$ (4)

No charges: $i_2(L) = W \cdot \frac{\partial}{\partial \overline{V}_{\rm GB}} \left\{ \int_0^L Q_{\rm inv}(\overline{V}(x), \overline{V}_{\rm GB}, x) \cdot \frac{x}{L}\,{\rm d}x \right\} + \frac{W\cdot\mu}{L} \cdot \int_0^L \frac{\partial Q_{\rm inv}}{\partial x}(\overline{V}(x), \overline{V}_{\rm GB}, x) \cdot v_2(x)\,{\rm d}x,$

$$-i_2(0) = W \cdot \frac{\partial}{\partial \overline{V}_{\rm GB}} \left\{ \int_0^L Q_{\rm inv}(\overline{V}(x), \overline{V}_{\rm GB}, x) \cdot \left(1 - \frac{x}{L}\right){\rm d}x \right\} - \frac{W\cdot\mu}{L} \cdot \int_0^L \frac{\partial Q_{\rm inv}}{\partial x}(\overline{V}(x), \overline{V}_{\rm GB}, x) \cdot v_2(x)\,{\rm d}x. \quad (5)$$

Capacitance model: $v_1(x) = {\rm e}^{\Gamma(x)} \cdot \left(\overline{v}_{\rm SB} + C \cdot T(x) - \overline{v}_{\rm GB} \cdot \int_0^x \frac{\frac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}(\overline{V}(s), \overline{V}_{\rm GB}, s)}{Q_{\rm inv}(\overline{V}(s), \overline{V}_{\rm GB}, s)} \cdot \frac{{\rm d}\overline{V}(s)}{{\rm d}s} \cdot {\rm e}^{-\Gamma(s)}\,{\rm d}s \right),$

$$C = \frac{1}{T(L)} \cdot \left(\overline{v}_{\rm DB} \cdot {\rm e}^{-\Gamma(L)} - \overline{v}_{\rm SB} + \overline{v}_{\rm GB} \cdot \int_0^L \frac{\frac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}(\overline{V}(x), \overline{V}_{\rm GB}, x)}{Q_{\rm inv}(\overline{V}(x), \overline{V}_{\rm GB}, x)} \cdot \frac{{\rm d}\overline{V}(x)}{{\rm d}x} \cdot {\rm e}^{-\Gamma(x)}\,{\rm d}x \right),$$

$$v_2(x) = {\rm e}^{\Gamma(x)} \cdot \frac{L}{\mu} \cdot \left(T(x) \cdot \int_0^L \frac{-\Delta Q_{\rm inv}(s)}{C_{\rm ox}} \cdot \left(1 - \frac{T(s)}{T(L)}\right){\rm d}s - \int_0^x \frac{-\Delta Q_{\rm inv}(s)}{C_{\rm ox}} \cdot (T(x) - T(s))\,{\rm d}s \right),$$

$$\Gamma(x) = -\int_0^x \frac{\frac{\partial Q_{\rm inv}}{\partial V}\left(\overline{V}(s), \overline{V}_{\rm GB}, s\right)}{Q_{\rm inv}\left(\overline{V}(s), \overline{V}_{\rm GB}, s\right)} \cdot \frac{{\rm d}\overline{V}(s)}{{\rm d}s}\,{\rm d}s, \qquad T(x) = \frac{C_{\rm ox}}{L} \cdot \int_0^x \frac{{\rm e}^{-\Gamma(s)}}{-Q_{\rm inv}\left(\overline{V}(s), \overline{V}_{\rm GB}, s\right)}\,{\rm d}s. \quad (6)$$

Figure 1: Derivation of the new capacitance model, for a laterally non-uniform MOS device with its inversion charge $Q_{\rm inv}$ *explicitly* dependent on the lateral position x. Here, I denotes the current through the device, V denotes the quasi-Fermi potential, μ the electron mobility, $C_{\rm ox}$ the oxide capacitance per unit area, and W the width and L the length of the device.

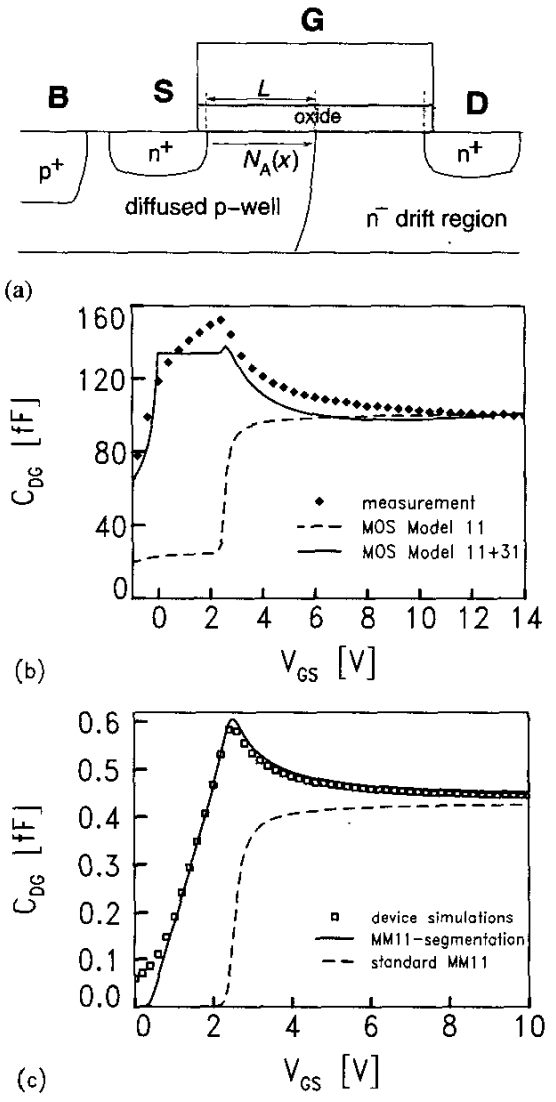

Figure 2: **(a)** Cross-section of an LDMOS device with a diffused p-well MOS channel region and an n^--type drift region. **(b)** Drain-gate capacitance of an LDMOS device, with total oxide capacitance $C_{ox,tot} = 180$ fF, at $V_{DS} = 0$V: symbols represent measurements; lines represent compact model simulations. Note that the threshold voltage observed in the capacitance resulting from MM11 is dictated by the I-V characteristic, which in its turn is determined by the threshold voltage of the channel region at the source side. **(c)** Drain-gate capacitance of a MOSFET ($C_{ox,tot} = 0.86$ fF) with a non-uniform channel doping profile at $V_{DS} = 0$V: symbols represent device simulations using MEDICI; the dashed line represents a compact model simulation using MM11; the solid line represents a simulation using 20 segments each modeled by MM11 with parameters varying according to the doping profile (see also [11]).

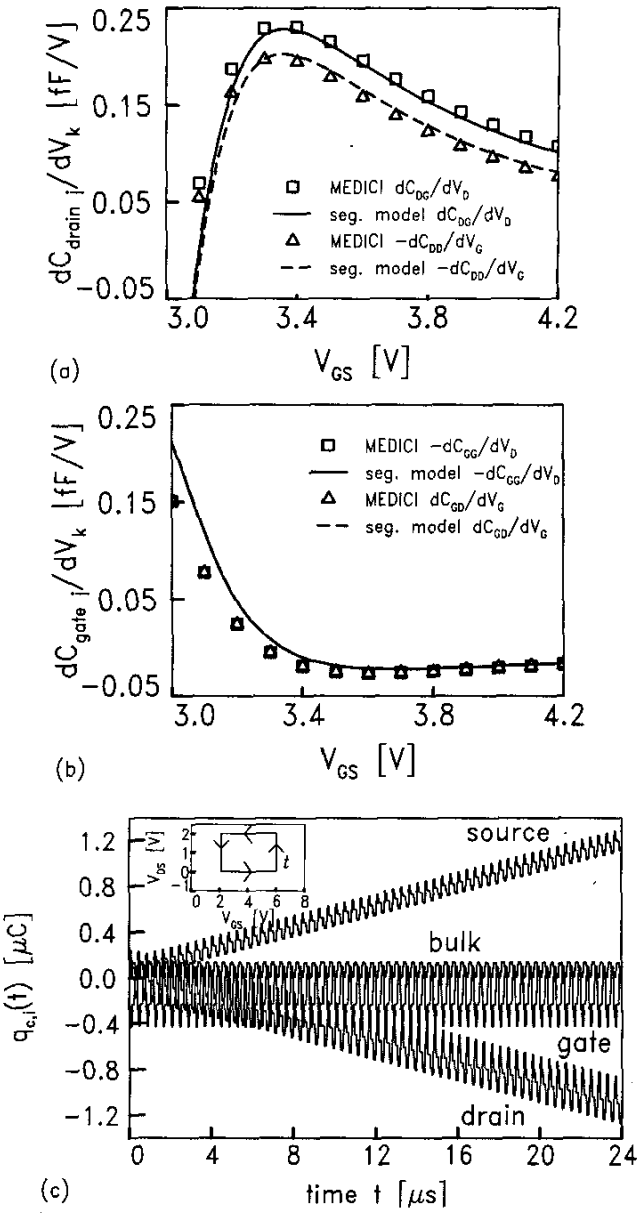

Figure 3: Partial derivatives of drain **(a)** and gate **(b)** related capacitances for a laterally non-uniform MOSFET with diffused doping profile $N_A(x) = N_{A0} \cdot \exp(-D \cdot (x/L)^2)$, $D = 2.78$, at $V_{DS} = 0.5$V. Symbols represent MEDICI simulations and lines the segmentation model. **(c)** Integral of the charging current through the terminals of the same device for closed voltage cycles in time (according to the inset, 0.4μs cycle time), obtained using the segmentation model.

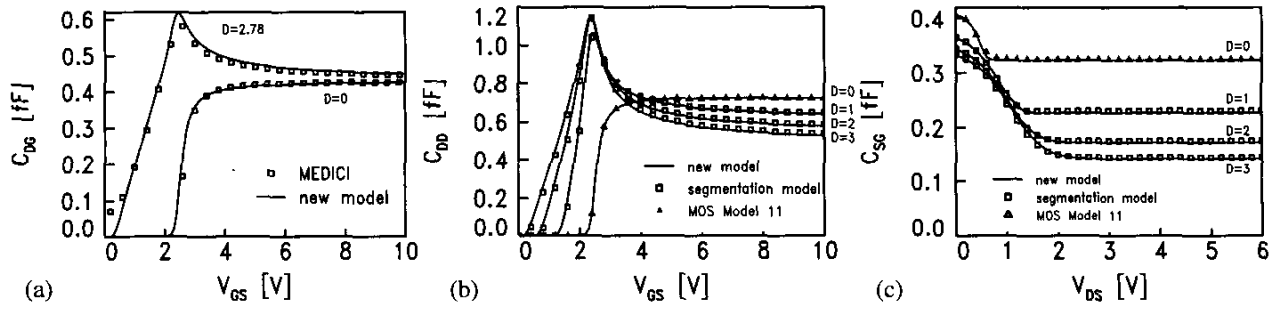

Figure 4: **(a)** Comparison of the drain-gate capacitance between MEDICI device simulations (symbols) and the new model (solid lines), for $V_{DS} = 0$V. Influence of the diffused doping profile $N_A(x) = N_{A0} \cdot \exp(-D \cdot (x/L)^2)$ on the **(b)** drain-drain capacitance for $V_{DS} = 0$V, and the **(c)** source-gate capacitance for $V_{GS} = 4$V, calculated by the new model (solid lines) and compared to MOS Model 11 for $D = 0$ and to the segmentation model for $D = 1$, 2 and 3 (symbols). In this figure the total oxide capacitance equals $C_{ox,tot} = 0.86$ fF.

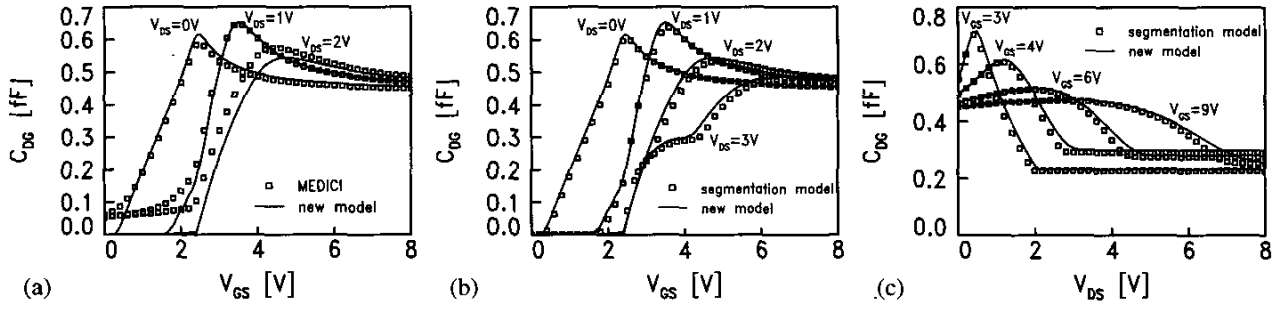

Figure 5: Drain-gate capacitance of the new model (solid lines) compared to **(a)** device simulations (symbols) and **(b,c)** segmentation model (symbols), for $C_{ox,tot} = 0.86$ fF, and a diffused doping profile $N_A(x) = N_{A0} \cdot \exp(-D \cdot (x/L)^2)$, $D = 2.78$.

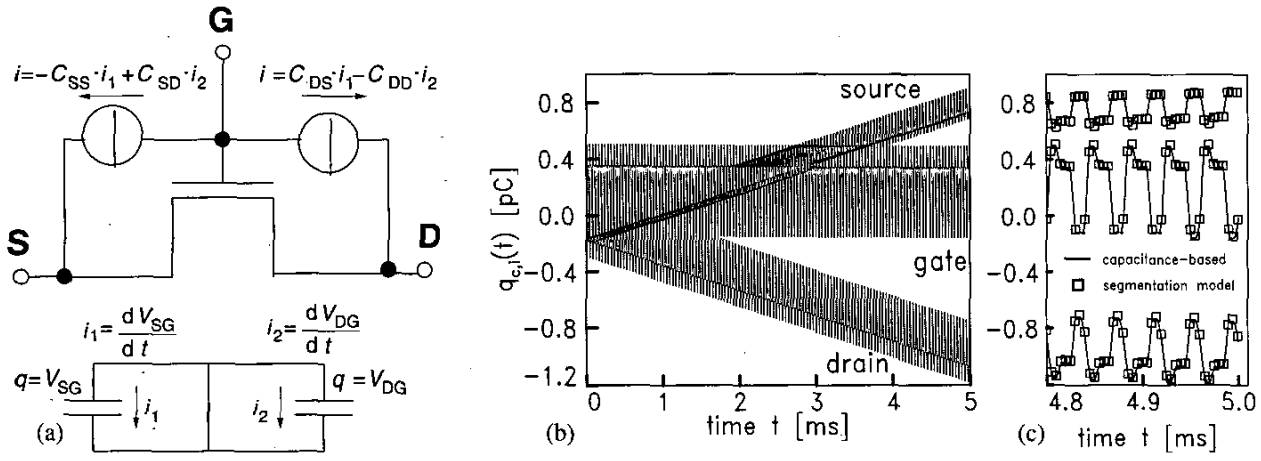

Figure 6: **(a)** Equivalent circuit for a three-terminal device illustrating the method to implement capacitances into circuit simulators. **(b)** Integral of the charging current through the terminals for closed voltage cycles in time (see Fig. 3c), obtained by means of a capacitance-based model developed along the lines of Fig. 1 (solid lines). **(c)** Detail of **(b)** of the integral of the charging currents, in comparison with those obtained by means of the segmentation model (symbols).