June 2006

Capacitance-voltage studies on enhancement-mode InGaAs metal-oxide-semiconductor field-effect transistor using atomic-layer-deposited AI2O3 gate dielectric

Y. Xuan
Birck Nanotechnology Center and School of Electrical and Computer Engineering, Purdue University,

H. C. Lin
Birck Nanotechnology Center and School of Electrical and Computer Engineering, Purdue University

P. D. Ye
Birck Nanotechnology Center and School of Electrical and Computer Engineering, Purdue University, yep@purdue.edu

G. D. Wilk
ASM America

Follow this and additional works at: http://docs.lib.purdue.edu/nanopub

Capacitance-voltage studies on enhancement-mode InGaAs metal-oxide-semiconductor field-effect transistor using atomic-layer-deposited Al₂O₃ gate dielectric

Y. Xuan, H. C. Lin, and P. D. Ye[a)]
*School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907
and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907*

G. D. Wilk
ASM America, 3440 East University Drive, Phoenix, Arizona 85034

Atomic layer deposition (ALD) Al_2O_3 is a high-quality gate dielectric on III-V compound semiconductor with low defect density, low gate leakage, and high thermal stability. The high-quality of Al_2O_3/InGaAs interface surviving from high temperature annealing is verified by excellent capacitance-voltage (CV) curves showing sharp transition from depletion to accumulation with "zero" hysteresis, 1% frequency dispersion per decade at accumulation capacitance, and strong inversion at split CV measurement. An enhancement-mode n-channel InGaAs metal-oxide-semiconductor field-effect-transistor is also demonstrated by forming true inversion channel at Al_2O_3/InGaAs interface. © *2006 American Institute of Physics.*
[DOI: 10.1063/1.2217258]

Innovative device structures and gate dielectrics are needed to further drive Si complementary metal-oxide-semiconductor (CMOS) integration, functional density, speed, and power dissipation and extend CMOS front-end fabrication to and beyond the 22 nm node. One emerging strategy is to use III-V compound semiconductors as conduction channels to replace traditional Si or strained Si, while integrating these high mobility materials with novel dielectrics and heterogeneously integrating them on Si or silicon on insulator (SOI). For more than four decades, the research community has been searching for suitable gate dielectrics or passivation layers on III-V compound semiconductors. There are tremendous efforts and many literatures in this field.[1–6] The main obstacle is the lack of high-quality, thermodynamically stable insulators on GaAs that can match the device criteria as SiO_2 on Si, e.g., a mid-band-gap interface trap density (D_{it}) of $\sim 10^{10}$/cm² eV. Recently, *in situ* molecular beam epitaxy (MBE) growth of $Ga_2O_3(Gd_2O_3)$ and *ex situ* atomic layer deposition (ALD) growth of Al_2O_3 attract particular attentions.[7–9] The research on ALD high-k dielectric is of particular interest, since the Si industry is getting familiar with ALD Hf-based dielectrics and this approach has the potential to become a manufacturable technology. In our previous work, we have succeeded to integrate ALD high-k dielectric Al_2O_3 on GaAs, InGaAs, and GaN and demonstrated high performed depletion-mode III-V metal-oxide-semiconductor field-effect-transistors (MOSFETs).[10–12] For very large scale integrated (VLSI) circuits or high-speed digital applications, enhancement-mode (E-mode) GaAs MOSFETs are the real devices of interest.[13,14]

In this letter, we report detailed CV measurements on high temperature annealed ALD Al_2O_3 dielectrics on InGaAs and IV characterization on a fabricated E-mode InGaAs MOSFET where the inversion channel is directly formed at the Al_2O_3/InGaAs interface. Al_2O_3 is a widely used insulat-

ing material for gate dielectric, tunneling barrier, and protection coating due to its excellent dielectric properties, strong adhesion to dissimilar materials, and its thermal and chemical stabilities. Al_2O_3 has a high band gap (~ 9 eV), a high breakdown electric field (5–30 MV/cm),[15] a high permittivity (8.6–10), and a high thermal stability. Compared to the conventional methods to form thin Al_2O_3 films, i.e., by sputtering, electron beam evaporation, chemical vapor deposition, or oxidation of pure Al films, the ALD Al_2O_3 is of much higher quality. The ALD high-k materials including Al_2O_3 are the leading candidates to substitute SiO_2 for sub-100 nm Si complementary MOSFET applications.[16] ALD also provides unique opportunity to integrate high-quality gate dielectrics on non-Si semiconductor materials such as Ge, the leading high mobility channel material for future p-type MOSFETs.[17]

Figure 1(a) shows the device structure of the fabricated E-mode n-channel $Al_2O_3/In_{0.2}Ga_{0.8}As/GaAs$ MOSFET and the capacitor to characterize the Al_2O_3/InGaAs interface. A 150 nm p-doped 4×10^{17}/cm³ buffer layer, a 285 nm p-doped 1×10^{17}/cm³ intermediate layer, and a 13.5 nm p-doped 1×10^{17}/cm³ $In_{0.2}Ga_{0.8}As$ channel layer, were sequentially grown by metal-organic chemical-vapor deposition (MOCVD) on a 2 in. GaAs p^+ substrate. After appropriate surface pretreatment, 16–30 nm ALD Al_2O_3 was
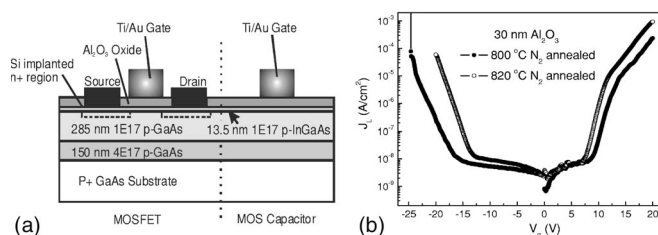

FIG. 1. (a) Cross sections of an *E*-mode Al_2O_3/InGaAs MOSFET and an Al_2O_3/InGaAs capacitor fabricated at the same process. (b) Leakage current density J_L (A/cm²) vs gate bias V_g (V) in different thermal processes. The data are taken from finished Al_2O_3/InGaAs MOSFETs with 30 nm thick gate dielectrics.

[a)]Author to whom correspondence should be addressed; electronic mail: yep@purdue.edu

88, 263518-1

deposited at 300 °C using an ASM Pulsar2000™ ALD module. The ALD Al_2O_3 is served not only as a gate dielectric but also as an encapsulation layer due to its high thermal and chemical stabilities. The source and drain contact regions are Si implanted and activated at 750–850 °C by rapid thermal annealing (RTA) in N_2 ambient. Dopant activation annealing is a very critical step which not only activates the dopant but also must preserve the smoothness of the interface at the atomic level. Using a wet etching in diluted HF, the oxide on the source and drain regions was removed while the gate area was protected by photoresist. Ohmic contacts were formed by electron beam deposition of Au/Ge/Au/Ni/Au and a lift-off process, followed by a 400 °C anneal in N_2 ambient. Finally, conventional Ti/Au metals were e beam evaporated, followed by lift-off to form the gate electrodes. The sheet resistance of the implanted source/drain region and its contact resistance are measured from transfer length method (TLM) to be $\sim 300 \ \Omega$/sq and $\sim 1.0 \ \Omega$ mm, which demonstrates good process on implantation and activation. The designed gate lengths of the measured devices are 0.65, 0.85, 1, 2, 4, 8, 20, and 40 μm. It is not a self-aligned process. The overlap length between gate and source/drain is estimated around $\sim 0.5 \ \mu$m or less.

The Al_2O_3 dielectric films are highly electrically insulating, showing very low leakage current density of $\sim 10^{-9}$–10^{-8} A/cm^2 for amorphous films thicker than 6 nm.[15] The leakage current density starts to increase after high temperature annealing which is required to activate Si dopants implanted in GaAs. The increase of leakage currents is due to the creation of more leakage paths around crystallized grains in the amorphous films after high temperature annealing. As shown in Fig. 1(b), we measure the leakage current density (J_L) on 30 nm ALD Al_2O_3 versus the applied potential on the capacitor (V_g) with high annealing temperatures. The positive bias means that the metal electrode is positive with respect to GaAs, as shown in Fig. 1(a). The plot shows extremely low leakage current density in ALD Al_2O_3 films even after 800 °C annealing, though a significant increase in current density exhibits with increasing annealing temperature to 820 °C. 850 °C is the critical temperature when the crystallization in amorphous Al_2O_3 becomes severe and the leakage current increases dramatically.

The CV measurements are widely used to quantitatively study a MOS structure. Three quantities are the most important factors to evaluate high-k dielectrics on novel channel materials. The first is the amount of hysteresis that results when the MOS capacitor is biased well into accumulation and inversion. The second is the interface trap density D_{it} at the interface showing in CV curve how rapid the transition is between accumulation and inversion. The third is the frequency dispersion on accumulation capacitances and flatband shifts. We focus on the CV characterization of ALD Al_2O_3 on InGaAs after high temperature annealing between 750 and 850 °C which is required to activate Si dopants in InGaAs. Note that better CV curves or D_{it} might exhibit under annealing temperature between 450 and 600 °C under certain ambient or complicated annealing process. But it is not directly relevant to the MOS interface needed for realizing inversion-channel E-mode GaAs MOSFET using implantation process.

The high-frequency (10 kHz) CV curves for a capacitor with a 30 nm ALD Al_2O_3 on InGaAs is shown in Fig. 2(a). This capacitor went through all device process and was an-
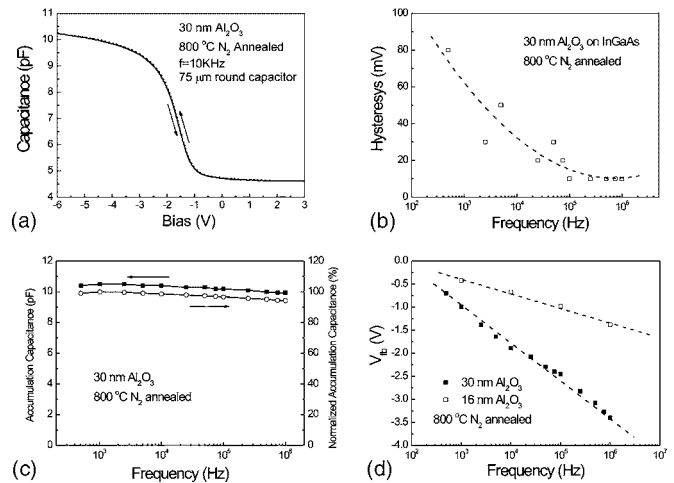

FIG. 2. (a) High-frequency (10 KHz) capacitance-voltage vs the ALD Al_2O_3/InGaAs MOS capacitor subjected to a RTA step of 800 °C for 10 s in nitrogen. The hysteresis is negligible. (b) Hysteresis in the CV loops measured at half value of accumulation capacitance vs the small signal frequency. The dashed line is a parabolic fitting. (c) The accumulation capacitances and the normalized ones vs the small signal frequency at a wide range on the similar device. (d) The flatband voltages vs the small signal frequency on the two representative devices with different oxide thicknesses of 16 and 30 nm. The theoretical V_{fb} is −0.95 V using 4.3 eV for the work function of Ti, 4.07 eV for the affinity of GaAs, and 1.18 eV for the band gap of $In_{0.2}Ga_{0.8}As$. The two dashed lines are guides for the eyes.

nealed with a RTA step of 800 °C for 10 s in nitrogen ambient. The solid curve is measured from −6 to +3 V with the sweep rate ~ 4 V/min, while the dashed line is taken from +3 to −6 V. There exhibits almost "zero" hysteresis in this CV loop with the maximum shift less than 20 mV. Figure 2(b) illustrates the hysteresis versus frequency observed on a typical MOS capacitor. It is in the range of 10–50 mV between 1 KHz and 1 MHz, and increases as the frequency goes down in general. The extremely low hysteresis, along with the sharp transition from depletion and accumulation, demonstrates the high quality of bulk and interface properties of ALD Al_2O_3 on InGaAs even after high temperature annealing. The effects of the annealing step on the chemical and structural properties of the interface are very complex and difficult to quantify in detail. The general observations of hysteresis on ALD Al_2O_3 on GaAs or InGaAs are the following (1) The unannealed device exhibits a hysteresis of ~ 200–500 mV depending on n-type or p-type surfaces,[18,19] surface pretreatment, ALD growth temperature, and others. Slow traps dominate on unannealed MOS structures. (2) The RTA step improves the interface characteristics and reduces both slow and fast traps significantly. The most efficient annealing temperature is between 450 and 600 °C, depending on different channel materials and ambient conditions. (3) The bulk and interface properties start to degrade after the RTA step with the annealing temperature higher than 800 °C due to the interdiffusion between Al_2O_3 and GaAs or InGaAs and As outgassing from GaAs. Al_2O_3 is a promising dielectric for E-mode GaAs MOSFET applications because it is chemically and thermodynamically stable at high temperature process as demonstrated in Figs. 1(b) and 2(a).

The frequency dispersion on accumulation capacitance C_{max} is another issue for high-k dielectrics on III-V materials.[16] This dispersion could be as large as 50% or more in the frequency range of 1 kHz–1 MHz, which stymies all efforts to estimate D_{it} using high-low frequency capacitance method. Figure 2(c) summarizes the accumulation capaci-
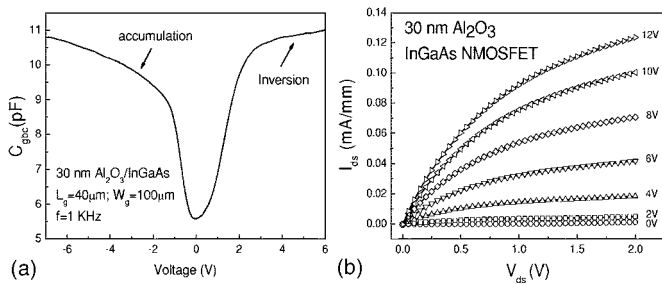
FIG. 3. (a) C_{gbc} by split-*CV* measurement on a MOSFET with a 40 μm gate length and 100 μm gate width at frequency as high as 1 kHz. (b) *I-V* characteristic of a 1 μm-gate-length inversion-channel enhancement-mode In-GaAs MOSFET with a 30 nm ALD Al_2O_3 as a gate dielectric.

tance C_{max} measured on 800 °C annealed capacitors in the wide frequency range from 500 Hz up to 1 MHz. The frequency dispersion is only 1% per decade at this frequency range. This experiment unambiguously demonstrates that the major part of frequency dispersion on nonideal oxide/III-V material interface does relate to the interface properties instead of simple parasitic effect, which can be corrected by two-frequency correction or multicircuit element models.[20,21] The dielectric constant is ~8.1 deduced from the measured C_{max}, the area of the capacitor and the film thickness.

The flatband shift is also an issue at the beginning for alternative dielectrics research on Si. Here we focus on the observed frequency dependent flatband shift of 800 °C annealed capacitors. Figure 2(d) plots the summary of V_{fb} versus frequency on 16 and 30 nm thick ALD Al_2O_3 films. The frequency dependent flatband shift is much less on medium temperature (450–600 °C) annealed capacitors. The phenomenon is less significant on 16 nm thick film compared to 30 nm thick one. It is roughly scaled with the film thickness and linearly dependent on $\log(f)$. The real origin for this frequency dependent flatband shift is unknown yet. The film thickness dependence of this flatband shift is under systematic investigation.

Clear *n*-channel inversion on *p*-type InGaAs is realized at Al_2O_3/InGaAs interface, which is demonstrated by measuring C_{gbc} (split-*CV* method) on InGaAs MOSFETs, as shown in Fig. 3(a). The *CV* curve is taken on a real MOS-FET with 40 μm gate length and 100 μm gate width at frequency as high as 1 kHz. At the conventional MOS configuration as measured in Fig. 2(a), no *n*-channel inversion is observed at frequency as low as 100 Hz. It is understood that the minority carriers (electrons) are provided by the source and drain diffusions and not by thermal generation in the depletion region. In the split-*CV* or MOSFET configuration with source and drain grounded at the same time, majority (holes) and minority (electrons) carrier capacitances can be measured independently at the same frequency. Using low-frequency capacitance C_{LF}=5.5 pF, high-frequency capacitance C_{HF}=5.0 pF, and oxide capacitance C_{ox}=11.0 pF, the middle gap interface trap density D_{it} is determined to be 2.9×10^{11}/cm^2 eV. Figure 3(b) illustrates the *IV* characteristics of a typical 1×100 μm^2 gate geometry enhancement-mode *n*-channel InGaAs MOSFET with ALD Al_2O_3 as a gate dielectric. The gate voltage is varied from 12 to 0 V in steps of −2 V and the threshold voltage V_T is ~0. The low drain current could be improved by optimizing implant and annealing conditions to reduce parasitic resistance and surface scattering. The maximum drain current on this device is only ~0.12 mA/mm so far, which is comparable to the

GaAs based E-mode MOSFET reported previously at $Ga_2O_3(Gd_2O_3)$/GaAs interface.[22] Combining the *CV* result in Fig. 3(a) and the *IV* result in Fig. 3(b), it clearly demonstrates that the true inversion *n*-channel can be formed at ALD Al_2O_3/InGaAs interface. More work is ongoing to further improve the interface quality, device structure, and fabrication process to truly realize a high-performance E-mode III-V MOSFET.

In summary, we have systematically studied *CV* characteristics on both ALD Al_2O_3/InGaAs MOS capacitors and E-mode MOSFETs, in particular, after high temperature RTA. The leakage current remains extremely low at the needed process temperatures. "Zero" hysteresis in *CV* loops and less than 1% per decade frequency dispersion at accumulation capacitance are demonstrated on the devices even after high temperature annealing. The true inversion *n*-channel is observed in the split-*CV* measurements. Meanwhile the functional E-mode *n*-channel InGaAs MOSFET is also demonstrated.

[1] T. Mimura and M. Fukuta, IEEE Trans. Electron Devices **ED-27**, 1147 (1980), and references therein.
[2] *Physics and Chemistry of III-V Compound Semiconductor Interfaces*, edited by C. W. Wilmsen (Plenum, New York, 1985), and references therein.
[3] B. J. Skromme, C. J. Sandroff, E. Yablonovitch, and T. Gmitter, Appl. Phys. Lett. **51**, 2022 (1987).
[4] G. G. Fountain, R. A. Rudder, S. V. Hattangady, R. J. Markunas, and J. A. Hutchby, Tech. Dig. - Int. Electron Devices Meet. **1989**, 887.
[5] M. Akazawa, H. Ishii, and H. Hasegawa, Jpn. J. Appl. Phys., Part 1 **30**, 3744 (1991).
[6] J. Reed, G. B. Gao, A. Bochkarev, and H. Morkoc, J. Appl. Phys. **75**, 1826 (1994).
[7] M. Passlack, M. Hong, and J. P. Mannaerts, Appl. Phys. Lett. **68**, 1099 (1996).
[8] B. Yang, P. D. Ye, J. Kwo, M. R. Frei, H.-J. L. Gossmann, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude, J. Cryst. Growth **251**, 837 (2003).
[9] P. D. Ye, G. D. Wilk, J. Kwo, B. Yang, H.-J. L. Gossmann, M. Frei, S. N. G. Chu, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude, IEEE Electron Device Lett. **24**, 209 (2003).
[10] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H.-J. L. Gossmann, S. N. G. Chu, S. Nakahara, H.-J. L. Gossmann, J. P. Mannaerts, M. Sergent, M. Hong, K. Ng, and J. Bude, Appl. Phys. Lett. **83**, 180 (2003).
[11] P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, H.-J. L. Gossmann, M. Hong, K. Ng, and J. Bude, Appl. Phys. Lett. **84**, 434 (2004).
[12] P. D. Ye, B. Yang, K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, Appl. Phys. Lett. **86**, 063501 (2005).
[13] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, IEEE Trans. Nanotechnol. **4**, 153 (2005).
[14] S. Datta, T. Ashley, J. Brask, L. Buckel, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, Tech. Dig. - Int. Electron Devices Meet. **2005**, 783.
[15] H. C. Lin, P. D. Ye, and G. D. Wilk, Appl. Phys. Lett. **87**, 182904 (2005).
[16] S. Koveshnikov, W. Tsai, I. Ok, J. C. Lee, V. Torkanov, M. Yakimov, and S. Oktyabrsky, Appl. Phys. Lett. **88**, 22106 (2006).
[17] C. O. Chui, H. Kim, P. C. McIntyre, and K. C. Sarawat, IEEE Electron Device Lett. **25**, 274 (2004).
[18] D. Yan, F. H. Pollak, T. P. Chin, and J. M. Woodall, Phys. Rev. B **52**, 4674 (1995).
[19] M. D. Pashley, K. W. Haberern, R. M. Feenstra, and P. D. Kirchner, Phys. Rev. B **48**, 4612 (1993).
[20] M. L. Huang, Y. C. Chang, C. H. Chang, Y. J. Lee, P. Chang, J. Kwo, T. B. Wu, and M. Hong, Appl. Phys. Lett. **87**, 252104 (2005).
[21] Z. Luo and T. P. Ma, IEEE Electron Device Lett. **25**, 655 (2004).
[22] F. Ren, M. Hong, W. S. Hobson, J. M. Kuo, J. R. Lothian, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, Solid-State Electron. **41**, 1751 (1997).