[17] H. Kriplani, F. N. Najm, and I. N. Hajj, "Pattern independent maximum current estimation in power and ground buses of CMOS VLSI circuits: Algorithms, signal correlations, and their resolution," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 14, no. 8, pp. 998–1012, Aug. 1995.
[18] M. Nemani and F. N. Najm, "High-level power estimation for VLSI circuits," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 18, no. 6, pp. 290–298, Jun. 1999.
[19] ——, "Toward a high-level power estimation capability," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 15, no. 6, pp. 588–598, Jun. 1996.
[20] K. M. Buyuksahin and F. N. Najm, "High-level power estimation with interconnect effects," in *Proc. Int. Symp. Low-Power Electron. Design*, 2000, pp. 271–274.
[21] F. N. Najm, R. Burch, P. Yang, and I. N. Hajj, "Probabilistic simulation for reliability analysis of CMOS VLSI circuits," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 9, no. 4, pp. 439–450, Apr. 1990.
[22] F. N. Najm, "Transition density: a new measure of activity in digital circuits," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 12, no. 2, pp. 310–323, Feb. 1993.
[23] S. Ramprasad, N. R. Shanbhag, and I. N. Hajj, "Analytical estimation of signal transition activity from word-level statistics," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 16, no. 7, pp. 718–733, Jul. 1997.
[24] J. H. Satyanarayana and K. K. Parhi, "Theoretical analysis of word-level switching activity in the presence of glitching and correlation," *IEEE Trans. VLSI Syst.*, vol. 8, no. 2, Apr. 2000.
[25] V. K. Rohatgi, *An Introduction to Probability and Statistics*. New York: Wiley, 2001.
[26] S. Gupta and S. Katkoori, "Intra-bus crosstalk estimation using word-level statistics," in *Proc. 17th Int. Conf. VLSI Design*, 2004, pp. 449–454.
[27] ——, "A fast word-level statistical estimation technique for intra-bus crosstalk," in *Design Automation Test Eur.*, 2004, pp. 1110–1115.

Capacitive Coupling Noise in High-Speed VLSI Circuits

Payam Heydari and Massoud Pedram

***Abstract*—Rapid technology scaling along with the continuous increase in the operation frequency cause the crosstalk noise to become a major source of performance degradation in high-speed integrated circuits. This paper presents an efficient metric to estimate the capacitive crosstalk in nanometer high-speed very large scale integration circuits. In particular, we provide closed-form expressions for the peak amplitude, the pulsewidth, and the time-domain waveform of the crosstalk noise. Experimental results show that the maximum error of our noise predictions is less than 13%, while the average error is only 5.82%.**

***Index Terms*—Capacitance, CMOS circuits, crosstalk, deep submicron, interconnect, noise, very large scale integration (VLSI).**

I. Introduction

Shrinkage of the minimum feature size of the semiconductor devices to 130 nm and below and increase in the clock frequency to 3 GHz and above have caused crosstalk noise to become a serious problem in integrated circuits. More precisely, crosstalk noise has evolved as the key source of performance degradation and signal integrity problems in high-speed very large scale integration (VLSI) designs.

Various techniques have been proposed to evaluate the crosstalk noise in integrated circuits. The most accurate approach is to use a transistor-level circuit simulator. This approach is, however, computationally inefficient, and hence, is not applicable to large circuit structures. For example, our experiments show that simulating a small circuit structure consisting of a collection of ten coupled lossy transmission lines with HSPICE takes almost 3 min on a 1.5-GHz Intel Pentium IV-based computer system. Since interconnects are modeled as linear time-invariant systems, model reduction techniques [1]–[6] can be utilized to reduce the computational complexity. These model order-reduction techniques may be incorporated into the noise analysis and calculation programs to accurately determine the noise behavior of the circuit under study. For example, [7] enumerates different types of environmental noise sources that have a major impact on digital VLSI circuit performance. Next, it proposes a fast methodology using noise graphs to analyze the noise. The main shortcoming of this work is that it does not accurately model the on-chip interconnects. Reference [8] incorporates a model order-reduction technique to efficiently simulate the on-chip interconnects as distributed *RC* sections. However, it does not present any analytical expression for the crosstalk noise. Moreover, in spite of employing model reduction techniques, this approach cannot completely solve the problem of long computation times associated with this kind of noise analysis. In addition, neither [7] nor [8] provide any insight into the circuit designers as to how to modify the circuit structures in order to reduce or control the crosstalk noise.

It is desirable to use closed-form expressions, instead of simulation tools, to predict the noise effects in a circuit as long as their prediction accuracy is acceptable. This is especially true during the early stages of the design process when one does not afford simulating a large number of possible circuit structures and layout solutions. Consequently, a number of researchers have addressed the problem of obtaining simple, closed-form expressions for crosstalk noise in VLSI circuits. Vittal *et al.* in [9] provide bounds for the crosstalk noise using a lumped *RC* model. This work, however, ignores the interconnect resistance. Later, the same authors, in [10], make use of geometric considerations to obtain expressions for the peak amplitude and the pulsewidth of the noise. Knowing the noise pulsewidth is important because, in general, the noise margin of a gate depends on both the noise peak amplitude and the noise pulsewidth. Their technique can handle arbitrary input signals. In [11], Devgan proposes a clever technique for finding an upper bound on the crosstalk noise. The author himself mentions that his model exhibits a large error when the signals are fast and the rise and fall times are short. Unfortunately, this latter scenario occurs frequently when practical values of the interconnect parasitics and signal frequencies are used. We have observed that the percentage of the estimated error in such cases can be as much as 60%. In addition, [11] does not predict the noise pulsewidth.

Kuhlmann *et al.* in [12] and [14] propose an exact crosstalk noise-estimation method for a distributed *RC*(L) model of the VLSI interconnect. They employ a moment-matching technique and Devgan's metric to effectively reduce the Laplace transform of the coupled interconnect to a low-order rational function. More specifically, for a distributed *RC* interconnect, a high-order transfer function is first reduced to a third-order rational transfer function by using a combination of moment-matching technique and Devgan's metric. The poles of the reduced-order transfer function are then derived to examine the stability of the reduced system. If the reduced system

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is unstable, a second-order transfer function will be used instead. Authors demonstrate the accuracy of their proposed method by comparing its performance with that of HSPICE. The metric proposed in [12] and [14] is less intuitive in terms of the circuit interpretation, and requires two tree traversals (one for the aggressor net and the other one for the victim net), a diagonal matrix–vector multiplication for the dc component of the Taylor series expansion of the victim voltage in the Laplace-domain, two additional tree traversals per moment, and two diagonal matrix-vector multiplication for high moments of the victim and the aggressor voltages. The tree traversal and the multiplication are of the order of $O(n)$ for n nodes. In addition, for every run of the circuit simulator on the system, roots of the reduced third-order model should be obtained for the stability check. This operation is also of the order of $\mathrm{O}(n)$. The number of tree traversals and matrix multiplications to generate the third-order model are six and 20 times more than those in the Devgan's metric, respectively [14]. The authors in [13] proposed a conventional lumped 2-p *RC* circuit for the victim net, while postulating that the slew rate at the coupling location is obtained by simple slew-rate calculation from the aggressor driver, which is not accurately correct for long parallel wires. The reason is that the slew-rate calculation for the aggressor net must account for the distributed nature of the coupling between the adjacent lines. Although a lumped 2-π model can help us derive closed-form analytical models for the noise attributes, the results lead to large and unacceptable errors for long aggressor and victim nets. Using this model, the authors calculated the noise peak and pulsewidth, and defined the amplitude pulsewidth product. Several experiments in this paper have shown that the noise peak amplitude will have a more contribution to the circuit failure than the noise pulsewidth. Therefore, a new definition is needed to emphasize the bigger impact of the noise peak amplitude. Takahashi *et al.* in [15] proposes a 2-π equivalent circuit to estimate crosstalk noise of partially coupled *RC* trees. This paper assumes the aggressor waveform to be an exponential function, which then yields a more accurate estimate than that case that either a step input or a saturated ramp input are assumed. Unfortunately, the proposed analytical model for the interconnect is a 2-π *RC* network, which cannot capture the distributed nature of a long *RC* interconnect. This is the major shortcoming of the work by Takahashi *et al.* Ding et al. [16] have proposed a fast aggressor and tree reductions to estimate the crosstalk. Similar to [13] and [15], [16] employs double-pole approach for the crosstalk noise estimation.

In this paper, a new crosstalk noise metric is proposed, which is capable of predicting the noise amplitude and the noise pulsewidth of an *RC* interconnect as well as an overdamped resistance–inductance–capacitance (*RLC*) interconnect very efficiently. This paper is based on the work originally proposed in [17]. Several experiments reveal that the proposed metric, on average, predicts the peak crosstalk noise with the same or higher level of accuracy compared to the second-order reduced model proposed in [14]. Unlike [14], the proposed noise metric gives a rather simple analytical model of the crosstalk noise, which is efficient and sufficiently accurate to be effectively incorporated in state-of-the-art noise calculators. The proposed noise metric has a closed-form expression that clearly highlights the dependency of the noise on the aggressor and victim line circuit parameters as well as on the input signal rise/fall times.

This paper is organized as follows. In Section II, the interconnect coupling phenomenon is reviewed and, through experimental results, it is shown that the inductive coupling on chip is negligible for local wiring clocked at a target frequency of 1 GHz. This result justifies the focus of this paper, which is on the capacitive crosstalk effect. After a brief description of Devgan's metric in Section II-A, we introduce our new noise metric in Section II-B. We next compare our metric with the analytical models proposed by Vittal [10], Devgan [11], and Kuhlmann [12], [14] through a series of detailed simulation experiments. Finally, Section III provides the conclusion of this paper.

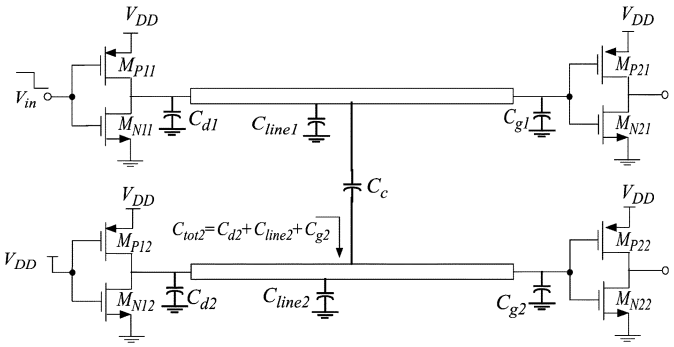

Fig. 1. Simplified circuit model of two capacitively coupled transmission lines.

II. Capacitive Coupling

The electromagnetic coupling of a signal from one conductor to another, which is called *crosstalk*, can be induced through two coupling mechanisms: capacitive and inductive.

All signal conductors exhibit some interwire capacitances among themselves. When the conductors are placed sufficiently close to each other, the capacitance becomes large enough to couple significant energy from one conductor, called an *aggressor* or *active* line, to another conductor, called a *victim* or *passive* line. Because, with each new process technology, the thickness (height) of the wires is not scaled down as aggressively as the width of the wires, and because the wires are packed increasingly closer to each other, the ratio of the coupling capacitance to the total capacitance (includes area and fringe capacitances) increases, and therefore, the capacitive coupling noise increases. Fig. 1 depicts a highly simplified analysis (neglecting the resistive loss and the magnetic coupling of the interconnect lines) of the essential attributes of the crosstalk noise. In this figure, coupled noise on line 2 results from a transition on line 1. In this simplified circuit model, the crosstalk voltage is obtained from a capacitive voltage division relationship as follows:

$$V_{x\,\mathrm{talk}}(t) = \left(\frac{C_c}{C_c + C_{\mathrm{tot}\,2}}\right) V_{\mathrm{DD}} e^{-t/\tau} u(t)$$

where $\tau = r_{\mathrm{DS},12}(C_c + C_{\mathrm{tot}\,2})$

where $u(t)$ represents the unit-step function, and $r_{\mathrm{DS},12}$ is the on resistance of the NMOS device of the victim line driver.

High-speed digital circuits often employ dynamic logic families (e.g., domino or true single-phase clocking) due to their higher switching speeds compared to the static logic family. Dynamic circuits are, however, more susceptible to crosstalk noise compared to the static logic because during some phase of the clock, the logic value is only stored on a floating capacitor. An induced noise that changes the logic value on this floating capacitor can cause the circuit to produce an incorrect result. Furthermore, as the circuit speed increases and the signal transient times decrease, the effects of on-chip crosstalk noise becomes more pronounced. Fig. 2 shows N neighboring wires. High-frequency operation of VLSI circuits causes on-chip wires to exhibit transmission line effects and, hence, electrical and magnetic couplings start to take place between pairs of wires. These electric and magnetic couplings reshape the signal waveforms and may induce delay in the signals traveling through the lines, thus causing the circuit to possibly violate its timing constraints.

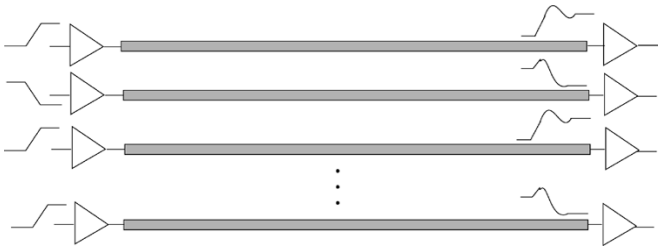

Fig. 2. Circuit schematic of N on-chip interconnects.

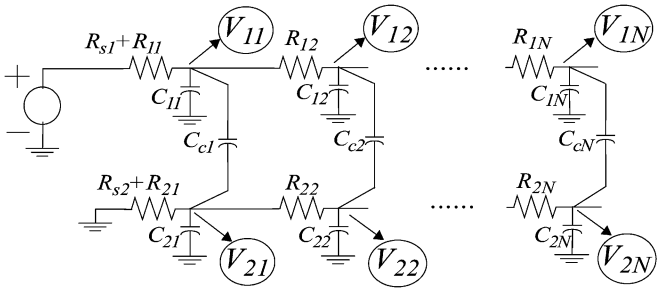

Fig. 3. Circuit schematic of capacitively coupled aggressor and victim nets.

Our goal is to develop a circuit model for the capacitive coupling between on-chip coupled interconnects and then use this model to derive a closed-form expression for the crosstalk noise. We start our analysis by reviewing Devgan's metric and its drawbacks in estimating the crosstalk noise in *RC* circuits. For a more comprehensive explanation of this metric, please refer to [11].

A. Devgan's Metric for Crosstalk Noise Estimation

Consider two capacitively coupled *RC* networks as shown in Fig. 3.

The *RC* ladder network representing the aggressor net is driven by a flattened ramp voltage, whereas the *RC* ladder network representing the victim net is quiet. For this circuit, the node voltage vector at the victim net, $\mathbf{V}_2 \in \Re^{N\times 1}$, is related to the voltage vector at the aggressor net $\mathbf{V}_2 \in \Re^{N\times 1}$ through the following:

$$[(s\mathbf{C}_2 - \mathbf{A}_{22}) - s\mathbf{C}_c(s\mathbf{C}_1 - \mathbf{A}_{11})^{-1}s\mathbf{C}_c]\mathbf{V}_2 = -s\mathbf{C}_c(s\mathbf{C}_1 - \mathbf{A}_{11})^{-1}\mathbf{B}_1\mathbf{V}_s \quad (1)$$

where $\mathbf{C}_i = \mathrm{diag}(C_{ij} + C_{cj})$ for $i = 1, 2$ and $j = 1, 2, \ldots, N$ and $\mathbf{C}_c = \mathrm{diag}(-C_{cj})$ for $j = 1, 2, \ldots, N$. $\mathbf{A}_{11}$ and $\mathbf{A}_{22}$ represent the equivalent node-resistance matrices of the aggressor net and the victim net, respectively. The steady-state values of node voltages at the victim net is calculated as

$$\mathbf{V}_{2,ss} = -\mathbf{A}_{22}^{-1}\mathbf{C}_c\mathbf{A}_{11}^{-1}\mathbf{B}_1\frac{V_{\mathrm{DD}}}{t_r} \quad (2)$$

where t_r is the rise-time of the input signal of the aggressor line driver. For simplicity, it is assumed that the rise and fall times are equal. Note that this result is valid only if the driving voltages of the interconnects are infinite ramps. This is a critical assumption that seriously and adversely affects the accuracy of capacitive crosstalk estimation. In practice, the actual driving voltages of the interconnects are saturated ramp inputs rather than infinite ramps. This means that the node voltages at the victim net reach their peak value approximately at $t = t_r$. This peak value is obviously different from the steady-state value under the infinite ramp input, and the error between these two values can be quite large if the rise-time of the input is fast.

To better understand the shortcoming of this approach, consider two second-order *RC* circuits with two floating capacitances connecting the corresponding nodes of these two circuits as depicted in Fig. 4. R_{s1} and R_{s2} represent the resistances of the input source. In reality, they represent the on-resistances of line drivers. The output impedance of line drivers can be modeled as another *RC* section that is connected to the distributed *RC* interconnect. Consider typical values of these parasitics, i.e., assume that $C_1 = 60$ fF, $C_2 = 120$ fF, $R_2 = 50\ \Omega$, $R_1 = 20\ \Omega$, $C_c = 180$ fF, $R_{s1} = 100\ \Omega$, $R_{s2} = 150\ \Omega$, and $t_r = 0.1$ ns.

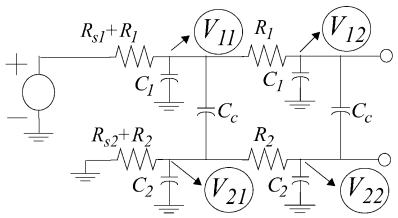

Fig. 4. Pair of capacitively coupled second-order *RC* circuits.

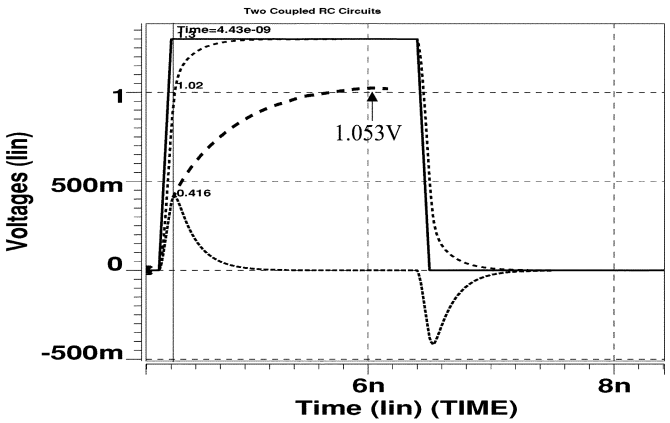

Fig. 5. Output voltage and the crosstalk of two coupled second-order *RC* circuits. $C_1 = 60$ fF, $C_2 = 120$ fF, $R_2 = 50\ \Omega$, $R_1 = 20\ \Omega$, $C_c = 180$ fF, $R_{s1} = 100\ \Omega$, $R_{s2} = 150\ \Omega$, and $t_r = 0.1$ ns.

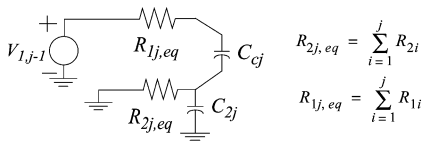

Fig. 6. Equivalent circuit for computing the time constant of the jth node of the victim net.

From HSPICE simulation, the reported peak value of voltage V_{22} at the far-end of the victim line is 0.416 V. Devgan's metric for the two coupled *RC* sections yields the following:

$$V_{21,ss} = 2\,(R_2 + R_{s_2})\,C_c\frac{V_{\mathrm{DD}}}{t_r} \quad (3)$$

$$V_{22,ss} = (3R_2 + 2R_{s_2})\,C_c\frac{V_{\mathrm{DD}}}{t_r}. \quad (4)$$

Using (4), $V_{22,ss}$ is 1.053 V. The estimated error is 153% verifying a well-known observation established by earlier published works that this metric can be inaccurate for deep sub-micron technologies [14].

Because the input signal rise-time is small, the crosstalk waveform rolls down quickly, and consequently, the error becomes unacceptably large (cf. Fig. 5). Notice that for cases where the input signal risetime is large compared to the interconnect delays, Devgan's metric accurately predicts the peak value. Unfortunately, cases in which the estimations are accurate (i.e., the slow slew rates for the pulses), are not the most important ones from a circuit performance viewpoint. The reason is that the peak value of the crosstalk is inversely proportional to the input risetime. For slow slew waveforms, the crosstalk also has a small peak value, and therefore, it has little impact on the circuit delay and the timing failure rate.

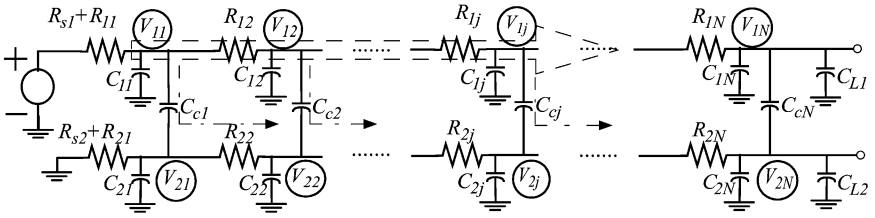

Fig. 7. *RC* signal paths through the aggressor line and floating capacitances.

In the next section, we derive a new, more accurate noise metric, and compare our results with Devgan's results and with HSPICE simulations.

B. New Metric for Crosstalk Noise Estimation

Close examination of the HSPICE results shown in Fig. 5 reveals a major source of inaccuracy in Devgan's metric. The large error in this example comes from the fact that the time constants of the exponentially rising portions of the victim node voltages, V_{2j} for $j = 1, 2, \ldots, N$, in the circuit of Fig. 5 are comparable to (or larger than) the input rise time. The actual peak value of the crosstalk occurs approximately at $t = t_r$ (or t_f, the fall-time, whatever the case may be). In fact, other works (e.g., [13]) proved theoretically that the peak noise is at t_r, under one-pole or two-pole approximation. For a flattened ramp input, it is easily seen that $t_{r(f)}$ sets a lower bound on the time instance at which the peak value of the crosstalk occurs. This is because, for an infinite ramp input, the voltage waveforms at the victim line nodes monotonically increase toward their steady state values as predicted by [11]. As the current drive capability of the line drivers decreases or as the driver sizes of the aggressor and victim lines become very different from one another, the peak value of the crosstalk may occur further away from $t = t_{r(f)}$. In contrast, as will be demonstrated through a number of circuit simulations later in this section, our proposed metric produces an accurate noise peak value and noise pulsewidth for all possible scenarios with regard to the victim and aggressor line drivers.

To compute the noise peak value, we observe that the capacitive crosstalk noise at every node of the victim net is a rising exponential function during the time interval that the input signal of the aggressor line driver is rising. The actual peak value of the crosstalk noise at each node of the victim net is in fact the value of the corresponding rising exponential function at $t = t_{r(f)}$. Recall that the steady-state value of this exponential function is determined by Devgan's metric.

$$\mathbf{V}_{2,\max} = \mathbf{V}_{2,ss}\left(\mathbf{I} - \mathbf{exp}\left(\mathbf{diag}\left(-\frac{t_{r(f)}}{\tau_{d_j}}\right)\right)\right), \quad \text{for} \quad j = 1, 2, \ldots, N \tag{5}$$

where $\mathbf{diag}(\mathbf{x})$ represents a diagonal matrix with all diagonal entries set to $\mathbf{x}$. τ_{d_j} is the time constant of the jth node voltage in the victim net, and $V_{2,ss}$ is the vector of steady state values of the crosstalk noise voltages at the victim nodes as calculated by Devgan's metric. Each node in the victim net sees two capacitances: a grounded area capacitance, C_{2j}, and a floating coupling capacitance, C_{cj}. The time constant at each victim node is thus equal to the summation of individual time constants due to each of these two capacitances. Similar to the open-circuit time-constant method that is employed for estimating the bandwidth of high-frequency amplifiers [18], the time-constant due to each capacitance is obtained by calculating the equivalent resistance seen across each capacitance with all the other capacitances open-circuited. Therefore, to accurately estimate the time constants due to capacitances C_{2j} and C_{cj}, we first construct an equivalent circuit consisting of C_{2j}, C_{cj}, and the equivalent resistances seen across these two capacitances and replace all of the other capacitances with open circuit connections. This circuit model is shown in Fig. 6.

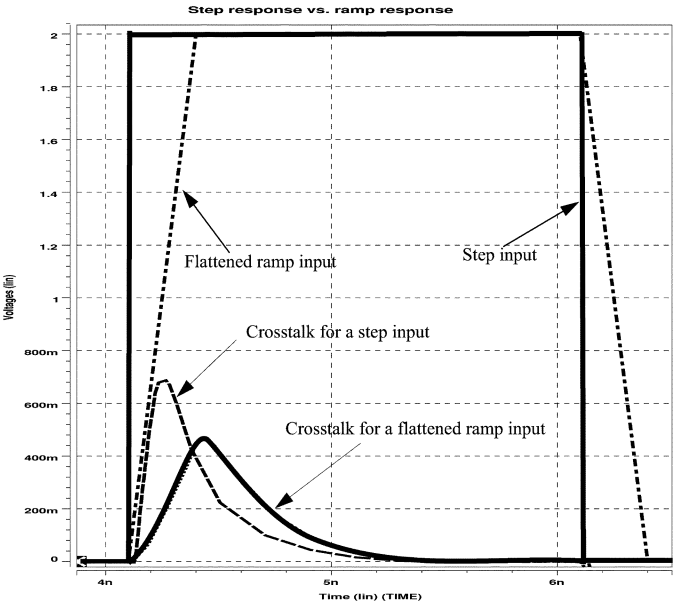

Fig. 8. Effects of zero initial slope and *RC* delay on the crosstalk.

The characteristic polynomial of this second-order transfer function is

$$\Lambda_j(s) = R_{1j,\mathrm{eq}}R_{2j,\mathrm{eq}}C_{2j}C_{cj}s^2 + \overbrace{[(R_{1j,\mathrm{eq}} + R_{2j,\mathrm{eq}})C_{cj} + R_{2j,\mathrm{eq}}C_{2j}]s + 1}^{\tau_{v_j}} \tag{6}$$

The time constant of this second-order circuit, which is roughly the inverse of the 3-dB bandwidth of its system transfer function, is equal to the coefficient of the first-order term, denoted by τ_{v_j}. In fact, τ_{d_j} must contain this coefficient as a part of its expression. Notice that the input voltage source must be a unit-step function for τ_{v_j} to properly represent the time constant at the jth node of the victim net. This is obviously not the case for the distributed coupled *RC* circuits. The input voltage to the jth node of the aggressor experiences an *RC* delay due to the *RC* path from the input to the jth node of the aggressor as is shown in Fig. 7. The *RC* delay cannot be computed using the Elmore delay formula because there is a signal path from the input node to each victim node V_{2j} through the floating capacitance C_{cj} that connects this victim node to the corresponding aggressor node V_{1j}. This *RC* delay also ought to be accounted for in the delay calculation of Fig. 7. The overall *RC* delay is thus computed differently from the Elmore delay.

Furthermore, for *RC* circuits with orders greater than one, the initial slopes of the step and ramp responses are zero. This zero initial slope leads to an increase in the circuit delay. Fig. 8 indicates all these delay effects on the crosstalk noise waveform for a flattened ramp input as well as a step input.

TABLE I
RESULTS OF SIMULATIONS ON THE TWO CAPACITIVELY COUPLED TRANSMISSION LINES USING STAR-HSPICE, COMPARING METHODS OF [10], [13], [14], AND OUR PROPOSED METRIC USING A 130-nm TECHNOLOGY AND $V_{\rm DD} = 1.3$ V. THE AGGRESSOR LINE INPUT IS A FLATTENED RAMP SIGNAL

c_1 (pF/m)	r_1 (kΩ/m)	r_2 (kΩ/m)	c_2 (pF/m)	c_c (pF/m)	R_{s1}	R_{s2}	C_{out1} (pF)	C_{out2} (pF)	t_r nsec	L (mm)	HSPICE volts	Pan volts	Vittal volts	Kuhlmann volts	Ours volts
60	11.47	10.2	64	100	1k	2k	0.09	0.08	0.05	0.2	0.113	0.137	0.1396	0.119	0.1271
72	9.55	9.55	72	150	527	527	0.2	0.1	0.04	0.7	0.168	0.201	0.2111	0.192	0.181
83	8.2	7.0	90	160	1013	920	0.3	0.1	0.03	0.8	0.143	0.165	0.1937	0.152	0.16
92	9.3	10	80	170	270	400	0.06	0.2	0.06	2.5	0.331	0.383	0.401	0.352	0.361
101	12	12	101	150	140	150	0.1	0.2	0.08	1.2	0.189	0.221	0.2096	0.202	0.1901
120	10	10	120	132	2k	4k	0.06	0.07	0.1	1.1	0.255	0.286	0.3573	0.268	0.285
108	15	15	108	200	20	30	0.2	0.1	0.15	1.3	0.0901	0.0972	0.1234	0.0905	0.089
130	13	20	100	220	670	720	0.3	0.05	0.09	1.6	0.26	0.278	0.324	0.2782	0.267
140	17	17	100	200	350	350	0.3	0.2	0.12	2	0.222	0.261	0.271	0.239	0.221
140	17	17	100	200	20	30	0.07	0.08	0.06	2	0.25	0.263	0.26	0.273	0.25
90	11	11	90	120	160	160	0.3	0.2	0.08	4	0.219	0.254	0.266	0.238	0.232
85	12	8.5	75	140	190	100	0.8	0.2	0.1	5	0.144	0.156	0.1847	0.157	0.153
65	13	7	120	170	600	80	0.08	0.5	0.05	6	0.075	0.089	0.1	0.078	0.082
110	6.5	7	90	180	80	75	0.6	0.7	0.08	7	0.238	0.261	0.305	0.264	0.259
100	8	14	40	110	200	1k	0.8	0.05	0.06	8	0.465	0.512	0.6365	0.489	0.513
92	13	7	170	260	1.5k	50	0.08	0.3	0.08	0.8	0.0218	0.0231	0.0232	0.0224	0.0229
110	8	4	200	300	1.2k	25	0.1	0.65	0.1	3	0.0185	0.0207	0.0212	0.02	0.0192
70	10	1.82	20	95	20	3k	0.2	0.07	0.2	1.1	0.573	0.584	0.584	0.597	0.596
100	7	16	14	100	37	5k	0.8	0.1	0.1	2	0.647	0.689	0.7274	0.688	0.693
97	9	15	30	120	26	2k	0.3	0.06	0.07	1.2	0.675	0.712	0.7062	0.724	0.6862

Consequently, the time constant of the jth node in the victim net consists of two additive terms τ_{v_j} and τ_{a_j}, with τ_{v_j} [given by (6)] represents the time constant of the jth node in the victim net under a unit-step input excitation, and τ_{a_j} represents the propagation delay of the signal coming from other paths established by the floating capacitances $C_{ck}(k = 1, \ldots, j-1)$ as illustrated above. According to Fig. 7, τ_{a_j} includes the signal delays of all additional signal paths through the coupling capacitances $C_{ck}(k = 1, \ldots, j-1)$ toward the jth node in the victim net. The overall delay from the aggressor input source to the jth node in the victim net is

$$\tau_{d_j} = \zeta \cdot \left[(R_{1j,\rm eq} + R_{2j,\rm eq})C_{cj} + R_{2j,\rm eq}C_{2j} + \tau_{a_j}\right], \quad \text{for } j = 1, 2, \ldots, N \tag{7}$$

where τ_{a_j} is

$$\tau_{a_j} = R_{1j,\rm eq}(C_{cj} + C_{1j}) + \sum_{k=1}^{j-1}[R_{1k,\rm eq}(C_{ck} + C_{1k}) + R_{2k,\rm eq}(C_{2k} + C_{ck})], \quad \text{for } j = 1, 2, \ldots, N \tag{8}$$

and ζ is a constant factor for the delay increase due to the nonzero, yet finite, input slope. Its value is in the range [1.00, 1.02]. Throughout our analysis, we use $\zeta = 1.01$. Combining (7) and (8) yields the following expression for τ_{d_j}:

$$\tau_{d_j} = \zeta \cdot \left[R_{1j,\rm eq}C_{cj} + \sum_{k=1}^{j}[R_{1k,\rm eq}(C_{ck} + C_{1k}) + R_{2k,\rm eq}(C_{2k} + C_{ck})]\right], \quad \text{for } j = 1, 2, \ldots, N. \tag{9}$$

The peak amplitude of the crosstalk is easily obtained from (5) with the expression for τ_{d_j} given by (9).

As a special case, we first concentrate on the circuit of Fig. 4 in which two second-order *RC* circuits are capacitively coupled. The peak voltage value of the node V_{22} is calculated using three different approaches: 1) HSPICE simulation; 2) Devgan's metric; and 3) our proposed analytical model. Applying (5) and (9) to the circuit of Fig. 4 yields the following closed-form expressions for the peak values of the nodes, V_{21} and V_{22}:

$$V_{21,\max} = V_{21,ss}\left(1 - \exp\left(-\frac{t_r}{\tau_{d_1}}\right)\right) \tag{10}$$

where $\tau_{d_1} = 1.01[(R_1 + R_{s1})(2C_c + C_1) + (R_2 + R_{s2})(C_c + C_2)]$

$$V_{22,\max} = V_{21,ss}\left(1 - \exp\left(-\frac{t_r}{\tau_{d_2}}\right)\right) \tag{11}$$

where $\tau_{d_2} = 1.01[(3R_1 + 2R_{s1})(C_c + C_1) + (3R_2 + 2R_{s2})(C_2 + C_c) + (2R_1 + R_{s1})C_c]$.

To verify the accuracy of our approach on multistage *RC* networks in comparison to other expressions proposed in [10], [13], and [14], we perform a number of experiments on a two-line structure in a 130-nm CMOS technology. In state-of-the-art CMOS technologies the coupling capacitance accounts for approximately 70%–95% of the total node capacitances, which makes the coupling noise analysis even more important. In our implementation of the algorithm presented in [14], the second-order reduced transfer function is utilized in order to avoid a potential stability problem. The coupled lengths of the adjacent interconnects are varied from 200 μm to 8 mm. The supply voltage is $V_{\rm DD} = 1.3$ V. Results are reported for a range of risetimes varying between 30 and 200 ps, and for different victim and aggressor driver resistances varying between 20 Ω and 5 kΩ. Table I contains the result of these comparisons. Of particular interest is the situation where the driver strengths of the aggressor and victim lines are vastly different. For instance, this circuit configuration is encountered when a global signal line is in the close vicinity of a local signal line. The last five experiments in Table I are devoted to this particular configuration. The mean and maximum error values are reported in Table II. These tables testify to the higher accuracy of our approach compared to these

TABLE II
PERCENTAGE ERROR COMPARISON FOR METHODS OF [10], [13], [14] AND OUR PROPOSED METRIC

	%Error Pan's	%Error Vittal's	%Error Kuhlmann	%Error Ours
	21.2	23.54	5.31	12.48
	19.64	35.45	14.29	7.74
	15.4	26.6	6.29	11.89
	15.7	21.15	6.34	9
	16.9	10.9	6.88	0.5
	12.16	40.12	5.1	11.76
	7.88	36.9	0.4	1.2
	6.9	24.62	8.46	2.69
	17.6	22.07	7.66	0.4
	5.2	4.0	9.2	0
	15.98	21.46	8.68	5.94
	8.33	28.26	9.03	6.25
	18.67	33.3	4	9.33
	9.66	28.15	10.92	8.82
	10.1	36.88	5.16	10.32
	5.96	6.4	2.75	0.4
	11.89	14.6	8.11	3.78
	1.92	1.92	4.2	4.1
	7.73	12.43	6.34	7.11
	5.48	4.62	7.26	2.67
Average	11.72	21.67	6.81	5.82
Maximum percentage error	19.64	40.12	14.29	12.48

TABLE III
RUNTIME COMPARISON BETWEEN THE PROPOSED NOISE METRIC AND [14] USING A 130-nm TECHNOLOGY AND $V_{\rm DD} = 1.3$ V

Wire-length (mm)	Run-Time (sec)	
	Kuhlmann [14]	The proposed metric
4	3	1
5	3	1
6	4	2
7	4	2
8	5	3

other approaches. More precisely, our proposed analytical model results in an average estimation error of only 5.82%, which is better than the 6.81% average estimation error resulting from the method of [14]m when a second-order reduced transfer function is employed. Interestingly, the proposed noise metric exhibits a better accuracy compared to [14], when the driver sizes of aggressor and victim lines are hugely different (i.e., the last five rows of Tables I and II). We expect that the method proposed in [14] gives rise to a higher accuracy once the third-order reduced transfer function is used. However, this increased accuracy comes at the expense of higher computational complexity due to the stability evaluation of the reduced system. Notice that the metric proposed in [12] and [14] involves multiple tree-traversals, diagonal matrix-vector multiplications, each of which is of order $\mathrm{O}(n)$, where n is the number of segment points, in order to compute each moment of each victim net node. From these moments, the noise waveforms at all victim nodes are subsequently calculated by solving a linear system of equations. In contrast, our metric presents closed-form expressions for noise waveforms at all victim nodes (including the far-end termination) with a computational complexity of $\mathrm{O}(n)$. The approach proposed in [13] gives rise to a slightly better accuracy for short aggressor nets, as also demonstrated in Table I.

The runtimes of the proposed noise metric with that of [14] is compared in Table III. In Table III, the peak value of the far-end crosstalk in a pair of geometrically identical aggressor and victim lines in a 130-nm technology is obtained using both the proposed metric and [14]. The line length varies from 4 to 8 mm, and the supply voltage is 1.3 V. To accurately model the interconnect, every 2 μm of each line segment is modeled with an *RC* ladder network.

Fig. 9(a)-(c) shows the crosstalk voltage waveforms obtained by using HSPICE simulation for the last three experiments in Table I, where the aggressor and victim driver sizes are very different. As mentioned earlier in this section, it is assumed that the peak value of the crosstalk occurs approximately at $t = t_{r(f)}$. As the current drive capability of the line drivers decreases, the peak value of the crosstalk may occur further way from $t = t_{r(f)}$. As an example, Fig. 10 shows the HSPICE simulation result for the far-end crosstalk

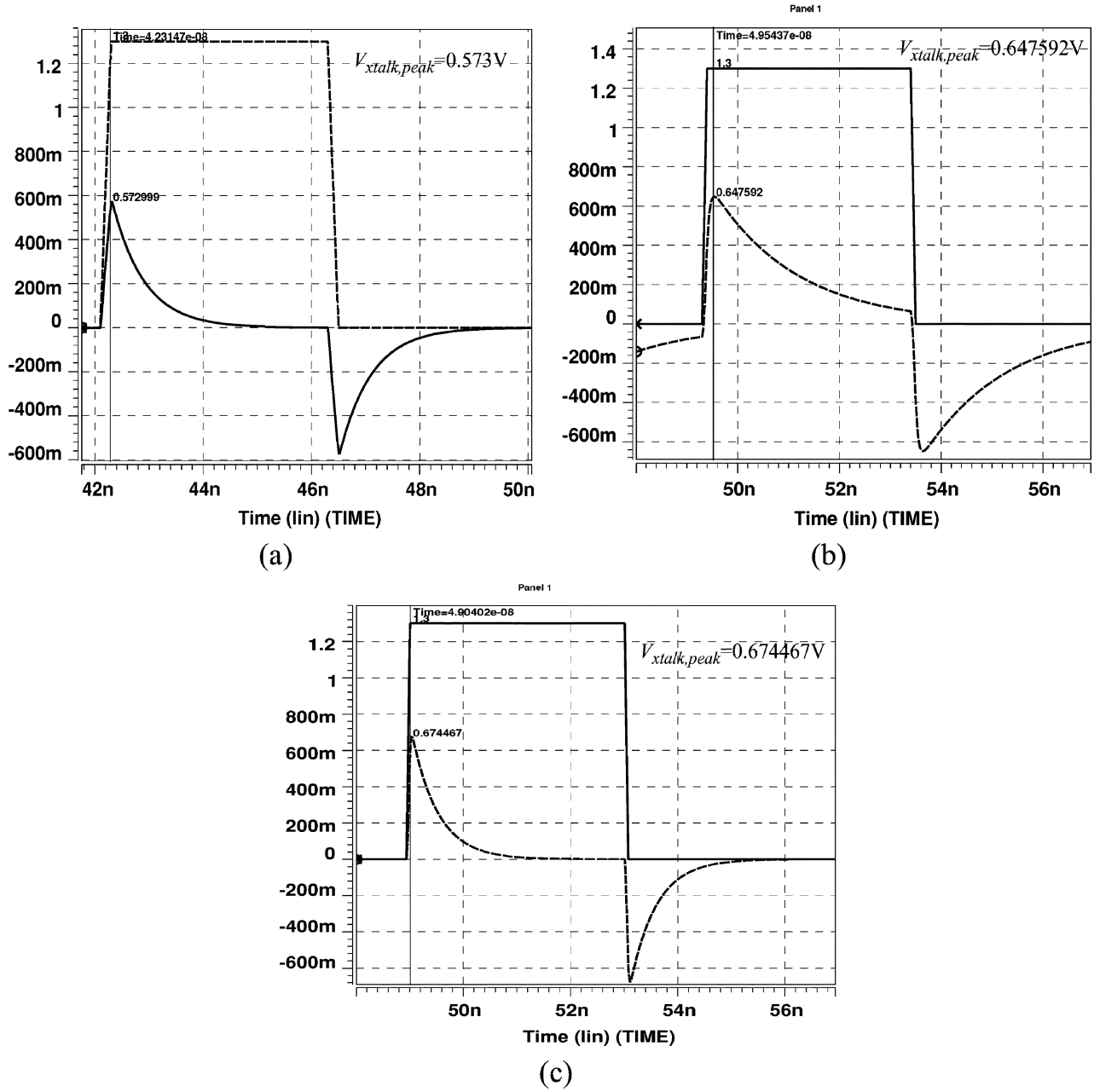

Fig. 9. Crosstalk waveforms obtained using HSPICE simulations for the last three experiments in Table I.

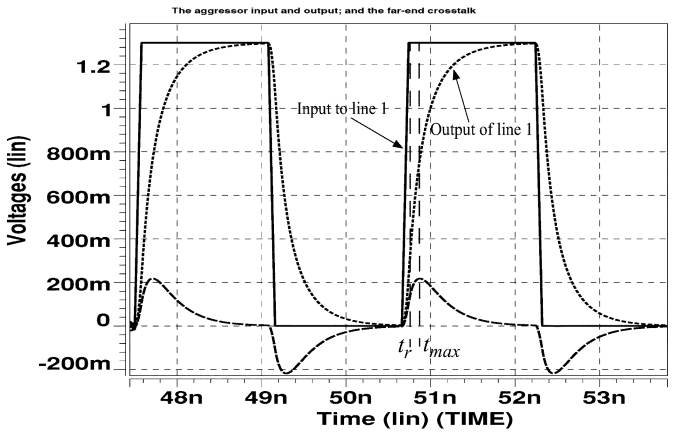

Fig. 10. Voltage waveforms at the input and output terminals of two adjacent interconnects of 4-mm length and with per-unit length electrical parameters $c_1 = c_2 = 90$ pF/m, $r_1 = r_2 = 11$ kΩ/m, $c_c = 120$ pF/m.

at the victim net along with the input waveform to the aggressor net. As seen in this figure, the time $t_{\max}$ approximated by [15] is quite different from $t_{r(f)}$. To examine the accuracy of the proposed metric for this case, Table I includes experiments where the source resistances R_{s1} and R_{s2} are large, and the neighboring lines are long. For instance, in one experiment given in Table I, where the line length is 4 mm, per-unit length parameters are $c_1 = c_2 = 90$ pF/m, $r_1 = r_2 = 11$ kΩ/m, $c_c = 120$ pF/m, and the source resistances are $R_{s1} = 160\ \Omega$ and $R_{s2} = 160\ \Omega$. Our metric predicts the peak crosstalk value to be 0.232 V, which constitutes less than 5.94% estimation error compared to the HSPICE result. Notice that the error is kept below 5.94%, although the peak value does not occur at t_r. It is easily proved that the proposed noise analytical model will result in accurate noise amplitude-pulse-width product. Therefore, we can state that our metric calculates the two important attributes of the capacitive crosstalk (i.e., the peak value and the noise pulsewidth) with a rather high accuracy.

TABLE IV
RESULTS OF SIMULATIONS ON THE CROSSTALK IN THE VICTIM NET OF FIG. 12 USING STAR-HSPICE, PAPER [10], PAPER [11], AND OUR METRIC USING A 130-nm TECHNOLOGY AND $V_{DD} = 1.3$ V

c_1 (pF/m)	r_1 (kΩ/m)	r_2 (kΩ/m)	c_2 (pF/m)	c_c (pF/m)	R_{s1}	R_{s2}	C_{out1} (pF)	C_{out2} (pF)	t_r nsec	l_1 (mm)	HSPICE volts	Devgan volts	Vittal volts	Ours volts
72	9.55	9.55	72	150	527	527	0.2	0.1	0.04	0.7	0.294	3.24	0.331	0.324
83	8.2	7.3	90	160	1013	920	0.3	0.1	0.03	0.8	0.301	5.3	0.321	0.343
92	9.3	10	80	170	270	400	0.06	0.2	0.06	2.5	0.469	4.5	0.511	0.502
101	12	12	101	150	140	150	0.1	0.2	0.08	1.2	0.282	0.662	0.328	0.297
120	10	10	120	132	2k	4k	0.06	0.07	0.1	1.1	0.345	6.86	0.402	0.394
108	15	15	108	200	20	30	0.2	0.1	0.15	1.4	0.118	0.118	0.127	0.117
130	13	20	100	220	670	720	0.3	0.05	0.09	1.6	0.368	4.36	0.425	0.401
140	17	17	100	200	350	350	0.3	0.2	0.12	2	0.326	2.02	0.39	0.362
140	17	17	100	200	30	30	0.07	0.08	0.06	2	0.46	0.85	0.531	0.488

TABLE V
ERROR COMPARISON FOR THREE NOISE METRICS

	%Error Devgan's	%Error Vittal's	%Error Ours
	1000	12.6	10.2
	1660.8	6.64	13.95
	859.5	8.96	7.04
	134.8	16.31	5.32
	1888.4	16.52	14.2
	0	7.63	0.85
	1084.8	15.49	8.97
	425	9.6	5.1
	84.78	15.43	6.1
Average	793.12	12.13	7.97
Maximum percentage error	1888.4	16.52	14.2

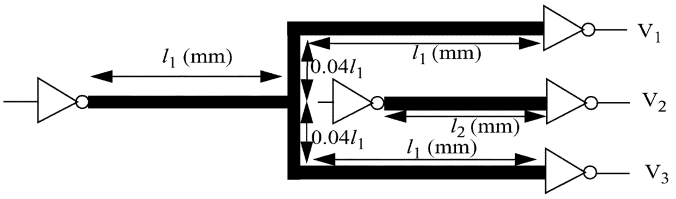

Fig. 11. Simple tree-network capacitively coupled to a single victim net.

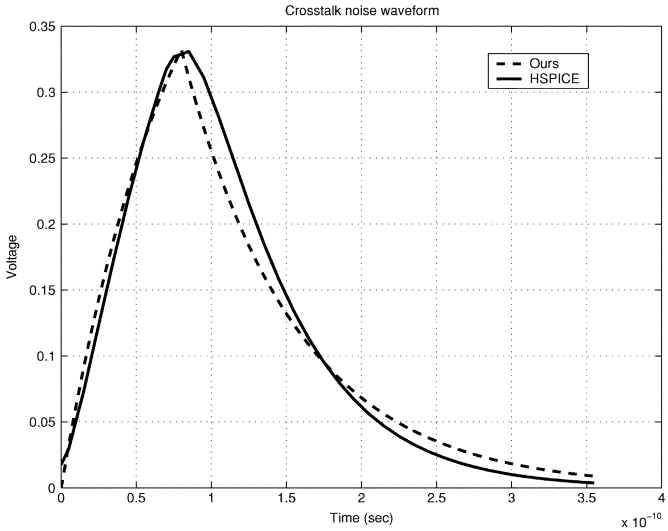

Fig. 12. Crosstalk noise waveforms for two coupled transmission lines.

The proposed analytical model can be extended to any *RC* tree network. Shown in Fig. 11 is the circuit consisting of a tree network a single interconnect line as a victim net. Such interconnect topology is often encountered in an integrated circuit, where local clock distribution networks are placed in the neighborhood of other signal lines. The circuit is realized in 130-nm CMOS technology.

Our model is compared with [10], [11], and [14]. Table IV reports the results of these comparisons for a wide range of rise-times varying between 40 and 400 ps, different line lengths, and different driver sizes. Without loss of generality, we assume that $l_2 = 0.6l_1$. To accurately model the interconnect, we model every 20 μm of each line segment with an *RC* ladder network, which results in sufficiently accurate HSPICE simulation forl_1 varying between 0.7 and 2 mm (cf. Table IV). Table V shows the estimated error of each model as compared to HSPICE results.

The susceptibility of logic gates to noise depends not only on the peak amplitude of the crosstalk noise but also on its duration. For example, digital circuits can often tolerate (and indeed filter out) spike-like crosstalk noise with a large peak amplitude and very small noise pulsewidth [10]. In static CMOS logic circuits, the peak amplitude of

TABLE VI
RESULTS OF SIMULATIONS ON THE TWO CAPACITIVELY COUPLED TRANSMISSION LINES USING STAR-HSPICE, COMPARING METHODS OF [10], [13], [14], AND OUR PROPOSED METRIC USING A 130-nm CMOS TECHNOLOGY AND $V_{\rm DD} = 1.3$ V. THE AGGRESSOR LINE INPUT IS A SATURATED EXPONENTIAL SIGNAL

c_1 (pF/m)	r_1 (kΩ/m)	r_2 (kΩ/m)	c_2 (pF/m)	c_c (pF/m)	R_{s1}	R_{s2}	C_{out1} (pF)	C_{out2} (pF)	τ_s nsec	L (mm)	HSPICE volts	Pan volts	Vittal volts	Kuhlmann volts	Ours volts
120	10	10	120	132	2k	4k	0.06	0.07	0.14	1.1	0.204	0.272	0.281	0.224	0.231
108	15	15	108	200	20	30	0.2	0.1	0.16	1.3	0.086	0.091	0.103	0.09	0.087
130	13	20	100	220	670	720	0.3	0.05	0.1	1.6	0.23	0.28	0.297	0.262	0.256
140	17	17	100	200	350	350	0.3	0.2	0.14	2	0.198	0.232	0.251	0.221	0.22
140	17	17	100	200	20	30	0.07	0.08	0.08	2	0.227	0.253	0.268	0.243	0.25
90	11	11	90	120	160	160	0.3	0.2	0.1	4	0.201	0.242	0.251	0.222	0.21
85	12	8.5	75	140	190	100	0.8	0.2	0.12	5	0.127	0.143	0.162	0.141	0.138
65	13	7	120	170	600	80	0.08	0.5	0.06	6	0.072	0.083	0.089	0.074	0.079
110	6.5	7	90	180	80	75	0.6	0.7	0.1	7	0.218	0.241	0.256	0.232	0.239
100	8	14	40	110	200	1k	0.8	0.05	0.08	8	0.441	0.492	0.534	0.472	0.461

TABLE VII
PERCENTAGE ERROR COMPARISON FOR METHODS OF [10], [13], [14] AND OUR PROPOSED METRIC

	%Error Pan's	%Error Vittal's	%Error Kuhlmann	%Error Ours
	33.1	37.75	9.8	13.24
	5.81	19.77	4.65	1.16
	21.7	29.13	13.91	11.3
	17.2	26.77	11.6	11.1
	11.45	18.06	7.05	10.13
	20.4	24.88	10.45	4.48
	12.6	27.56	11.02	8.66
	15.28	23.61	2.78	9.72
	10.55	17.43	6.42	9.63
	11.56	21.09	7.03	4.54
Average	15.97	24.6	8.47	8.4
Maximum percentage error	33.1	37.75	13.91	13.24

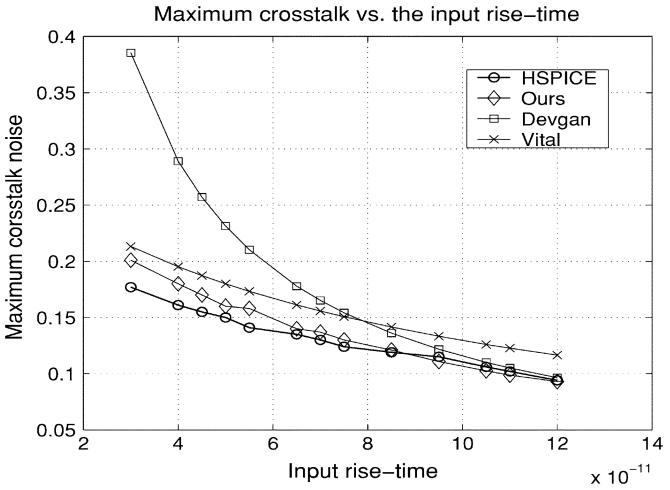

Fig. 13. Maximum crosstalk noise versus input rise-time.

crosstalk does not result in loss of signal values. Instead, it tends to cause an increase in propagation delay along the victim line, which in turn may cause setup time violation in high-speed circuits. These observations motivate the need for determining the noise pulse-width and the time-domain noise waveform.

Given the equivalent time constants of the crosstalk noise, $\tau_{d_j}^{(r)}$ and $\tau_{d_j}^{(f)}$, the peak amplitudes of the crosstalk noise, $\mathbf{V}_{2,SS}^{(r)}$ and $\mathbf{V}_{2,SS}^{(f)}$, corresponding to the rising and falling transitions of the input signal to the aggressor line, and the peak amplitudes of the crosstalk waveform, the noise waveform is readily calculated. For the general case of unequal rise and fall times, the noise waveform at each clock cycle time of T_c is computed as follows:

$$\boldsymbol{v}_2(t) = \boldsymbol{v}_{2r}(t)u(t) + \left|\boldsymbol{v}_{2f}\left(t - \frac{T_C}{2}\right)u\left(t - \frac{T_C}{2}\right)\right| \qquad (12)$$

where $\boldsymbol{v}_{2r}(t)u(t)$ and $\boldsymbol{v}_{2f}(t)u(t)$ are defined as follows:

$$\boldsymbol{v}_{2r}(t)u(t) = \begin{cases} \mathbf{V}_{2,SS}^{(r)}\left(\mathbf{I} - \mathbf{exp}\left(\mathbf{diag}\left(-\frac{t}{\tau_{d_j}^{(r)}}\right)\right)\right), & 0 \le t \le t_r \\ \mathbf{V}_{2,\max}^{(r)}\mathbf{exp}\left(\mathbf{diag}\left(-\frac{t-t_r}{\tau_{d_j}^{(r)}}\right)\right), & t \ge t_r \end{cases}$$

for $j = 1, 2 \ldots, N$

$$\boldsymbol{v}_{2f}(t)u(t) = \begin{cases} \mathbf{V}_{2,SS}^{(f)}\left(\mathbf{I}-\mathbf{exp}\left(\mathbf{diag}\left(-\frac{t}{\tau_{d_j}^{(f)}}\right)\right)\right), & 0 \le t \le t_f \\ \mathbf{V}_{2,\max}^{(f)}\mathbf{exp}\left(\mathbf{diag}\left(-\frac{t-t_f}{\tau_{d_j}^{(f)}}\right)\right), & t \ge t_f \end{cases}$$

for $j = 1, 2, \ldots, N$.

Notice that having the noise waveform gives us the maximum amount of information regarding the noise behavior including the peak amplitude of crosstalk noise and the noise pulsewidth. This information allows designers to find better solutions for noise avoidance. Fig. 12 compares (12) with HSPICE simulation for a pair of capacitively coupled nets. As one can see, our new metric accurately predicts not only the noise peak amplitude but also the noise pulsewidth. Indeed, the effective pulsewidth is estimated with a maximum error of only 5%. Our metric can easily be applied to the general case of having several parallel runs of on-chip interconnects (on the same metal layer or on different metal layers) by using the superposition principle [19].

Fig. 13 shows the change in crosstalk when the input rise time varies from 50 to 300 ps, while all of the geometrical parameters are fixed.

Comparing HSPICE results with our metric confirms that one achieves a high accuracy with our noise metric over a wide range of input rise-times. As expected, for long risetimes, Devgan's metric accurately predicts the peak amplitude of the noise. Vittal's metric exhibits higher fidelity compared to Devgan's, i.e., its estimation error remains roughly constant and does not present as large a dynamic range as Devgan's. Recall that, in [10], the authors use geometric considerations to obtain an expression for the crosstalk noise. As a result, they do not account for effects of the nonideal delays on the crosstalk peak estimation. In contrast, our metric is based on the actual characteristics of capacitively coupled *RC* circuits that are derived from simulations. In summary, our metric is more accurate than those proposed in [10] and [11].

C. Crosstalk Noise Estimation for the Saturating Exponential Input

The single-pole model proposed in Section II-B can easily be extended to predict the crosstalk noise when the input to the aggressor line is a saturating exponential signal as explained next. Consider

$$V_S(t) = V_{\mathrm{DD}}(1 - e^{-t/\tau_s})$$

where τ_s is the input time-constant. The crosstalk noise at the victim nodes becomes

$$V_2(t) = V_{\mathrm{DD}}\left[\mathbf{I}-\mathbf{diag}\left(\frac{1}{\tau_{d_j}^{(\mathrm{ex})}-\tau_s}\right)\left[\left(\frac{1}{\tau_{d_j}^{(\mathrm{ex})}}\right)\times\mathbf{exp}\left(\mathbf{diag}\left(\frac{1}{\tau_{d_j}^{(\mathrm{ex})}}\right)\right)-\mathbf{diag}\left(\frac{1}{\tau_s}\right)\times\mathbf{exp}\left(\mathbf{diag}\left(-\frac{1}{\tau_s}\right)\right)\right]\right] \quad \text{for } j = 1, 2, \ldots, N$$

where $\tau_{d_j}^{(\mathrm{ex})}$ represents the time constant of the jth node in the victim net under an exponential input excitation. $\tau_{d_j}^{(\mathrm{ex})}$ is roughly equal to $\tau_{d_j}^{(\mathrm{ex})} = (\tau_s \ln 2/t_r)\tau_{d_j}$, where t_r is the risetime of the curve-fitting flattened ramp input, and t_{dj} is the time constant of the jth node in the victim net under the curve-fitting flattened ramp input. In fact, this approximation contributes to a larger noise-estimation error.

Tables VI and VII demonstrate the accuracy of the proposed metric in calculating the peak amplitude of the coupling noise of two capacitively coupled interconnects in the presence of a saturated exponential signal at the input of the aggressor net. The noise estimation of the proposed metric is compared with the HSPICE simulation, and the techniques presented in [10], [12], and [14]. All comparisons are made using the device parameters for a 130-nm standard CMOS process. The coupled lengths of the adjacent interconnects are varied from 1.1 to 8 mm.

III. Conclusion

In this paper, we presented an efficient analysis technique for the capacitive crosstalk-noise calculation in subquarter micron VLSI interconnects. We derived closed-form expressions for the peak amplitude, the pulsewidth, and the time-domain waveform of crosstalk noise. Experimental results show that the maximum error is less than 13% and the average error is 5.82%.

References

[1] L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 9, no. 4, pp. 352–366, Apr. 1990.

[2] K. J. Kerns and A. T. Yang, "Stable and efficient reduction of large, multiport *RC* networks by pole analysis via congruence transformations," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 16, no. 7, pp. 734–744, Jul. 1997.

[3] P. Feldmann and R. W. Freund, "Efficient linear circuit analysis by Pade approximation via the Lanczos process," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 14, pp. 639–649, May 1995.

[4] A. Odabasioglu, M. Celik, and L. T. Pileggi, "PRIMA: Passive reduced-order interconnect macromodeling algorithm," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 17, no. 8, pp. 645–654, Aug. 1998.

[5] P. Heydari and M. Pedram, "Balanced truncation with spectral shaping for RLC interconnects," in *IEEE Proc. ASP-DAC*, Jan. 2001, pp. 203–208.

[6] ——, "Model reduction of variable geometry interconnects using variational spectrally-weighted balanced truncation," presented at the *IEEE/ACM Int. Conf. Computer-Aided Design*, San Jose, CA, Nov. 2001.

[7] K. Shepard and V. Narayanan, "Noise in submicron digital design," in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, Nov. 1996, pp. 524–531.

[8] K. Shepard, V. Narayanan, P. C. Elmendorf, and G. Zheng, "Globalharmony: Coupled noise analysis for full-chip *RC* interconnect networks," in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, Nov. 1997, pp. 139–146.

[9] A. Vittal and M. Marek-Sadowska, "Crosstalk reduction for VLSI," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 16, no. 3, pp. 290–298, Mar. 1997.

[10] A. Vittal, L. H. Chen, M. Marek-Sadowska, K. P. Wang, and S. Yang, "Crosstalk in VLSI interconnections," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 18, no. 12, pp. 1817–1824, Dec. 1999.

[11] A. Devgan, "Efficient coupled noise estimation for on-chip interconnects," in *Proc. IEEE ICCAD*, Nov. 1997, pp. 147–153.

[12] M. Kuhlmann, S. S. Sapatnekar, and K. K. Parhi, "Efficient crosstalk estimation," in *Proc. IEEE Int. Conf. Comput. Design*, Oct. 1999, pp. 266–272.

[13] J. Cong, D. Z. Pan, and P. V. Srinivas, "Improved crosstalk modeling for noise constrained interconnect optimization," in *Proc. IEEE ASP-DAC*, Feb. 2001, pp. 373–378.

[14] M. Kuhlmann and S. S. Sapatnekar, "Exact and efficient crosstalk estimation," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 20, no. 7, pp. 858–866, Jul. 2001.

[15] M. Takahashi, M. Hashimoto, and H. Onodera, "Crosstalk noise estimation for generic *RC* trees," in *Proc. IEEE Int. Conf. Comput. Design*, Sep. 2001, pp. 110–116.

[16] L. Ding, D. Blaauw, and P. Mazumder, "Efficient crosstalk noise modeling using aggressor and tree reductions," in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, Nov. 2002, pp. 595–600.

[17] P. Heydari and M. Pedram, "Analysis and reduction of capacitive coupling noise in high-speed VLSI circuits," in *Proc. IEEE Int. Conf. Computer Design*, Sep. 2001, pp. 104–109.
[18] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, UK: Cambridge Univ. Press, 1998, pp. 146–152.
[19] L. O. Chua, C. A. Desoer, and E. S. Kuh, *Linear and Nonlinear Circuits*. New York: McGraw-Hill, 1987.

On-Chip Embedding Mechanisms for Large Sets of Vectors for Delay Test

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***Abstract*—On-chip embedding of deterministic patterns is used for built-in test-pattern generation of large sets of vector pairs for path delay fault testing. A hardware efficient two-phase synthesis procedure is proposed to synthesize the test-pattern generator. Acceptable test-cycle requirements are met using a recent method, which reduces the test embedding problem to that of embedding the first vector in each pair. The approach is generalized to implement a hardware efficient on-chip pattern generator to test the embedded cores of a system on chip. The hardware overhead of the proposed method is reduced at a controllable increase on the number of test cycles.**

***Index Terms*—Delay estimation, digital system testing, self testing, time measurement.**

I. Introduction

The growing need for delay fault testing is a result of the advances in VLSI technology and the increase of design speed. With the ever-increasing speed of integrated circuits, violations of the performance specifications are becoming a major factor affecting the product quality level. The need for testing timing defects is further expected to grow with the current design trend of moving toward deep submicron devices. Several delay fault models, such as the transition fault and the path delay fault model, have been proposed. Difficulties are related to both the test generation and the test application process [1]. This is especially true for the path delay fault model, which accommodates better distributed delay defects and coupling effects in deep-sub micron technology.

Delay defects can only be activated and observed by propagating signal transitions through the design. This requires application of vector pairs, which significantly affect the delay testability of designs. Sequential circuits are especially difficult to test unless they are enhanced with full scan chains. The test set is generated by considering the combinational core of the circuit.

Test-pattern generators for the path delay fault model often produce lengthy test sequences and, often, it is time consuming to apply all precomputed test vectors (also called patterns) by automatic test equipment (ATE). Most importantly, chips no longer consist of a single circuit but host many embedded cores. Many input/output (I/O) pins of cores are not accessible and the precomputed test patterns cannot be directly applied to the target module. Built-in self test (BIST) is becoming an attractive alternative for such modern design technologies. The efficiency of a BIST implementation is characterized by both the test length and the hardware overhead.

Unless deterministic pairs of W-bit patterns obtained by an ATPG tool are embedded on chip, the fault coverage will be very low due to the complexity of the fault model. A recent method for test set embedding was recently proposed in [2], where the ATPG tool in [3] was used to generate a compact set of pair of test vectors. The contribution of [2] was an approach to reduce the test embedding problem to that of embedding the first vector in each pair. Once the first pattern is generated, combinational mapping logic is used to generate the second vector. A small number d of extra cells must be added to the W-bit pattern generator to ensure that the mapping logic implements legal functions, i.e., there are no vector pairs with the same first vector in two different vector pairs for which the second vectors have complimentary binary values at some bit [2]. Thus, patterns of bit length $W + d$ are generated by the test pattern embedding mechanism. The test-application time is exactly twice the time required to embed the first patterns of bit-length $W + d$. Any existing method for generating the first pattern can be used. They include the popular methods include the approaches in [4]–[11]. By definition, the smaller the value of d, the less the test length is under any existing mechanism. The method was implemented using weighted random linear feedback shift registers (LFSRs) (WLFSR) [4] and a formal justification for minimizing d was provided in [2] when WLFSR's are used.

The research efforts in [2] focused on developing algorithms to minimize the value d even when large sets of pairs of test patterns are used. Experimental results on the large test vectors by the automatic test pattern generator (ATPG) in [3] show that the expected number of test cycles are in practice double to the number of test cycles required to embed only the first vectors in the pairs [2]. In particular, the values of d are 1 or 2 in almost all examined cases. The algorithms of [2] hold independent of the mechanism used to embed the first patterns in the pairs. Experimental comparisons show that the method in [2] outperforms the embedding time of several conventional approaches such as the one that uses an embedding mechanism of length W to generate the first patterns and a $P \times W$ ROM to store the P second patterns.

Other approaches have been proposed for embedding a set of test vector pairs. In [2], it was observed that the built-in mechanisms of [7]–[9] could not generate all the vector pairs by [3]. In [10], an approach was proposed that generates pairs of patterns assuming that the second vector is obtained by applying the first vector on the circuit. This approach was shown to guarantee good fault coverage for the transition fault model, but our experimentation has shown that it does not ensure high fault coverage for the path delay fault model. The simple LFSR-based approaches in [10]–[13] and the multiple input signature register (MISR)-based method of [19] are time prohibitive, since they may require 2^W test cycles. In [20], the approach in [14] was refined so that shorter sequences from the MISR can be used, and this reduces significantly the test-application time. The method uses very time-consuming BDD-based manipulations that were limiting the approach to very small circuits. However, very recently, a SAT-based framework was proposed in [21] that significantly reduces the computational effort.

Although time efficient, the implementation of [2] is hardware demanding and this is due to the hardware overhead of the mapping logic. Reference [2] did not examine the synthesis of the mapping mechanism and, instead, proposed that the combinational mapping logic be implemented through a brute-force programmable logic array (PLA) synthesis [2]. The AND-plane of such PLA implementation has P NAND gates each of fanin $W + d$, requiring a total of $2(W + d)P$ transistors. An additional number of WA transistors for the OR-plane is required,

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