Capacitor Array Structure and Switch Control for Energy-Efficient SAR Analog-to-Digital Converters

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***Abstract*— This paper presents a new capacitor array structure and its switch control method for binary weighted SAR analog-to-digital converters, which can significantly lower the energy consumed in charge redistribution steps. The proposed method is analyzed theoretically and simulations are performed to verify the theoretical analysis. Simulation results show that the proposed capacitor array structure and switching method can reduce the average energy consumed in the capacitor array by 75% and 60% compared to the conventional method and the splitting capacitor method, respectively.**

I. INTRODUCTION

Since the charge-redistribution SAR analog-to-digital converter (ADC) was proposed about 20 years ago [1], it has been widely used in many applications. Along with the flash ADC [2] and the pipelined ADC [3], the SAR ADC is one of the most common topologies. As the dominant power is dissipated in switching the capacitor array in the SAR ADC, it is important to reduce the overall power dissipation by decreasing the capacitor switching power. The conventional switching method is not an energy-efficient method, because it wastes lots of charges. Recently, several energy-efficient switching methods such as capacitor splitting [4][5] and charge sharing [6] have been presented to reduce the switching energy by adding more switches or capacitors. In this paper, we propose a new capacitor array control method, which reduces the average switching power by 75% compared to the conventional method.

The rest of this paper is organized as follows. Section II briefly introduces the conventional SAR ADC method, and Section III explains the proposed method. The simulation results are described in Section IV along with comparisons with the previous methods.

II. CONVENTIONAL SAR ALGORITHM

Fig. 1 shows the block diagram of a SAR ADC that employs a binary-weighted capacitor array for the digital-to-analog converter (DAC). In the conventional SAR algorithm, the binary search algorithm is applied to determine the digital value. At the beginning, all the capacitors in the capacitor array sample the input voltage. As the SAR algorithm determines the digital value by determining one bit at a time, n cycles are taken for an n-bit SAR ADC. In the first cycle, all DAC control bits except the most significant bit (MSB) are set to zero to make a half of the reference voltage. The comparator determines the MSB by comparing the input voltage with the half reference voltage. In the second cycle,

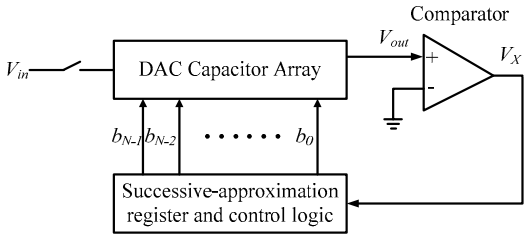

Fig. 1. Block diagram of a conventional SAR ADC

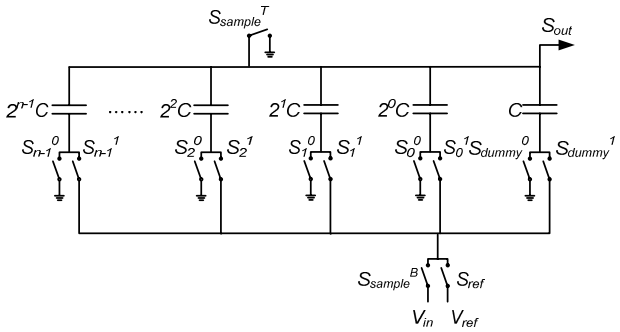

Fig. 2. The conventional DAC capacitor array for n bits

the next bit is determined by changing the MSB control bit according to the comparison result and by setting the second MSB to one. This process continues until we reach to the last bit.

Fig. 2 shows a conventional DAC capacitor array [7] that includes one dummy capacitor of capacitance C. The output voltage of this capacitor array is

$$V_{out} = -V_{in} + \frac{C_H}{C_H + C_L} V_{ref} \tag{1}$$

where C_H is the sum of all the capacitors connected to the reference voltage and C_L is that of all the capacitors connected to the ground as expressed below. More precisely, $C_H = \sum_i 2^i C$ for i such that S_i^1 is closed, and $C_L = \sum_i 2^i C$ for i such that S_i^0 is closed. Note that the dummy capacitor is always included in C_L. In other words, the dummy capacitor is always connected to the ground during the binary searching. A major point to be noticed in Eq. (1) is that V_{out} is dependent on the capacitance ratio of C_H to the total capacitors C_{tot} connected to either the ground or the reference voltage.

III. CAPACITOR SWITCHING METHOD

During the conversion process, the capacitor switches in a SAR ADC are connected first to the ground and then to the reference voltage or vice versa. When a transition occurs for a switch, e.g., the ground to the reference voltage or vice versa, it wastes energy as exemplified in Fig. 3. Let us assume that the top plate of the capacitor array is initially neutral as shown in Fig. 3(a), meaning that, on the top plate, the total number of positive charges is equal to that of negative charges. The reference voltage should supply eight positive charges to the bottom plate of C_3 to achieve the charge distribution shown in Fig. 3(a). Let us consider that switch transitions occur at the two largest capacitors corresponding to two most significant bits. In this case, the charge distribution is changed as shown in Fig. 3(b). For the charge redistribution, the reference voltage supplies ten positive charges to the bottom plate of C_2, while the bottom plate of C_3 dissipates its 12 charges. Thus, unnecessary 12 charges should be supplied from the voltage source.

In the previously proposed capacitor arrays including the conventional capacitor array and the splitting capacitor array, all the capacitors in the array are involved to derive V_{out}, that is, C_{tot} is constant. Therefore, it is inevitable to switch some of the capacitors to make a new capacitance ratio required for a desired V_{out}. To remove such an energy waste, this paper proposes a new capacitor array and its switching method. In the new capacitor array, there is no energy dissipation during the conversion process. The proposed scheme can reduce the switching energy of the capacitor array to the fundamental lowest limit.

A. Junction-Splitting Capacitor Array

The proposed capacitor array is shown in Fig. 4(a). Each box represents a sub-capacitor section of which structure is illustrated in Fig. 4(b), and the number in a box is the total capacitance of the sub-capacitor section. The proposed capacitor array has additional switches to connect the top plates of the sub-capacitor sections serially, thus it is called junction-splitting (J-S) capacitor array.

A conventional capacitor array makes a desired V_{out} by rearranging switches for a cycle. This causes energy waste as mentioned above. In contrast with the conventional capacitor array, however, the proposed J-S capacitor array makes a

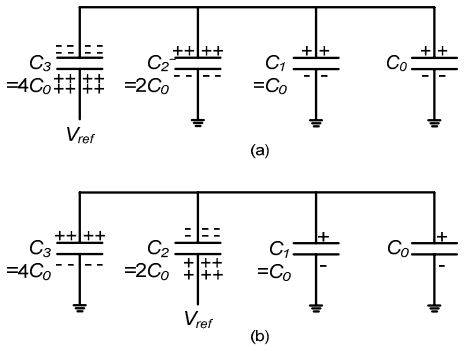

Fig. 3. Charge redistribution of a 3-bit conventional capacitor array when the switches changes from (a) to (b)

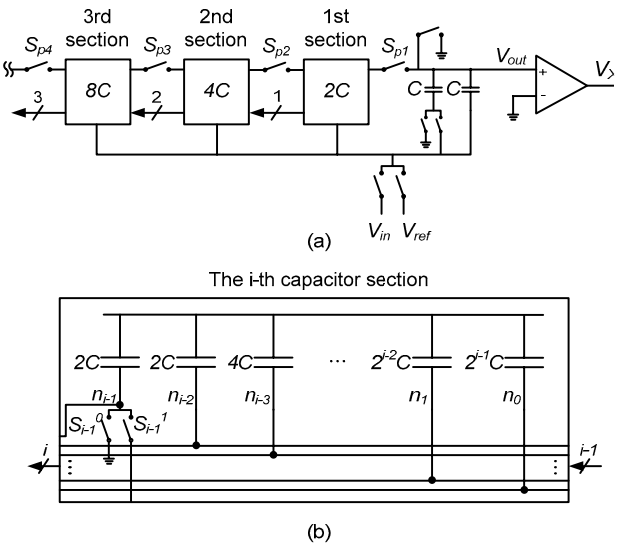

Fig. 4. Proposed SAR ADC structure. (a) SAR ADC using the proposed J-S capacitor array. (b) the i[th] sub-capacitor section of the J-S capacitor array.

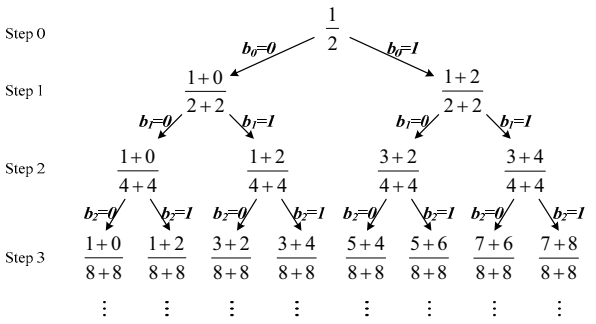

Fig. 5. How to make the desired capacitance ratio for the J-S capacitor array.

desired V_{out} by appending a sub-capacitor section to the previous capacitor array. In other words, C_{tot} is not constant, and it increases during the conversion process. How the proposed J-S capacitor array works is illustrated in Fig. 5, where the denominator and numerator represent C_{tot} and C_H, respectively. First, the MSB, b_0, is determined by comparing the input voltage with a half reference voltage. The half reference voltage is achieved by using the two smallest capacitors, one connected to the ground and the other connected to the reference voltage. Then, the next voltage to be compared is made by connecting a sub-capacitor section, one at a time.

As indicated in Fig. 5, the total capacitance of a sub-capacitor section to be added to the denominator, $C_{\Delta tot}$, is the same as that of the present total capacitance, whereas the capacitance to be added to the numerator, $C_{\Delta H}$, is determined by the results of previous comparisons, $\{b_i\}$. In general, $C_{\Delta H}$ to be added at step i ($i > 0$) is determined by $C(2^{i-1} b_0 + 2^{i-2} b_1 + 2^{i-3} b_2 + \cdots + 2^1 b_{i-2} + 2 b_{i-1})$, where C is a unit capacitance. In step 0, $C_{tot} = 2C$, and $C_H = C$. Hence, the i-th sub-capacitor section consists of i capacitors as shown in Fig. 4, where n_j means the node controlled by the j-th bit. The total capacitance of the i-th section is 2^iC, which is equal to the sum of

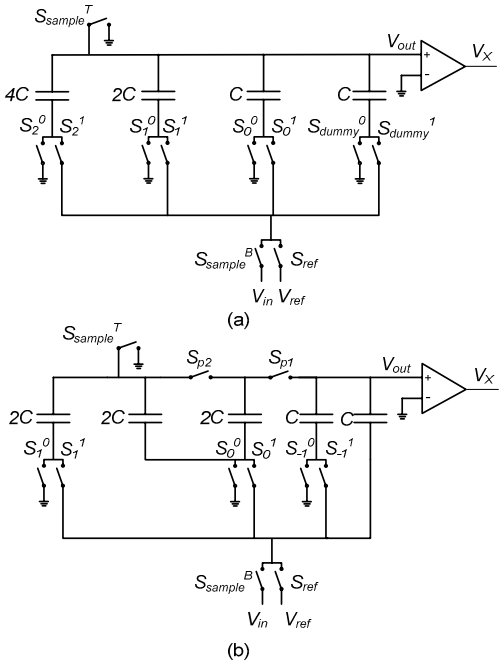

Fig. 6. A 3-bit SAR ADC. (a) A conventional 3-bit SAR ADC. (b) A 3-bit SAR ADC based on the J-S capacitor array.

capacitances of all the previous sections at the right side. In a section, each capacitor has two switches that are controlled by one of the previously determined bits. A capacitor is connected to the ground through a switch denoted by S_j^0 if the corresponding bit b_j is 0, otherwise it is connected to the reference voltage through a switch S_j^1. Since all the capacitors controlled by the same bit can be connected through a pair of switches, each section has a pair of switches for a capacitor and has connections to the switches in the right sections for the other capacitors, as drawn in Fig. 4. Therefore, a section has only a pair of switches. For *n*-bit digital outputs, the proposed J-S capacitor array structure has *3n-1* switches in total, because it consists of *n* sections including the *0*-th section each of which needs a pair of switches and two adjacent sections are serially connected through a switch, as exemplified in Fig. 4.

For easy explanation, the proposed switching method is described using a 3-bit SAR ADC shown in Fig. 6. The conventional 3-bit SAR ADC and the proposed 3-bit SAR ADC are illustrated in Fig. 6(a) and Fig. 6(b), respectively. The output of this ADC is a three-bit digital value represented as (b_0, b_1, b_2). In the sample mode [1], we close the switches for $S_{sample}{}^{B}$, $S_{sample}{}^{T}$, S_{p1}, S_{p2}, $S_{-1}{}^1$, $S_0{}^1$ *and* $S_1{}^1$ and open the others to sample the input voltage by connecting all the top plates to the ground and all the bottom plates to the input voltage. This makes every capacitor charged to the input voltage. In the hold mode [1], we open all the switches closed in the sample mode and close S_{ref} in order to preserve the charges on the top plates. Up to this point, the proposed switching control is exactly identical to the conventional method.

The redistribution mode [1] begins by testing the value of the MSB bit, b_0. As indicated in (1), the output voltage of the

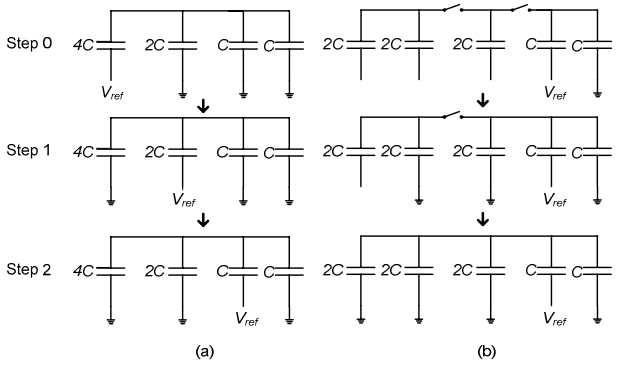

Fig. 7. Switch transitions of the 3-bit capacitor array in case of code 000. (a) For the conventional 3-bit capacitor array. (b) For the proposed 3-bit J-S capacitor array.

capacitor array is determined by the ratio of C_H to C_{tot}. In the first cycle of the redistribution mode, the output voltage of the conventional capacitor array should be $V_{out} = -V_{in} + \frac{1}{2}V_{ref}$. This voltage is achieved in the conventional method by connecting the capacitor of 4*C* to the reference voltage and the others to the ground. As the output voltage of the capacitor array is determined by the capacitance ratio not by the absolute capacitance, it is possible to achieve the same voltage by closing $S_{-1}{}^0$ and opening S_{p1} in Fig. 6(b).

The comparator now senses V_{out}. If $V_X > 0$, b_0 is set to 1 because the input voltage is larger than the half reference voltage, otherwise, b_0 is set to 0. If b_0 is set to 0, the MSB capacitor switch in the conventional capacitor array returns to the ground to prepare for the second cycle, leading to energy waste as mentioned above. However, the proposed J-S capacitor array does not change the switch connection to prevent unnecessary energy consumption. The proposed J-S capacitor array works as follows. If $V_{out} = -V_{in} + \frac{1}{2}V_{ref} > 0$, we set b_0 to 1 and close S_{p1} and $S_0{}^1$. Otherwise, we set b_0 to 0, and close S_{p1} and $S_0{}^0$. In a similar manner, b_1 and b_2 are determined in the next cycles.

B. Energy Efficiency of J-S capacitor array

To show the energy efficiency of the proposed J-S capacitor array, a 3-bit SAR ADC is considered in this section. For an output digital code of *000*, how the switches in the capacitor array change are drawn in Fig. 7, where (a) is for the conventional capacitor array and (b) for the J-S capacitor array.

Fig. 7(a) consumes energy in every redistribution step [5]. The energy consumed at each step can be computed as follows, where E_0, E_1 and E_2 represent the energy required to determine b_0, b_1 and b_2, respectively.

$$E_0 = -V_{ref} 4C(-\frac{1}{2}V_{ref} - 0) = 2CV_{ref}{}^2$$

$$E_1 = -V_{ref} 2C(-\frac{3}{4}V_{ref} - \frac{1}{2}V_{ref}) = \frac{5}{2}CV_{ref}{}^2$$

$$E_2 = -V_{ref} C(-\frac{7}{8}V_{ref} - \frac{3}{4}V_{ref}) = \frac{13}{8}CV_{ref}{}^2$$

Hence, the total energy is $E_T = \frac{49}{8} CV_{ref}{}^2$. However, for Fig. 7(b), the energy consumed in each step is reduced as follows.

$$E_0 = -V_{ref} C(-\frac{1}{2}V_{ref} - 0) = \frac{1}{2}CV_{ref}{}^2$$

$$E_1 = -V_{ref} C(-\frac{3}{4}V_{ref} + \frac{1}{2}V_{ref}) = \frac{1}{4}CV_{ref}{}^2$$

$$E_2 = -V_{ref} C(-\frac{7}{8}V_{ref} + \frac{3}{4}V_{ref}) = \frac{1}{8}CV_{ref}{}^2$$

Hence, the total energy consumption is reduced to $E_T = \frac{7}{8} CV_{ref}{}^2$.

In case of output code *000*, the proposed J-S capacitor array consumes one seventh of the energy required in the conventional capacitor array. As mentioned before, the positions of all the switches in the J-S capacitor array do not change during the redistribution mode. Therefore, the required energy is determined by the final state, which is the fundamental lowest level. Though the energy consumption depends on the input voltage, the proposed J-S capacitor array achieves remarkable energy saving for any input voltage, when compared to the splitting capacitor structure [4][5] as well as the conventional structure.

IV. Simulation Results And Comparisons

A SAR ADC model has been developed based on the theoretical analysis in order to calculate the switching energy of each output digital code, and the model is confirmed through rigorous Spice simulations. Fig. 8 shows the simulation result that compares three methods such as the conventional structure, the splitting capacitor structure [4][5] and the proposed J-S capacitor structure. With assuming a uniformly distributed input voltages, Table I compares the three switching methods in terms of the number of switches and the normalized energy consumption. In counting the number of switches, we include the switches required in the sample and hold modes. The total capacitances required in those structures are not shown in Table I, because all the structures need the same amount of capacitance to build the capacitor arrays regardless of the structure differences.

As indicated in Table I, the proposed J-S capacitor array saves 75% of energy compared to the conventional method, and 60% even compared to the splitting capacitor method. For output digital values represented in *n* bits, it requires *n-1* more switches compared to the conventional structure, but the increment is smaller than that of the splitting capacitor structure. As the process technology improves, the size of a switch becomes small compared to the capacitor array, thus the switch increment is not significant. As shown in Fig. 4, the proposed J-S capacitor structure requires splitting capacitors in a section. However, such capacitor splitting does not induce any penalty, as a large capacitor is usually made by arranging unit-sized capacitors to tolerate process mismatches.

TABLE I. Comparison of the number of switches and switching energy.

Method	Number of switches	Normalized Avg. Energy for uniform inputs
Conventional Cap.	2n+5	1.000
Split Cap.	4n+3	0.625
Proposed J-S Cap.	3n+2	0.250

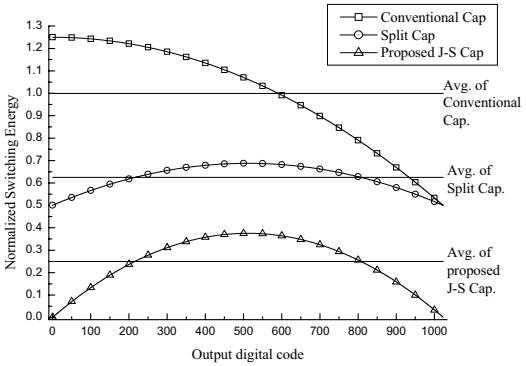

Fig. 8. Normalized switching energy

V. Conclusions

We have presented a new capacitor array structure for SAR ADCs and a new switching method that can reduce energy consumption significantly. The proposed structure consists of a number of serially connected sections each of which is composed of splitting capacitors. Each section is appended to determine one bit at a time. By employing the proposed capacitor array structure, the energy consumed in the capacitor array is reduced by about 75% and 60% compared to the conventional capacitor array and the splitting capacitor array, respectively. As the energy consumed in the capacitor array takes a large portion of whole energy consumed in SAR ADCs, the proposed J-S capacitor array plays an important role in lowering the power consumption of SAR ADCs.

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