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Capacitor Lifetime Extension in a Hybrid Active Neutral-Point-Clamped Inverter With Reduction of DC-Link Ripple Current and Common-Mode Voltage

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ABSTRACT This paper proposes a reduction method for DC-link ripple current and common-mode voltage (CMV) in a hybrid active neutral-point-clamped (ANPC) inverter. A Si and SiC hybrid ANPC inverter has been developed recently to overcome the extremely high cost of a full-SiC ANPC inverter. A hybrid ANPC requires much fewer SiC MOSFETs than a full-SiC ANPC inverter while providing a comparable power density. Voltage source inverters such as hybrid ANPC inverters utilize electrolytic capacitors, which have a large capacitance per volume, as a DC link. However, an electrolytic capacitor is one of the most vulnerable components in a power electronic converter due to its small allowable ripple current. A large ripple current flowing into the electrolytic capacitor generates a heat loss, which shortens the lifetime of the capacitor. Furthermore, the common-mode voltage (CMV) causes an undesirable leakage current and electromagnetic interference. The CMV depends on the pulse-width modulation of the voltage source inverters. The proposed method enhances the reliability of the hybrid ANPC inverter by reducing the DC-link ripple current and CMV simultaneously. The effectiveness and validity of the proposed method are verified through simulations and experimental results.

INDEX TERMS Capacitor, common-mode voltage, neutral point ripple current, hybrid ANPC inverter, space vector modulation.

I. INTRODUCTION

Multilevel inverters are suitable for high-power and medium-voltage renewable energy generation systems because of their small filter size, gradual dv/dt, and outstanding harmonic characteristics [1]–[3]. A three-level neutral-point-clamped (NPC) inverter is one of the most widely used multilevel inverters [4], [5]. However, it has the disadvantage of an unbalanced distribution of losses between the switching devices. The unbalanced loss causes a temperature imbalance between the switching devices, which results in different lifetimes of the switches [6]. To overcome this drawback, an active NPC (ANPC) inverter topology, which replaces the clamping diodes of the NPC inverter with a Si IGBT, and its pulse-width modulation (PWM) strategies have been developed [7]–[9]. In addition, a study for full SiC-based ANPC inverter was conducted to maximize its power density and efficiency [10]. As SiC devices have low switching loss, a SiC-based inverter can be driven with high switching frequency, thereby reducing the filter size of the output stage. However, SiC devices are several times more expensive than Si devices. Thus, a Si and SiC hybrid ANPC inverter has been proposed in [11] to alleviate this problem. Although the Si and SiC hybrid ANPC inverter requires only two SiC devices per leg, it has a switching loss similar to that of a full-SiC ANPC inverter.

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A hybrid ANPC inverter utilizes electrolytic capacitors as the DC-link to stabilize the DC-link voltage. Electrolytic capacitors have a short lifetime due to the wear out caused by the electrolyte evaporation and electrochemical reaction [12]. The electrolyte evaporation and electrochemical reaction depend on the hot-spot temperature of the capacitor, which varies with the loss caused by its equivalent series resistance (ESR). As the loss caused by the ESR varies with the root mean square (RMS) value of the ripple current flowing to the capacitor, the reliability of the capacitor can be improved by reducing the ripple current of the capacitor [13]. Some studies have attempted to reduce the DC-link ripple current. In [14], [15], methods for reducing the DC-link ripple current in a two-level back-to-back converter were proposed. These methods were implemented by changing the offset voltage for the discontinuous PWM or shifting the carrier. However, they are applied to a back-to-back converter. A switching method for reducing the DC-link ripple current of a three-level inverter was proposed in [16]. Although the proposed switching method could reduce both the DC-link ripple current and common-mode voltage (CMV), the performance for the reduction of the DC-link ripple current was insufficient.

CMV is generated in a PWM inverter such as a hybrid ANPC inverter. It is a major area of interest in motor drive applications and photovoltaic (PV) inverters. It is well known that bearing currents, shaft voltage, electromagnetic interference (EMI), and leakage current are induced by CMV [17]. In addition, as the CMV issue is exacerbated with the increase in switching frequency, it must be addressed in hybrid ANPC inverters operating at a high switching frequency [18]. The two types of solutions to cope with CMV are hardware and software solutions. In [19]–[21], strategies for CMV reduction using an active or passive filter were studied. Although these hardware solutions have demonstrated an outstanding CMV reduction performance, they require additional devices. Hence, software solutions based on PWM were proposed in [22]–[27]. [22] proposed a new CMV reduction method suitable for Quasi Z-source three-level inverter. This method modified large-medium-zero vector modulation (LMZVM) for quasi Z-source three-level inverter by applying the additional shoot-through voltage vector. An improved space vector modulation (SVM) is proposed in [23] to reduce CMV and compensate the neutral point (NP) AC and DC unbalance for the three-level inverters. Its CMV and NP balancing control is performed by calculating and applying a suitable small vector duty cycle to LMZVM. In [24] and [25], a double modulation wave CBPWM strategy and virtual SVPWM was proposed to reduce CMV for three-level inverter. Although these strategies reduce NP AC voltage ripple and CMV effectively, the number of switching of power semiconductors increases when performing pulse width modulation (PWM). In [26], hybrid modulation method of LMZVM and large-medium-small vector modulation (LMSVM) is proposed for CMV reduction and DC voltage balance in DC-link capacitors. The proposed hybrid modulation method reduces CMV and maintains voltage of each the split capacitor to $V_{DC}/2$ simultaneously by applying LMSVM according to the division of space vector diagram. In [27], a common-mode voltage reduction pulsewidth modulation (CMV-R PWM) is proposed. This method also reduces CMV by using a different voltage vector instead of the existing small vector, and applies a separate controller to control the DC-link capacitor voltage stable. However, all of these methods do not consider the effect of the DC-link ripple current according to the change in the PWM method.

This paper presents a switching strategy to suppress the DC-link ripple current and CMV in a hybrid ANPC. The proposed switching scheme is simply implemented by replacing the voltage vectors that cause the large capacitor current and high peak-to-peak CMV with different voltage vectors. In addition, the proposed method extends the lifetime of the DC-link capacitor and reduces the leakage current in the hybrid ANPC. The feasibility and effectiveness of the proposed switching scheme have been demonstrated through simulations and experiments.

II. OPERATION OF HYBRID ANPC INVERTER

A leg of hybrid ANPC is composed of four Si IGBTs and two SiC MOSFETs as shown in Fig. 1 [11]. SiC MOSFETs, which have a low switching loss, should take most of the switching burden to minimize switching losses. Therefore, separate reference voltages for controlling the Si IGBT and SiC MOSFET are required to decrease the power loss of the hybrid ANPC inverter.

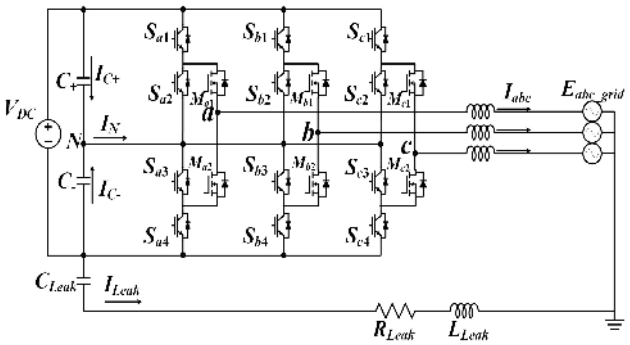

FIGURE 1. Configuration of a hybrid ANPC inverter.

Fig. 2 shows normalized reference pole voltage and the reference voltages for the Si IGBTs and SiC MOSFETs. Their reference voltages are represented by (1) and (2), respectively [11].

$$V^*_{xN\_IGBT} \begin{cases} 1 & (V^*_{xN\_norm} \geq 1) \\ 0 & (V^*_{xN\_norm} < 1) \end{cases} \tag{1}$$

$$V^*_{xN\_MOSFET} = V^*_{xN\_norm} - V^*_{xN\_IGBT}. \tag{2}$$

When the command voltage is in the positive half-period, the reference voltage $V^*_{xN\_IGBT}$ is clamped to 1. Accordingly, for the half-period, the IGBTs S_{x1}, S_{x3} are turned ON, and the IGBTs S_{x2}, S_{x4} are turned OFF. When the reference voltage is

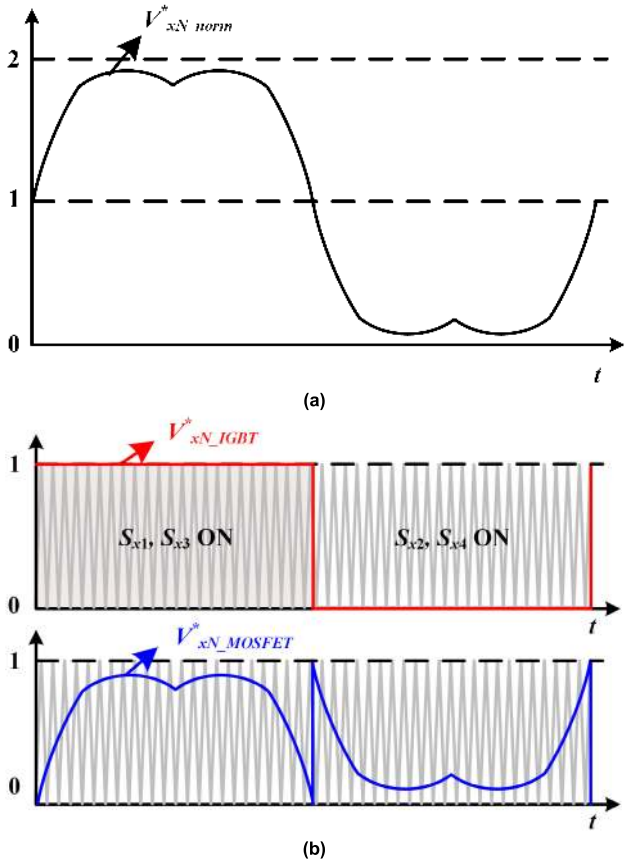

FIGURE 2. Reference pole voltages (a) Normalized reference pole voltage, (b) pole voltages for Si IGBT and SiC MOSFET.

in the negative half-period, $V^*_{xN\_IGBT}$ is clamped to 0. Accordingly, the IGBTs S_{x2}, S_{x4} are turned ON and the IGBTs S_{x1}, S_{x3} are turned OFF. A reference voltage such as that in (2) is used for the PWM of the SiC MOSFET. When this modulation method is applied to a hybrid ANPC inverter, the Si IGBT operates at the line frequency and the SiC MOSFET operates at the switching frequency. Consequently, the losses caused by the Si IGBT are mostly conduction losses, and most of the switching losses are generated by the SiC MOSFET. A MOSFET has a small switching loss, and this modulation method increases its power conversion efficiency. The pole voltages of the hybrid ANPC inverters have four switching states ([N], [O$^+$], [O$^-$], and [P]). When $V^*_{xN\_IGBT}$ is 1, S_{x1} and S_{x3} are turned on and the [P]- and [O$^+$]-states are generated according to the switching operation of the SiC MOSFET. In contrast, when $V^*_{xN\_IGBT}$ is zero, S_{x2} and S_{x4} are turned on and the [N]- and [O$^-$]-states are generated by the switching of the SiC MOSFET.

III. REALIABILITY OF CAPACITOR

A power converter is composed of various components. The failure distribution of the capacitor accounts for a significant portion of the failure distribution [28]. Among capacitors, electrolytic capacitors are frequently used as the DC-link due to their large capacitance per volume and low cost. An electrolytic capacitor has three failure modes: short circuit, open circuit, and wear-out failure. Among these failure modes, wear-out failure is an inevitable but controllable failure mode. Therefore, the reliability of the capacitor can be improved by delaying the occurrence time of wear-out failure. Aged capacitors have reduced capacitance and increased ESR due to the wear-out caused by electrolyte evaporation. In particular, after the capacitance decreases by 20% and the ESR doubles, the rates of change of the capacitance and ESR are accelerated rapidly. This point is generally regarded as the wear-out failure of the capacitor [29].

The process of lifetime prediction was studied in [13] to predict the wear-out failure of capacitors. First, the loss caused by the ESR of the capacitor is as follows:

$$P_{loss,ESR} = \sum_{i=1}^{n} [I^2_{RMS}(f_i) \times \mathrm{ESR}(f_i)], \tag{3}$$

where $I_{RMS}(f_i)$ and ESR(f_i) are the RMS value of the ripple current and the ESR at frequency f_i, respectively. From the above equation, it can be observed that the loss caused by the ESR depends on the RMS value of the capacitor current. The hot-spot temperature of the capacitor is expressed by

$$T_{hot-spot} = T_{ambient} + R_{ha} \times P_{loss,ESR}, \tag{4}$$

where $T_{ambient}$ is the ambient temperature and R_{ha} is the equivalent thermal resistance for the variation in temperature from ambient to hot-spot temperature. The lifetime of the capacitor is finally calculated using the hot-spot temperature as follows:

$$L = L_0 \times \left(\frac{V}{V_0}\right)^{-p_0} \times 2^{\frac{T_0 - T_{hot-spot}}{p_1}}, \tag{5}$$

where L_0, V_0, T_0, and V are the rated lifetime, rated voltage, maximum allowable hot-spot temperature, and real voltage, respectively. For the electrolytic capacitor, the constant p_0 ranges from approximately 3 to 5 and p_1 is approximately 10 [13]. From the above lifetime model, it can be observed that the lifetime of the capacitor increases, as the hot-spot temperature of the capacitor decreases. As the hot-spot temperature is dependent on the loss, which decreases with a reduction in the RMS value of the capacitor current, the lifetime of the capacitor is extended by reducing the ripple current of the capacitor.

IV. ANALYSIS ON DC-LINK RIPPLE CURRENT AND CMV

The currents flowing to the upper and lower DC-link capacitors are combined at the neutral point as shown in Fig. 1, which is expressed as

$$I_N = I_{C+} + I_{C-}, \tag{6}$$

where I_{C+} and I_{C-} are the upper- and lower-side capacitor currents, respectively. Therefore, it is possible to reduce the ripple current of the upper and lower DC-link capacitors by reducing the neutral point ripple current. Only in the case of the [O$^+$] or [O$^-$] state, the phase current flows to the

neutral point through the inner switches S_{x2} or S_{x3}, which are connected to the neutral point. For example, if the switching state is [PO$^+$N], the b-phase current I_b flows to the neutral point; in contrast, in the case of [PO$^+$O$^-$], the b- and c-phase currents $I_b + I_c$ flow to the neutral point. The neutral point currents according to the switching state of the three-level inverter are shown in Table 1.

TABLE 1. Switching state and magnitude of neutral point current.

Switching state		Neutral point current (I_N)
Large vector	[PPN], [PNP], [NPP] [NNP], [NPN], [PNN]	0
Medium vector	[OPN], [ONP] [PON], [NOP] [PNO], [NPO]	I_a I_b I_c
Small vector	[OPP], [ONN] [POO], [NOO] [POP], [NON] [OPO], [ONO] [PPO], [NNO] [OOP], [OON]	I_a $I_b + I_c = -I_a$ I_b $I_a + I_c = -I_b$ I_c $I_a + I_b = -I_c$
Zero vector	[PPP], [OOO], [NNN]	0

Fig. 3 shows the space vector diagram and reference voltage vector in conventional space vector PWM (SVPWM). In the marked sector, the order of magnitudes of the output currents is $|I_a| > |I_b| > |I_c|$. In conventional SVPWM, the voltage vectors (large vector: [PNN], medium vector: [PNO$^-$], small vectors: [PO$^-$O$^-$], [O$^+$NN]) are used to generate the reference voltage vector V^*.

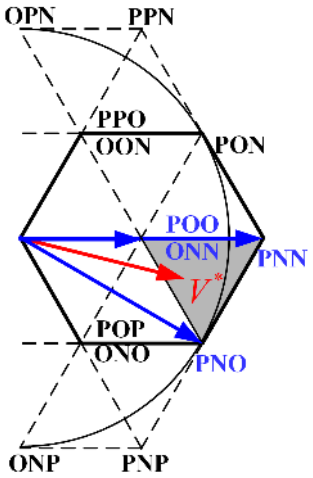

FIGURE 3. Space vector diagram in conventional SVPWM.

Fig. 4 shows the switching sequence used to generate the reference voltage vector in Fig. 3 and the resulting neutral point current I_N. In this sector, the absolute value of I_a is the largest; hence, the use of [PO$^-$O$^-$] and [O$^+$NN] causes the largest capacitor ripple current. [PO$^-$O$^-$] and [O$^+$NN] are the small vectors adjacent to the reference voltage vector.

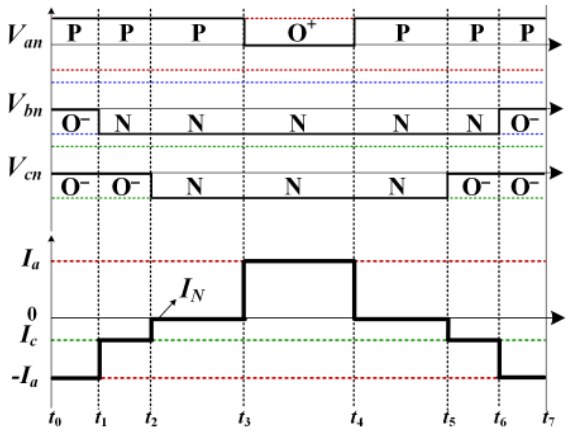

FIGURE 4. Neutral point current according to the switching states in conventional SVPWM.

In a typical three-phase voltage source inverter, CMV is the average value of the three-phase output voltages and is expressed as

$$V_{CMV} = \frac{V_{an} + V_{bn} + V_{cn}}{3} \tag{7}$$

where V_{an}, V_{bn}, and V_{cn} are the three-phase output pole voltages. As shown in Fig. 5, the CMV changes from $V_{dc}/6$ to $-V_{dc}/3$ within a switching period in Sector 1-(a). Among the switching states, the small vectors ([PO$^-$O$^-$] and [O$^+$NN]) generate the largest ($V_{dc}/6$) and smallest ($-V_{dc}/3$) values of CMV. That is, both a large current ripple and a peak-to-peak value of CMV are caused by the small vector closest to the V^*.

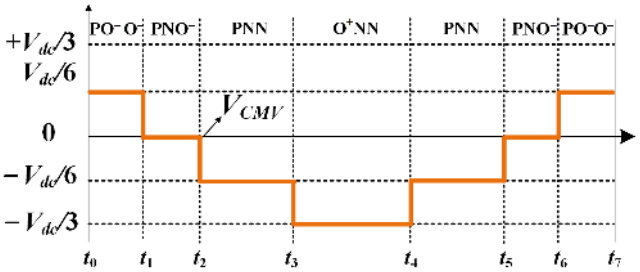

FIGURE 5. CMV in conventional SVPWM.

V. REDUCTION OF DC-LINK RIPPLE CURRENT AND CMV

A. PROPOSED SWITCHING METHOD

According to the analysis presented in Section IV, the small vector adjacent to the reference voltage induces a large ripple in the DC-link current and a higher peak-to-peak voltage as well. This paper proposes a switching scheme utilizing another vector instead of the small vectors adjacent to the reference voltage. For implementing the proposed method, the space vector diagram is divided into six sectors, and each sector is divided into sections (a) and (b). The substituted vectors are small and medium vectors located in

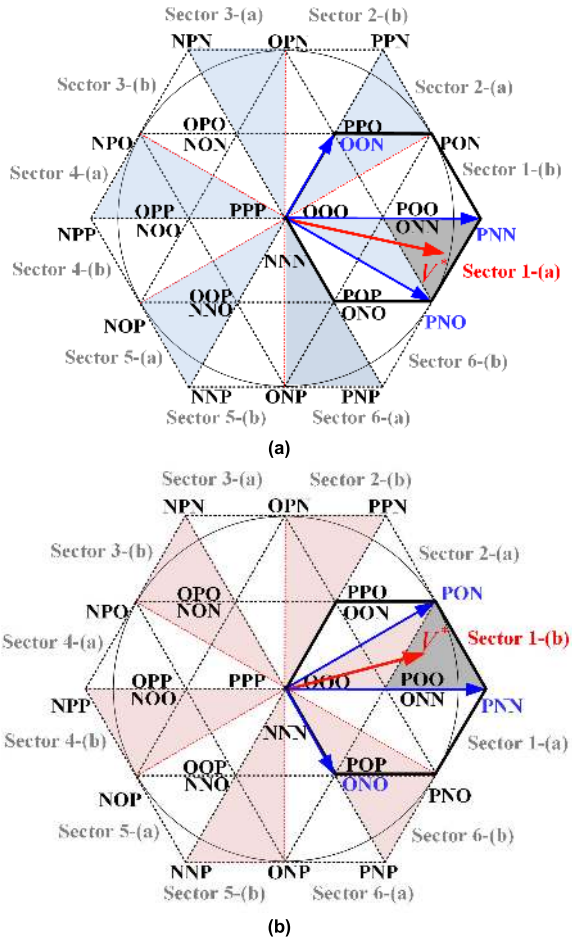

FIGURE 6. Sector segmentation and voltage vectors for generating the reference voltage, (a) Sector 1-(a), (b) Sector 1-(b).

the other sector and current sector, respectively. In section (a) of each sector, the small vector in the next sector is selected to replace the existing small vector. In contrast, in section (b) of each sector, the small vector in the previous sector is selected. Fig. 6(a) shows examples of generating the reference voltage vector V^* using the proposed method in Sector 1-(a). Conventional SVPWM selects [PO$^-$O$^-$], [O$^+$NN], [PNO$^-$], and [PNN] to generate V^*. However, the proposed method uses [O$^+$O$^-$N] and [PNO$^-$] instead of the small vectors [O$^+$NN] and [PO$^-$O$^-$]. The switching sequence is [PO$^-$O$^-$]-[PNO$^-$]-[PNN]-[O$^+$NN]-[PNN]-[PNO$^-$]-[PO$^-$O$^-$] with conventional SVPWM. It is converted to [PNO$^-$]-[PNO$^-$]-[PNN]-[O$^+$O$^-$N]-[PNN]-[PNO$^-$]-[PNO$^-$] when the proposed switching scheme is applied.

Fig. 7 shows the reconfigured switching sequence obtained using the proposed method for generating the reference voltage vector in Sector 1-(a). As analyzed above, the vectors [PO$^-$O$^-$] and [O$^+$NN] in Sector 1-(a) are replaced with [PNO$^-$] and [O$^+$O$^-$N]. [PNO$^-$] and [O$^+$O$^-$N] are symmetrically located on the basis of [PO$^-$O$^-$] and [O$^+$NN], and are applied for the same dwelling time as [PO$^-$O$^-$] and [O$^+$NN], so that the same reference voltage as in conventional SVPWM

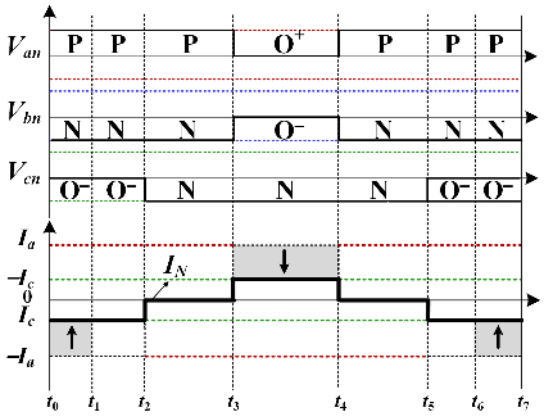

FIGURE 7. Reduction of neutral point current with a reconfigured switching sequence using the proposed switching strategy.

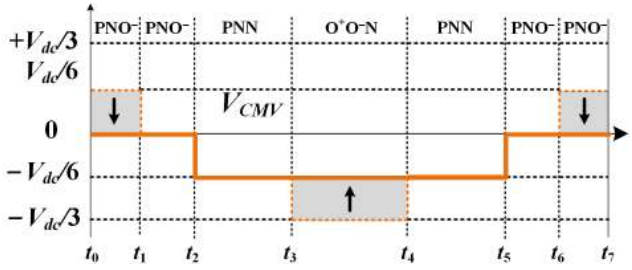

FIGURE 8. CMV reduction with the proposed switching strategy.

can be generated. As the substitution, the c-phase current, which is the smallest current in Sector 1-(a), flows to the neutral point. Using the proposed technique, only a zero current or the smallest current among the three-phase output currents flows to the neutral point in all the sectors. The reduction of the neutral point current induces the suppression of the DC-link ripple current, which causes an increase in the service life of the DC-link capacitor.

In addition, the peak-to-peak value of the CMV is reduced by applying the proposed switching scheme, which does not use the small vector closest to the reference voltage. Fig. 8 shows the CMV within a cycle when the proposed switching method is applied. Due to the use of [PNO$^-$] and [O$^+$O$^-$N], the CMV varies from $-V_{dc}/6$ to zero. The peak-to-peak value of the CMV is reduced to approximately 1/3 of the CMV obtained when applying conventional SVPWM. Reduction of CMV improves system reliability by reducing EMI and bearing current.

The proposed method incurs the same amount of loss as conventional SVPWM. This is because the number of switching operations and the turn-on time of each switch are the same as those in conventional SVPWM. However, as shown in Table 2, the proposed switching scheme increases the period to maintain the same switching state. If the same switching state persists, the total harmonic distortion (THD) deteriorates as the current continues to increase or decrease during this period. Although the proposed method itself causes a deterioration of the THD, when it is applied to a system having a leakage current such as a PV inverter, the THD

TABLE 2. Switching sequences obtained with the proposed method.

Sector	Proposed switching strategy
1-(a)	[PNO$^-$]-[PNO$^-$]-[PNN]-[O$^+$O$^-$N]-[PNN]-[PNO$^-$]-[PNO$^-$]
1-(b)	[PO$^-$N]-[PO$^-$N]-[PNN]-[O$^+$NO$^-$]-[PNN]-[PO$^-$N]-[PO$^-$N]
2-(a)	[O$^+$PO$^-$]-[PPN]-[PO$^+$N]-[PO$^+$N]-[PO$^+$N]-[PPN]-[O$^+$PO$^-$]
2-(b)	[PO$^+$O$^-$]-[PPN]-[O$^+$PN]-[O$^+$PN]-[O$^+$PN]-[PPN]-[PO$^+$O$^-$]
3-(a)	[O$^-$PN]-[O$^-$PN]-[NPN]-[NO$^+$O$^-$]-[NPN]-[O$^-$PN]-[O$^-$PN]
3-(b)	[NPO$^-$]-[NPO$^-$]-[NPN]-[O$^-$O$^+$N]-[NPN]-[NPO$^-$]-[NPO$^-$]
4-(a)	[O$^-$O$^+$P]-[NPP]-[NPO$^+$]-[NPO$^+$]-[NPO$^+$]-[NPP]-[O$^-$O$^+$P]
4-(b)	[O$^-$PO$^+$]-[NPP]-[NO$^+$P]-[NO$^+$P]-[NO$^+$P]-[NPP]-[O$^-$PP]
5-(a)	[NO$^-$P]-[NO$^-$P]-[NNP]-[O$^-$NO$^+$]-[NNP]-[NO$^-$P]-[NO$^-$P]
5-(b)	[O$^-$NP]-[O$^-$NP]-[NNP]-[NO$^-$O$^+$]-[NNP]-[O$^-$NP]-[O$^-$NP]
6-(a)	[PO$^-$O$^+$]-[PNP]-[O$^+$NP]-[O$^+$NP]-[O$^+$NP]-[PNP]-[PO$^-$O$^+$]
6-(b)	[O$^+$O$^-$P]-[PNP]-[PNO$^+$]-[PNO$^+$]-[PNO$^+$]-[PNP]-[OO$^-$P]

degradation can be offset by the leakage current reduction effect of the proposed switching method. The impact of the proposed switching method on the THD will be discussed through simulation and experimental results.

In addition, the proposed switching method is applicable to all three-level inverters such as NPC-type or T-type inverters and hybrid ANPC inverters.

B. COMPARISON WITH EXISTING DC-LINK RIPPLE CURRENT REDUCTION METHOD

In [16], a DC-link ripple current reduction method (Method-I) is proposed. This switching method reduces neutral-point ripple current and CMV simultaneously. These effects are similar to the proposed method in this paper. However, the reduction ratio of the neutral-point ripple current is different between the Method-I and proposed method.

Fig. 9 Shows the space vector diagram for each sector in Method-I. In Sector 1-(a), Method-I selects [PO$^-$N] and [O$^+$NO$^-$] vectors instead of [PO$^-$O$^-$] and [O$^+$NN] vectors, while the proposed method selects [PNO$^-$] and [O$^+$O$^-$N]. When a vector is selected in this way, the b-phase current, which is the second largest vector in Sector 1-(a), flows to the neutral point. As a result, the neutral point ripple current reduction effect of Method-I is inferior to the proposed switching method. Fig. 10 shows the NP current reduction effect when Method-I is applied. The a-phase current caused by [PO$^-$O$^-$] and [O$^+$NN] is replaced by b-phase current. However, the neutral point reduction effect is inferior to the proposed method in which a smaller c-phase current flows to the neutral point instead of the b-phase current.

C. COMPARISION WITH EXISTING CMV REDUCTION METHOD

Fig. 11(a) shows CMV in Sector 1-(a) when LMZVM used in [22] and [23] is applied. LMZVM is a method of generating a reference voltage using only large, medium, and zero

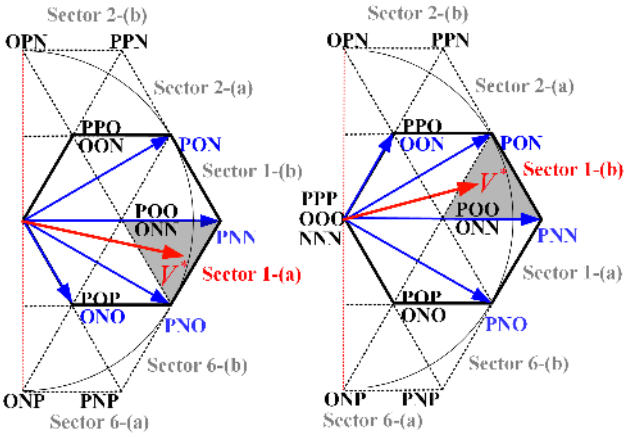

FIGURE 9. Sector segmentation and voltage vectors for generating the reference voltage in Method-I.

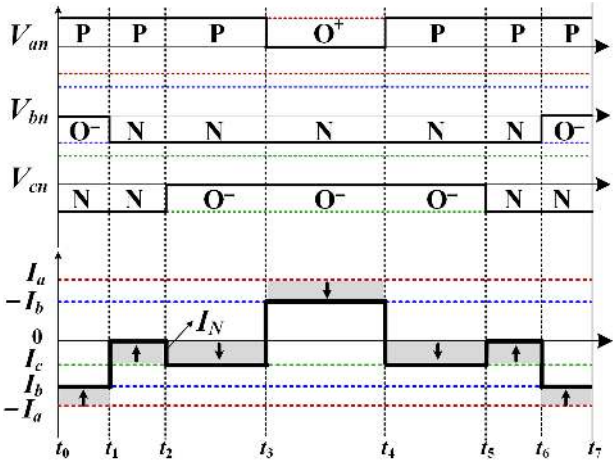

FIGURE 10. Reduction of neutral point current with a reconfigured switching sequence using the Method-I.

vectors. This is the same as replacing small vectors [PO$^-$O$^-$] and [O$^+$NN] with zero vector and large vector. When the proposed LMZVM is applied, the amount of change in CMV is reduced to $V_{DC}/3$.

In [26], for DC balance of DC-link capacitors, LMZVM and LMSVM are applied to some of Sector 1-(a). Fig. 11(b) shows CMV in Sector 1-(a) when the LMSVM used in [26] is applied. Even when the LMSVM used for DC voltage balance is applied, the change in CMV is $V_{DC}/6$.

Fig. 11(c) shows the CMV in Sector 1-(a) when a switching method proposed in [16] and [27]. In this switching method, [PO$^-$N] and [O$^+$NO$^-$] vectors are applied instead of [PO$^-$O$^-$] and [O$^+$NN] vectors in Sector 1-a, and accordingly, the change of CMV is reduced to $V_{DC}/6$ as well.

As the above analysis, the proposed method has the CMV reduction performance corresponding to that of the existing CMV reduction methods.

VI. SIMULATION RESULTS

The hybrid ANPC inverter was simulated using the PSIM software tool, and the simulation environment is shown in Table 3.

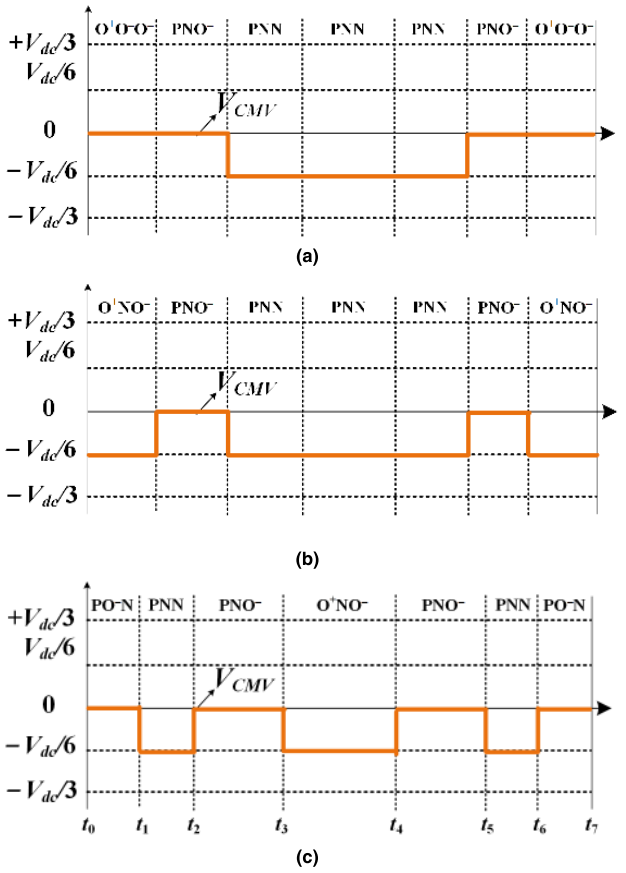

FIGURE 11. CMV reduction performance, (a) LMZVM, (b) LMSVM, (c) Method-I and the method in [27].

TABLE 3. Simulation specifications.

Parameter	Value
Rated power	15 [kW]
Grid voltage (line-to-line)	380 [V_{rms}]
Grid frequency	60 [Hz]
Switching frequency	30 [kHz]
DC-link voltage	600 [V]
DC-link capacitor	1000 [μF]
Filter inductor	1.5 [mH]

Fig. 12 provides the comparison between conventional SVPWM and the proposed method in terms of the output current, neutral point currents I_N, and gate signals of the IGBT and MOSFET. The neutral point current I_N is reduced from 5.82 A_{RMS} to 2.34 A_{RMS}, which represents a reduction of 58%. The THD of the three-phase current is changed from 1.10% to 2.32% after applying the proposed method. The THD characteristic is degraded when the proposed method is applied. In addition, the low and high switching operations of the IGBTs and MOSFETs in the hybrid ANPC are maintained even when the proposed method is applied.

Table 4 and 5 shows the specification and the comparison of capacitor lifetimes calculated using (3)-(5). In case of conventional SVPWM, $P_{loss,ESR}$ and $T_{hot-spot}$ are calculated

TABLE 4. Specification of DC-link Capacitor (DS138S).

Parameter	Value
Ambient temperature, T_a	60 [°C]
Allowable hot-spot temperature, T_0	105 [°C]
Equivalent thermal resistance, R_{ha}	6 [K/W]
ESR	105 [mΩ]
Rated lifetime, L_0	1.14 [years]

TABLE 5. Comparison of capacitor lifetimes.

Modulation method	Capacitor lifetime
Conventional SVPWM	19.78 [years]
Proposed switching scheme	32.61 [years]

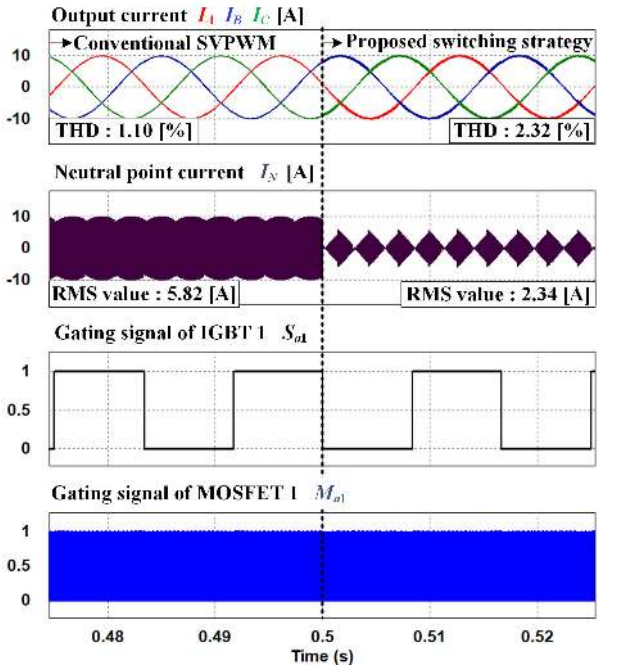

FIGURE 12. Output current, neutral point current, and gating signals with and without the proposed switching method.

as 1.76 W, and 70.52 °C when the simulation conditions of Table 3 is applied. In this case, the lifetime of the DC-link capacitor calculated by (5) is 19.78 years. When the proposed method is applied, $P_{loss,ESR}$ decreases to 0.31 W by reducing the neutral point current. Thus, the $T_{hot-spot}$ decreases to 61.88 °C. In this case, the lifetime of the capacitor increases to 32.61 years.

Fig. 13 shows the CMV of the hybrid ANPC inverter. The CMV has a magnitude ranging from –100 to 200 V and –200 to 100 V before applying the proposed switching

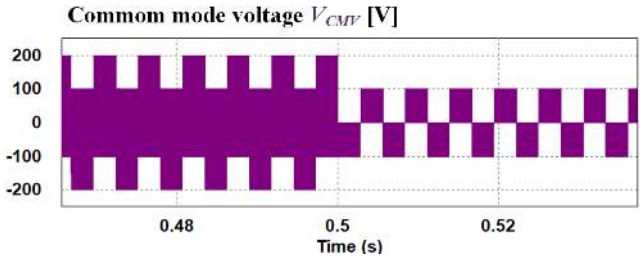

FIGURE 13. Comparison of CMV reduction performances.

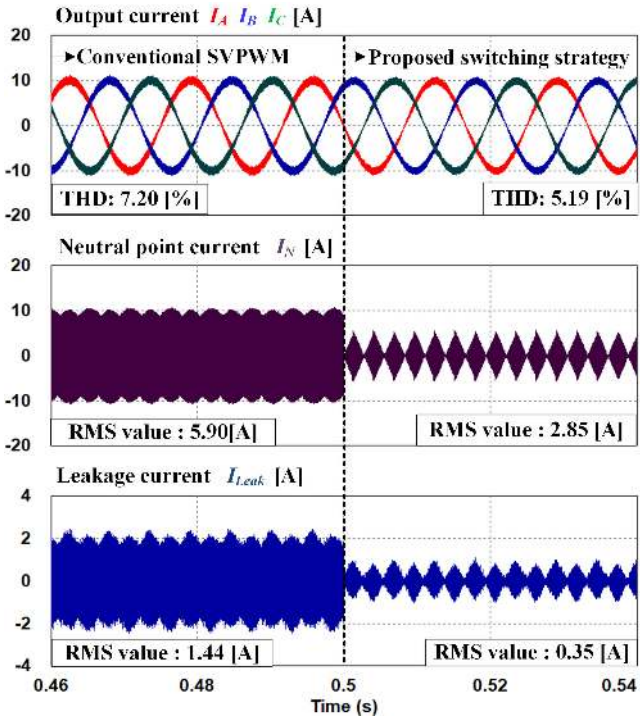

FIGURE 14. Output current and neutral point current when the leakage current is considered.

method. After applying the proposed method, the magnitude of the CMV varies from –100 to 0 V and 0 to 100 V.

Fig. 14 depicts the output currents, neutral point currents, and leakage currents before and after applying the proposed switching scheme. A leakage capacitor (0.3 μF) and a resistor (10 Ω) were installed to confirm the effect of the decrease in I_{Leak} due to the reduction of CMV. The output current before applying the proposed technique has a THD of 7.20% due to the leakage current flowing into the leakage capacitor. The RMS values of the neutral point current I_N and leakage current I_{Leak} are 5.90 A and 1.44 A, respectively. When the proposed method was applied, the leakage current was decreased by the reduction of the CMV. The RMS value at this time was 0.35 A, which was reduced by approximately 76% compared with the aforementioned value, and the THD of the output current was rather improved. Therefore, the proposed method is suitable for applications such as PV inverters having a leakage current.

Fig. 15 provides represents the line-to-line voltage with conventional SVPWM, Method-I and the proposed

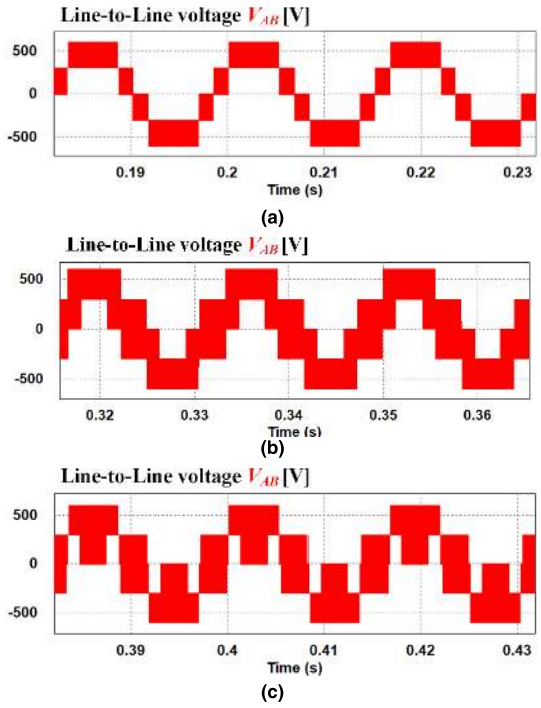

FIGURE 15. Simulation waveforms of line-to-line voltage, (a) Conventional SVPWM, (b) Method-I, (c) proposed switching method.

switching method. As shown in Fig. 15(a), the change of line-to-line voltage within one switching period is $V_{DC}/2$. When the Method-I is applied, the variation of the line-to-line voltage is increased to V_{DC} in some sections as shown in the Fig. 15(b). In addition, when applying the proposed switching method, the change of the line-to-line voltage also increases from $V_{DC}/2$ to V_{DC} in some sections as shown in Fig. 15(c). This causes an increase in output current THD. Although the quality of the output current is degraded, the blocking voltage of power switch is the same as the conventional SVPWM and the hot-spot temperature of the capacitor is reduced due to the reduction of the ripple current of the capacitor.

Fig. 16. shows the comparison of the performances for the reduction of I_N and CMV among conventional SVPWM, the switching method in [16] (Method-I), and the proposed method. Based on Sector 1-(a), Method-I replaces the [PO^-O^-] and [O^+NN] states with [PO^-N] and [O^+NO^-]. The replaced vectors cause the second largest current in Sector 1-(a) to flow to the neutral point. Method-I can reduce the DC-link ripple current by approximately 25%. It also reduces the peak-to-peak value of the CMV by 1/3 compared with conventional SVPWM in the case of a high modulation index (MI). Moreover, Method-I has a similar CMV reduction performance as the proposed method, but its I_N reduction performance is not sufficient. In addition, Method-I shows low performances for the reduction of the neutral point current and CMV in the case of low MI. In contrast, the proposed switching method maintains good performances for the reduction of I_N and CMV regardless of MI. Fig. 17 compares

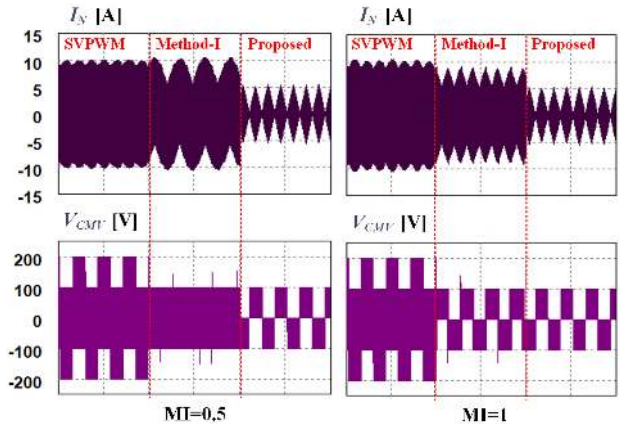

FIGURE 16. Neutral point current and CMV according to the switching method and MI.

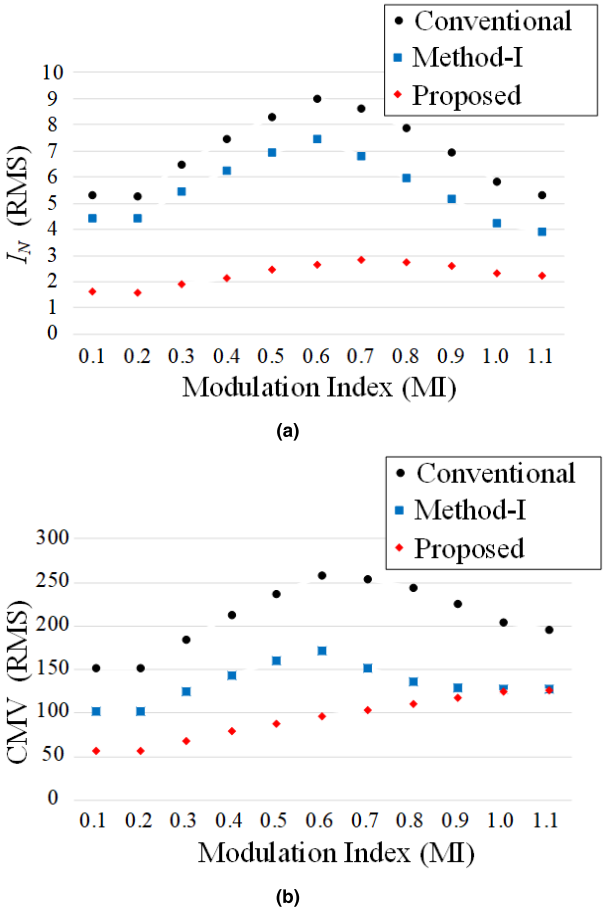

FIGURE 17. Comparison of performances for the reduction of neutral point current and CMV, (a) reduction of neutral point ripple current, (b) CMV reduction.

the performances for the reduction of I_N and CMV according to the switching method and MI.

Fig. 18 compares the I_N and CMV reduction performance according to the switching method and power factor (PF) angle. Simulation was performed with the MI set to 1.1. In the case of the proposed method, the outstanding I_N reduction performance was shown at the low PF angle, but the reduction

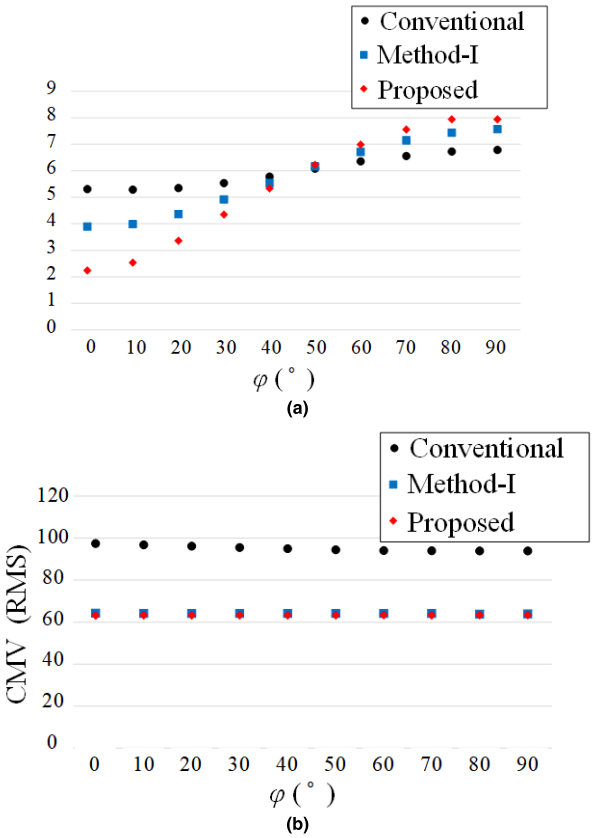

FIGURE 18. Comparison of performances for the reduction of neutral point current and CMV according to the PF angle, (a) neutral point ripple current, (b) CMV.

performance decreased as the PF angle increased. However, CMV reduction performance is maintained regardless of the power factor angle.

Fig. 19 shows the comparison of power losses between the conventional SVPWM and proposed switching method. As the analysis in Section V, even if the proposed method is applied, the number of switching and the dwelling time of the active voltage vector are the same as the conventional SVPWM. The power loss when before and after applying the proposed switching scheme are theoretically equivalent. As shown in Fig. 19(a) and (b), most of the switching losses are concentrated in the SiC MOSFET due to the special switching operation of the hybrid ANPC. The total loss that occurs in a leg is 9.53 W. When the proposed switching method is applied, the pattern of the loss distribution remains the same and the total loss is 9.55 W. This result indicates that the power loss of the proposed switching scheme is almost the same as the power loss of the conventional SVPWM.

VII. EXPERIMENTAL RESULTS

Experimental results were obtained using a prototype of the hybrid ANPC inverter to verify the proposed switching scheme. The hardware setup for the experiment is shown in Fig. 20, and the experimental environment is the same as the simulation environment shown in Table 3. The controller board is composed of the DSP (TMS320F28377S).

TABLE 6. Performance Comparison between the CMV Reduction Methods.

Switching method	Peak-to-peak value of CMV	Voltage level of line-to-line voltage	CMV fluctuation time within T_s	Simultaneous switching	Switching time within T_s
Conventional SVPWM	$V_{DC}/2$	5-level	6	N	6
[16], [27] (Method-I and CMV-R PWM)	$V_{DC}/6$	5-level, 3-level	6	N	6
[22], [23] (LMZVM)	$V_{DC}/6$	5-level, 3-level	2	Y	6
[26] (hybrid modulation)	$V_{DC}/6$	5-level, 3-level	2 or 4	Y	4 or 6
Proposed switching method	$V_{DC}/6$	5-level, 3-level	2	Y	6

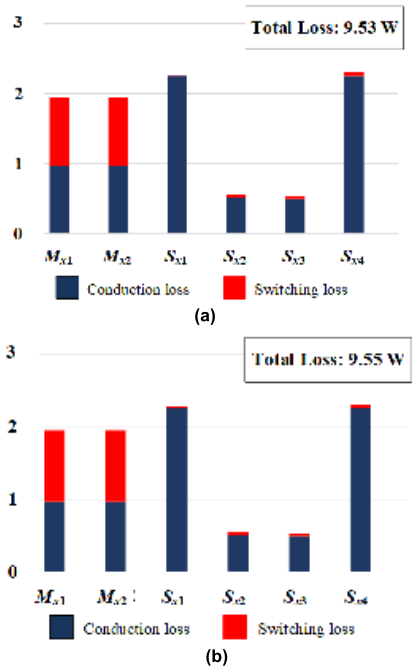

FIGURE 19. Comparison of power losses (a) conventional SVPWM, (b) proposed switching method.

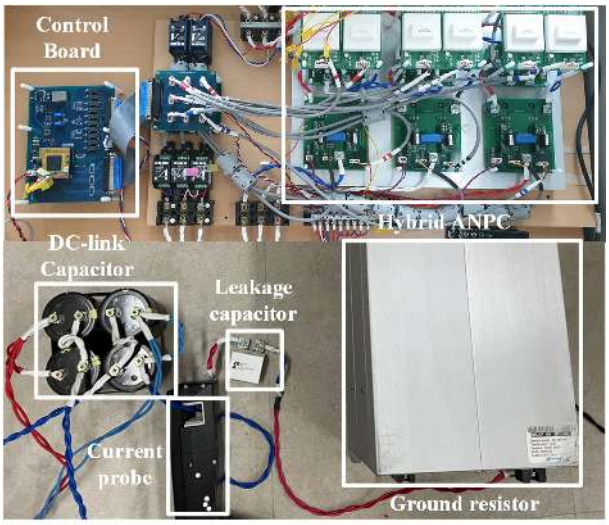

FIGURE 20. Experimental setup.

The Si-IGBTs in the hybrid ANPC inverter are implemented by using the SK75GBB066T which is an IGBT module made by Semikron. For the SiC MOSFETs, C2M0040120D made by CREE is used.

Fig. 21 shows the comparative result of the three-phase current and I_N. In Fig. 21(a), the RMS value of I_N is 6.10 A with conventional SVPWM. After applying the proposed switching method, the RMS value of I_N is considerably suppressed to 2.93 A_{RMS} in Fig. 21(b). The reduction ratio of I_N is consistent with that of the simulation. The quality of the output current is degraded by applying the proposed switching method. The THD of the output current increases from 1.3% to 2.6%.

Fig. 22 shows the experimental waveforms of the line-to-line voltage of switching methods. In the conventional SVPWM, the line-to-line has five level voltage. On the other hand, in Method-I and the proposed method, the voltage level in some sections decreases to three. Because of this effect, the THD of the output current increase. Therefore, an appropriate system filter design is required. However, the blocking voltage per power semiconductor is the same as the conventional SVPWM.

Fig. 23 shows the performance of the proposed switching method for the reduction of the leakage current I_{Leak} and CMV. To consider I_{Leak}, a leakage capacitor (0.3 μF) and a resistor (10 Ω) were connected between the bottom of the DC-link capacitor and the rear end of the load. It can be observed that I_{Leak} decreased with the reduction in the CMV by the proposed method. The peak-to-peak value of the CMV was suppressed from $V_{dc}/2$ to $V_{dc}/6$ as in the previous analysis and simulation results. Consequently, the RMS value of I_{Leak} was also reduced from 1.79 to 0.55 A, which indicates a reduction of 71%.

As shown in Fig. 24, in the case of conventional SVPWM, a high peak-to-peak value of CMV induced a large I_{Leak}, which deteriorated the quality of the current. The THD of the output current was 5.75%, and the RMS value of I_N was 6.11 A. When the proposed switching method was applied, the improvement of the THD of the output current with the reduction of I_{Leak} was more dominant than the deterioration of the THD of the switching technique itself. The THD of the current improved from 5.75% to 4.28% after applying the

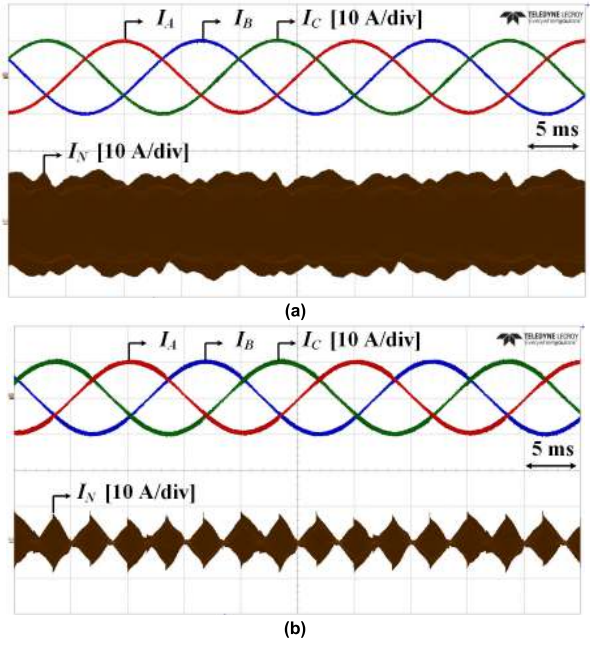

FIGURE 21. Experimental waveforms of the output current and neutral point current of (a) conventional SVPWM, (b) proposed switching method.

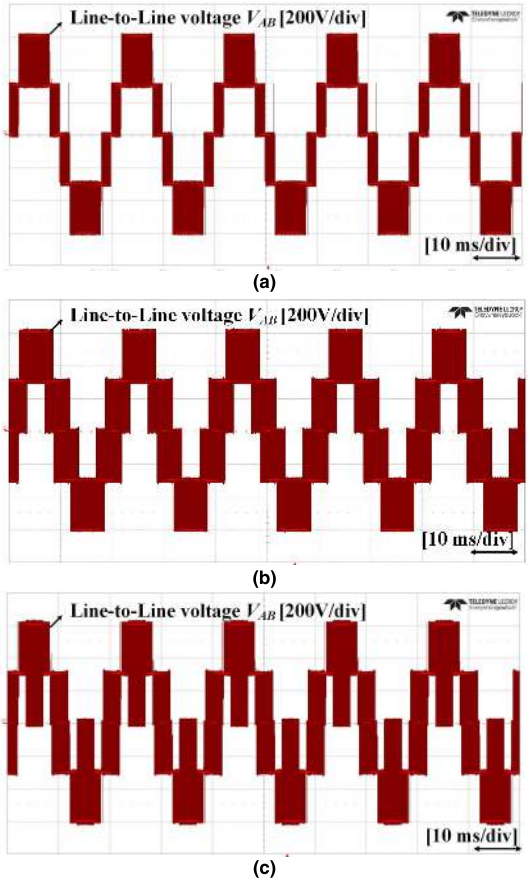

FIGURE 22. Experimental waveforms of the line-to-line voltage, (a) conventional SVPWM, (b) Method-I, (c) proposed switching method.

proposed method. Therefore, the proposed method is suitable for applications such as PV inverters.

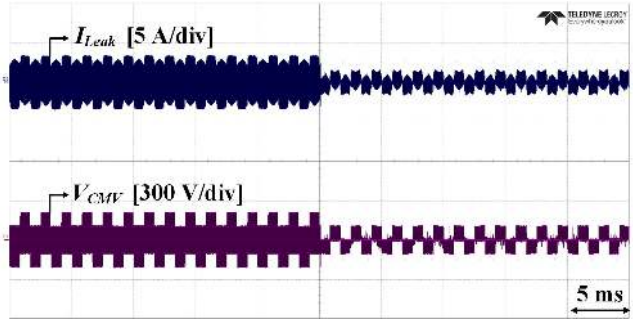

FIGURE 23. Experimental waveforms of the performances of the proposed switching method for the reduction of the leakage current and CMV.

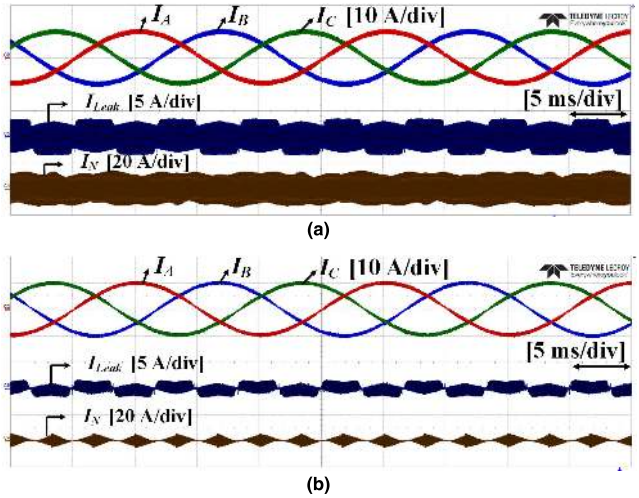

FIGURE 24. Experimental waveforms of the output current and neutral point current when the leakage current is considered, (a) conventional SVPWM, (b) proposed switching method.

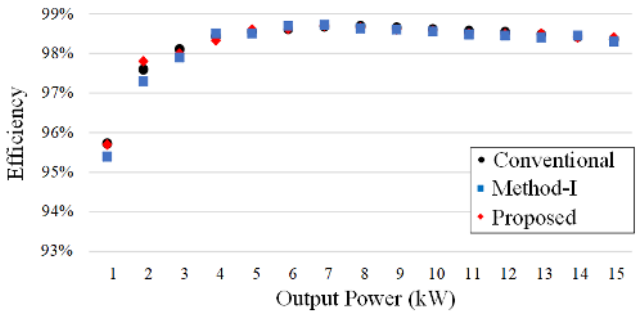

FIGURE 25. Experimental waveforms of the output current and neutral point current when the leakage current is considered.

Table 6 shows the performance comparison between the CMV reduction methods. All the CMV reduction methods reduce the peak-to-peak value of CMV to $V_{DC}/6$. However, all the methods have a disadvantage of voltage level reduction line voltage in some section which degrades the quality of the output currents. The LMZVM and proposed switching method have the minimum value of the CMV fluctuation time between the CMV reduction method. On the other hand,

since LMZVM and proposed method perform simultaneous switching, the quality of output current is worse than other methods.

Fig. 25 shows the result of efficiency test according to the type of the modulation methods. The efficiency test is implemented by using the power analyzer (WT3000) made by Yokogawa. In both Method-I and the proposed switching method, the power loss in the inverter is theoretically the same. This is because the dwelling time of the active voltage vector and the number of switching are the same. However, since the THD characteristic of the output current is degraded compared to the conventional SVPWM, the additional loss due to the harmonic currents. However, this loss occupies small ratio, and as the result of the actual efficiency test, the switching methods have almost the same efficiency.

VIII. CONCLUSION

This paper proposed a switching method for a hybrid ANPC inverter to reduce the DC-link ripple current and CMV. The switching states causing a large DC-link ripple current and high CMV were defined. The proposed switching method replaced the small vector causing a large neutral current and high CMV with other voltage vectors. The proposed switching method can be implemented through simple software programming. The proposed method also extends the service life of the capacitor approximately 1.7 times. In addition, when this method is applied to a PV inverter, the quality of the output current is improved with the reduction in the leakage current due to the reduced CMV. The validity and effectiveness of the proposed method were demonstrated through simulations and experimental results.

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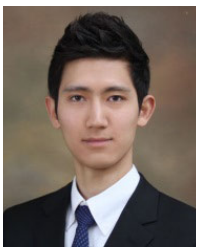

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