Capacity Limits and Matching Properties of Integrated Capacitors

Roberto Aparicio, *Student Member, IEEE,* and Ali Hajimiri, *Member, IEEE*

***Abstract*—Theoretical limits for the capacitance density of integrated capacitors with combined lateral and vertical field components are derived. These limits are used to investigate the efficiency of various capacitive structures such as lateral flux and quasifractal capacitors. This study leads to two new capacitor structures with high lateral-field efficiencies. These new capacitors demonstrate larger capacities, superior matching properties, tighter tolerances, and higher self-resonance frequencies than the standard horizontal parallel plate and previously reported lateral-field capacitors, while maintaining comparable quality factors. These superior qualities are verified by simulation and experimental results.**

***Index Terms*—Analog–digital conversion, calibration, capacitance measurement, capacitors, digital–analog conversion, fractals, integrated circuits, *LC* tank, passive circuits, resonators, sampled data circuits.**

I. Introduction

CAPACITORS are essential components in many integrated circuits, such as sample and holds, analog-to-digital (A/D) and digital-to-analog (D/A) converters, switched-capacitor and continuous-time filters, as well as many radio frequency (RF) building blocks. In many of these applications, capacitors consume a large fraction of the chip area. Therefore, capacitors with higher capacitance density are very desirable. In analog applications the other desired properties for capacitors are close matching of adjacent capacitors, linearity, small bottom-plate capacitor, and the absolute accuracy of the value (i.e., tolerance). In RF applications, it is essential for the capacitors to have self-resonance frequencies well in excess of the frequency of interest and large quality factors Q. Good linearity and large breakdown voltage are the other two desired properties for a good RF capacitor.

Several approaches have been taken to improve the area efficiency of capacitors. Nonlinear capacitors with high capacitance density such as junction or gate oxide capacitors have been used in applications where the linearity, breakdown voltage, and the quality factor Q are not important. Unfortunately, these capacitors need a dc bias and are strongly process and temperature dependent. Thus, in high precision circuits, such as data converters, their use is limited to bypass and coupling capacitors, or varactors in RF circuits.

On the other hand, metal-to-metal and metal-to-poly capacitors have very good linearity and quality factors. However, they suffer from a low capacitance density which mainly arises from the large metal-to-metal or metal-to-poly vertical spacing that determines the capacitance in the multiple parallel plate structure of Fig. 1. Unfortunately, in today's process technologies, this vertical spacing does not shrink as fast as the lateral separation to avoid excessive crosstalk between the digital metal lines in different layers. Thus, the parallel plate capacitors consume a larger fractional die area. Although an extra processing step to deposit a thin layer of insulator between two metal or poly layers can mitigate this problem [1], this extra step is not available in many of the standard silicon-based technologies. Even if such special capacitor layers were available, the parallel plate structure does not necessarily result in the highest possible capacitance density, as will be shown later in this paper.

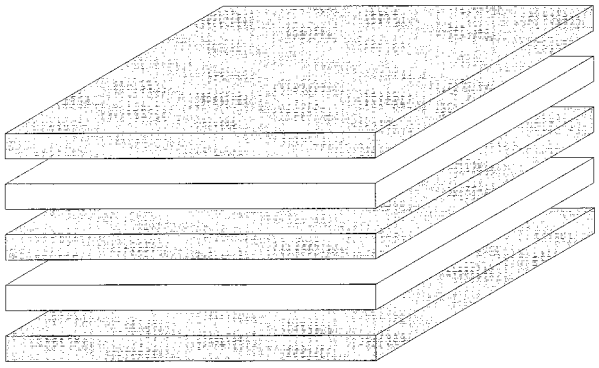

Fig. 1. Parallel plate capacitor.

The capacitance density can be improved by exploiting both lateral and vertical electric field components. A well-known example of such structures is the interdigital or *parallel wires* (PW) structure shown in Fig. 2 [2]–[6]. Recently, several new structures, such as *quasifractal* and *woven* structures were suggested as methods of obtaining higher capacitance per unit area [5]. These structures essentially demonstrate the same linearity as parallel plate metal-to-metal and metal-to-poly capacitors but with higher capacitance densities. They also provide lower bottom-plate capacitance since more field lines terminate on the adjacent metal lines as opposed to the substrate.

Despite these advantages, lateral-flux and quasifractal capacitors have not been widely used in the signal path of analog circuits, as predicting their absolute value can be complicated and time-consuming. Also, it is not clear if they are always advantageous over the more regular structures such as the parallel wires structure shown in Fig. 2. This paper addresses some of these issues by focusing on the fundamental properties of the capacitance densities of integrated capacitors. Section II illustrates some of the improvements in other properties of integrated capacitors, due to higher capacitance density. In Section III, it is shown that the density of any arbitrary capacitor can be decomposed as the

Manuscript received July 23, 2001; revised October 19, 2001.

The authors are with the California Institute of Technology, Pasadena, CA 91125 USA (e-mail: aparicio@its.caltech.edu).

Publisher Item Identifier S 0018-9200(02)01684-0.

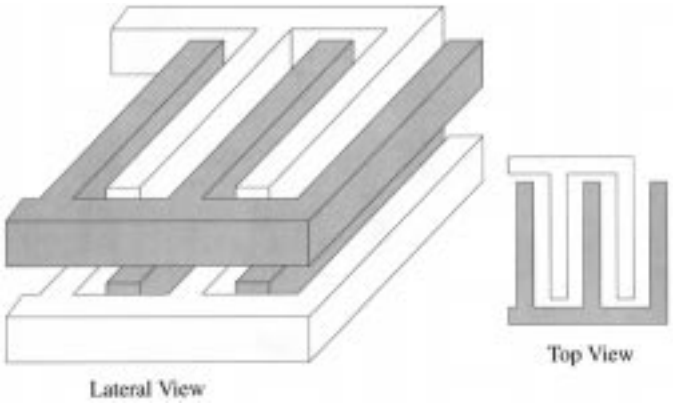

Fig. 2. Parallel wires configuration.

sum of the individual capacitance contributions of the lateral and vertical electric field components. This decomposition will be used to derive new theoretical limits for the capacitance density of integrated capacitors. These theoretical limits lead to two new capacitor structures introduced in Section IV. These new capacitors demonstrate superior densities, matching, tolerances, and self-resonance frequencies when compared to previously reported lateral-field and quasifractal capacitors, while maintaining a comparable quality factor. The superior capacitance density of the new structures will be corroborated in Section V. Finally, in Section VI, experimental results verify the superior area efficiency, higher self-resonance frequency, tighter tolerance, and better matching properties of these new capacitors.

II. Effect of Density on Other Capacitor Properties

A higher capacitance density and hence a smaller physical size for a given capacitance will automatically result in a few important improvements in other properties of the capacitor. This higher capacitance density can be achieved in many different ways, such as using a material with higher dielectric constant [1] or using the lateral field components [2]–[8]. For a given capacitor value, smaller physical dimensions will result in a smaller series inductance, since the average ac current path is shorter. Hence, a higher self-resonance frequency can be obtained. Also, a smaller area usually translates to shorter metal lengths which in turn result in a smaller series resistance and therefore, a higher quality factor Q. The bottom-plate capacitance also shrinks automatically in a capacitor with a smaller area due to the smaller area of the bottom plate itself. On the other hand, it is generally believed that a capacitor with a smaller size usually results in a larger fractional variations in the exact value of the capacitor. We will investigate the validity of these statements experimentally in Section VI.

It has been proposed to use lateral field components to enhance the capacity of the standard parallel plate structure shown in Fig. 1 [2]–[8]. Lateral electric fields are particularly useful as the minimum lateral spacing of metal layers shrinks quickly with process scaling, while the vertical spacing does not scale down as fast. Interdigitated structures similar to those shown in Fig. 2 have been proposed to enhance the density and lower the bottom plate capacitance [2]–[6]. These structures combine the lateral and vertical field components very tightly. This has an undesirable effect on the matching properties of the capacitor, as will be demonstrated later in this paper, and thus should be avoided.

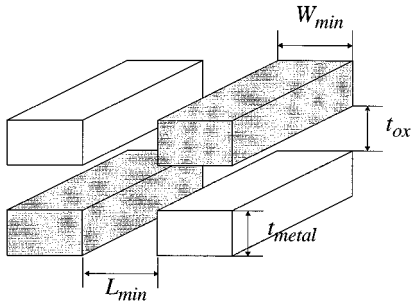

Fig. 3. Dimensions of the metal lines.

Increasing the periphery of a lateral field capacitor has been suggested as a means to enhance the capacitance density [5]. Quasifractal structures have been considered as one such alternative. Unfortunately, these structures are time consuming to generate. Furthermore, they are difficult to predict and simulate in a time-efficient manner. They also suffer from the same strong coupling between the vertical and lateral field components which can degrade their matching and tolerance, as will be discussed later.

From these different approaches to capacitance optimization, it is not clear which structure results in the best capacitors. Therefore, it is essential to form a deeper understanding of the underlying capacity limits for integrated capacitors to be able to identify the best capacitive structure for any given application. We study these limits in the following section.

III. Capacity Limits

To gain more insight into the tradeoffs in using the lateral and vertical field components, we now set the basis for the capacitance decomposition, starting from the relationships between the capacitance and the electric field in three dimensions. This decomposition leads to theoretical upper bounds on the maximum capacitance of rectangular (*Manhattan*) structures. This can be done by noting that the total electrostatic energy U_E in a capacitor C is given by

$$U_E = \frac{C \cdot \Delta V^2}{2} \tag{1}$$

where ΔV is the voltage drop across its two terminals. The capacitance of an arbitrary structure can be calculated by integrating the electrostatic energy density u over the entire dielectric volume to obtain the total stored electrostatic energy U_E for a given voltage drop ΔV between the two terminals of the capacitor, i.e.

$$C = \frac{2 \cdot U_E}{\Delta V^2} = \frac{2}{\Delta V^2} \int_{\mathrm{Vol}} u(\boldsymbol{r})\, dv \tag{2}$$

where $\boldsymbol{r}$ is the position vector and dv is the differential unit of volume. For an isotropic dielectric material, the electrostatic energy density is given by

$$\begin{aligned} u(\boldsymbol{r}) &= \frac{\boldsymbol{E}(\boldsymbol{r}) \cdot \boldsymbol{D}(\boldsymbol{r})}{2} \\ &= \frac{\varepsilon_r \varepsilon_0}{2} \boldsymbol{E}^2(\boldsymbol{r}) \\ &= \frac{\varepsilon_r \varepsilon_0}{2} \left[E_x^2(\boldsymbol{r}) + E_y^2(\boldsymbol{r}) + E_z^2(\boldsymbol{r})\right] \\ &= u_x(\boldsymbol{r}) + u_y(\boldsymbol{r}) + u_z(\boldsymbol{r}) \end{aligned} \tag{3}$$

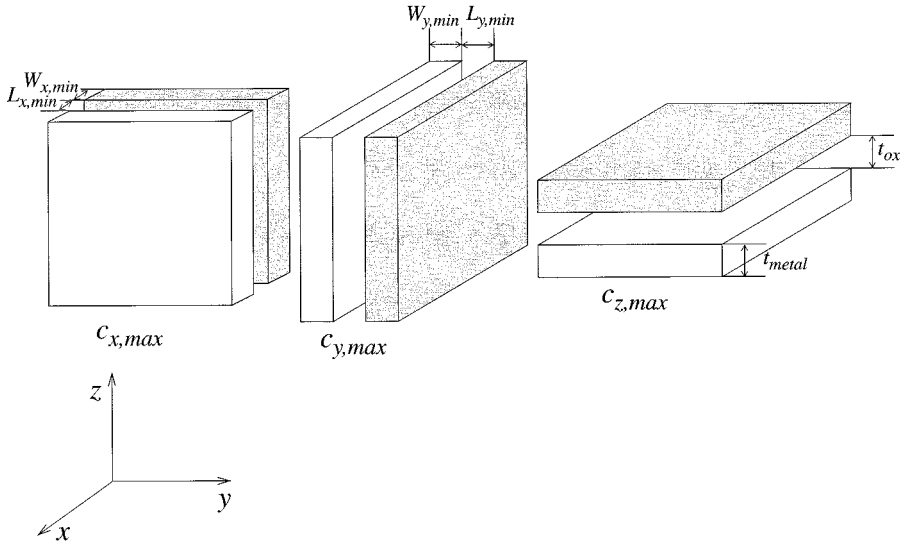

Fig. 4. Parallel plate structures normal to the Cartesian axis.

where $\boldsymbol{E}$ and $\boldsymbol{D}$ are the electric and displacement vectors, ε_0 is the permittivity of free space, ε_r is the relative permittivity of the dielectric, and u_x, u_y, and u_z are the electrostatic energy densities due to the electric field components along the three Cartesian axes, namely, E_x, E_y, and E_z, respectively. Therefore, the density (capacitance per unit volume) can be calculated by integrating the sum of the three electrostatic field energy density components over the dielectric volume, i.e.

$$c = \frac{C}{\text{Vol}} = \frac{1}{\text{Vol}} \cdot \frac{2}{\Delta V^2}\left[\int_{\text{Vol}} u_x(\boldsymbol{r})\,dv + \int_{\text{Vol}} u_y(\boldsymbol{r})\,dv + \int_{\text{Vol}} u_z(\boldsymbol{r})\,dv\right] = c_x + c_y + c_z \quad (4)$$

where c is the capacitance density of the structure (in Farads per cubic meter) and c_x, c_y, and c_z are the capacitance densities due to the electric field components E_x, E_y, and E_z, respectively.

As mentioned earlier, we are interested in maximizing the capacitance density c for integrated capacitor structures. Let us consider a process technology with a minimum lateral spacing of $L_{\min}$, minimum metal width of $W_{\min}$, a vertical spacing between two adjacent metal layers t_{ox}, and a metal thickness t_{metal}, as shown in Fig. 3. We would like to determine the maximum achievable capacitance density c for such process technology.

The total capacitance density c cannot exceed the sum of the maximums of its individual components, namely, $c_{x,\max}$, $c_{y,\max}$, and $c_{z,\max}$. In other words, we have to maximize the capacitance density due to each component of the electric field separately, to obtain an upper bound on the density.

We can maximize the capacitance contribution of the electric field along the x axis, c_x, (with no constraint on the contributions of other field components) by using a parallel plate structure with minimum plate width $W_{x,\min}$ and minimum spacing $L_{x,\min}$, perpendicular to the x axis. The capacitive components along the y and z axes can be maximized in a similar fashion by using minimum spacing and minimum width parallel plate structures normal to these axes, as shown in Fig. 4. Therefore, an upper bound on the total capacitance density can be obtained by adding the individual maximums of the capacitance density components, i.e.

$$\begin{aligned} c_{\max} &= c_{x,\max} + c_{y,\max} + c_{z,\max} \\ &= \varepsilon_r\varepsilon_o\left[\frac{1}{L_{x,\min}(L_{x,\min}+W_{x,\min})} + \frac{1}{L_{y,\min}(L_{y,\min}+W_{y,\min})} + \frac{1}{t_{\text{ox}}(t_{\text{ox}}+t_{\text{metal}})}\right] \end{aligned} \quad (5)$$

where $L_{x,\min}$, $L_{y,\min}$, $W_{x,\min}$, and $W_{y,\min}$ represent the minimum lateral spacing and metal width along the x and y axis, respectively. Equation (5) reduces to

$$c_{\max} = \varepsilon_r\varepsilon_0\left[\frac{2}{L_{\min}(L_{\min}+W_{\min})} + \frac{1}{t_{\text{ox}}(t_{\text{ox}}+t_{\text{metal}})}\right] \quad (6)$$

for $L_{x,\min} = L_{y,\min} \equiv L_{\min}$ and $W_{x,\min} = W_{y,\min} \equiv W_{\min}$, which is often the case. This is a capacitance per unit volume, and can be easily translated to capacitance per unit area for a known number of metal layers. This maximum in the capacitance density will be referred to as *Theoretical Limit 1* (TL1). A tighter upper bound on the capacitance density, referred to as *Semi-Empirical Upper Bound*, will be introduced in the Appendix.

These theoretical limits can be very helpful for integrated circuit designers, as they set an upper bound for the minimum attainable die area for a given value of capacitance and for a specific process technology. In practice, for a given capacitive structure, c_x, c_y, and c_z are correlated and cannot be maximized all at the same time, therefore, the ratios of the capacitance density of any given structure to these theoretical limits can be defined as figures of merit for the capacitor of interest and used for comparison of various structures.

IV. Purely Lateral Field Capacitive Structures

The theoretical limit shown in (6) demonstrates an inverse square law dependence on the minimum lateral and vertical dimensions of the process technology. In today's standard process

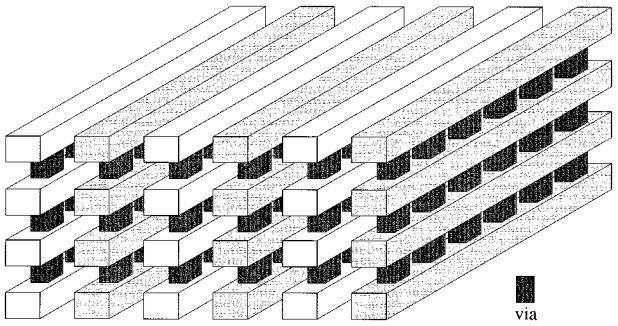

Fig. 5. Vertical parallel plates structure.

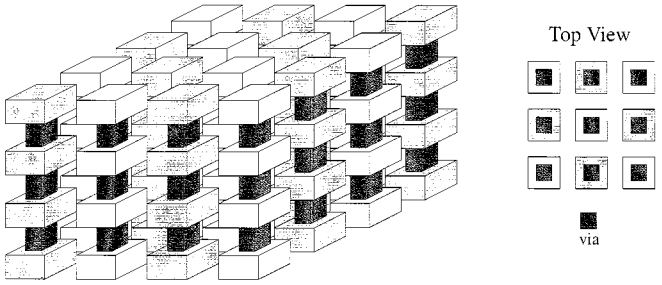

Fig. 6. Vertical bars structure.

technologies, the minimum lateral dimensions, $L_{\min}$ and $W_{\min}$, are smaller than the vertical dimensions, $t_{\rm ox}$ and $t_{\rm metal}$. Therefore, in properly designed capacitors the lateral component of the capacitance density should be the dominant contributor to the overall density. Furthermore, this maximization of the lateral field component leads to further improvements in the density with process technology advancements. Additionally, the processes used in the back-end metallization allow the lateral dimensions to be controlled more accurate and repeatable (e.g., lithography and etching) when compared to the vertical dimensions (e.g., deposition).

Therefore, (6) directs us in the direction of structures with purely lateral capacitance component and no vertical component. Fig. 5 shows the first of these structures, called vertical parallel plates (VPP) [7], [8]. It consists of metal slabs connected vertically using multiple vias to form vertical plates. This structure takes full advantage of the lateral dimension scaling. Note that different shadings are used to distinguish the two terminals of the capacitor throughout this paper.

It is noteworthy that while each via may present a reasonably large series resistance, a large number of them are connected in parallel in each plate. This large number of parallel small capacitors will reduce the series resistance significantly, which in turn, will reduce the loss of the structure. In other words, very little ac current flows through each via, reducing the effective series resistance of the capacitor. This statement will be verified experimentally in Section VI.

Although the fabrication of the VPP structure relies on stacked vias which may not be available in all process technologies, close approximations to this structure can be fabricated by interleaving vias. Also, long electromagnetic capacitance simulations are rather unnecessary as the capacitance of the VPP structure can be predicted using simple expressions for parallel plate structures with fringing [9].

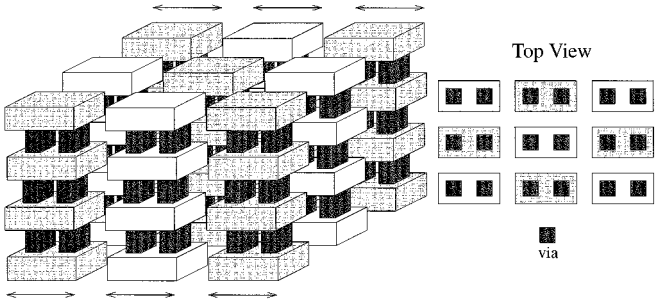

Fig. 7. Modified vertical bars structure.

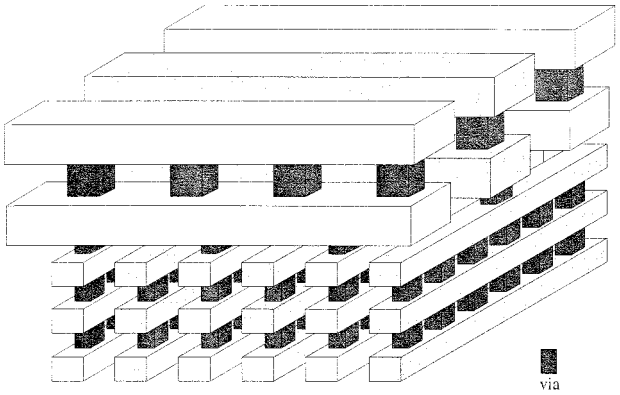

Fig. 8. Modified vertical parallel plates structure.

We can take this maximization one step further by using both lateral dimensions in the vertical bars structure (VB) shown in Fig. 6 [7], [8]. It consists of vertical bars made out of metal squares and vias. The length of the bars is limited by the number and thickness of metal layers. This structure utilizes the electric field in both lateral dimensions and has even higher capacitance density than the VPP structure. In practice, the interconnection of the bars to the terminals of the capacitor require the use of at least one metal layer, reducing the effective volume of the capacitor. Therefore, in certain process technologies the overall capacitance of the VB structure will be smaller than that of the VPP.

The VB structure can show a larger series resistance compared to the VPP capacitor. However, the series resistance of the VB structure is mainly determined by the via resistance. Again, a large number of small capacitors in parallel form the total capacitance and hence the overall series resistance is the parallel combination of these resistors, which will be much smaller than an individual via. The choice between VPP and VB will depend on the application. A compromise between the higher quality factor of the VPP and the larger capacitance density of the VB structures can be achieved by extending the widths of the vertical bars in one dimension, as shown in Fig. 7. In the limiting case, this intermediate structure will become the VPP capacitor.

In some process technologies, the minimum lateral spacing between different metal layers may vary significantly. To achieve the highest capacitance density in such processes, we can use a modified version of the VPP structure, shown in Fig. 8. This structure consists of multiple vertical parallel plate capacitors placed orthogonally and connected through interleaved vias. In the limiting case, it reduces to the woven structure [5] discussed in the next section. This configuration takes advantage of all the available metal layers and hence

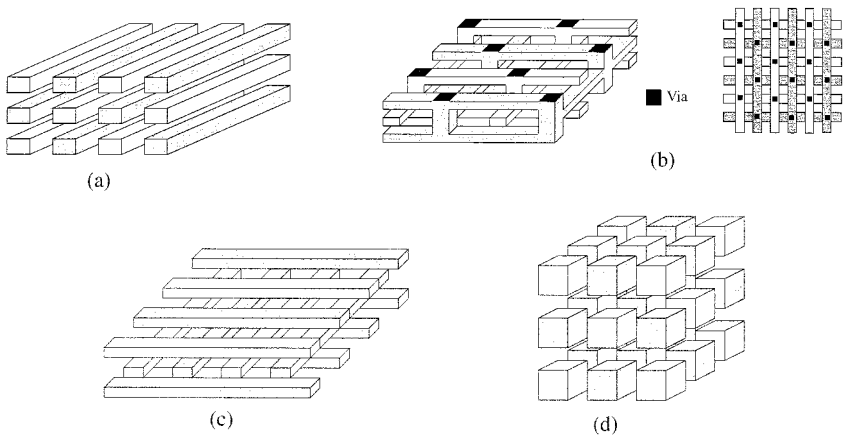

Fig. 9. Manhattan capacitor structures. (a) Parallel wires (PW). (b) Woven. (c) Woven no via. (d) Cubes 3D.

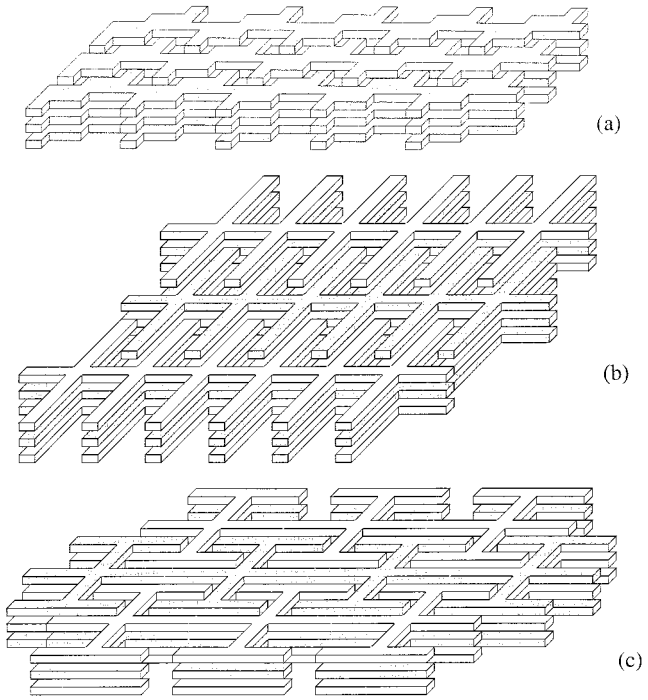

Fig. 10. Quasifractal capacitor structures.

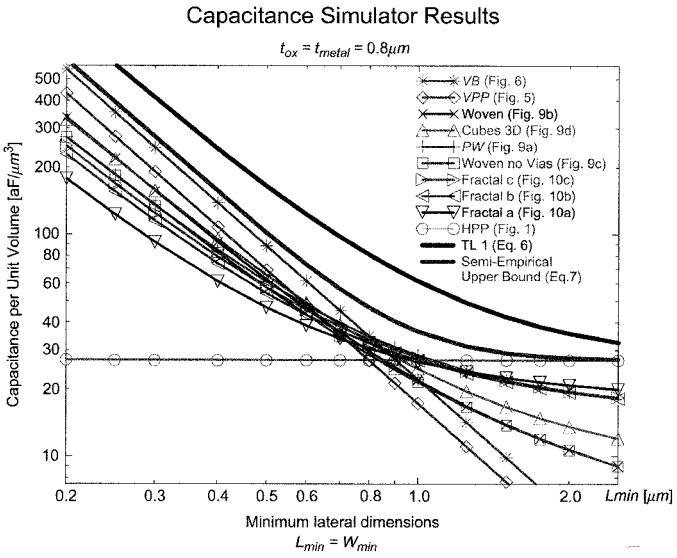

Fig. 11. Capacitance density versus minimum lateral dimensions for $t_{ox} = t_{\mathrm{metal}} = 0.8\ \mu$m.

achieves higher capacitance density, at the extra cost of combining vertical fields which will degrade the matching properties of the structure, as will be seen next.

The value of the standard parallel plate capacitor of Fig. 1 is primarily determined by the oxide thickness. On the other hand, the exact values of the VPP and VB capacitors are determined by lithography and etching. These two processes are quite accurate in today's process technologies. It is therefore reasonable to suspect that the lateral component of the capacitor should be more repeatable and have a smaller variation across the wafer. In this case, it is clear that any structure combining the lateral and vertical field components will suffer from the worse accuracy of the vertical capacitance component, which will lead to inferior matching and tolerance properties. Practically, all of the existing integrated capacitive structures use the vertical fields and hence cannot achieve the best possible accuracy. This hypothesis will be verified in Section VI.

V. Capacitance Comparison

In this section, we will demonstrate the superior capacitance density of the new proposed structures through capacitance simulations. Several previously known structures which exploit lateral and vertical fields will be compared to the VPP and VB structures under different conditions.

Some of the more uniform structures, which we will refer to as lateral flux capacitors, are shown in Fig. 9. Three examples of structures using more random patterns mostly inspired by fractal geometries that will be referred to as quasifractal structures after [5] are depicted in Fig. 10. While not exclusive, the structures in Figs. 9 and 10 are chosen to reflect a wide range of possible rectangular (Manhattan) geometries alternatives to the horizontal parallel plate of Fig. 1.

Fig. 9(a) shows the interdigitated metal slabs or parallel wires used for high-frequency bypassing and coupling in integrated circuits [10]–[14]. Fig. 9(b) shows the top view and the three-dimensional (3D) perspective of the woven structure mentioned in [5]. A no-via variation of this structure is illustrated in Fig. 9(c) for comparison purposes. This structure will be mainly used

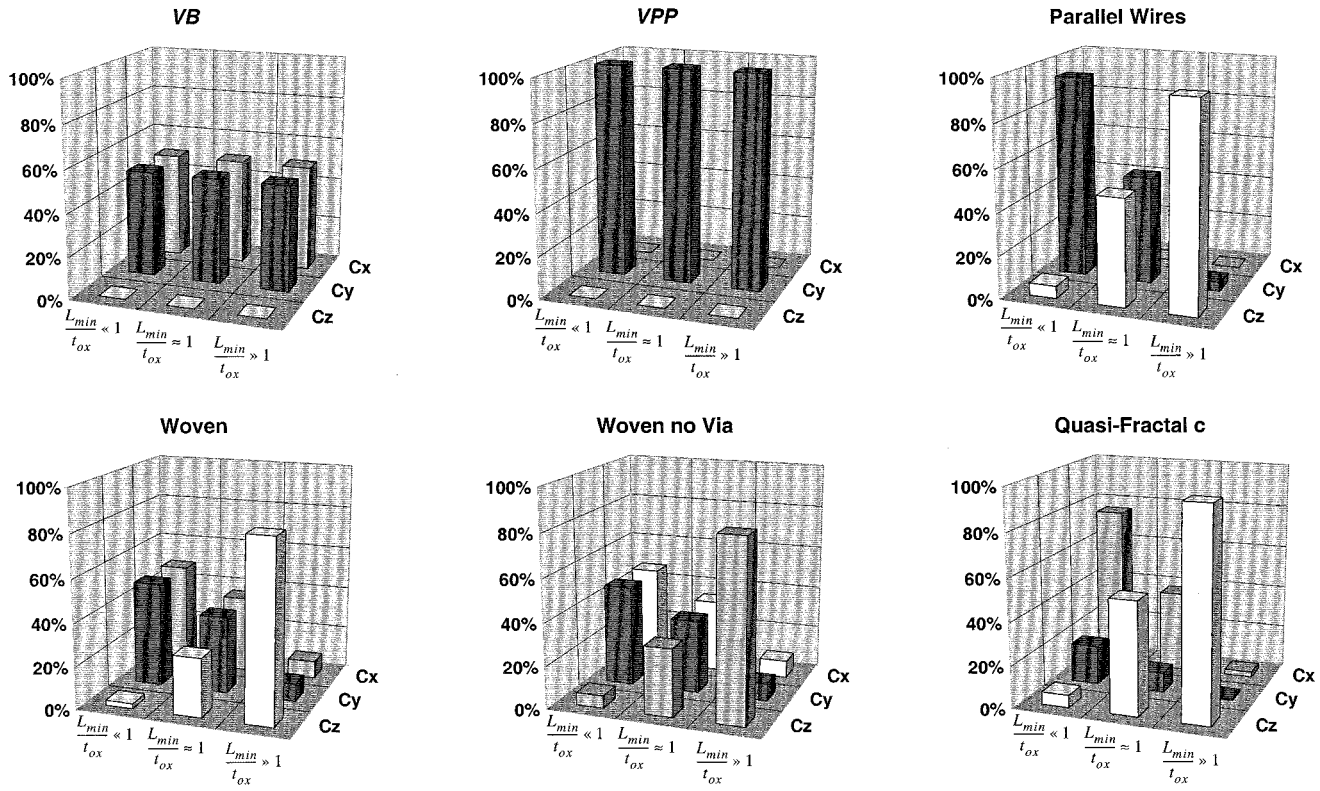

Fig. 12. Field usage efficiencies for $L_{\min}/t_{\rm ox} \ll 1$, $L_{\min}/t_{\rm ox} = 1$ and $L_{\min}/t_{\rm ox} \gg 1$.

to determine the effect of vias in the regular woven structure. Fig. 9(d) depicts minimum-sized cubes spaced at minimum lateral spacing and cross-connected three-dimensionally to maximize the fringe fields. It is noteworthy that this structure is only used for comparison and cannot be fabricated in reality due to lack of means to maintain every other cube at the same potential.

As mentioned before, the structures in Fig. 10 are intended to imitate segments of quasifractal structures. The structure in Fig. 10(a) is aimed at maximizing the vertical field usage, enhanced by moderate lateral fields. On the other hand, the capacitive structures of Fig. 10(b) and (c) are more aggressive with the lateral field and try to use both vertical and lateral fields more equally.

To simulate the capacitance densities of the capacitive metal configurations of Figs. 9 and 10, as well as the two new proposed structures, we have developed a special purpose field solver working based on an enhanced relaxation algorithm [15].

In the first set of simulations, both $t_{\rm ox}$ and $t_{\rm metal}$ are kept constant at 0.8 μm. It is also assumed that $L_{\min} = W_{\min}$. The equality of $L_{\min}$ and $W_{\min}$ is common in contemporary process technologies and hence will be used in this comparison. The simulation results showing the capacitance density per unit volume versus the minimum lateral spacing, $L_{\min}$, for the structures of Figs. 1, 5, 6, 9, and 10 are depicted in Fig. 11. Although this graph is for a $t_{\rm ox}$ and $t_{\rm metal}$ of 0.8 μm, it can be easily used for other vertical spacings through a simple scaling, as long as $t_{\rm ox} = t_{\rm metal}$ and $L_{\min} = W_{\min}$. This property can be traced back to the scale invariance of electrostatic equations [16].

It is instructive to investigate the behavior of the capacitance density for very small and very large lateral spacings in Fig. 11. For large lateral spacings (right-hand side of the graph), the capacitance densities reach plateaux as the lateral fields become inconsequential and the capacitance is dominated by the vertical fields. The horizontal parallel plate structure of Fig. 1, has the best performance in this region due to its optimal usage of vertical fields. Also note that the capacitance densities of the VPP and VB structures continuously diminish due to the lack of any vertical field component. Other structures fall in between these two extremes and reach a capacity limit controlled by their vertical-to-lateral field usage efficiency.

At the other extreme, when the minimum lateral spacing becomes much smaller than the vertical separation (left-hand side of the graph), the capacitance density becomes inversely proportional to $L_{\rm min}^2$ because the lateral plate spacing decreases linearly with $L_{\min}$ resulting in a linear increase in the capacitance per plate. Also, the number of plates per unit volume grows linearly with decreasing $L_{\min}$ due to smaller metal width and spacing. This dual dependence results in an inverse $L_{\rm min}^2$ dependence, as predicted by (6). In this region, the VB structure shows the maximum capacitance density followed by the VPP structure due to their optimum usage of lateral fields. The later structure benefits from shrinking in one lateral-dimension only, while the former makes the most of the two lateral-dimensions shrinkage. On the other hand, the horizontal parallel plate structure has the worst performance in this region, due to lack of any lateral-field components. It is also noted that the vias enhance the lateral-flux density in the dielectric/oxide inter-layer separa-

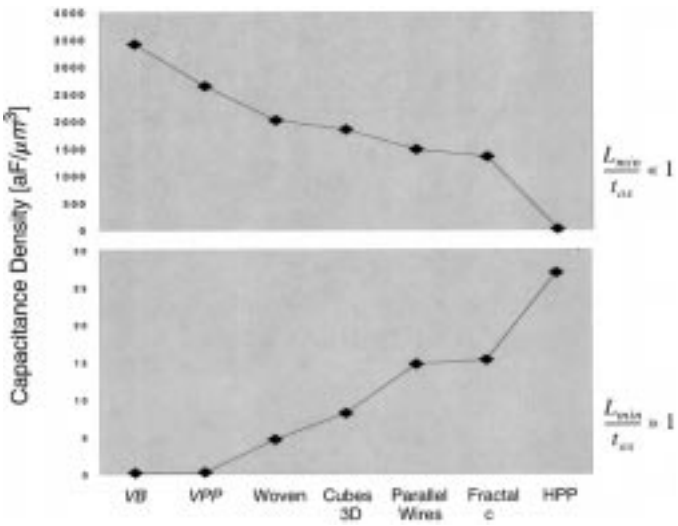

Fig. 13. Capacitance densities for $L_{\min}/t_{\rm ox} \ll 1$ and $L_{\min}/t_{\rm ox} \gg 1$.

tion. As an example, the woven structure of Fig. 9(b) shows an advantage over that of Fig. 9(c), due to the lateral field enhancement caused by the vias. This is another very important characteristic of the two new proposed structures, as they use vias that maximize the lateral field usage in the vertical inter-layer dielectric separation between different metal layers.

To gain more insight into the contributions of the capacitance components to the overall density, the *field usage efficiency* of different structures are plotted in three different regions of the $L_{\min}/t_{\rm ox}$ ratios in Fig. 12. Field usage efficiency can be defined as the ratio of each of c_x, c_y, and c_z to the total capacitance density, which represent the percentage of energy stored in each component of the electric field. For the $L_{\min}/t_{\rm ox} \ll 1$ region, the lateral components are the main contributor to the total capacitance. In contrast, for the $L_{\min}/t_{\rm ox} \gg 1$ region, the vertical component forms the main portion of the total capacitance. To visualize this tradeoff further, the capacitance density of different structures are plotted in Fig. 13 for the $L_{\min}/t_{\rm ox} \ll 1$ and $L_{\min}/t_{\rm ox} \gg 1$ regions. Interestingly, the order almost completely reverses when going from small to large $L_{\min}/t_{\rm ox}$ ratios, i.e., the best structures become the *worst* and vise versa. This can be explained by the inherent tradeoff between lateral and vertical field utilization, as lateral field usage can only be increased by introducing dielectric regions between metal lines in the same layer, which in turn results in loss of some vertical component.

Finally, Table I compares the simulated capacitance densities of all the structures discussed so far. These results are normalized to the Theoretical Limit 1 and semi-empirical upper bound, and are considered for $L_{\min} = W_{\min} = 0.1$ μm and $t_{\rm ox} = t_{\rm metal} = 1$ μm (or for any other case where the minimum lateral dimensions are ten times smaller than the vertical dimensions). As can be seen, the two new proposed structures attain the highest capacitance density among these structures. The VB and VPP achieve a capacitance density of 91% and 71% when compared to the semi-empirical upper bound, respectively, while the woven and quasifractal structures attain 54% and 25%, respectively.

TABLE I
CAPACITANCE COMPARISON

Structure	Ratio to *TL1*	Ratio to *Semi-Empirical Upper Bound*
VB	64%	91%
VPP	50%	71%
Woven	38%	54%
Cubes 3-D	35%	49%
Parallel Wires	28%	40%
Woven no vias	28%	40%
Quasifractal c	25%	36%
Quasifractal b	23%	33%
Quasifractal a	18%	25%
HPP	0.5%	0.7%

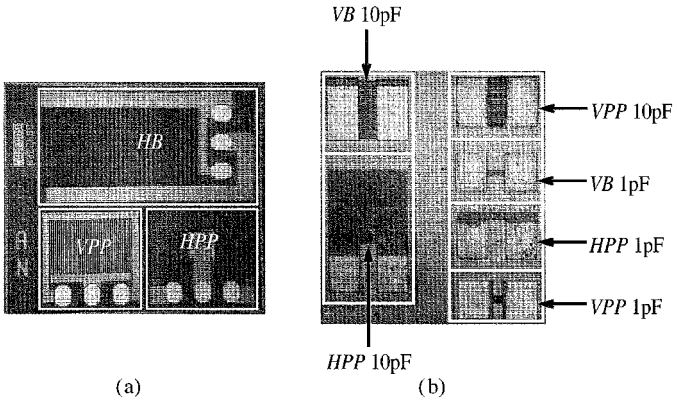

Fig. 14. Die micrographs of the test capacitors. (a) First set for $L_{\min} = W_{\min} = 0.5$ μm. (b) Second set for $L_{\min} = W_{\min} = 0.24$ μm.

VI. MEASUREMENT RESULTS

Two sets of test capacitors were fabricated in two different process technologies. The first set of test capacitors were fabricated in a 3-metal layer process with two thin metal layers and an additional thick metal layer. For this process, the dielectric material is silicon dioxide and the metal material is aluminum. The two lower metal layers have $L_{\min} = W_{\min} = 0.5$ μm, $t_{\rm ox} = 0.95$ μm, and $t_{\rm metal} = 0.63$ μm. The fabricated structures in this process include the VPP (Fig. 5), interdigitated or parallel wires (Fig. 2) and horizontal parallel plate (HPP) (Fig. 1) capacitors that occupy 0.12 mm^2, 0.33 mm^2, and 0.19 mm^2, respectively, as shown in Fig. 14(a). The performance numbers for these structures are summarized in Table II. The VPP capacitor achieves a factor of 4.4 capacitance density improvement over the standard HPP using only two metal layers, but also *for equal capacitance values* demonstrate a higher self-resonance frequency than the HPP structure. This is based on the size-normalized self-resonance frequencies of the structures listed in Table II. In terms of series resistance, the VPP capacitor has a series resistance r_s of 0.57 Ω comparable to r_s of 1.1 and 0.55 Ω for the HPP and PW capacitors, respectively. It is noteworthy that the commonly used interdigitated (or PW) structure of Fig. 2 is inferior to the newly introduced VPP capacitor, in capacitance density, quality factor, and self-resonance frequency.

To investigate the tolerance properties of the VPP capacitor, the capacitance of these three structures were measured across 22 different sites at different locations on two quarters of

TABLE II
MEASUREMENT RESULTS—FIRST SET

Structure	*Cap. Density (c) [aF/μm²]*	*Ave. (C_{ave}) [pF]*	*Std. Dev. (σ_c) [fF]*	$\frac{\sigma_c}{C_{ave}}$	*f_{res} [GHz]*	*Q @ 1GHz*	*f_{res} (fixed L)[a] (C=6.94pF) [GHz]*	*f_{res} (scaled L)[b] (C=6.94pF) [GHz]*	*Rs (Ω)*	*Break-Down [Volts]*
VPP	158.3	18.99	103	0.0054	3.65	14.5	6.04	9.99	0.57	355
PW	101.5	33.5	315	0.0094	1.1	8.6	2.42	5.31	0.55	380
HPP	35.8	6.94	427	0.0615	6.0	21	6.0	6.0	1.1	690

a. Normalized self-resonance frequency calculated for a capacitance of 6.94pF (the value of the *HPP*) assuming that only the capacitor changes and that the inductor does not scale.
b. Normalized self-resonance frequency calculated for a capacitance of 6.94pF (the value of the *HPP*) scaling both the capacitor and the inductor with size.

TABLE III
MEASUREMENT RESULTS—SECOND SET (1 pF)

Structure	*Cap. Density (c) [aF/μm²]*	*Ave. (C_{ave}) [pF]*	*Area [μm²]*	*Cap. Enhancement*	*Std. Dev. (σ_c) [fF]*	$\frac{\sigma_c}{C_{ave}}$	*f_{res} [GHz]*	*Measured Q @ 1GHz*	*Break-Down [Volts]*
VPP	1512.2	1.01	669.9	7.4	5.06	0.0050	>40	83.2	128
VB	1281.3	1.07	839.7	6.3	14.19	0.0132	37.1	48.7	124
HPP	203.6	1.09	5378.2	1.0	26.11	0.0239	21	63.8	500
MIM	1100	1.05	960.9	5.4			11	95	

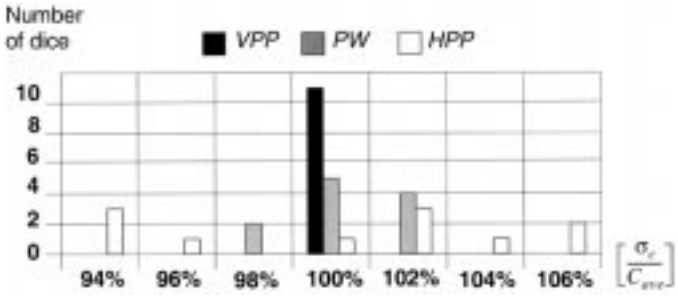

Fig. 15. Capacitance distribution of the VPP, PW, and HPP structures.

two different 8-in wafers. A histogram showing the relative capacitance value distribution across one of the quarter-wafers is shown in Fig. 15. The standard deviations of the capacitance normalized to the average value for these three structures are also shown in Table II. It can be easily seen that the absolute capacitance accuracy of the VPP capacitor is approximately an order of magnitude better than the conventional HPP. Comparison of the measurements on two different wafers also shows that wafer-to-wafer capacitance variation of the purely lateral structures is also improved significantly due to the higher repeatability of the lithography. Finally, due to the high breakdown voltage of the dielectric, the measured breakdown voltage of the implemented capacitors are in excess of 350 V, as shown in Table II.

The second set of test capacitors were fabricated in a purely digital CMOS 7-metal layer process technology with $L_{\min} = W_{\min} = 0.24$ μm, $t_{\rm ox} = 0.7$ μm, and $t_{\rm metal} = 0.53$ μm for the bottom five layers. For this process, the dielectric material is silicon dioxide and the metal material is aluminum. The implemented capacitors include a 5-metal layer HPP, a 5-metal layer VPP, and a 4-metal layer modified VB structures as shown in Figs. 1, 5, and 7, respectively. To perform a fair comparison, the value of the three different capacitor types are designed to be equal. A 1-pF and a 10-pF version of each structure were fabricated in the same die to provide an unbiased comparison of the structures' capacitance density, self-resonant frequency, tolerance and matching properties. Fig. 14(b) shows the capacitor test chip photograph.

The summary of the measurements for the 1-pF capacitors is presented in Table III. For the sake of comparison, the performance measures of a 1-pF MIM capacitor is also included in this table. Due to the lack of any MIM capacitor in the purely digital CMOS technology used, these performance measures are obtained from the design manual information for an MIM capacitor of a very similar process technology with $L_{\min} = 0.28$ μm and mixed signal capabilities.

Due to the high lateral field efficiency of the new proposed structures, the VPP and VB capacitors show 7.43 and 6.29 times more capacitance density than the standard multiplate HPP of Fig. 1, respectively, which are the highest reported to date. This corresponds to a capacitance density of 1.51 fF/μm^2. Moreover, the capacitance density of the VPP capacitor is even 37% higher than the capacitance density of the MIM capacitor.

Because of the multiple via connections and the large number of vertical plates connected in parallel, the VPP structure presents a quality factor higher than the HPP, whereas the quality factor of the VB structure is relatively lower because of the rather high via resistance of the process technology, as summarized in Table III.

As the proposed structures attain higher capacitance densities, their physical dimensions are smaller and hence show higher self-resonance frequencies. The admittance versus frequency measurement of Fig. 16 shows a self-resonance frequency in excess of 40 GHz for the 1-pF VPP capacitor. This is twice the self-resonance frequency of the HPP capacitor, and 4 times higher than that of the MIM capacitor.

To verify our earlier hypothesis of better tolerance and matching properties of the purely lateral structures, the capacitance of capacitors of same values implemented using different structures were measured across 37 usable sites of an 8-in

TABLE IV
MEASUREMENT RESULTS—SECOND SET (10 pF)

Structure	*Cap. Density* (c) [$aF/\mu m^2$]	*Ave.* (C_{ave}) [pF]	*Area* [μm^2]	*Cap. Enhancement*	*Std. Dev.* (σ_c) [fF]	$\frac{\sigma_c}{C_{ave}}$	f_{res} [*GHz*]	*Measured Q @ 1GHz*	*Break-Down* [*Volts*]
VPP	1480.0	11.46	7749	8.0	73.43	0.0064	11.3	26.6	125
VB	1223.2	10.60	8666	6.6	73.21	0.0069	11.1	17.8	121
HPP	183.6	10.21	55615	1.0	182.14	0.0178	6.17	23.5	495
MIM	1100	10.13	9216	6.0			4.05	25.6	

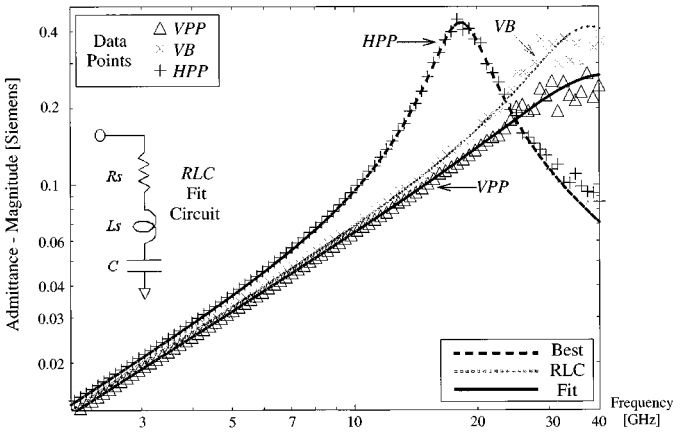

Fig. 16. High frequency admittance measurement results for the HPP, VB, and VPP structures.

wafer. The standard deviation normalized to the average value of each 1-pF structure is shown in Table III. As can be seen, the VPP structure presents almost 5 times better capacitance tolerance than the HPP structure across the wafer.

Although the tolerance of capacitors is an important property to quantify, in many analog applications, the parameter of more significance is the ratio between two adjacent capacitors. To confirm the better matching properties of the new structures, the ratio of adjacent 10-pF and 1-pF capacitors of the same type on the same site were compared across the wafer. The variations of this ratio normalized to its average, $\sigma_r/r_{\rm ave}$, is a better measure to quantify matching. The VPP, VB, and HPP capacitors show a $\sigma_r/r_{\rm ave}$ of 0.6%, 1%, and 1.3%, respectively. Due to the higher accuracy of the lithography process, the two new lateral field structures present better matching properties than the standard horizontal parallel plate capacitor, as suggested earlier. It is noteworthy that in practice, an accurately defined ratio is achieved by using multiple parallel capacitors of the same size and shape.

Finally, the summary of the measurements for the 10-pF capacitors are shown in Table IV. For the sake of comparison, it also includes the estimated performance measures of a 10-pF MIM capacitor. The VPP and VB capacitors show 8.0 and 6.6 times more capacitance density than the 10-pF standard multiplate HPP of Fig. 1. This corresponds to a 34% higher capacitance density of the VPP capacitor when compared to the MIM. The self-resonance frequencies of the proposed structures are in excess of 11 GHz, which is almost twice the self-resonance frequency of the HPP capacitor, and approximately 3 times higher than that of the MIM of the same value. Finally, the 10-pF VPP and VB capacitors present almost 3 times better capacitance tolerance than the HPP structure across the wafer.

VII. CONCLUSIONS

A new theoretical framework which shows the capacity limits of integrated capacitors were presented. This new framework can be used to evaluate the performance of the existing capacitive structures and leads to two purely lateral capacitors. These structures demonstrate: higher capacitance density, better tolerance and matching properties, and higher self-resonance frequency than previously reported capacitor structures, MIM and standard HPP capacitors, while maintaining a comparable quality factor. These two new structures are standard CMOS compatible and do not need an extra processing step, as is the case with special MIM capacitors.

APPENDIX
TIGHTER UPPER BOUND ON THE CAPACITANCE DENSITY

Although the horizontal and vertical parallel plate capacitor structures of Fig. 4 have the maximum horizontal and vertical field usage, respectively, they cannot be implemented in the same spatial location simultaneously. This makes it impossible to achieve the maximum electric field usage in the x, y, and z dimensions at the same time, and therefore (5), while being correct, is too conservative. The orthogonality of the electric field components implies that the horizontal and vertical parallel plate capacitance densities, c_x, c_y, and c_z *may* form an orthogonal basis for decomposition of capacitance densities as visualized in Fig. 17. This orthogonal decomposition can be used to obtain a new tighter upper bound for the capacitance density of structures with rectangular (Manhattan) boundaries. Noting that the maximum capacitance is given by the magnitude of the vector sum of $c_{x,\max}$, $c_{y,\max}$, and $c_{z,\max}$ (Fig. 17), the maximum capacitance density for any given process technology will be given by

$$c_{\max} = \sqrt{c_{x,\max}^2 + c_{y,\max}^2 + c_{z,\max}^2} = \varepsilon_0\varepsilon_r\sqrt{\frac{2}{L_{\min}^2(L_{\min}+W_{\min})^2} + \frac{1}{t_{\rm ox}^2(t_{\rm ox}+t_{\rm metal})^2}} \tag{7}$$

for $L_{x,\min} = L_{y,\min} \equiv L_{\min}$ and $W_{x,\min} = W_{y,\min} \equiv W_{\min}$. To verify the validity of this hypothesis, (7) is plotted along with the simulated results in Fig. 11 as semi-empirical upper bound. It can easily be seen that none of the simulated structures shows a capacitance density above that of (7) for any value of $L_{\min}$.

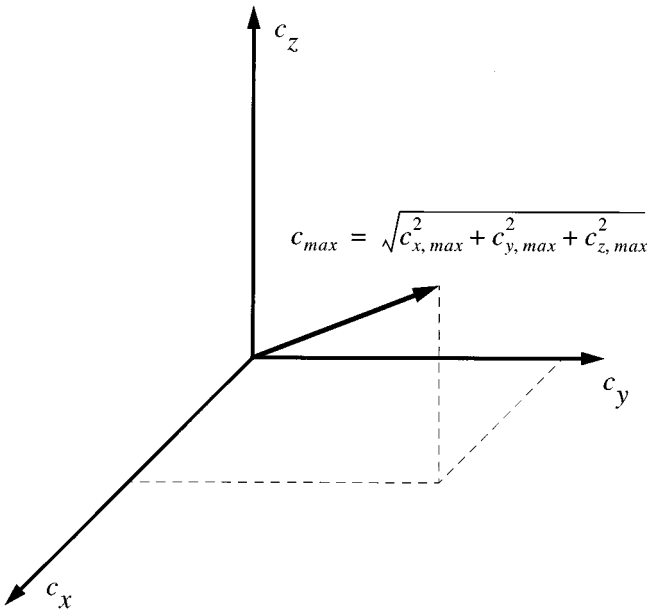

Fig. 17. Ortho-normal decomposition into lateral and vertical parallel plates.

ACKNOWLEDGMENT

The authors would like to thank Conexant Systems, Newport Beach, CA, and, in particular, S. Lloyd, R. Magoon, F. In't veld, B. Bhattacharyya, J. Yu, and R. Hlavac of the Wireless Communications Division, and M. Racanelli, S. Stetson, and A. Karroy of the Silicon RF Platform Division for their help. The authors would also like to acknowledge I. Aoki, D. Ham, H. Hashemi, S. Kee, S. Koudounas, S. Mandegaran, and H. Wu of the California Institute of Technology for helpful discussions.

REFERENCES

[1] M. E. Elta, A. Chu, L. J. Mahoney, R. T. Cerretani, and W. E. Courtney, "Tantalum oxide capacitors for GaAs monolithic integrated circuits," *IEEE Electron Device Lett.*, vol. EDL-3, May 1982.

[2] M. N. Yoder, "Recessed interdigitated integrated capacitor," U.S. Patent 4 409 608, Oct. 11, 1983.

[3] O. E. Akcasu, "High capacitance structure in a semiconductor device," U.S. Patent 5 208 725, May 4, 1993.

[4] A. C. C. Ng and M. Saran, "Capacitor structure for an integrated circuit," U.S. Patent 5 583 359, Dec. 10, 1996.

[5] H. Samavati, A. Hajimiri, A. R. Shahani, G. N. Nasserbakht, and T. H. Lee, "Fractal capacitors," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2035–2041, Dec. 1998.

[6] A. Stolmeijer and D. C. Greenlaw, "High quality capacitor for sub-micrometer integrated circuits," U.S. Patent 5 939 766, Aug. 17, 1999.

[7] A. Hajimiri and R. Aparicio, "Capacity limits of lateral flux and quasifractal capacitors," in *2000 Symp. VLSI Technology*, withdrawn after submission.

[8] R. Aparicio and A. Hajimiri, "Capacity limits and matching properties of lateral flux integrated capacitors," in *IEEE CICC Dig. Tech. Papers*, May 2001, pp. 365–368.

[9] J. B. Marion and W. F. Hornyak, *Principles of Physics*. New York: Holt-Saunders, 1984.

[10] G. D. Alley, "Interdigital capacitors and their application to lumped-element microwave integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 18, pp. 1028–1033, Dec. 1970.

[11] J. L. Hobdell, "Optimization of interdigital capacitors," *IEEE Trans. Microwave Theory Tech.*, vol. 27, pp. 788–791, Sept. 1979.

[12] R. Esfandiari, D. W. Maki, and M. Siracusa, "Design of integrated capacitors and their application to gallium arsenide monolithic filters," *IEEE Trans. Microwave Theory Tech.*, vol. 31, pp. 57–64, Jan. 1983.

[13] E. Pattenpaul, H. Kapusta, A. Weisgerber, H. Mampe, J. Luginsland, and I. Wolff, "CAD models of lumped elements on GaAs up to 18 GHz," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 294–304, Feb. 1988.

[14] K. C. Huang, D. Hyland, A. Jenkins, D. Edwards, and D. Dew-Hughes, "A miniaturized interdigital microstrip bandpass filter," *IEEE Trans. Appl. Superconduct.*, vol. 9, pp. 3889–3892, June 1999.

[15] J. C. Strikwerda, *Finite Difference Schemes and Partial Differential Equations*. Belmont, CA: Wadsworth, 1989.

[16] J. D. Jackson, *Classical Electrodynamics*. New York: Wiley, 1999.

Roberto Aparicio (S'00) was born in Puebla, Mexico, in 1975. He received the B.S. degree in electronics from Universidad Autonoma de Puebla, Mexico, in 1999 and the M.S. degree in electrical engineering from the California Institute of Technology, Pasadena, in 2001, where he is currently working toward the Ph.D. degree.

His current research interests include RF integrated circuits with an emphasis on oscillators, frequency synthesizers, and optimization of on-chip passive elements.

Mr. Aparicio ranked first at the Universidad Autonoma de Puebla and earned the Phoenix Medal in 1998. He was a Fulbright Scholarship recipient at the California Institute of Technology from 1999 to 2001, and received the Walker von Brimer Foundation Outstanding Accomplishment Award and the Analog Devices Outstanding Student Designer Award, both in 2001.

Ali Hajimiri (S'95–M'98) received the B.S. degree in electronics engineering from the Sharif University of Technology, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1996 and 1998, respectively.

He was a Design Engineer with Philips Semiconductors, where he worked on a BiCMOS chipset for GSM and cellular units from 1993 to 1994. In 1995, he was with Sun Microsystems, where he worked on the UltraSPARC microprocessor's cache RAM design methodology. During the summer of 1997, he was with Lucent Technologies Bell Labs, Holmdel, NJ, where he investigated low-phase-noise integrated oscillators. In 1998, he joined the Faculty of the California Institute of Technology, Pasadena, as an Assistant Professor of electrical engineering, where his research interests are high-speed and RF integrated circuits. He is a coauthor of *The Design of Low Noise Oscillators* (Boston, MA: Kluwer, 1999), and has received several U.S. and European patents. He is an associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II and a member of the Technical Program Committees of the International Conference on Computer Aided Design (ICCAD). He has also served as Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and on the Guest Editorial Board of Transactions of Institute of Electronics, Information and Communication Engineers of Japan (IEICE).

D. Hajimiri was the Gold Medal winner of National Physics Competition and the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, the Netherlands. He was a corecipient of the International Solid-State Circuits Conference (ISSCC) 1998 Jack Kilby Outstanding Paper Award and the winner of the IBM faculty partnership award.