Capacity Limits and Matching Properties of Lateral Flux Integrated Capacitors

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Abstract

Theoretical limits for the capacitance density of lateral flux and quasi-fractal capacitors are calculated. These limits are used to investigate the efficiency of various capacitive structures such as lateral flux and quasi-fractal structures. This study leads to two new capacitor structures with high lateral-field efficiency. Simulation and experimental results demonstrate higher capacity and superior matching properties compared to the standard horizontal parallel plate and previously reported lateral-field capacitors.

Introduction

Capacitors are essential elements in integrated circuits. Metal-to-metal and metal-to-poly capacitors are inevitable when linearity and high quality factor, Q, are needed. Unfortunately, these capacitors consume larger chip areas and therefore their area efficiency is of considerable importance. Lateral-flux and quasi-fractal capacitors have been proposed to exploit the lateral as well as the vertical fields to increase the capacitance per unit area [1][2][3]. Despite these advances, it is not clear what the upper limit of capacitance density for a given process technology is and which structures are optimum. Also the matching properties of such capacitors need further study, as the vertical and lateral capacitances are controlled by two different processes, namely, deposition and lithography.

Theoretical limits for the capacitance density of any capacitive structure in terms of process parameters are derived. These theoretical upper bounds lead to two new capacitor structures which demonstrate higher capacitance density compared to the standard *Horizontal Parallel Plate* (*HPP*) and previously reported lateral-flux capacitors such as interdigitated (a.k.a. *Horizontal Bars* or *HB*) [1] and quasi-fractal capacitors [2]. Finally, their superior matching properties are verified experimentally.

Capacity Limits

In this section, we will show that the capacitance of any arbitrary capacitive structure can be decomposed into three components associated with three orthogonal spacial dimensions and use this decomposition to find theoretical upper bounds for the total capacitance of such structures.

The electrostatic energy density in a homogenous isotropic dielectric media can be decomposed as:

$$u(\boldsymbol{r}) = \frac{\varepsilon_r\varepsilon_0}{2}\boldsymbol{E}^2(\boldsymbol{r}) = \frac{\varepsilon_r\varepsilon_0}{2}[E_x^2(\boldsymbol{r}) + E_y^2(\boldsymbol{r}) + E_z^2(\boldsymbol{r})] \quad (1)$$

where $\boldsymbol{r}$ is the position vector, $\boldsymbol{E}$ is the electric field vector, ε_0 is the permittivity of vacuum, ε_r is the relative permittivity of the dielectric medium and E_x, E_y, and E_z, are the x, y, and z electric field components, respectively. The capacitance density [F/m^3] of any conductor-dielectric structure can be calculated by integrating the energy density over the volume. Noting that capacitor's electrical energy is

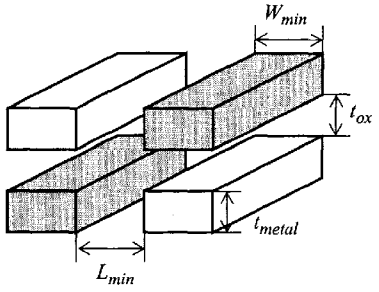

Figure 1. Dimensions of the metal lines

$U_E = C\Delta V^2/2$, the capacitance density, c, can be decomposed into three components, c_x, c_y and c_z, due to E_x, E_y, and E_z, respectively, *i.e.*,

$$c = \frac{1}{vol}\cdot\frac{\varepsilon_r\varepsilon_0}{\Delta V^2}\left[\int_{vol}E_x^2(\boldsymbol{r})dv + \int_{vol}E_y^2(\boldsymbol{r})dv + \int_{vol}E_z^2(\boldsymbol{r})dv\right] = c_x + c_y + c_z \quad (2)$$

where ΔV is the electric potential difference between the terminals of the capacitor, dv is the differential unit of volume and vol is the volume of interest.

An upper bound for the capacitance is obtained by setting c_x, c_y and c_z to their maximum values independently. The maximum capacitance density for each spacial direction is obtained using a parallel plate structure normal to that direction with minimum plate spacing to achieve maximum electric field and minimum plate thickness to achieve minimum volume at the same time. This upper bound is referred to as *Theoretical Limit 1* (*TL1*) and can be expressed as:

$$c_{max} = c_{x,max} + c_{y,max} + c_{z,max} = \varepsilon_r\varepsilon_o\left[\frac{2}{L_{min}(L_{min}+W_{min})} + \frac{1}{t_{ox}(t_{ox}+t_{metal})}\right] \quad (3)$$

where t_{ox}, and t_{metal} denote the inter-layer vertical separation and the vertical metal thickness, and L_{min} and W_{min} are the minimum lateral spacing and the minimum metal width for the process technology of choice, respectively, as shown in Fig 1. Eq. (3) defines an upper bound for the capacitance density of any metallic structure and can serve as a reference for comparison of various capacitive structures.

A tighter upper bound can be obtained noting that although the horizontal and vertical parallel plate capacitor structures have the maximum horizontal and vertical field usage, respectively, they cannot be implemented in the same spatial location simultaneously. Therefore, a tighter upper bound for the capacitance density of structures with rectangular boundaries can be obtained by maximizing the magnitude of the vector associated with orthonormal basis formed by c_x, c_y and c_z [4], *i.e.*,

$$c_{max,2} = \sqrt{c_{x,max}^2 + c_{y,max}^2 + c_{z,max}^2} \quad (4)$$

which will be referred to as *Theoretical Limit 2* (*TL2*).

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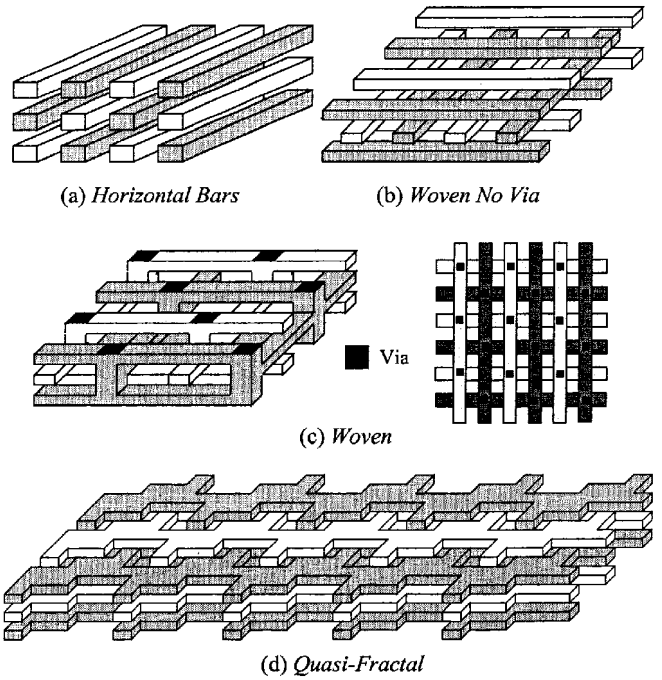
Capacitor Scaling with Minimum Lateral Spacing

To gain more insight into the effectiveness of lateral and vertical field usage in metal-to-metal capacitors, the capacitance densities of the structures shown in Fig. 2 are simulated using a special purpose field solver using an enhanced relaxation algorithm [4]. The simulated structures include the standard parallel plate, the horizontal bars (*HB*) [1], *woven* [2], *woven without vias* and a *quasi-fractal* structure of moderate dimension [2]. Different shadings are used to show the terminals of the capacitors throughout this paper.

The simulated capacitance densities per unit volume as a function of the minimum lateral spacing, L_{min}, are plotted in Fig. 3. Equal lateral metal spacing and thickness is assumed, *i.e.*, $L_{min} = W_{min}$. Both t_{ox} and t_{metal} are also kept constant at $0.8\mu m$. This is in accordance with the observation that lateral spacings keep scaling down as lithography advances, while the vertical dimensions do not scale at the same rate. Even though the graph of Fig. 3 is for a particular value of t_{ox} and t_{metal}, it can be easily used for other vertical spacings through a simple scaling as long as $t_{ox} = t_{metal}$ and $L_{min} = W_{min}$. This property can be traced back to the scale-invariance of electrostatic equations [5]. *TL1* and *TL2* are also plotted in this graph. As can be seen, none of the capacitance densities exceed either of the limits.

Two important regions can be identified in the simulation results of Fig. 3. For large lateral spacings, *i.e.*, $L_{min} \gg t_{ox}$ (right hand side of the graph), the capacitance density reaches a plateau as the lateral fields become inconsequential and the capacitance is dominated by the vertical fields. As can be seen, the *HPP* structure has the best performance in this region due to its optimal usage of vertical fields.

At the other extreme, when the minimum lateral spacing is much smaller than the vertical separation, *i.e.* $L_{min} \ll t_{ox}$ (left hand side of the graph), the capacitance densities of the lateral field structures become inversely proportional to L_{min}^2 because the lateral plate spacing decreases linearly with lateral shrinkage resulting in a linear increase in the capacitance per plate. Also the number of plates per unit volume grows linearly with decreasing L_{min} due to smaller metal width and spacing resulting in an inverse L_{min}^2 dependence. It is therefore desirable to choose a capacitor with maximum lateral field usage as the feature sizes shrink. This will in turn result in a capacitor with minimum vertical field usage due to the inherent trade-off between lateral and vertical field utilization. In other words, the lateral field usage can only be increased by introducing dielectric regions between metal lines in the same layer, which in turn results in loss of the vertical component.



(a) *Horizontal Bars* (b) *Woven No Via*

(c) *Woven*

(d) *Quasi-Fractal*

Figure 2. Manhattan Capacitor Structures

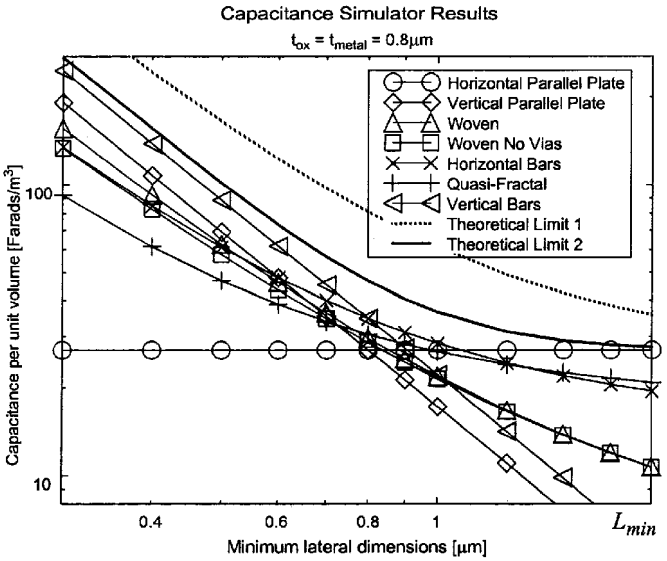


Figure 3. Capacitance Density vs. Minimum Lateral Dimensions

Maximum Lateral Field Usage Capacitive Structures

As discussed earlier, the maximization of the capacitance density in one lateral dimension (*e.g.*, c_x) leads to the structure shown in Fig. 4a which we will refer to as *Vertical Parallel Plates* (*VPP*). Unlike the *HB* structure [1] of Fig. 2a, it has no vertical field component and maximizes the lateral flux by using vertical parallel-plates made out of metal strips connected with vias that maximize the lateral area of the plates. This difference has important implications on the capacity density and matching of *VPP* capacitors. The via interconnections are an important feature of this structure, as they increase the effective area of the lateral parallel plates. Even if stacked vias are not supported in a process technology, a close approximation to this structure can be fabricated by interleaving vias. Top metal layer which is usually thicker and has different design rules can be used to make the connection between the capacitor terminals and outside circuitry. It should also be noted that time consuming

electromagnetic simulations are rather unnecessary for this structure, as its capacitance can be predicted using simple expressions for parallel plate structures with fringing. This is another major advantage of this structure, compared to the quasi-fractal capacitors [2].

It may seem that the series resistance of the vias can increase the losses of the capacitor significantly. Fortunately, very little ac current flows through each vias of the *VPP* structure and therefore the high via resistance is even less important. In other words, the effective series resistance of the capacitor is determined by the resistance of a large number of vias in parallel. This claim is also supported through experimental verification as will be seen shortly.

The abovementioned *VPP* structure maximizes the lateral field usage in one dimension. It is possible to perform this maximization in two dimensions using the *Vertical Bars* (*VB*) structure shown in Fig. 4b. It consists of vertical bars made out of metal squares and vias. The length of the bars is limited by the number and thickness of metal layers. This structure utilizes the electric field in both lateral dimensions and has an even higher capacitance density than the *VPP* structure. However, the series resistance of this structure is mainly determined by the via resistance and can be high depending on the number of metal layers and via resistance in the process of interest. Although vias have a large series resistance, a large number of them are used in parallel. As the number of parallel metal bars in this structure is large, the entire capacitor can be modeled as a parallel combination of N series RC branches. The equivalent series resistance and capacitance are $R_s = r_s/N$ and $C = N \cdot c_s$, where r_s and c_s are the large resistance and the small capacitance of each small section, respectively. It can be seen that the equivalent series resistance, R_s, decreases linearly with the total capacitance, C. A similar argument is valid for the series resistance of the metal slabs. Therefore, for any capacitor structure what really matters is the capacitance enhancement for the excess series resistance *per unit area*.

The choice between *VPP* and *VB* will depend on the application. A trade-off between high quality factor of the *VPP* and high capacitance density of the *VB* can be achieved by extending the widths of the vertical bars in one dimension. In the extreme case, this intermediate structure will turn into the *VPP* capacitor.

The simulated capacitance densities of these two structures vs. the minimum lateral spacing L_{min} are also depicted in Fig. 3 for the same set of constraints. For $L_{min} < t_{ox}$, the *VB* and *VPP* attain the highest capacitance density of all the structures, while for $L_{min} > t_{ox}$, *VPP* and *VB* continuously degrade due to the lack of any vertical field component. Theoretical limits such as *TL2* can be used as a means of efficiency comparison. For instance, for $L_{min} \ll t_{ox}$, *VB* and *VPP* achieve a remarkable 90% and 60% capacitance efficiency compared to *TL2*. In contrast, the quasi-fractal structure of Fig. 2d achieves only an efficiency of 20%.

Matching properties of capacitors are of great importance in applications such as A/D and D/A converters [6][7] and

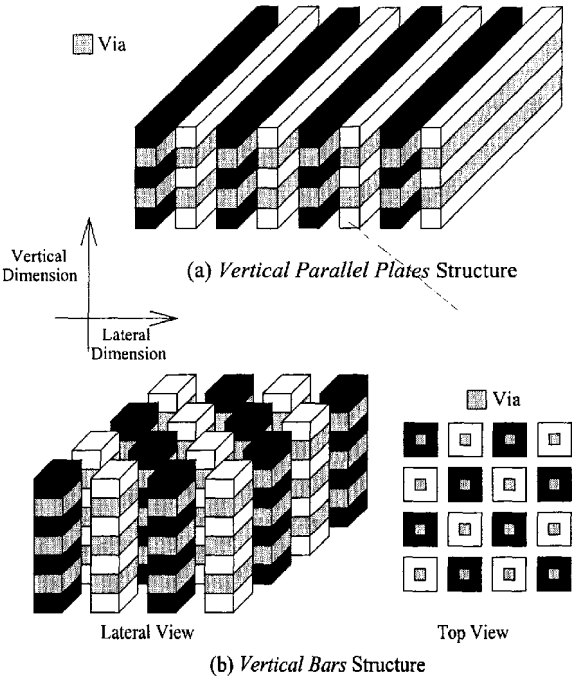


Figure 4. High Efficient-Lateral Field Structures

poly-phase filters [8]. Noting that lithography usually has much better accuracy and repeatability than the dielectric deposition across the wafer, we expect capacitors solely using lateral fields to demonstrate better matching properties than the structures using a combination of lateral and vertical fields or just the vertical field. In practice, *VPP* structures show an order of magnitude improvement in their matching across the wafer and from wafer to wafer compared to standard parallel plate structures as shown in the experimental results.

Experimental Results

A three metal layer CMOS technology with $L_{min} = 0.5\mu m$, $W_{min} = 0.5\mu m$, $t_{ox} = 0.95\mu m$ and $t_{metal} = 0.63\mu m$ is used to fabricate the *VPP*, *HB* and *HPP* structures that occupy a die area of $0.12mm^2$, $0.33mm^2$ and $0.19mm^2$, respectively. Fig. 6 depicts the high-frequency one-port measurements of these structures while the performance numbers for these structures are summarized in Table 1. As can be seen, the *VPP* structure not only achieves a factor of 4.4 and 1.6 improvement in capacitance density over the standard *HPP* and *HB*, respectively, but also *for equal capacitance values* will have higher self-resonance frequency, based on either of the two scaling methods shown in the table. To investigate the absolute accuracy and matching properties of *VPP*, capacitance measurements were performed on two quarters of two different 8-inch wafers, where each quarter wafer has eleven usable test sites on it. The relative capacitance variations of the *VPP*, *HB* and *HPP* are shown in Fig. 7 while the measured and statistical results are also summarized in Table 1.

Table 1. Measurement Results

Cap.	*Cap. Density (c) [fF/μm²]*	*Ave(C_{ave}) [pF]*	*Std. Dev. (σ_c) [fF]*	$\frac{\sigma_c}{C_{ave}}$	*f_{res} [GHz]*	*Q @ 1GHz*	*f_{res} (fixed L)[a] (C=6.94pF) [GHz]*	*f_{res}(scaled L)[b] (C=6.94pF) [GHz]*	*Rs (Ω)*
VPP	158.3	18.99	103	0.0054	3.65	14.5	6.04	9.99	0.57
HB	101.5	33.5	315	0.0094	1.1	8.6	2.42	5.31	0.55
HPP	35.8	6.94	427	0.0615	6.0	21	6.0	6.0	1.1

a. Normalized self-resonance frequency calculated for a capacitance of 6.94pF (the value of the *HPP*) assuming that only the capacitor changes and that the inductor does not scale.

b. Normalized self-resonance frequency calculated for a capacitance of 6.94pF (the value of the *HPP*) scaling both the capacitor and the inductor with size.

It can easily be seen that the relative capacitance accuracy of *VPP* is approximately *an order of magnitude* better than the conventional *HPP*. Comparison of the measurements on two different wafers also shows that wafer-to-wafer capacitance variations also improved significantly due to better repeatability of the lithography. Finally the chip photo is shown in Fig. 8.

Conclusions

A new theoretical framework which shows the capacity limits of different capacitor structures is presented in this work. This new framework can be used to evaluate the performance of the existing capacitive structures and leads to new capacitor structures achieving a factor of 4.4 increase in the capacitance densities. In addition to higher capacitance density, purely lateral structures demonstrate an order of magnitude better matching than the parallel plate structures implemented on the same wafer, while offering comparable or better self-resonance frequency and series resistance.

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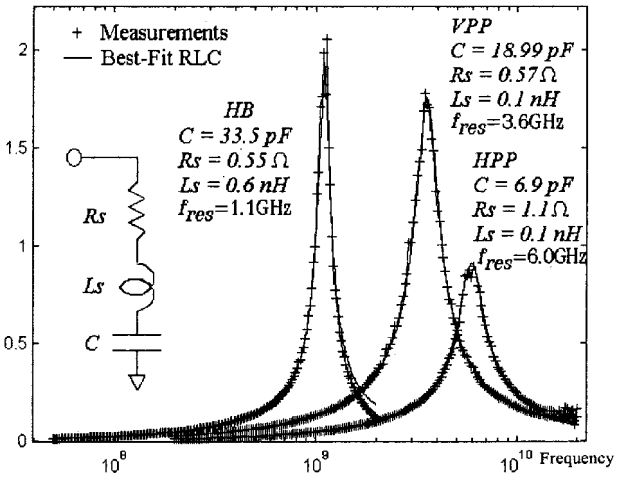

Figure 6. One Port High-Frequency Measurements

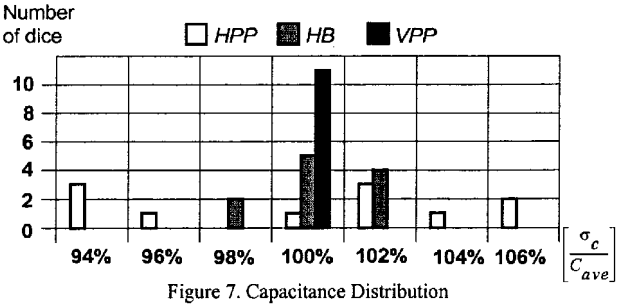

Figure 7. Capacitance Distribution

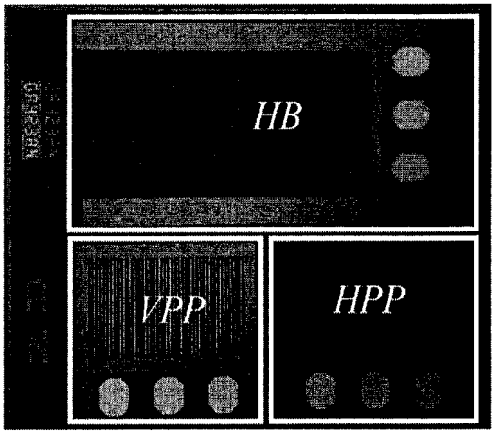

Figure 8. Die Photo of the *HB*, *VPP* and *HPP* structures