Carbon Nanotube Field-Effect Transistors and Logic Circuits

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ABSTRACT

In this paper, we present recent advances in the understanding of the properties of semiconducting single wall carbon nanotube and in the exploration of their use as field-effect transistors (FETs). Both electrons and holes can be injected in a nanotube transistor by either controlling the metal-nanotube Schottky barriers present at the contacts or simply by doping the bulk of the nanotube. These methods give complementary nanotube FETs that can be integrated together to make inter- and intra-nanotube logic circuits. The device performance and their general characteristics suggest that they can compete with silicon MOSFETs. While this is true when considering simple prototype devices, several issues remain to be explored before a nanotube-based technology is possible. They are also discussed.

Categories and Subject Descriptors

B.6.0 [**Logic Design**]: General – *novel logic devices.*

General Terms

Measurement, Performance, Design, Experimentation.

Keywords

Nanoelectronics, Carbon Nanotube, Semiconductor, Field-Effect Transistor, FET, Schottky Barrier, Circuits, Inverter, Logic Gate, SWNT.

1. INTRODUCTION

The single-wall carbon nanotube (SWNT) is a one-dimensional conductor that can be either metallic or semiconducting depending on the arrangement of the carbon atoms (see Figure 1). [1] The band-gap, Eg, of a semiconducting nanotube depends strongly on its diameter, d, as Eg $\propto$ 1/d. Fig.1 presents two examples of possible structures for a 1.4nm diameter SWNT with their corresponding electronic structures calculated using a tight-binding model. [1] Both metallic and semiconducting nanotubes are attractive for applications. On one hand, the conductivity of metallic nanotubes and their robustness are attracting interest for future interconnects. [2] On the other hand, the semiconducting carbon nanotubes exhibit the desired properties for making field-effect transistors and logic switches [3-9]. In principle, the combined properties of both kinds of nanotubes can form a unique set of building blocks for future electronics.

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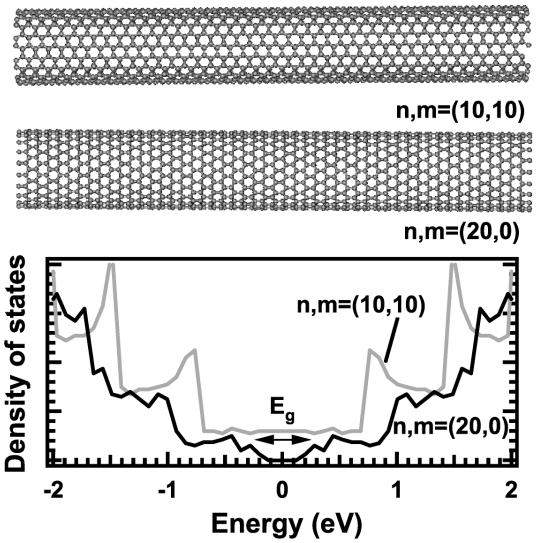

Figure 1. Model of the structure of a single-wall nanotube. Although the nanotubes shown on top have the same composition, one is metallic and the other is semiconducting. Bottom is the density of states calculated for both tubes.

2. Nanotube Transistors

Early experiments [3,4] on SWNT FETs (CNFETs) demonstrated that they behave much like conventional semiconductor transistors. There are, however, some important differences: i) the carbon nanotube is one-dimensional which greatly reduces the scattering probability. [10] As a result, the devices may operate in the ballistic regime. [10,11] ii) The nanotube conducts essentially on its surface where all the chemical bonds are saturated and stable. Therefore, there is no need for careful passivation of the interface between the nanotube channel and the gate dielectric, i.e. there is no equivalent of the silicon/silicon dioxide interface. iii) The Schottky barrier at the metal-nanotube contact is the active switching element in an intrinsic nanotube device. [12] These properties make the one-dimensional transistor action in nanotube unique and interesting. Here we review their characteristics, the properties of the barriers, and discuss the integration of nanotube devices into logic circuits.

Early nanotube FETs used a non-local back-gate with the nanotube side-bonded to noble metal electrodes. This arrangement gave large contact resistances and poor characteristics [3-5].

Since then, significant improvements in the performance of CNFETs have been achieved. New structures are now built with top-gate geometry and they resemble, in many respects, conventional silicon CMOS devices. An example of the characteristics of a top-gated CNFET is shown in Fig. 2. This CNFET is contacted with titanium carbide electrodes and the gate electrode is made of Al separated by 15 nm of gate oxide (SiO_2). [13] Its relevant parameters are presented in Table 1. They are also compared with an earlier back-gated CNFET and to a conventional Si MOSFET of 100nm gate length. First, we observe a very large improvement compared to the early nanotube devices. This improvement is mainly due to the scaling of the dimensions (mostly the gate oxide thickness) and the adoption of a better device geometry. In addition, the comparison of key parameters suggests that the performance of CNFETs, once the device is scaled properly, would be comparable to, if not better than, conventional Si MOSFET.

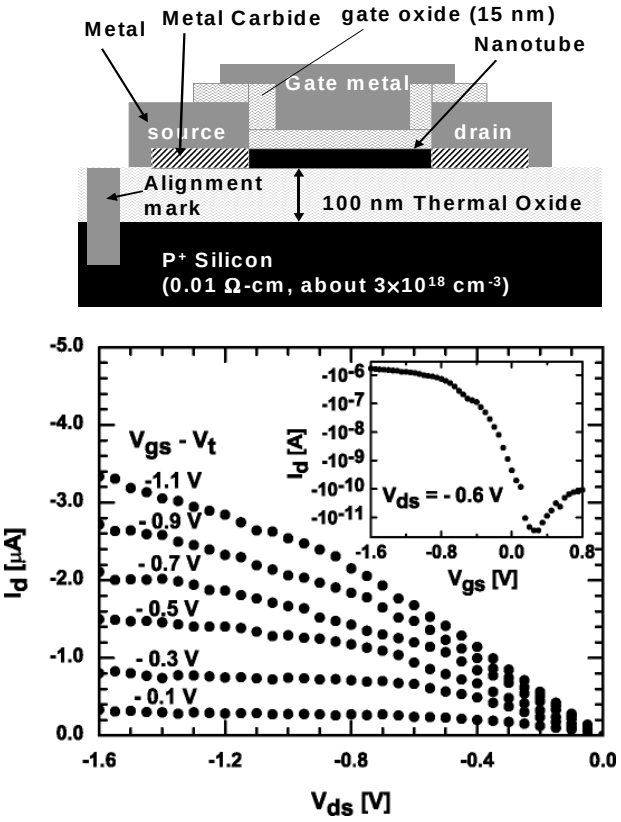

Figure 2. Characteristics of a single-wall nanotube field-effect transistor. The parameters and structure are shown in the schematics above.

While CNFETs show improvement with scaling, we note that their scaling properties are not conventional. [12] They rather follow the behavior of a Schottky barrier MOSFET, i.e. the switching behavior involves mostly the contacts, as oppose to the bulk of the tube. [12] In this respect, the extrapolation of the measured performance for those nanotube transistors to shorter channel devices, i.e. in the limits of scaling, is still unclear. The actual performance, however, suggests that the nanotube transistors, in the structure of an array, will provide enough gain and fan-out for applications. Moreover, it is possible that the CNFET may outperform silicon MOSFET in the limits of scaling.

Table 1 Comparison of the characteristics of CNFETs and Si MOSFETs

p-type FETs	Back-gated CNFET [6]	Top gated CNFET [13]	Si MOSFET [19]
Gate length (nm)	1030	260	100
Gate oxide thickness (nm)	150	15	0.8
Trans-conductance	~0.3 μS/tube (244 μS/μm)*	~3μS/tube (2100 μS/μm)*	460 μS/μm
Subthreshold slope (mV/dec)	730	130	80
ON/OFF ratio	10^5	10^6	10^6

* The transconductance is normalized by the width of the nanotube, i.e. 1.4 nm. A more realistic normalization and comparison with Si MOSFET would take into account an array of nanotubes as discussed in Ref. 6.

3. Nanotube-Metal Schottky Barrier

The CNFETs measured in air, as in Fig. 2, are p-type, i.e. the tubes conduct holes upon applying a negative gate voltage and they show no evidence of electron conduction even at very large positive gate voltage. In addition, the CNFETs in air also show ohmic IVs at small source-drain voltage in the ON state of the device (i.e. at negative gate bias). This situation changes when the devices are annealed in vacuum. This annealing step removes the adsorbed oxygen and yields a reversible transformation of the CNFET from p- to n-type. An example of such a transformation is presented in Fig. 3. Initially, a p-type CNFET is annealed in vacuum and transformed into a n-type device. Then, oxygen is slowly introduced into the chamber and IVs are acquired at intermediate stages of the transformation. This simple annealing technique is described elsewhere. [7,14,15] The intermediate stages (blue curves) are ambipolar, i.e. the tube can conduct both electrons and holes. This transformation can be easily rationalized by considering the presence of tunneling barriers at the contact. [14, 15] Each situation is presented in Figure 4. In Fig. 4a, the Fermi level at the metal-nanotube junction in air is closer to the valence band of the nanotube. This leads to hole conduction and p-type behavior. The annealing step leads to a change in the line-up of the bands at the junction (Fig. 4c) and to lowering of the barrier for electron injection. This modification at the contacts also introduces an increase of the barrier height for hole injection, leading to an n-type CNFET. [15] The intermediate stage, however, simply occurs when the contact Fermi level is around mid-gap. This is the situation illustrated in Fig. 4b. This special situation gives similar barriers for electron and hole injection and the device is ambipolar. [14]

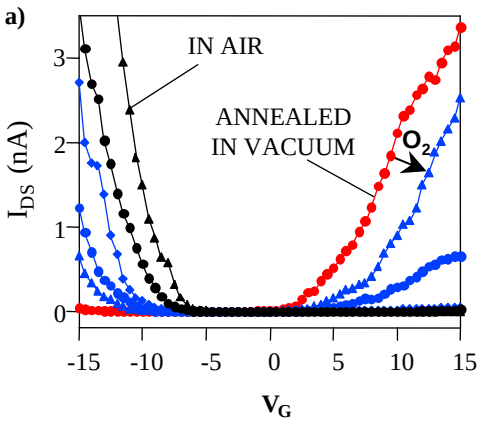

Figure 3 Transformation from n- to p-type of a CNFET as a function of oxygen dose. This conversion is reversible.

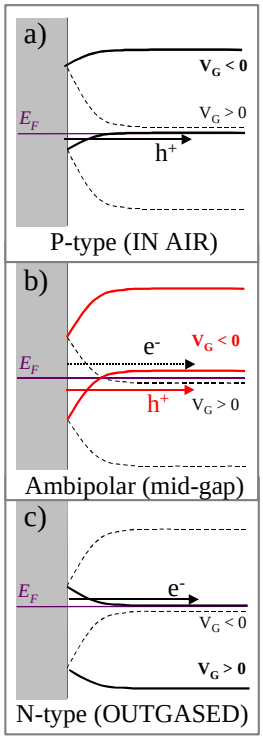

Figure 4.

Schematic of the bands in the vicinity of the contacts as a function of the electrostatic gate field for p-type (a), ambipolar (b), and n-type (c) CNFETs. The effect of annealing the device in vaccum is to change the situation at the contacts from a) to c). Introducing air (oxygen) reverses the process and converts back the device to the situation illustrated in b) first (partial conversion) and finally in a).

3.1 Ambipolar Nanotube Transistors

The ambipolar CNFET is particularly interesting in that it allows us to explore in depth the properties of a one-dimensional (1D) metal-nanotube junction. Although the situation for the ambipolar device is consistent with a mid-gap injection, which implies that the barriers for electron and hole injection are high (Eg/2~300mV), the IVs at room temperature are ohmic (see Figure 5b). [14] This behavior is not expected in presence of a conventional Schottky barrier. This peculiar observation led us to investigate the temperature dependence of the IV curves for an ambipolar device. The results are presented in Figure 5 for the case of hole transport. The results are essentially the same in the region of electron accumulation. In fact, the measured barrier heights for both electrons and holes are very small, at least 20 times lower than expected (~15meV instead of ~300meV). Therefore, the Schottky barrier in the strong accumulation of either holes or electrons is so thin that the junction is quasi-transparent for carrier injection, i.e. there is a very efficient tunneling through the barrier. However, the shape of the barrier of this 1D junction presents also a tail that extends deeper into the nanotube channel. This extension of the barrier is too thick for tunneling to occur unless the source-drain field is larger than the height of the effective barrier introduced by the tail (i.e. V > 15mV). This tail is very particular to nanotube-metal 1D junction and largely determines the effective barrier which is measured. [14,16] The shape and the thickness of this 1D Schottky barrier are also non-uniform and strongly depend on the gate field. [17] As a result, the injection of carriers may become very asymmetrical depending on the conditions at the contact. [15]

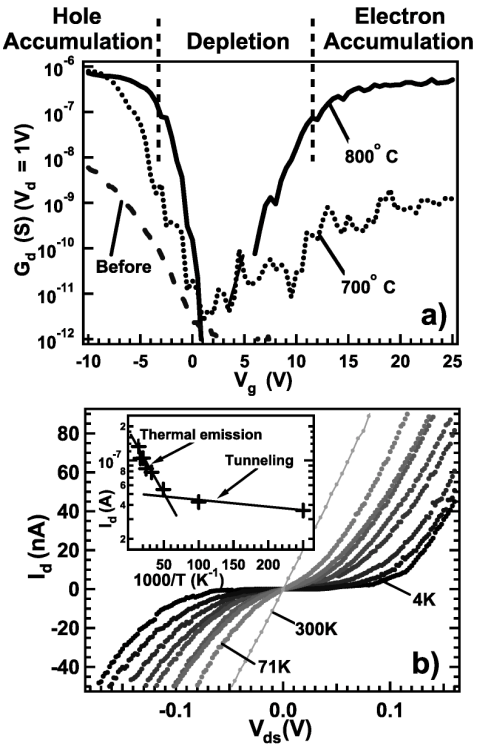

Figure 5. Transformation of a p-type CNFET into an ambipolar device after annealing. The nanotube is contacted with carbide electrodes and the device is protected with a CVD oxide. The ambipolar device is obtained after annealing at 800°C in argon and it is stable in air. The barriers of this 1D junction between the nanotube and the carbide contacts are characterized in the lower figure as a function of temperature.

4 Doping and Contact Injection

As mentioned earlier, the CNFET in air is p-type. The p-character was initially assumed to be due to a charge transfer by a high workfunction metal contact with this transfer accounting for some hole doping. The impact of oxygen was reported earlier and the conclusion was that oxygen also dopes the nanotube with holes, thereby making it p-type. [18] We tested these assumptions using selective doping of the nanotube with an electron donor (potassium). The idea was to reverse the doping caused by

oxygen. The results are presented in Fig. 6. They are very different when compared with the results of annealing followed by exposure to oxygen (Fig. 3). Therefore, they support a very different conclusion as discussed below.

As expected, increasing the doping level in the nanotube with potassium leads to the conversion from p- to n-type (curves 1-12, Fig. 6a). This transformation is similar to the previous one obtained by annealing in vacuum. However, the details of the transformation are very different. i) Potassium is known to effectively dope the nanotube with the main effect being a shift of the threshold voltage toward more negative gate voltage (see the trend in curves 1-6). This shift is not observed in the annealing experiment (Fig. 3). ii) The intermediate stages do not involve an ambipolar device. It is therefore a different process: The doping with potassium is consistent with the doping of the bulk of the tube, as illustrated in Fig. 6 b and c. The conversion to n-type only occurs when the level of electron doping is high and significantly affects the barrier thickness at the contacts. Moreover, the absence of the ambipolar stage implies that the doping of the bulk of the nanotube does not shift the Fermi-level at the contacts. The barriers at the contact are therefore pinned and do not change as a function of bulk doping. In contrast, the main effect of oxygen on the n-type CNFET in Fig. 3 is not to dope the nanotube but rather to shift the Fermi-level at the contacts and modify the contact barriers.

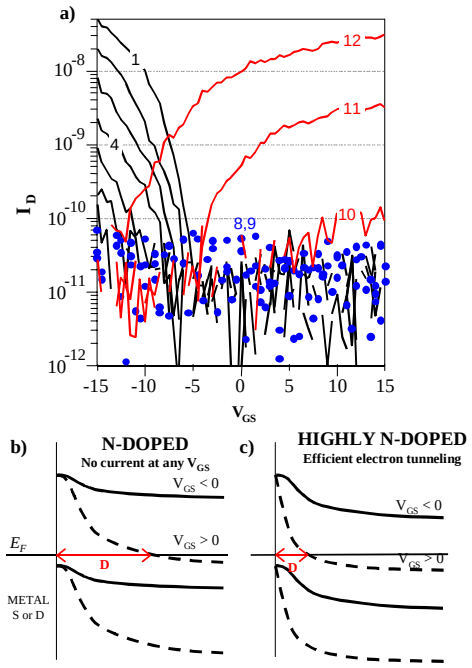

Figure 6. a) Effect of potassium doping on a CNFET. The FET is initially p-type. Doping is done by step from 1 to 12. For higher doping level, the device becomes n-type (red curves 10-12). b) and c) Schematic of the bands in the region of the metal-nanotube contact. b) The case of an n-doped CNFET that was not previously outgassed (curves 8-9), and c) the same but for a higher doping level. D corresponds to the barrier thickness.

5. Nanotube Logic Gates

Having developed ways to fabricate p- and n-type CNFETs with local gating, the next step is to produce integrated circuits out of them. Of particular interest are logic gates that form the basis of today's computer logic. Our approach is to use complementary CNFETs placed in circuit to operate simple logic functions. This kind of nanotube-based circuit is the analogue to the conventional CMOS based logic gates and has the same advantages. That is, logic circuits based on complementary devices aim to consume low power, favor higher gain, be stable, and allow easy implementation in integrated circuits. In this last section, we present our recent advances in making logic functions out of nanotube devices.

A simple example is presented in Fig. 7. By bonding together two ambipolar CNFETs stable in air, we fabricated a logic gate. An offset voltage (V_{shift}) between the isolated transistor back-gates allows adjustment of the threshold of the p- and n-CNFET characteristics so that the inversion function is optimal. The response of this circuit is abrupt and the operating voltage is well below 5V.

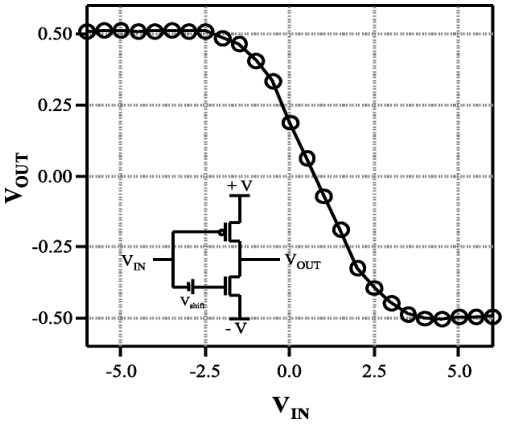

Figure 7 Logic device ("NOT" gate) made with two ambipolar CNFETs. The circuit consists of an inverter device shown in the inset (|V|=0.5V). An oxide layer protects the devices so that the inverter circuit functions in air. [19]

However, the ultimate integration in nanotube electronics would be to build a circuit along the length of the same nanotube, i.e. produce an *intra-nanotube* logic circuit. We were able to implement this integration as shown in Figure 8. The top of Fig. 8 shows an atomic force microscope (AFM) image of a small single-wall nanotube bundle deposited on top of gold electrodes. The entire device is covered by a polymer film (PMMA). Then, a window is opened in the PMMA using electron beam lithography. Last, potassium is used to dope half of the bundle through this window to produce an n-CNFET, while the other CNFET, protected by the PMMA film, remains p-type. The doping is adjusted so that the thresholds for switching of the p- and n-CNFETs overlap. This design indeed leads to an intra-molecular NOT gate. The relative position of the two thresholds voltages was adjusted by choosing the appropriate doping level.

Although the intra-nanotube inverter shown in Fig. 8 is not optimized in terms of structure, it has already a gain of about 1.6. Therefore, its output can be used to drive another gate or a more

complicated logic circuit. However, the gain of the gate depends solely on the characteristics of the CNFETs. As shown before, the improvements in the CNFETs and their device geometry (in particular the gate oxide) will further increase the performance of the nanotube-based inverter.

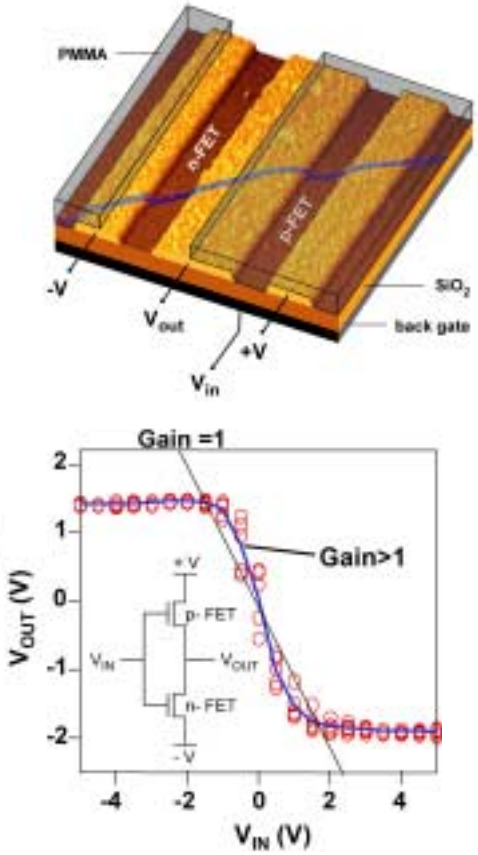

Figure 8. Intra-nanotube inverter. Top: AFM image of the device. A single-wall nanotube is placed to bridge several gold electrodes and produces two p-type CNFETs along the same tube. Then, the CNFETs are patterned with resist (PMMA) and doped selectively with potassium. The window in the PMMA allows the conversion of only one device into n-CNFET. The other is protected and remains p-type. Bottom: Characteristics of the intra-molecular inverter (V= ±2V). The straight line corresponds to an output/input gain of one.

6. Conclusion and Perspectives

The prospect for nanotube-based electronics is attractive but it is not realistic to expect new products soon. Several issues need to be resolved. For example, as-grown nanotubes come in a mixture of semiconducting and metallic types. There is currently no method to selectively separate them. Moreover, there is still no effective ways to make controlled arrays of nanotubes. In addition, as much as we have learned to date, the understanding of the physics of the nanotube devices is also at an early stage. Furthermore, significant advances in processing the material and in controlling the chemistry of nanotubes are needed. Nevertheless, the nanotube transistors show very high performance and integration capabilities. The use of independent gates, such as the top-gate device in Fig. 2 or local bottom-gate structures as in Ref [8], and the capability to make complementary devices allow for the construction of more complex circuits. Overall, the nanotube presents all the desirable properties needed for future electronic applications.

7. ACKNOWLEDGMENTS

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