Carbon nanotube memory devices of high charge storage stability

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Molecular memory devices with semiconducting single-walled carbon nanotubes constituting a channel of 150 nm in length are described. Data storage is achieved by sweeping gate voltages in the range of 3 V, associated with a storage stability of more than 12 days at room temperature. By annealing in air or controlled oxygen plasma exposure, efficient switching devices could be obtained from thin nanotube bundles that originally showed only a small gate dependence of conductance.
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Recent progress in the assembly of a small number of molecules between two electrodes in sandwich configuration has resulted in electrical devices revealing switching behavior[1,2] or negative differential resistance.[3] These achievements strongly encourage the development of molecular electronic devices[4] with the potential to overcome the limitations of silicon-based microelectronics.[5] Single-walled carbon nanotubes (SWCNTs), with a diameter in the nanometer range and a length of several micrometers, are especially attractive for that purpose due to their electronic, mechanical, and chemical properties.[6] To date, a number of molecular devices have been realized with SWCNTs, including field-effect transistors,[7,8] room-temperature single-electron transistors,[9,10] logic gate circuits,[11] inverters,[12] and electromechanical switches.[13,14] Very recently, the first prototypes of memory devices based on SWCNT field-effect transistors were also reported.[15,16] Here, we report easy-to-fabricate SWCNT memory devices exhibiting an extraordinarily high charge storage stability of more than 12 days at room temperature.

In our experiments, SWCNT raw material (arc–discharge product purchased from Carbolex®, Lexington, USA) was dispersed in an aqueous surfactant solution (1 wt % lithium-dodecylsulfate), and purified by centrifugation. The tubes were then deposited on a highly Sb-doped silicon wafer with a 100 nm thick thermally grown SiO_2 layer previously surface modified by amino-silanization. Typically one third of the deposited objects are individual SWCNTs, whereas two thirds consist of small SWCNT bundles with a diameter in the range of 2–4 nm. Source and drain contacts (15 nm AuPd without any adhesion layer), separated by ~150 nm, were defined on top of the SWCNTs by electron-beam lithography. The n^+-doped Si wafer was used as the back gate. All electrical measurements were performed under ambient conditions, except for the temperature dependence which was studied with the sample in a vacuum ($p=10^{-4}$ mbar).

A significant fraction (~50%) of the investigated semiconducting SWCNTs (thin bundles) revealed memory effects, as reflected in reproducible hysteresis in the drain current (I_D) versus gate potential (V_G) characteristics. A representative example is displayed in Fig. 1(a), which shows the I_D-V_G curve of an individual SWCNT (~2 nm in height) at room temperature. The gate voltage was swept continuously from 0 to +3 V, then to −3 V, and back to 0 V, corresponding to the loop ①→②→③→④→①. The observed conductance decrease for increasing gate potential is in accordance with the known *p*-type semiconducting behavior of air-exposed SWCNTs.[7,17] The two conductance states at $V_G=0$ V (points ① and ③) differ by more than two orders of magnitude, associated with a threshold voltage shift of 1.25 V. The reversibility of switching between the high con-

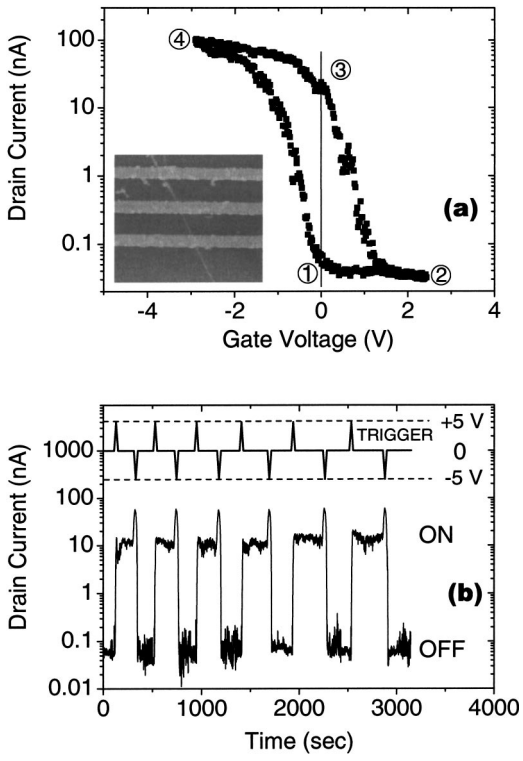

FIG. 1. Memory effects observed at room temperature in an individual SWCNT with a diameter of ~2 nm. The bias voltage V_{bias} is 10 mV. (a), Hysteretic behavior of drain current as a function of gate voltage. A threshold voltage shift of ~1.25 V is observed upon sweeping the gate voltage along the points ①→②→③→④→①. The inset on the left-hand side shows the atomic force microscopy image of the nanotube between electrode lines separated by ~150 nm. (b), Switching behavior of the memory device at $V_G=0$ V by triggering the device with the gate voltage signal shown in the inset. The peaks observed when the device is switched from the ON to the OFF state correspond to the maximum drain current at the gate voltage of −5 V.

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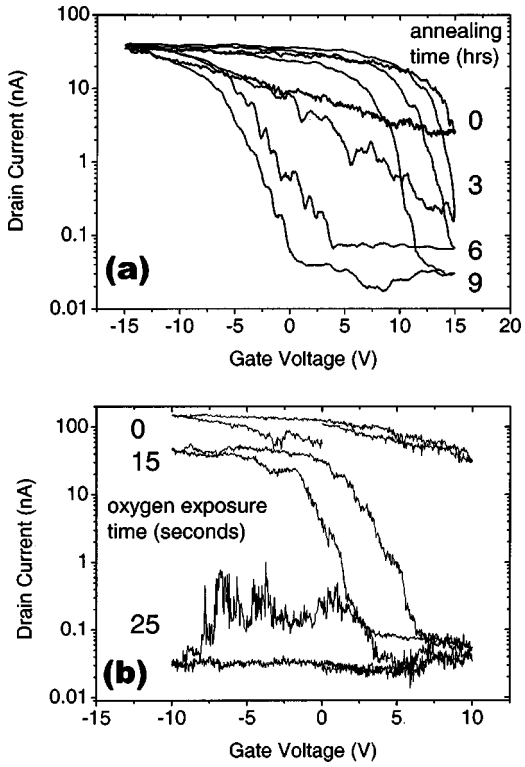

FIG. 2. (a), Evolution of memory effects in a thin SWCNT bundle upon thermal annealing at 335 K in air. The different loops correspond to the data obtained at room temperature with $V_{bias}=1$ mV after annealing for 0, 3, 6, and 9 hr, respectively. (b) Memory effects for a thin SWCNT bundle at room temperature after subsequent oxygen plasma treatments. The three curves correspond to the data obtained with $V_{bias}=10$ mV after plasma exposure for 0, 15, and 25 s, respectively.

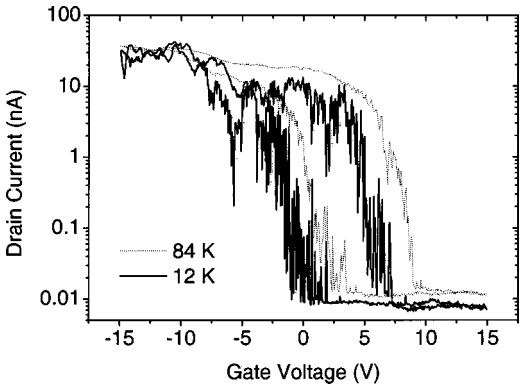

FIG. 3. Low-temperature (84 and 12 K) memory effects in the annealed SWCNT bundle of Fig. 2(a).

ductance (ON) and low conductance (OFF) states within the SWCNT device is demonstrated in Fig. 1(b). The two stable states at $V_G=0$ V can be reproducibly adjusted by triggering the device with the gate voltage signal (varying between ± 5 V) displayed in the inset. When the devices were held at zero-gate voltage or removed from the sample holder, and stored under ambient conditions, both the ON and OFF state turned out to be stable over a period of at least 12 days.

Memory devices of the same high storage stability could be obtained also from thin SWCNT bundles which consisted of a mixture of semiconducting and metallic tubes, and therefore showed only a weak gate dependence of conductance. For that purpose, two different methods proved to be effective. In the first case, the samples were heated for several hours in air. Figure 2(a) illustrates the evolution of hysteretic behavior of a SWCNT bundle subjected to three annealing steps, performed at 335 K for 3, 6, and 9 h in total, respectively. While before annealing, no clear hysteresis loop was observed within the gate voltage range of ± 15 V, pronounced memory effects are found after 6 h annealing. The ratio between the current in the ON and OFF state has increased from 10 at the beginning to more than 10^3 after 9 h of annealing. It is further noticed that although the OFF current is significantly decreased upon annealing, the ON current remains almost unchanged. Noteworthy, SWCNT bundles revealing similar hysteresis at the beginning as in Fig. 2(a), but annealed in a vacuum ($p=10^{-7}$ mbar) at 340 K for 9 hr, displayed only little change in the I_D-V_G curves.

The second method involves controlled oxygen plasma treatment at room temperature. Starting from a thin SWCNT bundle with small gate dependence, corresponding to the top curve in Fig. 2(b), a significantly increased gate dependence and hysteresis were obtained after 15 s of oxygen plasma treatment (50 W, oxygen pressure 0.5 mbar). As can be seen from the middle loop, the conductance of the plasma-modified bundle can be modulated via the gate potential over almost three orders of magnitude. For longer plasma treatments, destruction of the nanotubes became apparent. The bottom loop indicates that after 25 s of oxygen plasma exposure, the conductance of the bundle has decreased by more than three orders of magnitude, and no regular hysteresis can be detected any more.

The changes observed in Figs. 2(a) and 2(b) could be explained by two possible effects of the heat treatment in air and the exposure to oxygen plasma. First, the metallic tube(s) within a SWCNT bundle may be preferably oxidized under these conditions, resulting in an increased gate dependence due to the remaining, intact semiconducting tubes. Second, oxidation-related defects are likely to be formed in the remaining amorphous carbon particles on the bundle surface, in the originally intact metallic tubes within a bundle, or at the SiO_2 surface.[15] These types of defects could act as charge storage traps, and their close proximity to the surface of the semiconducting SWCNT(s) would account for the large threshold voltage shifts observed for small gate potentials. Charge carriers injected from the SWCNT(s) into these traps will allow the devices to function similar to electrically erasable, programmable, read-only memories.[18] That such closely attached charge storage units are indeed responsible for the memory effects is supported by electrical measurements at low temperatures. This is exemplified in Fig. 3, which shows data obtained from the same bundle as in Fig. 2(a). Although at 12 K, the threshold voltage shift is reduced by a factor of ~ 2 as compared to room temperature, the switching between the ON and OFF states differing by more than three orders of magnitude in conductance is still existent at lower temperatures. Reproducible switching was detected down to 5 K. It is noticed that the curve measured at 12 K displays numerous sharp peaks originating from single-electron charging of the tube, which is generally observed at sufficiently low temperatures.[19] The persistence of hysteresis at low temperature excludes that mobile ions within the SiO_2 insulator are the origin of the memory effects, since ion hopping is frozen out at liquid-helium temperature due to the

high associated activation energies in the range of 0.4–0.6 eV.[20] The memory effects observed in the SWCNTs before intentional modification (Fig. 1) may also be related to oxidation-related defects as charge storage sites, in this case, introduced by slow reaction with air at room temperature.

The two presented methods used to fabricate nanoscale memory devices from SWCNT bundles are technologically straightforward, and avoid the need to separate SWCNT bundles from individual SWCNTs during sample preparation. The obtained devices can be reversibly switched between bistable states by small gate potentials, and exhibit a high storage stability of >12 days at room temperature. Although the chemical nature of the modifications deserves further careful investigation, the memory devices represent a significant extension of the range of SWCNT applications. When assembled into large arrays, the SWCNT switching elements could be used as key building blocks for low-cost memories with ultrahigh storage densities. Improved device characteristics may be achieved via more defined SWCNT modifications, for example by chemical attachment of functional groups capable of charge storage.

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