

2-1-2008

Carbon nanotubes for high-performance electronics - Progress and prospect

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Carbon Nanotubes for High-Performance Electronics—Progress and Prospect

The prospect, for nanotube field effect transistors that can compete with silicon technology, is extremely promising but critical tasks still lie ahead.

By J. APPENZELLER, Senior Member IEEE

ABSTRACT | Carbon nanotube devices offer intrinsic advantages for high-performance logic device applications. The ultrasmall body of a carbon nanotube—the tube diameter—is the key feature that should allow aggressive channel length scaling, while the intrinsic transport properties of the nanotube ensure at the same time high on-currents. In addition, the narrowness of the tube is critical to implementation of novel device concepts like the tunneling transistor. By understanding the unique capabilities of carbon nanotubes and using them in unconventional designs, novel nanoelectronic applications may become feasible. However, much better control of materials quality must be obtained, and new fabrication processes must be developed before such applications can be realized.

KEYWORDS | Carbon nanotube; nanoelectronics; one-dimensional transport; tunneling device

I. INTRODUCTION

With the field of nanoelectronics still in its infancy, the challenges to the realization of practical applications are becoming more obvious. In the past, merely demonstrating the operation of a device was of interest, but attention is beginning to shift toward issues such as performance relative to established devices and technologies. Eventually, practical matters of cost and manufacturability will become central. This is true in particular for carbon

nanotubes, which have been extensively explored as electronic materials over the last five years or so. Here we review the current understanding of the promise of carbon nanotubes for electronic applications. We conclude with a brief sketch of some outstanding problems in the development of a practical high-performance carbon nanotube device technology.

We focus on field-effect transistors (FETs) that make use of semiconducting carbon nanotubes as channel material between two metal electrodes that act as source and drain contacts. It is often stated that the smallness of carbon nanotubes should enable high levels of integration. However, to compete with the established silicon device technology, it is important that the new material offer additional advantages such as high speed and low power consumption.

II. NANOTUBES FOR A HIGH ON-STATE PERFORMANCE

In general, switching speeds of FETs can be improved in two distinct ways [1]. The dominant approach, pursued now for many decades, is to reduce the device dimensions. The classical scaling scheme ensures that all fields, the drain as well as the gate field, are scaled simultaneously by adjusting gate-oxide thickness, junction depth, and doping level together with the gate length. The performance improvement in this case is a result of the possibility to reduce the supply voltage without sacrificing the on-state current level. The second approach to improved switching speed is the improvement of material properties, particularly the mobility of electrons and/or holes.

Manuscript received November 2, 2006; revised August 2, 2007.
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Digital Object Identifier: 10.1109/JPROC.2007.911051

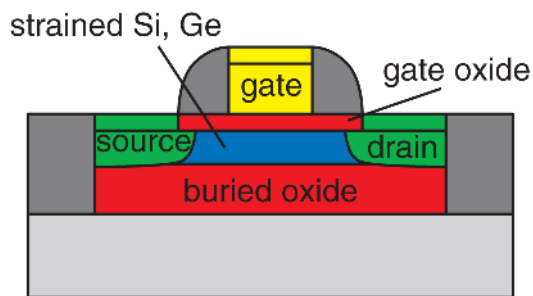


Fig. 1. Schematic of a transport enhanced MOSFET. Through the introduction of strained silicon or germanium higher channel mobilities, and thus a better on-state performance of the device, are achieved.

Interestingly, experience suggests that shrinking conventional semiconductor devices to very small dimensions comes at the expense of a reduced channel mobility. Consider the use of strained silicon or germanium as channel material as sketched in Fig. 1. Reduction of the channel length must be realized while preserving so-called long-channel device characteristics (where the gate field rather than the drain field controls the electrostatics inside the transistor channel). In the past this has been accomplished by simultaneously scaling the gate length L_g and the gate oxide thickness t_{ox} . But with gate-oxide thicknesses approaching 1 nm, gate leakage currents prevent a further reduction. Although the introduction of new high-dielectric-constant (high-k) gate insulators may help, the most important option left at this point is to reduce the thickness of the channel t_{body} itself. This is the reason why ultrathin body devices such as FinFETs (see Fig. 2) have received increasing attention in recent years [2]. However, various studies [3] have shown that reducing the body thickness of the channel comes at the price of a reduced mobility, primarily due to an increase in surface roughness scattering. For a silicon structure with $t_{body} \approx 1$ nm, Uchida *et al.* [4] find, e.g., a mobility reduction by a factor of four in case of an n-type silicon metal–oxide semiconductor (MOS) FET. The same trend is to be expected using

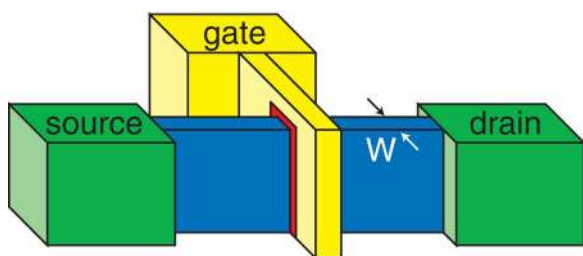


Fig. 2. Sketch of a FinFET structure with the gate impacting the two sides of the fin simultaneously. The important length scale, the “body thickness” t_{body} , is the width W of the fin.

alternative channel materials that allow for an improved on-state performance in a bulk-type device. So far, it has not been demonstrated that both high mobilities and ultrathin body channels with dimensions of just a few nanometers can be attained in a planar structure.

On the other hand, body thicknesses as small as a few nanometers are indeed desirable from an electrostatics standpoint. The screening length λ derived for a planar gate, planar channel geometry, such as a single-gated MOSFET on silicon on insulator is [5], [6]

$$\lambda = \sqrt{\frac{\epsilon_{body} \cdot t_{body} \cdot t_{ox}}{\epsilon_{ox}}} \quad (1)$$

For a body thickness of $t_{body} = 1$ nm, $t_{ox} = 1$ nm and an epsilon ratio of $\epsilon_{body}/\epsilon_{ox} = 3$, one can calculate with the help of (1) a screening length of around $\lambda = 1.5$ nm. With the rule of thumb that the actual gate length should be approximately three times larger than the length scale λ on which potential variations occur, this should allow L_g to be reduced to around 4.5 nm.

A. Optimum Device Design

In the context of the above discussion, carbon nanotubes (CNs) offer an obvious intrinsic advantage. They are the ideal combination of a high mobility, ultrathin body channel if used in a CNFET design as shown in Fig. 3. The figure depicts a coaxially gated CNFET structure—a device that has not been realized experimentally so far but has been simulated extensively [7], [8]. A dielectric film (red) is wrapped around a portion of an undoped semiconducting nanotube. A metal gate (yellow) surrounds the dielectric. Portions of the tube (blue) are ungated to reduce parasitic contributions [9] from the overlap between the gate and the source/drain contacts (green). Those ungated regions have to be heavily doped to allow for a low series resistance in the on-state. (It is worth noting that while doping of carbon nanotubes has been explored by various groups [10]–[13], critical requirements in the context of high-performance devices have still not been met.¹) This device design would allow optimum gate control and thus the most aggressive gate length scaling. At the same time, the carbon nanotube ensures through its intrinsic property of ballistic transport over several hundred nanometers at room temperature [14]–[16] and a large carrier velocity of around $8 \cdot 10^7$ cm/s [17] large currents in the transistor on-state.

While gate-all-around silicon nanowire FETs with excellent performance specs have already been demonstrated [18], [19], experimental demonstration of a

¹For device applications, high doping levels need to be achievable in a controllable and reproducible way. Moreover, dopants need to be immobile, air stable and need to withstand postprocessing at least up to a couple of hundred degrees Celsius.

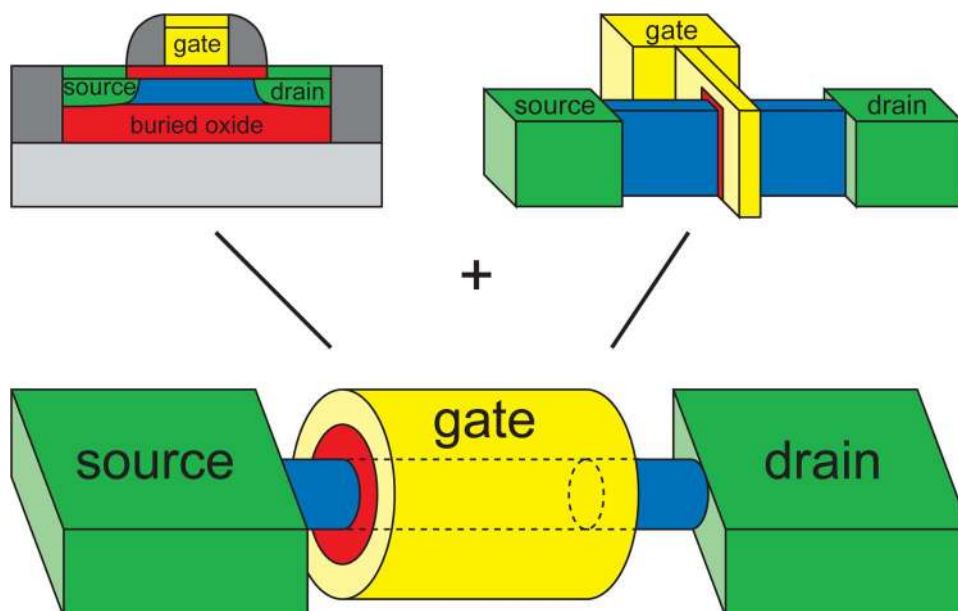


Fig. 3. Combining the right type of high-mobility channel material with an ultrathin body semiconductor allows for improved on-state performance.

coaxially gated CNFET is still evolving. After the initial demonstration of transistor operation in 1998 [20], [21], more sophisticated device designs with individually gated nanotube transistors and improved device performance were soon reported [22]–[24]. Today's CNFETs reach transconductance values g_m per tube in the 10–20 μS range [25], [26] with theoretically predicted values as high as $\sim 60 \mu\text{S}$ for reasonably scaled gate capacitances [7]. Since channel widths are only $\sim 1 \text{ nm}$, these transconductances are substantially larger per unit width than those reported in any other material system.

A recent example of a CNFET is shown in Fig. 4. The design that has been adopted with the gate on top of [27]

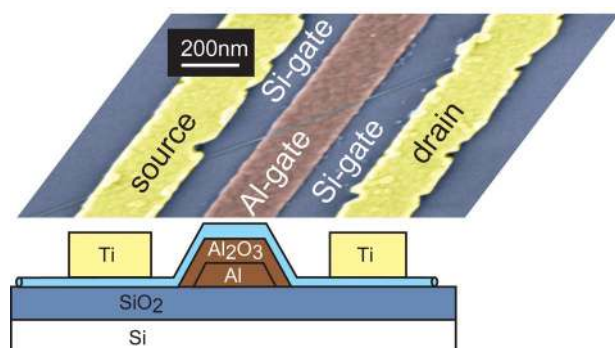


Fig. 4. Scanning electron microscope of a dual-gate CNFET. Both the silicon substrate and the local aluminum gate allow electrostatic control of the nanotube channel. The schematic below shows the vertical arrangement of gates, contacts, and the nanotube.

and underneath the nanotube [28], [29] resembles to a large extent the CNFET sketched in Fig. 3. Conventional looking device characteristics are obtained when the silicon gate is biased sufficiently negative (to simulate high p-type doping) and the aluminum gate is swept. Fig. 5 shows the subthreshold characteristics of the dual-gate CNFET with an excellent inverse subthreshold slope of around $S = 65 \text{ mV/dec}$. The main difference between the dual gate device and the coaxially gated CNFET is that the latter will ultimately allow for the most aggressive channel length scaling. Consequently, various groups are working on ways to create a uniform dielectric layer around a carbon nanotube [30], [31].

By means of atomic layer deposition, Farmer and Gordon [31] even managed to wrap both a thin aluminum oxide layer and a tungsten nitride metal layer around a carbon nanotube—a critical step towards a coaxially gated CNFET.

B. Contact Formation in CNFETs

In addition to gate control, it is equally important for high-performance nanotube devices that proper contact formation is ensured. To explore the impact of various contact materials on the CNFET performance, Chen *et al.* [32] have built around 100 nanotube devices with three different types of metal electrodes. Source/drain contacts from palladium, titanium, and aluminum were used to study the CNFET on-state performance. Interestingly, it was found that despite identical processing, devices with the same type of contact material still exhibited on-currents I_{on} that differed by orders of magnitude. Through

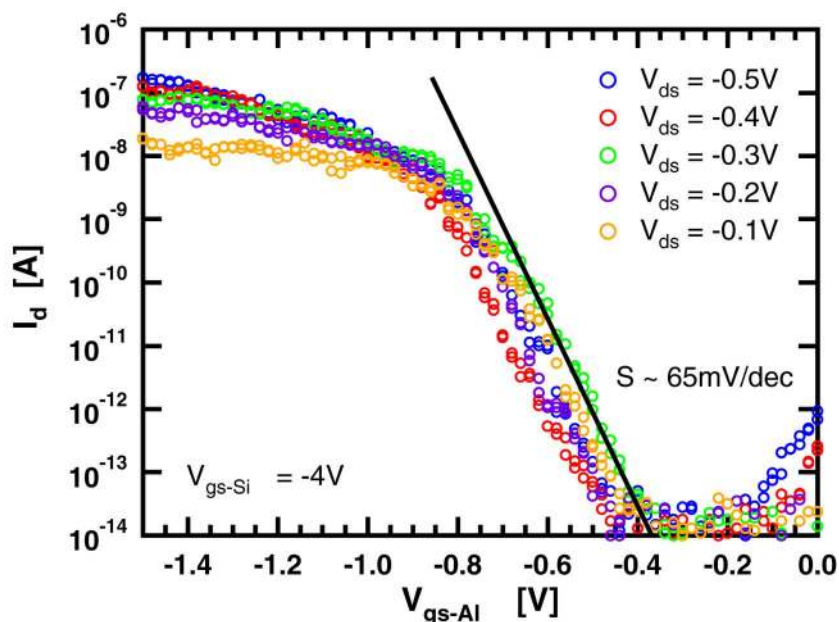


Fig. 5. Subthreshold characteristics of the dual-gate CNFET at room-temperature. The silicon back gate is biased at $V_{gs-Si} = -4$ V while the aluminum gate voltage is varied.

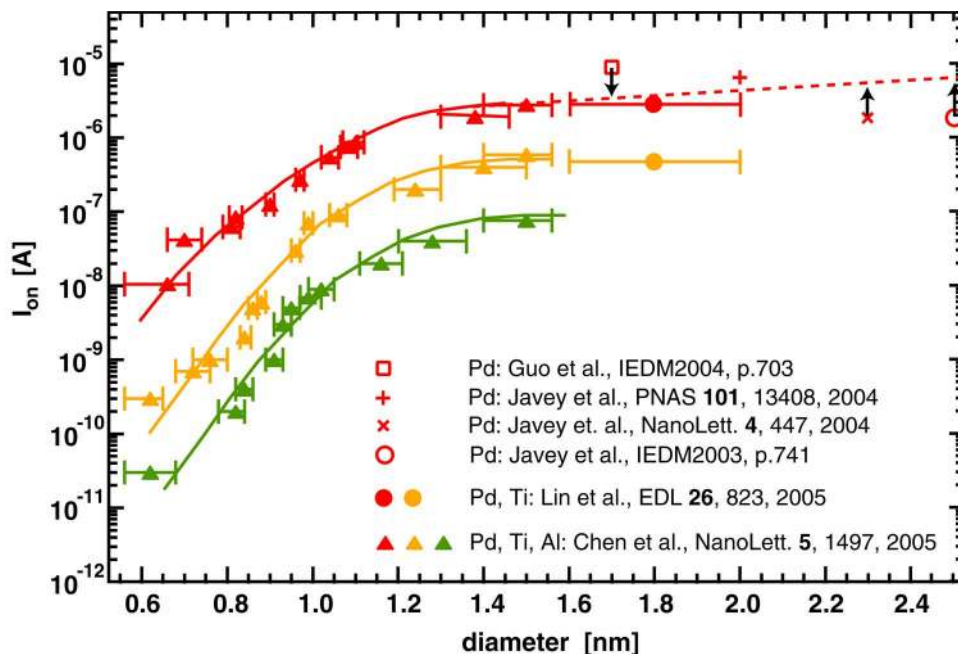


Fig. 6. Diameter and workfunction dependence of the CNFET on-current for a variety of samples from different sources.

detailed study of the nanotube diameter distribution by transmission electron microscopy (TEM), the authors were able to separate the impact of the two critical parameters—the tube diameter t_{body} and the contact metal work function Φ_M —on the transistor on-current. Fig. 6 summarizes the findings. In the plot, I_{on} is evaluated at a

supply voltage of $V_{dd} = 0.5$ V for p-type CNFET devices.² Note the two important trends: 1) I_{on} increases with

²It is important to note that nanotube devices without doping and a gate that impacts the entire tube channel, including the contact areas, always show both n-type and p-type behavior at the same time, as is discussed in detail [33].

increasing nanotube diameter t_{body} and 2) I_{on} increases with increasing Φ_{M} ($\Phi_{\text{Pd}} > \Phi_{\text{Ti}} > \Phi_{\text{Al}}$).

Both of the trends can be easily understood within the framework of Schottky barrier dominated transport in CNFETs [34], [35]. The smaller the nanotube bandgap and the larger the workfunction of the metal that is used as contact material, the lower the Schottky barrier at the metal contact/nanotube interface to the valence band. A p-type device exhibits high on-current levels under these conditions. A small bandgap arises for tubes with a large diameter and consequently a larger t_{body} results in an increase of I_{on} . The universal character of the plot becomes apparent when considering that nanotubes from different sources all follow the same trend. Tubes, e.g., produced by means of an arc-discharge [25] generally exhibit diameters of 1.6–2 nm and show a much narrower on-current distribution if used in a field-effect device design than tubes produced by the method of laser ablation [36] with significantly smaller diameters. Electrical data from other groups (see history within Fig. 6) also support the main picture that current variations from device-to-device are less processing related than previously assumed but instead strongly depend on t_{body} . The arrows at some of the data points indicate that different gate oxide thicknesses, channel lengths, and/or drain voltages were used for those CNFETs and that the extracted on-currents would have to be corrected accordingly for a fair comparison.

C. AC Characteristics and Capacitance Considerations

All of the preceding discussion is relevant to the dc performance of CNFETs while it is, of course, the high frequency response that matters. However, measuring the ac performance of CNFETs cannot employ conventional measurement schemes. The input impedance of a nanotube transistor even with ideal contacts is much larger than 50 Ω and the associated gate capacitance C_g , typically in the attofarad range, is much smaller than what can be resolved with a conventional measurement setup. At the same time, it is rather challenging to keep parasitic capacitance contributions smaller or comparable to C_g . This is why the first reports on ac performance of CNFETs did not appear until 2004 [37], [38].

Fig. 7 illustrates how these measurements were performed in a rather unconventional way. The idea is that the dc current of a device can be impacted by an ac voltage contribution if the associated IV-characteristic is nonlinear. Applying a voltage V_{ac} effectively results in a larger measurable dc current I . This is true as long as the corresponding ac signal can propagate inside the device structure. Observing the dc signal of an FET structure can thus provide insights into its ac performance. Fig. 8 shows an actual measurement of the current change as a function of the gate voltage V_{gs} for different frequencies. The ac signal is applied to the source of the CNFET.

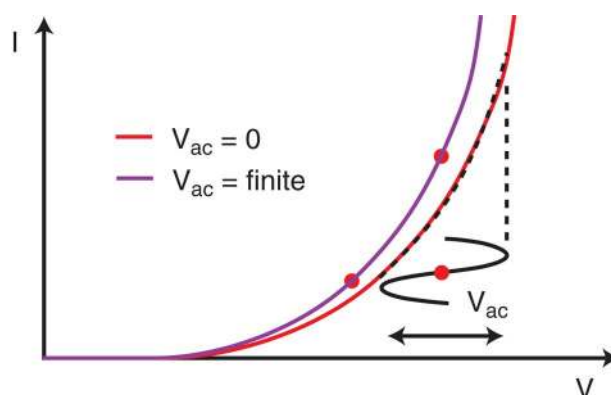


Fig. 7. The graph illustrates how an ac voltage V_{ac} superimposed on a dc bias V results in a measurable change of the dc current signal for nonlinear device characteristics.

Between 1 and 580 MHz, the curves all show effectively the same change in I_d . Up to this frequency, the device operates without any signal deterioration that would result in a decrease of the device current level towards the curve labelled “no ac.” The maximum reported frequency of 580 MHz measured with this approach is limited by the measurement setup and not the intrinsic tube properties.

Progress after this initial demonstration has been rapid. Measurements with a frequency up to 2.6 [39], 8 [40], 12 [41] (note that both semiconducting and metallic nanotubes contributed), and 50 GHz [42] have been reported. However, experimental data still do not reach the predicted terahertz performance range [43]. At this time, there is still a strong need to obtain further information about the intrinsic ac performance limits of CNFETs.

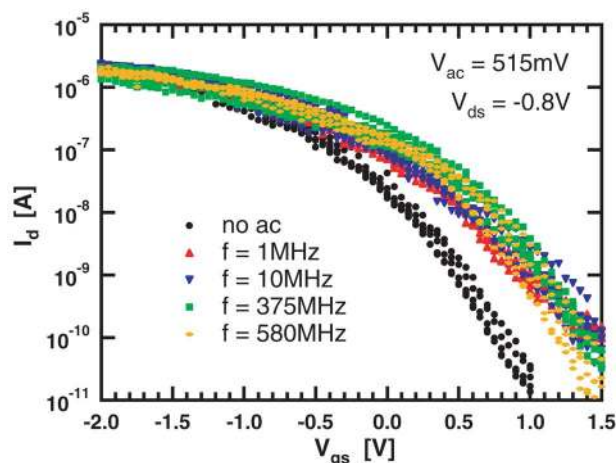


Fig. 8. Actual measurement on the ac response of a carbon nanotube transistor.

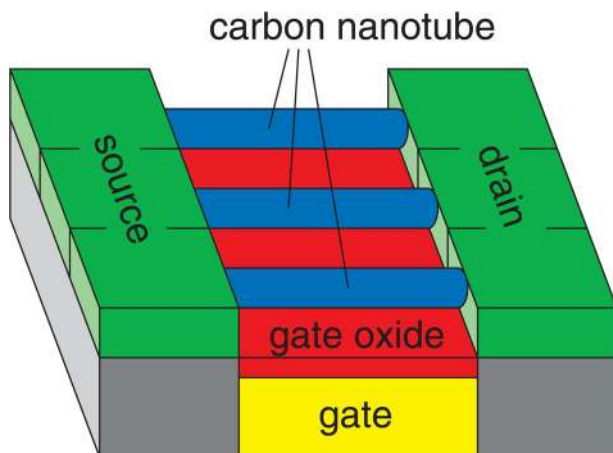


Fig. 9. Schematics of a gated array of carbon nanotubes. The total current is enhanced by utilizing several nanotubes in parallel.

A device geometry that would be desirable in this context is sketched in Fig. 9. By using several nanotubes in parallel, the sample impedance is reduced while the total gate capacitance is increased. If the device layout ensures at the same time that parasitic capacitance contributions are not too large, a structure as shown will prove useful in a more conventional S-parameter measurement. More details about current key problems and envisioned solutions are addressed in the later sections.

D. A CNFET-Based Ring Oscillator

The fabrication of circuits is an important benchmark in the development of carbon nanotube devices. In 2006,

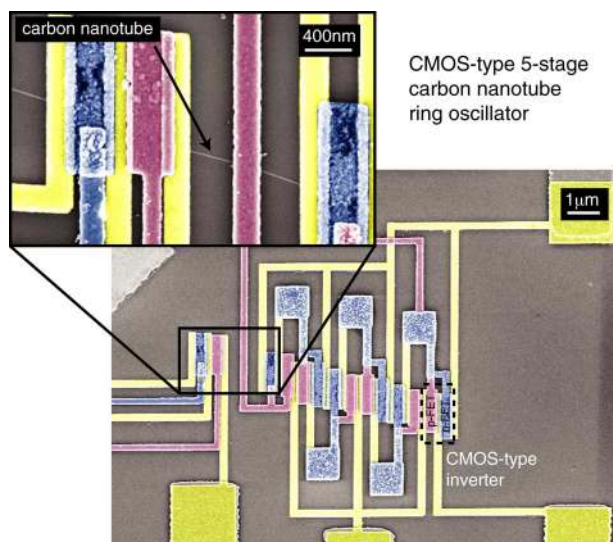


Fig. 10. Implementation of a CMOS-type five-stage ring oscillator on a single carbon nanotube.

Chen *et al.* [44] demonstrated the first complete circuit on one individual carbon nanotube. The circuit, a ring oscillator, that is shown in Fig. 10 consists of 12 individual nanotube transistors, with six of them operating as p-type FETs (purple colored gates) and six as n-type FETs (blue colored gates).

Five pairs of p- and n-CNFETs are used to create the five inverter stages. The sixth inverter (marked by the dashed square in Fig. 10) operates as a readout stage. The signal from this inverter is input into a spectrum analyzer to monitor the frequency response of the ring oscillator (RO). The main breakthrough that made this application possible is again related to the unique properties of nanotubes. As has been discussed in Section II-B, the metal workfunction of the source/drain electrode can substantially impact the device on-state by means of the metal Fermi level lineup with the semiconducting nanotube. For the ring oscillator, the same property was employed to adjust the threshold voltage of the p-type and n-type FETs. By using two types of metal gates, palladium and aluminum, one segment of the same undoped nanotube was used as a p-type CNFET while the other one operates as an n-type CNFET. Since dopant fluctuations in the channel of conventional silicon devices can become a serious issue for scaled FETs, adjusting the device characteristics without the introduction of dopants is desirable. A one-dimensional system as a nanotube does not suffer from surface state pinning [45], and the impact of the metal gate workfunction directly translates into a threshold voltage shift of the CNFET device characteristics, as has been experimentally demonstrated in the context of the RO for the first time.

The spectrum measured with the CNFET ring oscillator showed a frequency response up to 72 MHz [46]. While this result is still far below the expected intrinsic response of nanotubes as discussed in Section II-C, it is quantitatively understandable exclusively as a result of the circuit layout. Taking into account the build-in parasitic contributions due to wiring and gate-to-source/drain overlap as well as the circuit-to-substrate capacitance, the expected frequency response can indeed not exceed the measured value. The intrinsic nanotube properties are thus not limiting the circuit performance at this point in time, and an improved circuit layout can be expected to substantially improve the ac performance of next-generation nanotube-based circuits.

III. NANOTUBE DEVICE CONSIDERATIONS FOR REDUCED POWER CONSUMPTION

Having discussed the on-state performance of CNFETs in the previous sections, this section focuses on device designs for reduced power consumption. It is once more the particular transport in nanotubes that lends itself to a novel type of device concept. As discussed in Section II,

the screening length λ can be on the order of nanometers in carbon nanotubes due to their small body thickness—the nanotube diameter. Since band-bending occurs on the length scale of λ , potential barriers in nanotube-based devices are typically very thin, and tunneling phenomena are very pronounced in all types of CNFETs [47]. While in most instances rather undesirable, the device concept described below makes explicit use of the tunneling properties in CNFETs.

The transistor structure that enables the so-called tunneling CNFET (T-CNFET) consists of a sequence of n-type, intrinsic, and p-type doping, as illustrated in Fig. 11, and has been proposed recently as a viable device concept for carbon nanotubes [47], [48]. Its operation can be understood as follows: the device is in its off-state if the gated intrinsic portion of the nanotube prevents current flow between the two highly doped areas (n-type on the left and p-type on the right). This is the case for $V_{gs} = -0.25$ V, half of the applied drain voltage of $V_{ds} = -0.5$ V, as displayed in Fig. 11. The device turns on for more negative drain voltages. At $V_{gs} = -0.65$ V, for example, the intrinsic portion of the semiconducting tube is moved sufficiently upwards to allow for hole injection from the n-type region of the nanotube by band-to-band (BTB) tunneling into the intrinsic part indicated by the arrow in Fig. 11.

The most important aspect is that the transition between the device on-state and off-state is accomplished with a change of gate voltage ΔV_{gs} that is smaller than what is needed for a conventional MOSFET to change the

current by the same amount. In other words, the inverse subthreshold slope S is smaller than ~ 60 mV/dec at room temperature. This becomes possible since the device off-state is no longer determined by the electrons or holes in the high energetic tail of the Fermi distribution as in conventional MOSFETs. In fact, the high energetic charges get back-reflected into the source while the carriers close to the Fermi level are most relevant for the band-to-band tunneling process. This effective “cooling” of the electronic system is the key for obtaining small S -values. While in principle, by utilizing BTB-tunneling, S -values smaller than 60 mV/dec are also achievable in silicon MOSFET [49], experimentally this situation has not yet been realized [50], [51]. Carbon nanotubes, on the other hand, offer the ideal combination of intrinsic properties such as ballistic transport, ultrasmall t_{body} , small effective masses for electrons and holes, and a direct energy bandgap to make gate-controlled tunneling a highly effective concept for T-CNFETs.

Experimentally, this n/i/p doping profile has not yet been demonstrated in a T-CNFET configuration. However, experimental evidence for the possibility to obtain inverse subthreshold slopes smaller than ~ 60 mV/dec has been obtained recently [52]. The nanotube device structure employed for this is shown in Fig. 4. By using the silicon back gate to effectively dope the nanotube segments close to the metal electrodes, a p/i/p doping profile is implemented. Scanning the voltage (V_{gs-Al}) at the aluminum gate in the middle of the device structure, a subthreshold characteristic as shown in Fig. 12 is obtained.

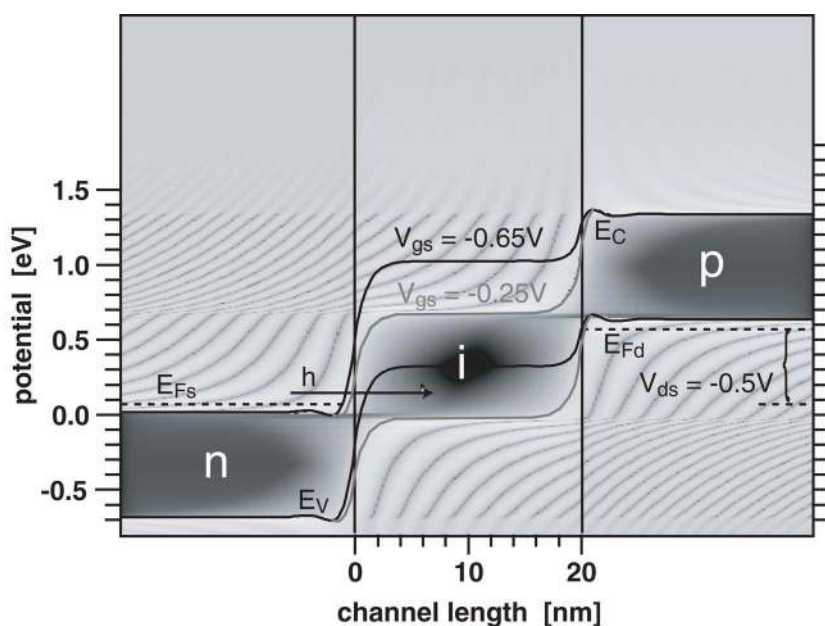


Fig. 11. Simulation of the conduction and valence band for a T-CNFET at $V_{ds} = -0.5$ V for two different gate voltages of $V_{gs} = -0.65$ V (on-state) and -0.25 V (off-state), respectively. The parameter set used for the calculation is $E_g = 0.7$ eV, $t_{ox} = 1$ nm, $t_{body} = 1$ nm, and $m^* = 0.1 m_0$.

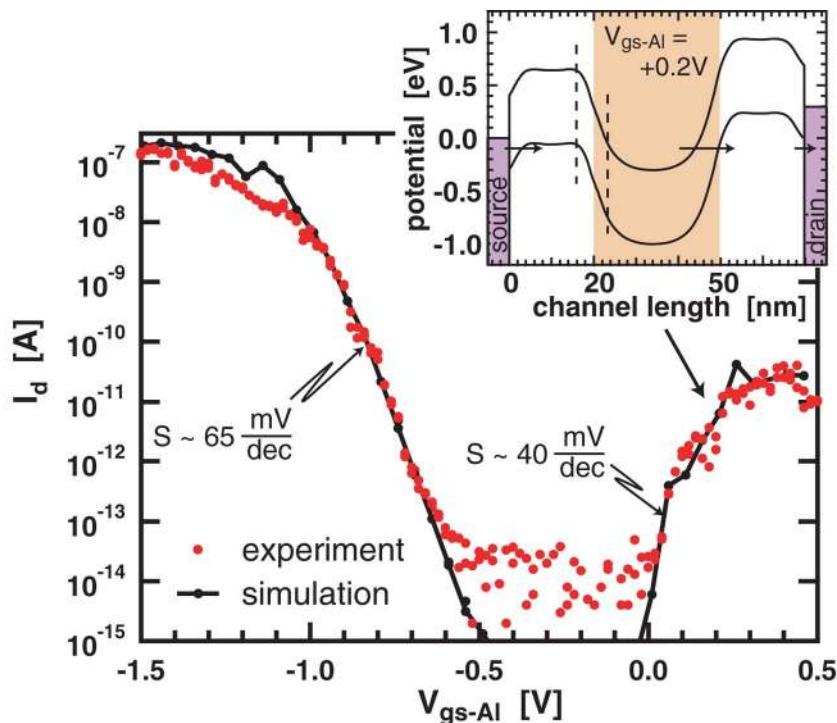


Fig. 12. Experimental and simulated $I_d(V_{gs-Al})$ for a drain voltage of $V_{ds} = -0.5$ V and $V_{gs-Si} = -3$ V. The upper inset shows the band bending situation under tunneling conditions from the simulation.

The red circles in Fig. 12 are data taken at room temperature. At negative V_{gs-Al} values, the device operates as a conventional p-type FET in the on-state. Increasing the aluminum gate voltage (making it more positive) turns the device off, similar to the situation in a conventional MOSFET. For even larger V_{gs-Al} , the band-to-band tunneling conditions displayed in the upper inset of the figure are reached. Holes injected from the source undergo two BTB-tunneling events before reaching the drain electrode. The crucial finding is that it is indeed possible in a gate-controlled tunneling process to obtain an inverse subthreshold slope substantially smaller than ~ 60 mV/dec—a proof of principle that the proposed T-CNFET concept is indeed a viable approach. In the displayed case, $S \approx 40$ mV/dec has been achieved.³ Moreover, Fig. 12 also shows the result of our simulations [52].

Simulations in Figs. 11 and 12 were carried out using the nonequilibrium Green's function (NEGF) formalism [54]. The charge in and current through the transistor are calculated self-consistently using the NEGF formalism together with a modified one-dimensional (1-D) Poisson equation according to Young [6]. The 1-D Poisson equation accounts for the impact of gate oxide thickness t_{ox} and tube diameter t_{body} on the electrostatics conditions inside the

nanotube channel. An effective mass description is adopted for the conduction and valence band, and the complex band structure in the semiconducting nanotube gap is taken into account by an energy-dependent effective mass [55]. For channel lengths below a couple of hundred nanometers, it is appropriate to assume ballistic transport conditions. Despite the fact that this approach simplifies the actual situation, excellent quantitative agreement between experiment and simulation is achieved, as apparent from Fig. 12. This indicates in particular that the main aspect of the tunneling device is indeed captured by the simulation.

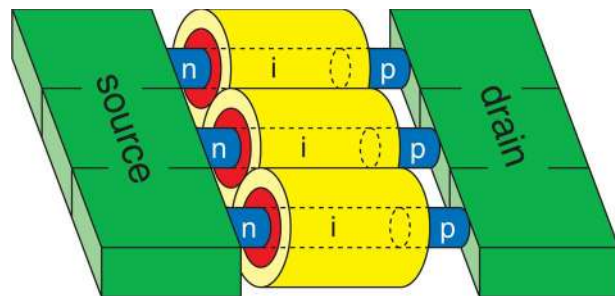


Fig. 13. Schematic of an array of coaxially gated T-CNFETs as envisioned for low power consumption applications. The parallel tube array ensures that reasonable current levels are attained.

³After submission of this manuscript, we became aware of a recently published paper [53] that demonstrated a T-CNFET exhibiting an S-value of 25 mV/dec.

The next important step is to combine the abrupt switching behavior through gate-controlled tunneling with a high on-current level in the device. While tunneling processes typically do not allow for a high transistor on-state performance, the intrinsic properties of nanotubes discussed above—in particular the small achievable value of λ —ensure reasonable currents per unit width [47]. Further increasing I_d is achievable by means of an array of FETs, as discussed in Section II-C. Fig. 13 shows a schematic of the envisioned array of T-CNFETs with the desirable n/i/p doping profile. For most aggressive length scaling, a coaxially gated transistor structure is used according to Section II-A.

IV. FUTURE PROSPECTS AND KEY PROBLEMS

With such promising results obtained in exploratory devices, it is time to consider the very difficult challenges that must still be met in order to fabricate practical high-performance devices and circuits. Indeed, many of the processes needed to build the preferred device structures sketched above simply do not exist, or exist in only rudimentary form. Great improvements and further invention will be needed in:

- 1) growth and placement:
 - a) controlled synthesis of nanotubes of given diameter and chirality or postgrowth separation of nanotubes by diameter and chirality;
 - b) lithographically templated placement of nanotubes;
- 2) enabling processes and technologies:
 - a) conformal deposition of ultrathin high-k dielectrics on nanotubes;
 - b) charge-transfer doping of nanotubes with a high degree of degeneracy;
- 3) devices and circuits:
 - a) development of low power circuits based on nanotubes' unique tunneling properties;
 - b) integration of nanotubes in circuit architectures that consider their one-dimensional character.

For example, all existing processes for synthesis or growth of nanotubes produce tubes with a range of diameters and

chiralities. Unless far more selective growth processes can be developed (along the lines of recent progress [56], [57]), the starting material will have to be purified. Progress in purification is being reported [58]–[61], giving hope that “electronic grade” nanotubes will eventually be available. Progress is also being made in chemical functionalization of nanotubes so that they will attach preferentially to lithographically patterned structures [62]–[65]. However, there is still a gulf between these promising early results and the extremely tight control of placement that would be needed to build a structure like that of Fig. 13. Moreover, devices as those displayed in Fig. 13 require a very tight gate control through ultrathin high-k gate dielectrics and extremely abrupt doping profiles. Further progress along the lines of the existing work discussed in Section II-A is urgently needed. Lastly, the various device ideas and considerations have to be translated into actual nanotube-based circuits. Those circuits should make use of existing architectures to the largest possible extent while at the same time benefiting from the unique nanotube properties. The ring oscillator design discussed above [44], [46] is just the first step in this direction.

V. SUMMARY

The discussion in the previous sections clearly highlights the uniqueness of carbon nanotubes for transistor applications. Both the demonstrated as well as predicted on- and off-state performance of tube-based devices is extremely promising. Tasks ahead that will have an immediate impact on nanotube devices are related to an improved control of doping profiles and the formation of arrays of CNFETs. The coaxially gated nanotube transistor is certainly one of the most critical demonstrations on the device level that is missing at this point in time. With future activities focusing more on the aspect of ac transport in carbon nanotube devices and circuit applications, critical insights will certainly become available in the near future. Lastly, it is worth noting that most of the findings discussed in the previous sections on logic also apply to analog applications, and the smaller amount of transistors needed for analog circuits may facilitate implementation. ■

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