Cascadable direct current driven skyrmion logic inverter gate

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Nanoscale skyrmions enable ultralow-power nonvolatile logic gate designs due to their current-driven motion and topological protection. A key building block in skyrmion-based digital spintronics is the logic inverter (NOT) gate. Despite recent computational and practical demonstrations, a skyrmion-based low-power, wideband, and cascadable inverter gate is still a long way off. For skyrmion-based logic circuits, a systematic design and analysis of an inverter gate is essential. Here we present a skyrmion logic inverter design and analyze its full operation using micromagnetic modeling. Because of the substrate thermal conductivity, our investigations reveal that the all-metallic inverter gate can function with direct current drive, wide bandwidth, submicron footprint, no or low external magnetic field, cascadability, and with room-temperature thermal stability despite Joule heating. Using magnetic insulators for eliminating Joule heating and lowering the exchange stiffness, magnetic moment and other factors might further assist in reducing power consumption by more than four orders of magnitude.

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I. INTRODUCTION

Magnetic skyrmions are chiral spin structures which stabilize in magnetic materials due to the competition between Dzyaloshinskii-Moriya interaction (DMI) and other energy terms such as Heisenberg exchange, uniaxial anisotropy, demagnetizing, and external magnetic fields [1–7]. Skyrmion lattices were first observed in noncentrosymmetric magnetic crystals like MnSi [8–11] and as single skyrmions in bi- and multilayers of magnetic materials and heavy metals [6,12]. The equilibrium diameters of skyrmions are smaller than 100 nm due to DMI and the perpendicular magnetic anisotropy terms. Skyrmions provide a rich materials and device physics for understanding and control by a total effective magnetic field via geometry or multilayers, applied voltage, external magnetic field, and current. The sub-100-nm dimensions of skyrmions make these spin structures promising signal carriers for high-density and low-power computation or memory applications [13,14]. The geometric extent of skyrmions allows for micromagnetic continuum models to realistically capture skyrmion physics and help avoid computationally demanding discrete quantum spin models [15]. Thus individual skyrmions, devices, and even scalable skyrmion logic circuits could be modeled using computational micromagnetics [13,15,16].

Previous studies on skyrmion logic devices consist of ungated logic by merging skyrmions without an inversion gate, voltage gated logic [17,18], domain wall-gated logic [2,19], and skyrmion-skyrmion logic gates. The lack of logic inversion operation, necessity of synchronization of the logic input and gating signals, hybrid spin and charge carrier nature of the information-carrying signals [2,17–19], lack of a viable design for scalability, and complicated geometric designs of the systems call for a new design to address these problems. Besides, the new design should consume low power, operate with nanosecond delay or less, and be cascadable, thermally stable, and ideally require no external magnetic field for spintronic logic processor applications. Among the suggested studies for skyrmionic logic gates, the domain wall gating methods present a potential for asynchronous, thermally stable, and scalable logic systems.

In the domain wall gated skyrmion logic [2,19], both gating signals and the in-plane input signals are hybrids of charge currents and skyrmions. The inefficient charge-current-driven nucleation of domain walls via the polarizer and electrode layers is used in both studies to accomplish signal gating (by blocking or passage). This hybrid nature of the information-carrying signals hinders the scalability of the system by necessitating a conversion of skyrmion-to-charge currents for the cascaded gates. Since one of the major issues in spintronics is the low power conversion efficiency between spins/skyrmions and charge currents, skyrmion-to-charge current conversion steps must be eliminated and logic processing must be based purely on skyrmions for low-power, high-bandwidth, and high-density circuits. In addition, skyrmion-to-charge conversion also causes significant thermal instabilities and prevents cascadable operations. Therefore a simpler and preferably all-skyrmionic inverter logic gate design based on domain wall gating is needed.

In this study we propose, demonstrate, and analyze an all-skyrmion inverter logic gate with small footprint (∼300 nm), low delays (∼5 ns), cascadability, and thermal stability at room temperature. In the inverter gate shown in Fig. 1, a domain wall is generated from a skyrmion logic input by converting the skyrmion to a domain wall and using current-induced expansion of magnetic domains. Then the probing skyrmion along the horizontal channel is blocked by the domain and the output becomes no skyrmion (logic low). In case when there is no gating domain wall, the probing skyrmion

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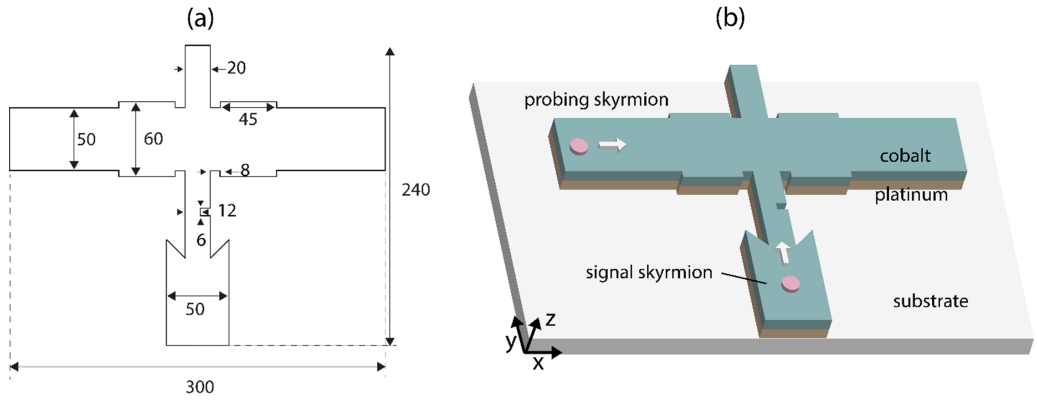

FIG. 1. Schematic of the logic inverter gate and its materials: (a) dimensions of the device in nanometers and (b) a three-dimensional sketch of the device.

can pass through the gate and yield a logic high output. We demonstrate the cascaded functional operation of the gates for a modular and scalable skyrmion logic circuit design. Accurate finite temperature modeling and validation of these logic gates is necessary, as thermal noise may cause stochastic pinning and make the devices not functional. We model and demonstrate robust operation of our inverter gate with notches comparable to skyrmion sizes despite finite temperature effects. By analyzing the time evolution of the inverter's power consumption, we also demonstrate a low energy cost of all-skyrmion logic inversion.

II. MICROMAGNETISM AND SKYRMION MODELING

A. Micromagnetic models and current-driven skyrmion motion

The modeling of the inverter gate is carried out in the micromagnetic framework with MUMAX3 software. The magnitude of the magnetization vector is considered to be constant and equal to the saturation magnetization M_s. Since M_s is constant, the magnetization can be fully described with M_s, and the unit vector of the direction $\mathbf{m}(\mathbf{r}) = (\sin\Theta\cos\Phi,\ \sin\Theta\sin\Phi, \cos\Theta)$, where $\Theta(r,\ \phi)$ and $\Phi(r,\ \phi)$ are polar and azimuthal angles, respectively. The magnetization profile of a skyrmion centered at the origin could be described by $\Theta = \Theta(r)$, $\Phi = v\phi + \gamma$, where v is the vorticity and γ is the helicity. We aim to model bilayer or multistack films which have interfacial DMI. The interfacial DMI interaction results in Néel-type skyrmions with $\gamma = 0$ and $v = 1$.

One can define the skyrmion polarity as $p{=}[m_z(r{=}\infty) - m_z\ (r = 0)]/2$. In our modeling, the skyrmion has $p = 1$ because the film magnetization points towards $+z$ and the magnetization at the core of the skyrmion points towards $-z$ (red domains $+z$, blue domains $-z$).

In a general magnetic system, to find the magnetization vector direction the total free Gibbs energy density is calculated as

$$\begin{aligned}\mathcal{E} = {} & (A_{\text{ex}}[\nabla\mathbf{m}(\mathbf{r})]^2 - \mu_0 M_s\mathbf{m}(\mathbf{r})\cdot\mathbf{H}_{\text{external}} \\ & - \mu_0 M_s\mathbf{m}(\mathbf{r})\cdot\mathbf{H}_{\text{demag}} - K_u\{[\mathbf{m}(\mathbf{r})\cdot\mathbf{e}_z]^2\} \\ & + D_i\{m_z\nabla\cdot\mathbf{m}(\mathbf{r}) - [\mathbf{m}(\mathbf{r})\cdot\nabla]m_z\}). \end{aligned} \tag{1}$$

This energy is minimized when the system equilibrates. Thus the variation of the energy of the system is equal to zero in equilibrium.

In dynamic magnetic systems, where an external magnetic field, spin-polarized charge current, or spin current is interacting with the system, the dynamic effect of these physical stimuli must be calculated too. The dynamics of magnetic moments in a physical media are captured by the Landau-Lifshitz-Gilbert (LLG) equation. The LLG equation with torques transferred by current is

$$\begin{aligned}\frac{d\boldsymbol{m}}{dt} = {} & \gamma_{\text{LL}}\frac{1}{1+\alpha^2}(\mathbf{m}\times\mathbf{B}_{\text{eff}} + \alpha[\mathbf{m}\times(\mathbf{m}\times\mathbf{B}_{\text{eff}})]) \\ & + \tau_{\mathbf{ZL}} + \tau_{\mathbf{Sl}}, \end{aligned} \tag{2}$$

where γ_{LL} is the gyromagnetic ratio for the LLG equation, $\mathbf{B}_{\text{eff}}$ is the effective magnetic field, α is the damping coefficient, and τ_{ZL} is the Zhang-Li spin torque transfer (STT) for current in-plane (CIP), and τ_{Sl} is the Sloncewski STT term for current perpendicular to plane (CPP) current injection schemes.

The Zhang-Li equation captures the STT arising from the transferred torques of nonequilibrium conduction electrons of a current flowing in-plane in the magnetic layer [20]:

$$\begin{aligned}\tau_{\text{ZL}} = {} & \frac{1}{1+\alpha^2}\{(1+\xi\alpha)\mathbf{m}\times[\mathbf{m}\times(\mathbf{u}\cdot\nabla)\mathbf{m}] \\ & + (\xi-\alpha)\mathbf{m}\times(\mathbf{u}\cdot\nabla)\mathbf{m}\}, \end{aligned} \tag{3}$$

where

$$\mathbf{u} = \frac{\mu_B\mu_0}{2e\gamma_0 B_{\text{sat}}(1+\xi^2)}\mathbf{j} \tag{4}$$

and ξ is the measure for nonadiabaticity for STT, μ_B is the Bohr magneton, e is electronic charge, B_{sat} is the saturation magnetic flux density, and $\boldsymbol{j}$ is the current density vector with $\boldsymbol{j} = j\,\hat{e}_x$ for current flowing in the x direction. For eliminating the skyrmion Hall effect, we assume $\xi = \alpha$ and simplify the Zhang-Li term to

$$\tau_{\text{ZL}} = \frac{1}{1+\alpha^2}\times\frac{\mu_B\mu_0 j}{2e\gamma_0 B_{\text{sat}}}\mathbf{m}\times\left(\mathbf{m}\times\frac{\partial}{\partial x}\mathbf{m}\right), \tag{5}$$

TABLE I. Micromagnetic model parameters used for the inverter gate.

Parameter	Value
Uniaxial anisotropy coefficient (K_u)	0.8 MJm^{-3}
DMI (D)	3.5 mJm^{-2}
Saturation magnetization (M_s)	580 kAm^{-1}
Heisenberg exchange coefficient (A_{ex})	15 pJ m^{-1}
Damping (α)	0.3

which is a dampinglike nonadiabatic term. Here we have only the current in-plane bias and use the Zhang-Li term to model the effect of current-driven skyrmion and domain motion.

B. Logic gate energy, power, and thermal analysis

MUMAX3 [21] calculates the total energy and each energy term for every time step. The power consumption/input of the logic gate is calculated using a discrete derivative of total energy ($P = (E_n - E_{n-1})/\delta t$), where $\delta t = 10^{-12}$ s. The positive side of the input power of the gate, which is the work done on the system, is integrated over one operation cycle to estimate the logic gate energy consumption. The negative side of the power versus time curve [$P(t) < 0$] is lost to either heat or annihilated domains/skyrmions. For finite temperature simulations, the thermal noise is modeled according to Brown [22]:

$$\vec{B}_{\text{therm}} = \vec{\eta}_i \sqrt{\frac{2\mu_0 \alpha k_B T}{B_{\text{sat}} \gamma_{\text{LL}} \Delta V \Delta t}}\,. \tag{6}$$

Here α is the Gilbert damping, k_B is the Boltzmann constant, T is the temperature (Kelvin), B_{sat} the saturation magnetization expressed in Tesla, γ_{LL} the gyromagnetic ratio, ΔV the cell volume, Δt the time step, and $\vec{\eta}_i$ a random unit vector with a standard normal distribution and is updated after each time step i.

The device temperature equilibrates near room temperature ($\sim$38.5 °C) based on the dynamic thermal equilibrium which arises due to the energy balance of Joule heating and heat conduction to the substrate. See Sec. IV of the Supplemental Material [23] for details regarding this energy balance.

C. Material parameters

The system is modeled using typical cobalt material parameters along with a platinum interface (Co/Pt bilayer). Table I shows the modeling parameters for the system.

The simulations were implemented using a graphic processing unit (GPU) on high-performance computational clusters. The skyrmions were detected by image averaging a region of interest. See Supplemental Material [23] for all fully open-source simulation files.

III. THE INVERTER GATE OPERATION

The inverter gate consists of a vertical channel with a recessed notch and a horizontal channel with two wider protruding notches. The vertical channel is the signal channel and the horizontal channel is the periodic probing skyrmion channel from a skyrmion generator [24]. A skyrmion may or may not exist in the vertical channel (logic input 1 or 0, respectively), but a skyrmion appears in the left side of the horizontal channel every T nanosecond, where T is the operation period of the gate. Figure 2 shows the detailed operation stages of the logic gate. The upper three rows of Fig. 2(a) illustrate the case where a signal skyrmion (logic input 1, output 0) exists in the vertical channel, and Fig. 2(b) shows the case when there is no signal skyrmion present in the vertical channel (logic input 0, output 1). Each column of the figure shows one operational stage (initialization, transmission/blocking, clearance). These stages are presented in detail below.

A. Initialization

In the initialization stage (the first column of Fig. 2), a current with an appropriate magnitude is applied to the vertical channel. If a skyrmion exists in the logic input channel [Fig. 2(a)], this current pushes the skyrmion into the narrower 20-nm vertical channel. This breaks the topological protection of the skyrmion, producing two chiral domain walls. The first wall has a lower pinning current than the second wall. This difference enables the current-induced expansion of the magnetic domain. By applying the current until 0.46 ns, the magnetic domain fills the vertical channel. If there is no skyrmion in the logic input channel, there will be no magnetic domain in the vertical channel at 0.46 ns (first column, part b). Current in the vertical channel is then turned off. Figure 2(c) shows time evolution of the applied currents in the three different stages.

B. Transmission or blocking

After the initialization stage, a skyrmion enters from the skyrmion generator input (left) side of the device in the horizontal channel. This skyrmion is introduced periodically irrespective of the magnetic state of the vertical channel. Then current in the horizontal channel is turned on. If the skyrmion logic signal had existed in the previous stage, the vertical channel would be filled with a magnetic domain oriented towards the –z direction. This domain prevents the passing of the skyrmion to the right side of the horizontal channel. In this case the horizontal translation movement of the skyrmion is blocked and a logic output 0 is recorded at the output. On the other hand, if the skyrmion logic input had not been introduced in the initialization stage (logic input 0), the skyrmion in the horizontal channel would move to the right-hand side of the device and a skyrmion logic output 1 is obtained. This is the operation procedure of the skyrmion inverter logic gate. The existence of a skyrmion at the output (in the right side of the horizontal channel) at the end of the operation period corresponds to the Boolean complement operation of the skyrmion in the vertical channel at the beginning of the operation period. Thus this device is a NOT logic gate with the transmission delay of T nanoseconds. For the gate with the nominal values of Fig. 2, T is 5.23 ns.

C. Clearance

After these two steps are finished, the device needs to be ready for the next cycle of an arbitrary logic input of 1 or 0.

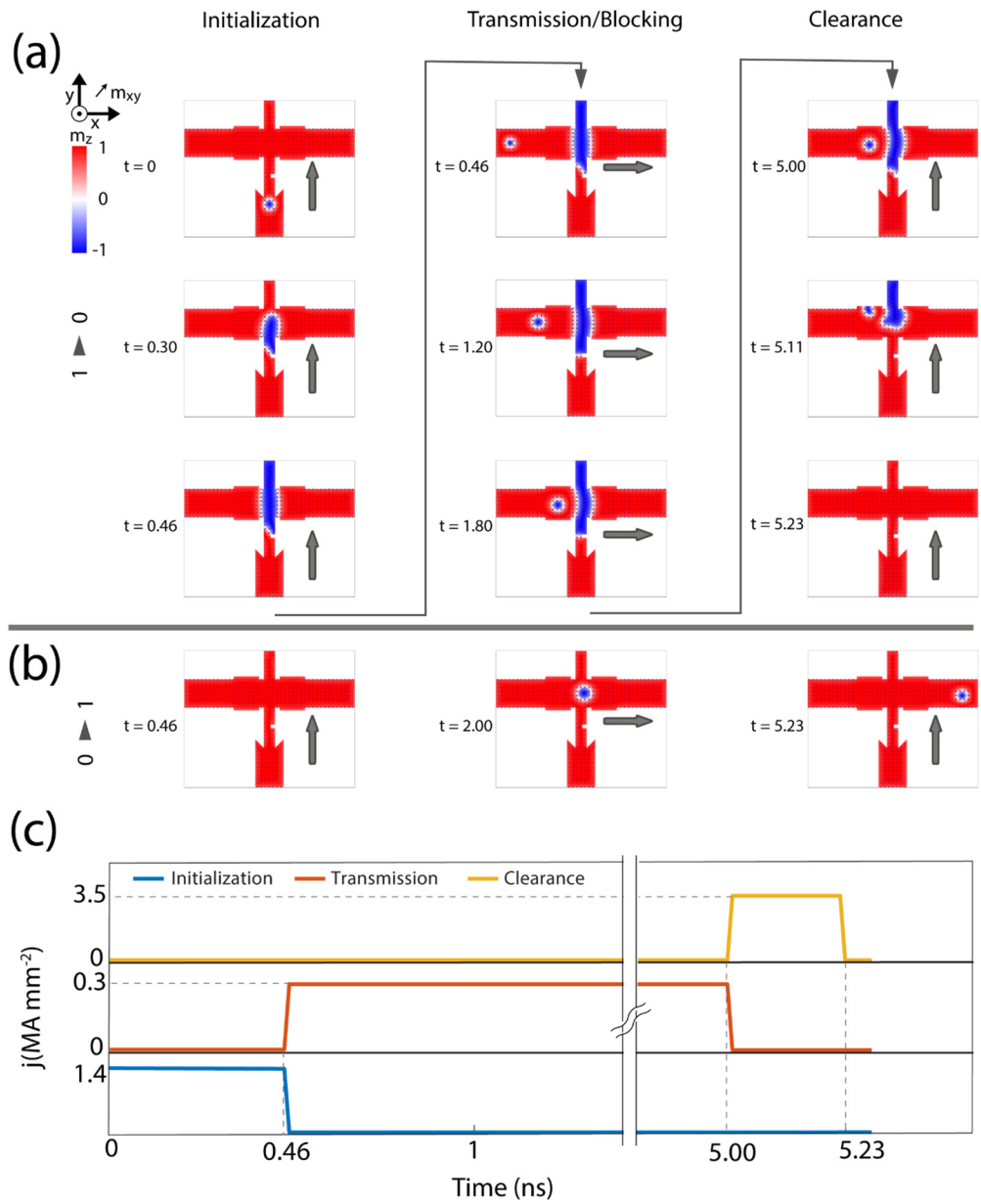

FIG. 2. The operation of the inverter gate (NOT gate). (a) The upper three rows show the $1 \rightarrow 0$ condition of the device and (b) the bottom row shows the $0 \rightarrow 1$ condition. The applied current densities are shown in part (c). See Supplemental Material [23] (Fig. S1) and the accompanying source PNG files for the exact dimensions of the gate.

Thus any magnetic domain needs to be cleared out from the device by applying a current to the vertical channel and two side notches. The current must be large enough to unpin the domain from the notch. After this clearance stage, the device is ready for the next cycle.

IV. DEVICE CHARACTERISTICS

A. Current density and external magnetic field dependence of logic gate delay

For optimal device operation, one needs to find the values and timings for currents at different stages. Figure 3 shows the summary of the optimization of current bias and timings. Figure 3(a) shows the current dependence of the initialization time, i.e., the time required to break a skyrmion input entering from the vertical logic input channel into a magnetic domain and expand the magnetic domain to fill this channel. The initialization time decreases by increasing the current density. Thus a higher current density would result in the shorter initialization time. Current densities lower than 1.3×10^{12}A m^{-2} are not strong enough to extend the magnetic domain, and currents higher than 1.96×10^{12}A m^{-2} unpin the magnetic domain walls and clear the vertical channel. These currents can be reduced by substituting cobalt with other materials with different combinations of saturation magnetization, exchange, DMI, and damping constants. Figure 3(b) shows the transmission time of a skyrmion from the left to the right-hand side of the device along a horizontal channel. This time is proportional to the length of the horizontal channel. Similar to the initialization time, this time decreases with

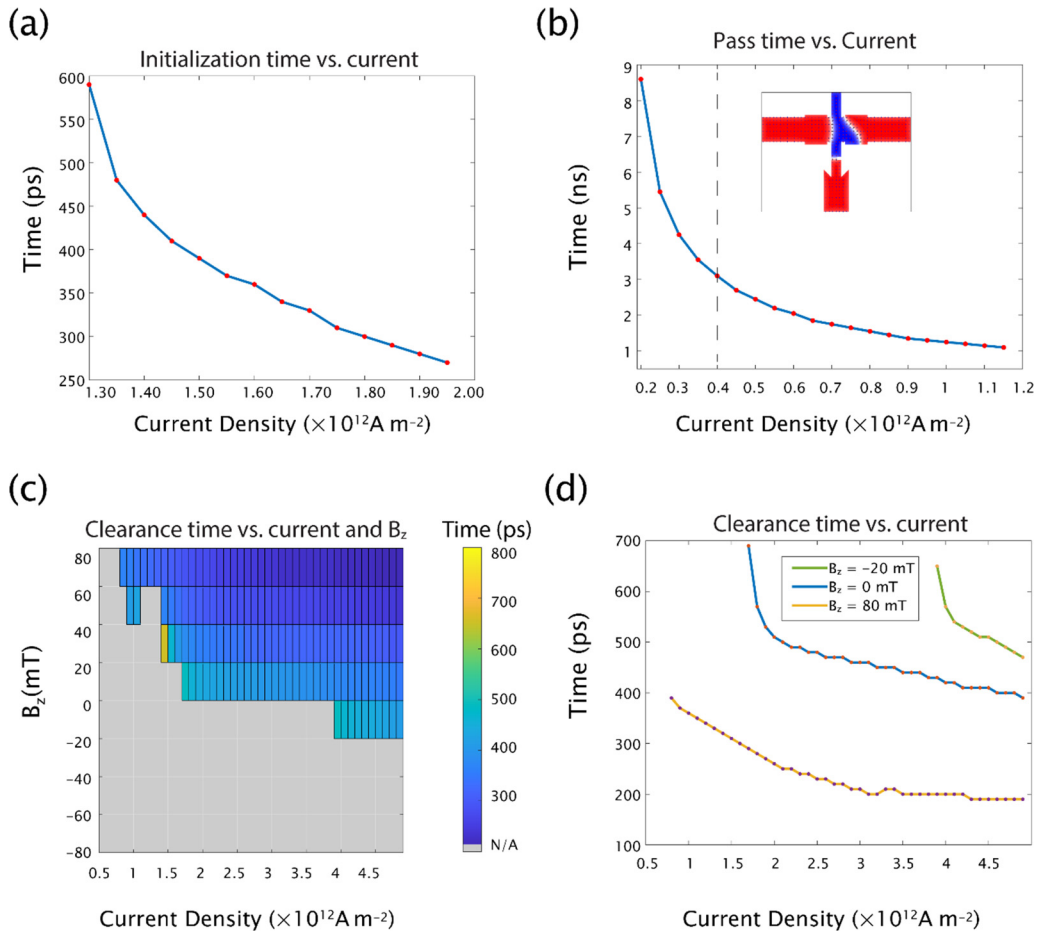

FIG. 3. Device characteristics as functions of applied current and external field. (a) The initialization time vs the current density and (b) skyrmion pass time vs current density. (c) Channel clearance time vs current density and external field show that higher current densities could help run the gate with lower delays. (d) The applied current density dependence of clearance time for three different external magnetic fields shows that the external field could be applied to reduce the required current density for operation and to operate the gate with lower clearance delay.

higher current densities. Two important thresholds need to be considered for this current. First, a current density higher than 0.4×10^{12} A m^{-2} would disrupt the magnetic domain in the vertical channel. This is undesirable for the device and must be avoided. Second, a current density higher than 0.6×10^{12}A m^{-2} will eliminate the skyrmion when it reaches the right wall of the device. This threshold needs to be observed to have scalable operation. These values might change with different channel widths or material parameters. The smaller of the two thresholds is the highest possible current for the horizontal channel. The disrupted magnetic domain and the disruption current threshold are shown in the inset of Fig. 3(b).

Figure 3(c) shows the dependence of the clearance time on the applied current and external magnetic field. This figure shows that an external magnetic field can decrease the current threshold and the time of the clearance stage. With a magnetic field directed to $+z$, the clearing of the magnetic domain is easier with lower current. There are two effects visible in this figure. First, increasing the magnitude of the magnetic field in the $+z$ direction decreases the clearance time. Second, it decreases the current requirement to clear the device. Magnetic fields applied towards $-z$ direction exert spin transfer torques on the domain walls with polarity opposing that of the applied current. Thus magnetic fields towards $-z$ will hinder the clearance operation.

Figure 3(d) shows the dependence of the clearance time on the applied current for three different magnetic field values. The clearance time decreases with the application of the magnetic field in the $+z$ direction. The difference in clearance time with different magnetic fields becomes smaller with increasing the applied current density.

B. Energy analysis

The energy input of the gate comes from the spin transfer torques of the spin-polarized electric current and the formation energies of logic one input skyrmion and probe skyrmions. The spin-polarized current changes the magnetization profile of the system. To calculate the energy consumption for one period of operation, one needs to record the total energy of the device as the sum of the energies contributing to the magnetization process. They can be decomposed as

$$\phi_t' = \phi_{\text{exchange}}' + \phi_{\text{zeeman}}' + \phi_{\text{anisotropy}}' + \phi_{\text{demag}}' + \phi_{\text{DMI}}'. \quad (7)$$

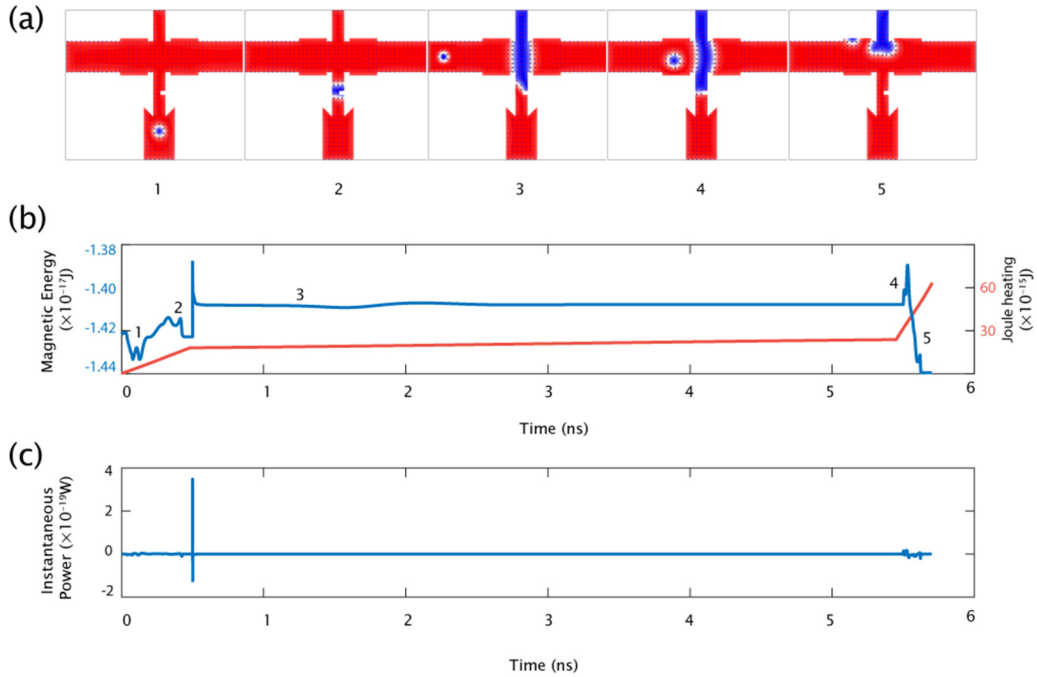

FIG. 4. The energy and power analysis of the inverter gate. (a) Snapshots of the operation steps of the device. (b) The time evolution of the calculated total energy of the system shows the change due to introducing a skyrmion (steps 1 and 3), overcoming a notch barrier (step 2), the repelling force between the skyrmion and the domain wall (step 4), and clearing of the domain wall from the channel (step 5). The numbers correspond to the snapshots in part (a). The right-hand vertical axis shows the Joule heating contribution for the all-metallic skyrmion logic gate. (c) The instantaneous power of the device, which is the time derivative of part (b). The energy consumption of the logic gate is the integration of the positive side ($P_{\text{input}} > 0$) of the power diagram in (c) for only the magnetic terms.

The transfer of energy from the current to the device is not adiabatic, i.e., the dissipated energy from the device is considered as the lost energy, as there is no mechanism to capture the energy and reuse it. Figure 4(a) shows a typical cycle of the device where the input is "1." We chose to show this case because case "0" is the much simpler case of one skyrmion moving through the horizontal channel. See Fig. S2 of the Supplemental Material [23] for the "0" case. To calculate the energy consumption [Fig. 4(b)] we sum the energy where the input energy is increasing, i.e., where the input power of the device is positive [$P(t) > 0$)]. Figure 4(c) shows the input power. The energy consumption for the $1 \rightarrow 0$ operation for a gate with 1 nm thickness is 9×10^{-19} J, and with 6 nm thickness it is 5.2×10^{-18} J. These energies correspond to 230 and 1347 $k_B T$ at $T = 300$ K for 1 and 6 nm, respectively. The uniaxial anisotropy, demagnetizing, and exchange energy term contributions for the gates with 1-, 4-, and 6-nm-thick cobalt layers are presented as functions of time (see Figs. S6–S8 of the Supplemental Material [23] for the plots).

For Fig. 4(b), the first peak is the skyrmion introduction energy (1). By pushing the skyrmion into the narrower channel, the topological protection of the skyrmion is broken and the energy of the system decreases (region 2). The magnetic domain fills the region and the energy of the system decreases due to the higher decrease in the demagnetization and exchange energies than the increase of the uniaxial anisotropy energy. Then another skyrmion is introduced from the horizontal channel and the energy goes up to about the beginning of the simulation. The small difference is because a part of the device is filled with the negative-pointing magnetization domain (3). The energy is constant until the skyrmion reaches close to the vertical domain. By pushing the skyrmion further towards the domain wall, the total energy increases because of the increase in the exchange energy due to the repulsion force between the domain wall and the skyrmion (4). Finally, the clearance current is applied and the energy of the system moves back to its minimum where the system has relaxed and is devoid of magnetic domains and skyrmions (5).

Metallic cobalt and platinum layers conduct spin-polarized charge currents and undergo Joule heating. Joule heating is $\Sigma_i(E_{\text{Joule}(i)}) = I_i V_i \Delta t_i$ $(i = 1, 2, 3)$, where I_i is the current, V_i is the applied voltage, and Δt_i stands for the pulse width for initialization ($i = 1$, 0–0.46 ns), transmission ($i = 2$, 0.46–5 ns), and clearance stages ($i = 3$, 5–5.23 ns), respectively, as shown in Fig. 2(c). Table II shows the Joule heating terms corresponding to each stage for the 1-nm-thick layer case.

TABLE II. Joule heating terms in every operation cycle when the device is made up of Co/Pt. The substrate (i.e., bulk silicon) is assumed to provide sufficient thermal conductivity and thermal sink to prevent thermal runaway.

Stage	Energy per 1 nm thickness
(1) Initialization	1.89×10^{-14} J
(2) Transmission	5.61×10^{-15} J
(3) Clearance	3.89×10^{-14} J

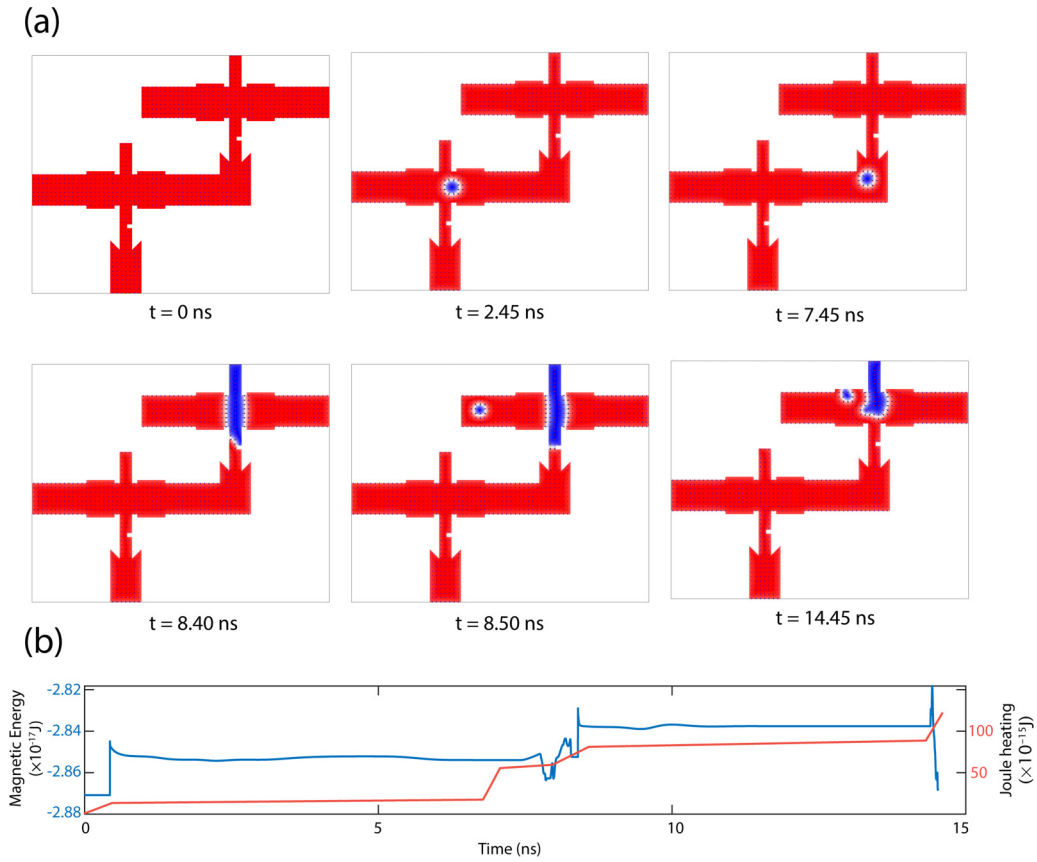

FIG. 5. Cascadable inverter gates. (a) The snapshots of the cascadable inverter gates for $0 \rightarrow 1 \rightarrow 0$ and (b) the time evolution of the total energy for two cascaded inverter gates. See Supplemental Material [23] Fig. S3 for the $1 \rightarrow 0 \rightarrow 1$ case.

C. Cascadability

Demonstration of cascaded operation of the gates is essential for larger scale integration of spintronic logic circuits. Here we show that the proposed inverter gate is cascadable by design, and the gate is cascadable with the same bias current values and geometries for a single inverter gate. Thus cascading two inverters is only a matter of duplicating the second gate and connecting the logic output of the first inverter to the logic input of the second inverter. Two cascaded inverters result in logic bit transfer operation. When cascading two inverters there exist two cases: (1) the logic input of the first gate is 0, and (2) the logic input of the first gate is 1.

Figure 5 shows the demonstration of the first case where the input of the first inverter gate is 0; see Sec. III of the Supplemental Material [23] for the other case. Figure 5(a) shows the snapshot of the cascaded inverters. There is no skyrmion in the vertical logic input channel of the first inverter so the periodic skyrmion passes through the horizontal channel. The current moves the skyrmion to the right side until the repulsion from the right wall of the horizontal channel stops the skyrmion. Now the initialization stage of the second gate starts. A current is applied to the vertical channel of the second gate. We picked a two-step initialization current when the first step value is about the current pushing the skyrmion in the horizontal channel. Then a current with a value equal to the initialization stage current is applied to the skyrmion. This ensures than no abrupt changes happen to the skyrmion and the skyrmion does not annihilate to the geometric complications. This two-step initialization current can be applied to a single gate too and is not unique to the cascaded gate. Thus, two-step initialization does not prevent cascadability.

Figure 5(b) shows the time evolution of the total energy of the cascaded inverter pair. The first 0.46 ns of the operation is the initialization stage of the first inverter, and since there are no skyrmions or domains in the system, the energy of the system corresponds to a minimum. The first peak corresponds to the skyrmion entering the first gate's horizontal channel. The energy is relatively constant, with minor changes due to skyrmion size changes because of the notches and constriction. At $t = 6.45$ ns, the skyrmion is at the input of the second NOT gate. Then the skyrmion is pushed into the second inverter's vertical channel. At 7.50 ns a skyrmion is introduced in the horizontal channel of the second inverter and the current pushes the skyrmion to the output of the second inverter. At 13.40 ns the clearance of the second logic gate starts.

D. Finite temperature stability

The inverter gate needs to be robust against room-temperature thermal fluctuations for experimental feasibility. Micromagnetic modeling studies usually ignore thermal noise because of the prohibitive computational power demands of finite temperature simulations. Micromagnetic models for the cascaded gates at 0 K and 1-nm cobalt thickness take 2 h at 0 K, and at 6-nm cobalt thickness they take 15 h, and

at 300 K and 6 nm they take 111 h on an NVIDIA Tesla k20m. The finite temperature effects, higher number of steps for equilibration, and the smaller time steps may increase the modeling time by about two orders of magnitude. Implementing high numbers of finite temperature simulations may not be feasible without using GPU-enabled computational clusters. Despite the order-of-magnitude computational cost difference between finite temperature and 0-K micromagnetic simulations, each design needs to be verified for finite temperatures.

We redesigned our inverter gate several times to achieve functional robustness against finite temperature noise. Two main factors should be considered when carrying out finite temperature simulations: First, the energy of the skyrmion and domain walls must be much bigger than the thermal energy k_BT at the temperature of interest. For this reason a 1-nm-thick cobalt layer does not provide enough total effective energy to stabilize a dynamic skyrmion in the thin film. By increasing the thickness to 6 nm, the skyrmion becomes stable at room temperature. Second, the geometric protrusions and constrictions of a channel introduce a complicated energy landscape for the skyrmion due to inhomogeneous demagnetizing fields with different extrema or saddle points. This issue brings up stochastic skyrmion collision into the physical walls of the track due to thermal noise or potentially pinning sites. Increasing the width of the horizontal channel decreases the disruption current threshold of the vertical channel domain, which leads to the need for wider side notches, which eventually leads to the thermal annihilation of skyrmions.

A small external magnetic field of 0.02 T introduces a shift in the energy landscape that can prevent the thermally induced annihilation of skyrmions. Finite temperature micromagnetic simulations validated that this external magnetic field eliminates all thermally induced annihilation of skyrmions (see videos SV1–SV7 in the Supplemental Material [23] for each case). This field can be estimated based on achieving enough Zeeman energy to overcome thermal fluctuations: $k_BT = 300\,k_B = 25.9\,\text{meV} \approx 1/2\,\text{B} \times \text{H} \times \text{V}$ where $B = 580\,\text{kA m}^{-1}$ (cobalt saturation magnetization) and V is the skyrmion volume of interest ($V = \pi \times (7.5\,\text{nm})^2 \times 4\,\text{nm}$) [2]. The H obtained from this calculation is the exact external magnetic field needed for stable room-temperature operation. This magnetic field does not alter the operation of the logic device at any other stages. Using magnetic materials with higher perpendicular magnetic anisotropy could raise the total effective energy above the range of thermal fluctuations and help eliminate the need of an external magnetic field for thermal stability.

V. SKYRMION-DOMAIN WALL INTERACTIONS

Here we expand the physical discussion to explain the different physical phenomena appearing in this study. We first demonstrate how a magnetic structure, such as a domain wall, moves microscopically. The nontrivial effects of our device, such as selective domain wall pinning, domain wall elongation, and transformation to other walls at the junction, are then explained. Although current-driven domain wall or skyrmion motion have been examined earlier, we use the energy landscape to justify the skyrmion domain wall repulsion within the context of our discussion.

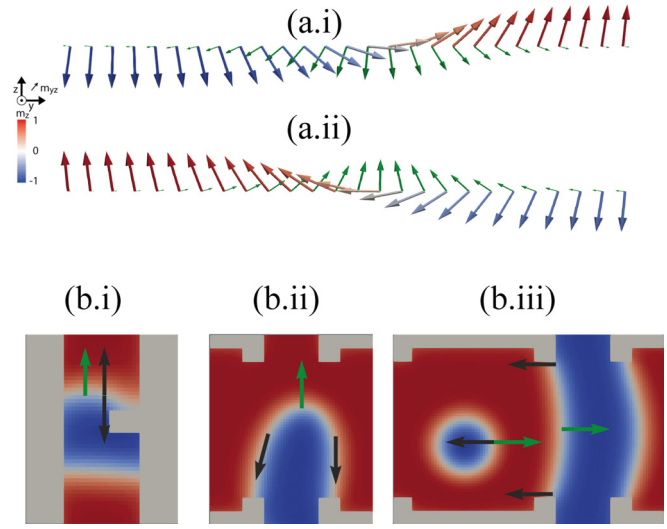

FIG. 6. Domain wall with generalized forces. (a.i) The lateral profile of the leading domain wall with the current-induced torques shown in green. (a.ii) the same image for the back domain wall. (b.i)–(b.iii) Magnetic structures and generalized forces for different regions of the device in key times. The current-induced torques are shown in green, and the counteracting forces arising from the magnetic energy are shown in black.

We start with STT-induced domain wall motion. When the skyrmion is pushed into the 20-nm channel, because the width of the channel is smaller than the diameter of the skyrmion, the skyrmion transforms into two Néel domain walls with the lateral configuration shown in Fig. 6(a). The STT is represented by green arrows, whereas the wall magnetization is represented by blue-white-red arrows. The exerted STT tries to align the local magnetization configuration towards its local direction. For both walls, each cell n at time t_0 aligns to the magnetization of the cell n-1 at time $t_0 + \Delta t$, where Δt depends on the material parameters and the local energy landscape of the device. This results in the $+y$ motion of the domain wall. With the y dimension of each cell being Δl_y, the speed of the domain wall motion is thus $v = \Delta l_y/\Delta t$. Since a higher STT aligns the cell magnetizations faster, i.e., decreasing Δt, the speed of the domain wall increases with higher STT. This domain wall motion can be thought of as a result of a force in the y direction. We call this force f_{STT}. The forces arising from STT are shown in green in Fig. 6(b).

The internal magnetic energy of a magnetic configuration like a domain wall or a skyrmion depends on the magnetization profile. For a system with N cells with magnetization $\mathbf{m}_\text{I}$ at the ith site, one can think of a generalized magnetization vector $X = (\mathbf{m}_1, \mathbf{m}_2, \ldots, \mathbf{m}_N)$. A change in X that results in a new vector $X' = X + \Delta X$, and a new energy $E' = E + \Delta E$ results in a counteracting force $\mathbf{f_X} = -\nabla_X E$, where the gradient is with respect to generalized magnetization dimensions. For a single cell $X = \mathbf{m}$ and $\mathbf{f_x} = \mu_0 \mathbf{M_s} \mathbf{H}_\text{eff} = -\nabla_m E$.

Because the magnetic system is always at equilibrium and since the micromagnetic energy terms are adiabatic, infinitesimal changes in X that move the system from the equilibrium state are opposed by a counteracting force. For example, if ΔX is realized as the movement of a rigid magnetic structure

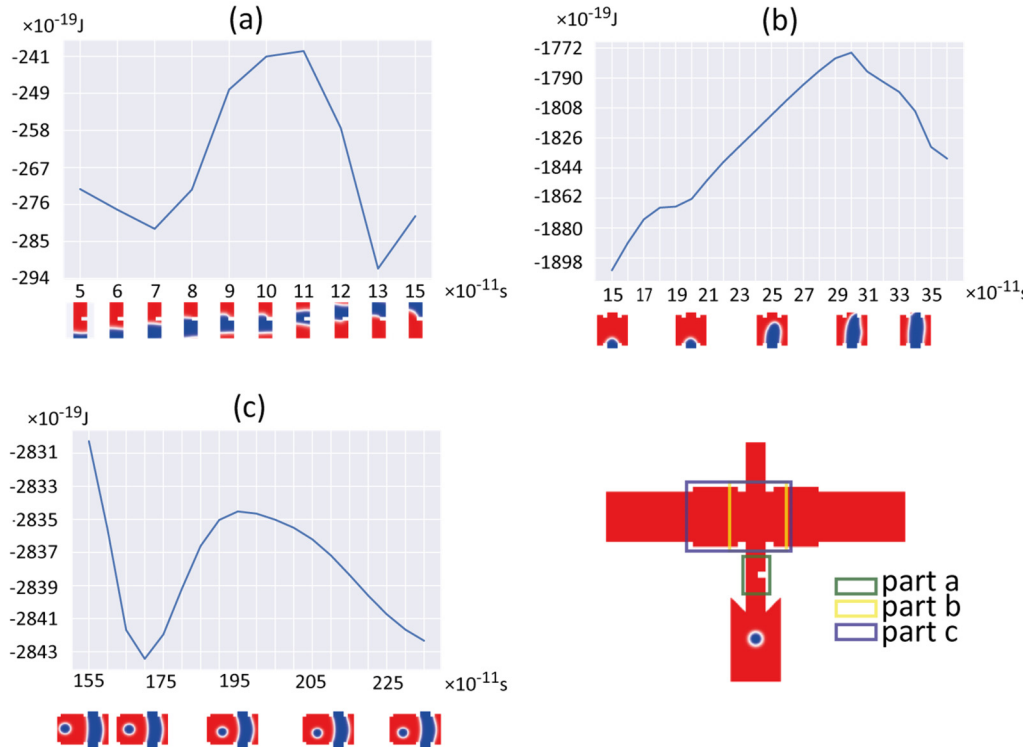

FIG. 7. Development in the magnetic structure of the system and the corresponding magnetic energy. (a) Domain walls pass and pin at the vertical channel notch. (b) Domain wall elongation and bending at the junction area. (c) Skyrmion repulsion by the vertical domain walls.

in **r** direction that results in a change in the free energy of the system ΔE, a generalized force acts on the magnetic structure in the direction **-r**.

Different generalized forces emerge depending on the type of change in X that results in the change of energy. When a magnetic structure approaches a geometric boundary, the total energy increases due to exchange and dipolar interactions between the nontrivial spin configuration of the magnetic structure and the tightly held boundary spins. The increase in energy causes a counteracting force in the opposite direction of the magnetic structure's movement. There is also a repulsion between two domain walls, a domain wall and a skyrmion, and two skyrmions. The direction of magnetization in the core of the domain walls opposes each other, as seen in Figs. 6(a.i) and 6(a.ii). As a result, the exchange energy and consequently the overall energy rise. Therefore a repulsion force between two domain walls is expected. After the current is switched off, the back domain wall retracts owing to repulsion between domain walls (see Supplemental Material [23] video SV8). Domain walls are low-energy magnetic configurations that link two magnetized zones with opposite spin alignment. The micromagnetic energy coefficients of the magnetic material determine the width of the domain wall (the extent of the domain wall in y direction of Fig. 6(a.i). The length of the domain wall [the extent of the domain wall in x direction of Fig. 6(a.i)] depends on the geometry. The energy of the thicker domain wall is greater than that of the shorter domain walls. Furthermore, raising the angle between consecutive magnetic moments by bending a domain wall in the xy plane [as shown in Fig. 6(b.ii)] adds to the energy per length of the domain wall. Straight domain walls, on the other hand, have less energy than bent domain walls of the same length. As a result, the shorter and straight domain walls are preferred to longer and bent domain walls. This causes the domain walls to contract. (See video SV9 in the Supplemental Material [23] for an illustration of the contraction of the domain walls when the current is switched off.) Because the shorter domain walls are preferable, antinotches provide a finite potential step for the domain walls, whereas notches produce a finite potential well.

Figure 6 depicts the forces generated by these magnetic energy exchanges with black arrows. Green arrows represent the forces generated by the STT. Figure 7 shows the energy profile of different regions of interest in the device for different working windows. Figure 7(a) shows the pass and pin process of the domain walls, Fig. 7(b) shows the domain wall extension and the transformation of the bent domain wall into three domain walls, and Fig. 7(c) shows the skyrmion domain wall repulsion force.

As the leading domain wall approaches the notch [see Fig. 7(a), 5–7], the energy decreases slightly due to a decrease in the demagnetization energy of the window resulting from the near equal proportions of spin-down and spin-up regions. Upward movement of the back domain wall and the pinning of the leading wall because of the opposite force from the pinning potential of the antinotch side of the notch to the leading wall results in a reduction of the distance between the back and leading domain walls. This results in an increase of the energy of the area up to when the repulsion and STT forces on the leading wall surpass the energy barrier of the upper side of the notch [Fig. 7(a), 11]. The slight increase in the energy from frame 10 to 11 is due to the elongation of

the leading domain wall. The force-dependent selective domain wall pinning process holds for the current density value used in this study, i.e., $J = 1.4 \times 10^{12}\,\mathrm{Am}^{-2}$ [12]. On the contrary, the influence of boundary conditions becomes the primary factor in the selective domain wall pinning process for current densities greater than $J = 1.5 \times 10^{12}\,\mathrm{Am}^{-2}$ [12,25]. After depinning, the leading domain wall moves further from the back domain wall and the energy decreases. The slight increase of the energy in frame 14 is due to the bending of the pinned back domain wall. The back domain wall, however, cannot pass the notch, because the STT force alone is not strong enough to push the domain wall past the potential step of the antinotch side without help from the repulsion force of another magnetic structure. With higher current densities the STT itself is strong enough to push both walls past the notch. This is used in the clearance stage of the device.

The next step is the elongation of the domain wall into the horizontal channel as shown in Fig. 7(b). The elongation and bending of the magnetic domain wall happen because the antinotch forces prevent the domain wall from extending in the horizontal channel while the STT force pushed the middle part of the domain wall. The energy of the region increases with the elongation and bending of the domain wall. This continues until the domain wall reaches the other side of the horizontal channel, resulting in a significant reduction in energy as the bent domain wall is transformed into three straight domain walls. As shown in Fig. 7(b) 34, further straightening and elimination of the top domain wall from the region results in a subsequent decrease in energy. This process confirms that the straight domain walls are preferred to bent domain walls.

Figure 7(c) shows a skyrmion approaching the vertical domain. The antinotches on the right side of each domain wall of the vertical domain (vertical channel for the left domain wall and a right lateral antinotch for the right domain wall) stabilize the vertical domain wall against the force exerted by the current. This means that increasing the height of the right antinotch increases the stability of the right vertical domain wall. As the skyrmion approaches the vertical domain, there exists an initial reduction of energy, Fig. 7(c) 31–34, because of the movement of the skyrmion from the narrower channel into a wider region of lateral left antinotch. From here on, the reduction in the distance between the skyrmion and the domain wall results in an increase of energy. This increase results in a force that prevents skyrmions from moving further than Fig. 7(c) at 195 ns. The bending of the domain wall and the chirality of the skyrmion results in a tilted force that pushes the skyrmion further away into the bottom left, which results in the longer distance between the skyrmion and the domain wall that causes a decrease in the energy of the region.

The overall domain wall dynamics here include significant complexities in skyrmion stabilization and the delicate balance of energy terms in running the inverter device under geometric, thermal, and material disorders and tolerances. In addition to the complex space of material and device parameters, Joule heating emerges as one of the most demanding subjects in future spintronic device development. Here our analysis indicates that the overall power consumption might be reduced by more than four orders of magnitude when one can eliminate Joule heating. Emerging directions for eliminating Joule heating include reduction of charge carrier concentration using 2D ferromagnetic insulator/semiconductor materials with large spin-orbit coupling, twisted 2D monolayer effects, spin waves, and surface acoustic waves triggered over magnetoelastic and piezoelectric layers. Thus surface energy terms such as DMI or other anisotropy energy terms might become important in the dynamics of upcoming skyrmion and domain wall logic devices.

VI. CONCLUSION

The inverter for digital skyrmionics is one of the key components of the universal set of Boolean logic gates and processors which still need improvements in order to achieve a low-power and compact gate design. In this study we used micromagnetic modeling to create and assess a simpler skyrmion-based inverter gate (NOT), both with and without thermal effects. The proposed gate can operate with subnanosecond delays, has a submicron footprint, and little or no external magnetic field requirements. All-metallic inverters are subjected to high Joule heating; however, the substrate helps maintain room-temperature thermal stability by preventing thermal drift. These advantages enable cascaded logic inverter operations. Cascadability is critical for scalable spintronic logic circuit designs. The topological protection of the skyrmions increases the robustness against geometric defects, and this property plays a key role in the operation of these logic devices.

In digital skyrmionics, two major consequences arise from our framework for skyrmion-domain wall interactions: (1) The ability to write and erase domain walls with the current-induced torques allows for operation with arbitrary inputs. (2) Generalized forces for distinct geometric regions of the device aid in the regulation of the skyrmion-domain repulsion and other forms of interactions, like the temporal and energetic landscape (Hamiltonian). The current-induced torques and the counteracting forces originating from the magnetic energy factors in the Hamiltonian indicate that energy usage in digital skyrmionics can be reduced significantly. Eliminating Joule heating by substituting all-metallic heterostructures with magnetic insulator/heavy metal or all-insulator heterostructures might be possible [with Joule heating $\sim 10^{-14}\,\mathrm{J/bit}$, without Joule heating $\sim 0.2 \times 10^{-17}\,\mathrm{J/bit}$, as shown in Fig. 4(b)]. Further energy savings may be attainable, since magnetic insulators often lower exchange stiffness, saturation magnetic moments, and other anisotropy factors by an order of magnitude when compared to magnetic metals. Integrating the inverter with Boolean AND and OR gates in a similar functional, thermally robust and cascadable way might also allow for the construction of arbitrary arithmetic or logic functionality.

ACKNOWLEDGMENTS

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Correction: An operator in Eq. (3) was removed during the proof production cycle and has been restored. Two values in the right column of Table I were incorrect and have been fixed.