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IOP Publishing Journal of Micromechanics and Microengineering
Journal **XX** (XXXX) XXXXXX https://doi.org/XXXX/XXXX

Cascadable Microelectromechanical Resonator Logic Gate

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Received xxxxxx
Accepted for publication xxxxxx
Published xxxxxx

Abstract

Micro/nano-electromechanical resonator-based logic elements have emerged recently as an attractive potential alternative to semiconductor electronics. The next step for this technology platform to make it into practical applications and to build complex computing operations beyond the fundamental logic gates is to develop cascadable logic units. Such units should produce outputs that can be used as inputs for the next logic units. Despite the recent developments in electromechanical computing, this requirement has remained elusive. Here, we demonstrate for the first time a conceptual framework for cascadable logic units. Cascadability is experimentally demonstrated through two case studies; one by cascading two OR logic gates. The other case is the universal NOR logic gate realized by cascading an OR and a NOT gate. The logic operations are performed by on-demand activation and deactivation of the second mode of vibration of a clamped-clamped microbeam resonator. We show that the demonstrated approach significantly lowers the complexity and number of microresonator-based logic functions compared to the CMOS-based counterparts, which improves energy efficiency. This can potentially lead toward the realization of a novel technology platform for an alternative computing paradigm.

Keywords: cascadability, second mode of vibration, NOR logic gate, clamped-clamped beam

1. Introduction

The last decade has seen a significant research focus on developing alternate computing technologies owing to the fact that the transistor is soon to reach its fundamental limits due to off-state leakage and heat generation issues. The aim is to replace transistors with leakage-free and energy efficient logic elements. Mechanical computation using micro/nanoelectromechanical systems (M/NEMS) has recently emerged as a strong candidate to achieve this goal [1-22]. M/NEMS switch based logic devices have been proposed due to their ideal leakage properties and harsh environment operation [1-7]. However, these devices suffer greatly from stiction and contact wearing issues. In order to overcome these challenges, M/NEMS resonator based logic has been proposed as logic elements [8-22]. The logic states are defined by the vibrational states of a resonator in this case.

The concept of M/NEMS resonator based logic device was first introduced as an energy efficient alternate computing technology [8]. For GHz frequency NEMS devices working with moderate *Q*, the minimum power required to activate these devices to a detectable limit is approximately 10^{-17} W [8]. Computing systems built with such devices will provide unprecedented energy efficiency. An XOR gate consuming only 5 fW of power built using a piezoelectric L-shaped NEMS structure was experimentally demonstrated [9]. Thereafter, several linear and nonlinear dynamic phenomenon have been exploited to realize resonator based logic units. Nonlinear jumps of the resonators in the hysteresis regime have been successfully used to perform various logic [10,11] and memory operations [12]. DC

[11,13,14] and electrothermal [15-19] modulation of the resonance frequency of the resonators have also been used as effective ways to realize logic operations. In such technologies each gate operates at a distinct resonance frequency. Finally, parametric excitation [20] and multi-frequency excitation [21] have also been used to perform logic operations.

In spite of some intriguing developments in this field, micro/nano-resonator based logic devices have been faced with challenges of their own. One major hurdle is the difficulty in cascading several logic elements for building complex logic circuits, which limits the practicality of the technology. Cascaded logic devices have been recently demonstrated in spintronics [22] and nanophotonic plasmon networks [23], however, yet to be demonstrated in micro/nano-resonator based logic elements. This is partly because the demonstrated works either rely on logic inputs and outputs of different signal types; DC as inputs and AC as outputs [10,12,13-19], or perform different logic operations at different frequencies/modes of vibration [9,20,24]. Operation of different gates at a single frequency and having similar signal type (AC/DC) as inputs and outputs are necessary prerequisites for cascading logic elements.

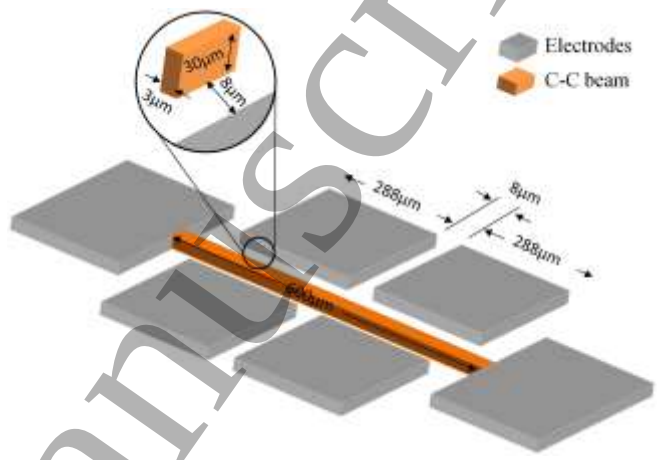
In order to realize more complex logic operations and envision a functional digital unit comprising of resonator based logic devices, cascadability of logic devices is essential. Toward this, we demonstrate cascadable logic elements that have a unified input and output signal waveform, i.e, AC signal, and operate at the same frequency. We demonstrate the cascadability through two case studies; one by cascading two OR logic gates and the other through realizing the universal NOR logic gate by cascading an OR and a NOT gate. In addition, we show that high logic depth and complexity can be achieved without the need for CMOS devices to boost and condition the intermediate signals between logic gates. The realization of fundamental logic gates and the universal logic gate NOR along with the unified input and output signals types lay the ground to develop any desirable logic functions.

The paper is divided as follows. Section 2 presents the design and fabrication. Section 3 shows the operating principle of the devices. Section 4 shows the experimental case studies for cascaded logic gates. Section 5 shows the discussion and Section 6 summarizes the conclusions

2. Design and Fabrication

The logic device comprises of a clamped-clamped microbeam operating at its second mode of vibration. Figure 1 shows the labelled schematic, SEM image, and fabrication cross section of the device.

The device is fabricated on a highly conductive Silicon on insulator (SOI) wafer using surface micromachining processes, Fig. 1(c). First, a 50nm/250nm layer of Cr/Au is sputtered and lifted off to form the bond pads. These bond pads are placed directly above the electrode/anchor pads and are wire bonded to provide electrical connection to these electrode/anchor pads. Next, the structural layer is patterned and the Si layer is etched using Deep Reactive Ion Etch (DRIE) to define the microbeam and the electrodes. Finally, HF vapor etch is used to released the insulating SiO_2 layer to suspend the microbeam in air.



(a)

(b)

(c)

Figure 1. (a) Schematic, (b) SEM image, and (c) fabrication cross section of the clamped-clamped microbeam.

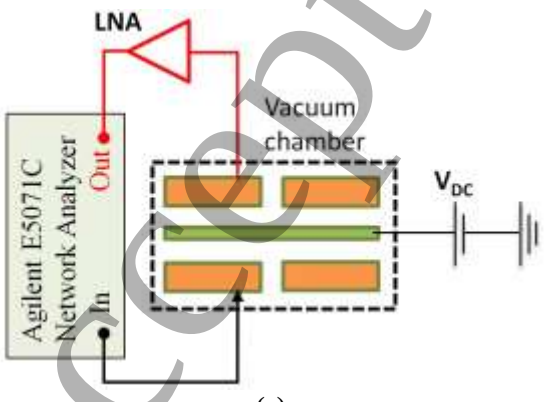
3. Experimental Setup

Figure 2(a) shows a schematic of the experimental setup used to drive the resonator and measure its output response. A

constant DC bias is applied to the resonator at all time. Network analyzer is used to provide the input AC signal to the resonator at the desired input electrodes. The output AC signal from the resonator is fed to network analyzer after pre-amplification using a low noise amplifier (LNA) SR560. The network analyzer measures the S_{21} parameter. S_{21} refers to two-port scattering parameter providing the forward voltage gain of the device under test, where port 1/port 2 is configured as input/output. The first and second natural frequencies of the resonator are measured around ~73.8 kHz and ~203 kHz, respectively.

4. Operating Principle

MEMS resonators can be excited at different modes of vibration by manipulating the input excitation frequency and force. However anti-symmetric modes of vibration are not easily excited and special input conditions and electrode configurations are required [25]. Figure 2(b) shows the response of the resonator near the second resonance mode to a half electrode (anti-symmetric) and full electrode (symmetric) excitation. It is observed that only an anti-symmetric excitation is able to activate the second resonance mode. Using a full electrode excitation, only the first frequency appears; the second frequency does not show up, as expected. Second mode excitation can be achieved by applying input through any of the four half electrodes present on both sides of the device, Fig. 1. Further, second mode of vibration can be even strongly excited by applying input on two half electrodes at the same time which are positioned diagonally across the microbeam. In this work, the basic logic gates OR and NOT will be achieved by selective activation and deactivation of the second mode of vibration of a clamped-clamped microbeam. These logic gates are then cascaded to realize the universal NOR gate. An on-resonance state, where the motional signal is high due to the microbeam vibrating with high amplitude, is assigned High "1" logic output state, while an off-resonance state, where the motional signal is negligible, is assigned Low "0" logic output state, Fig. 2(b). The maximum amplitude frequency is chosen as the operating point for the logic operation.



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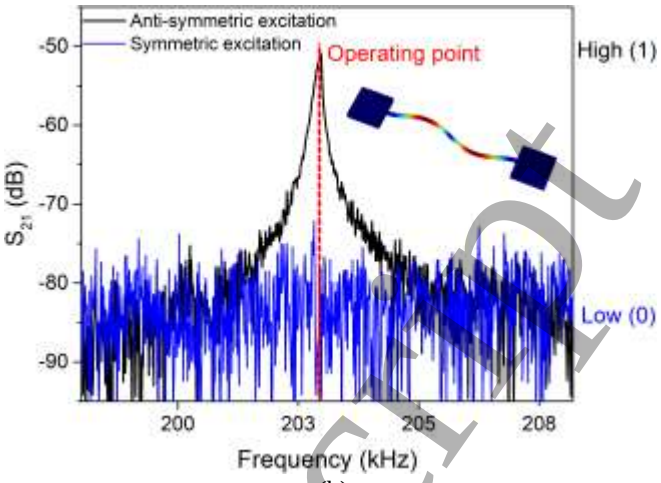

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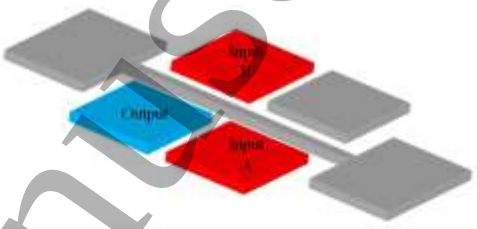
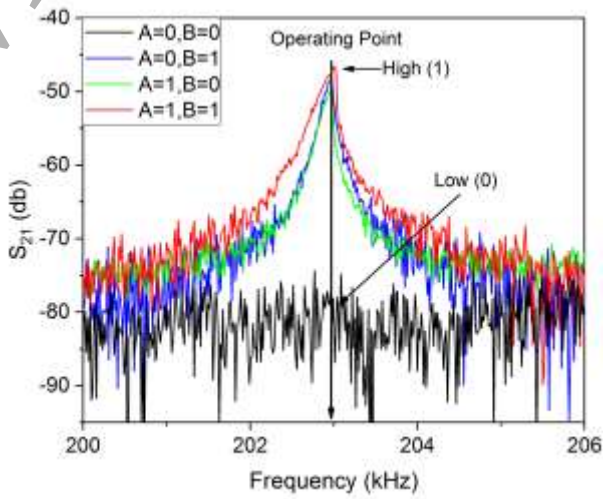


Input A	Input B	2nd resonance mode	Logic output
0	0	Not activated	0
0	1	Activated	1
1	0	Activated	1
1	1	Activated	1



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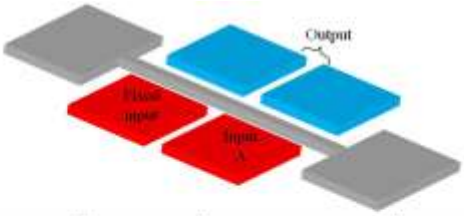
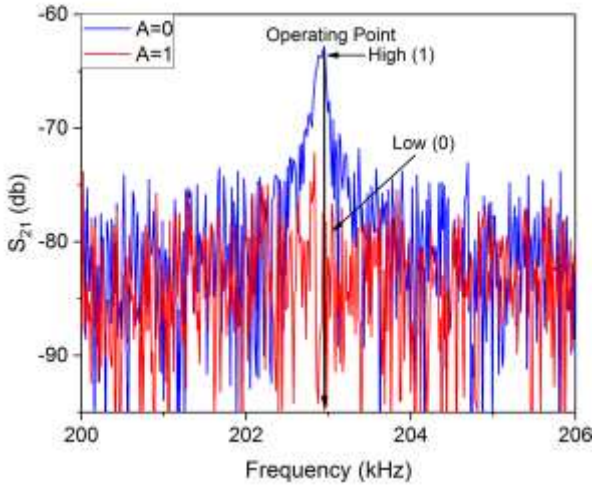


Fixed input	Input A	2nd resonance mode	Logic output
1	0	Activated	1
1	1	Not activated	0



(d)

Figure 2. (a) Schematic of the experimental setup used to characterize the microbeam. (b) Frequency response of the resonator at its second mode of vibration for an electrostatic loading of V_{DC} = 70V and gate input V_{AC} =-30 dBm (79.5 mV (RMS)). The anti-symmetric excitation via half electrode shows the second mode activated and an on-resonance response (black). The symmetric excitation via full electrode shows the second mode activated and an off-resonance response (blue). The inset shows a schematic of the second modeshape of the resonator. The maximum amplitude frequency point is chosen as the operating point for logic operations. An on-resonance (off-resonance) response is assigned the High "1" (Low "0") logic value. Schematic showing electrical interconnects, truth table, and frequency response for (c) OR and (d) NOT logic operation.

In order to perform the OR gate two inputs gates must be assigned to any of the two electrodes place diagonally across the beam, Fig. 2(c). In this case, if either of the input gate is active (1,0)/(0,1) or both the input gates are active (1,1), the resonator responds at the second mode of vibration and a "1" output is recorded. Since only the (0,0) case gives a "0" output, an OR gate operation is realized.

In order to perform a NOT gate, input gates must be assigned to two adjacent electrodes on either side of the resonator, while the remaining electrodes could be used for output detection, Fig. 2(d). One of the inputs is fixed at a constant High "1" state. When the gate input for NOT gate is ON "1", the microbeam is excited by a full electrode due to presence of the fixed input signal. In this case the second mode of resonance is not activated and an inverted output of "0" is recorded. Similarly, when the gate input is OFF "0", the resonator vibrates at the second mode of vibration due to half electrode excitation, caused by the fixed input signal, giving a High "1" output signal. This completes the NOT operation.

5. Cascaded Logic Gates

Having the same input and output signal waveforms (AC signals) and the same operational frequency among the various logic gates are key requirements for cascading. These features are inherently built-in in the proposed technological platform. To cascade multiple of these logic devices in series configuration, it is important to condition the output signal of a logic device such that it is suitable to drive the next logic device. Toward this, we use a custom built signal conditioning circuit comprising of buffers, amplifiers, and parasitic removal elements. Figure 3 shows the experimental setup and, as an example, the results of cascading in series two OR gates resonators. The response of OR_1 to logic inputs of (1,1) produces a weak output signal unfit to drive the next resonator logic device. The signal conditioning circuit, shown in Fig. 3(a), is used to amplify the output signal of OR_1, shown in Fig. 3(b), to the required level of the input signal, such that it can be used as an input signal for OR_2. Another major challenge in cascading is the intrinsic feed-through parasitic capacitance (C_p) that exists between the input and output electrodes. Our signal conditioning circuit consists of three stages: parasitic signal cancellation, current to voltage conversion, and an amplification stage. We use an external variable capacitor and adjust its value to match the value of C_p, which is one of the common techniques to cancel the feed-through signal [26,27]. This cancellation technique eliminates any unwanted parasitic signals coming from previous stages and results in obtaining the pure motional signal at the output of the resonator, which translates into larger difference between the high and low output states (i.e., larger noise margin). The extracted motional current is then converted into a voltage signal through the resistor R_1 (10MΩ). In the third stage, the extracted motional signal is amplified to make it strong enough to drive the other device. Two buffer stages are added to the circuit to ensure proper isolation of the signal conditioning circuits and logic elements.

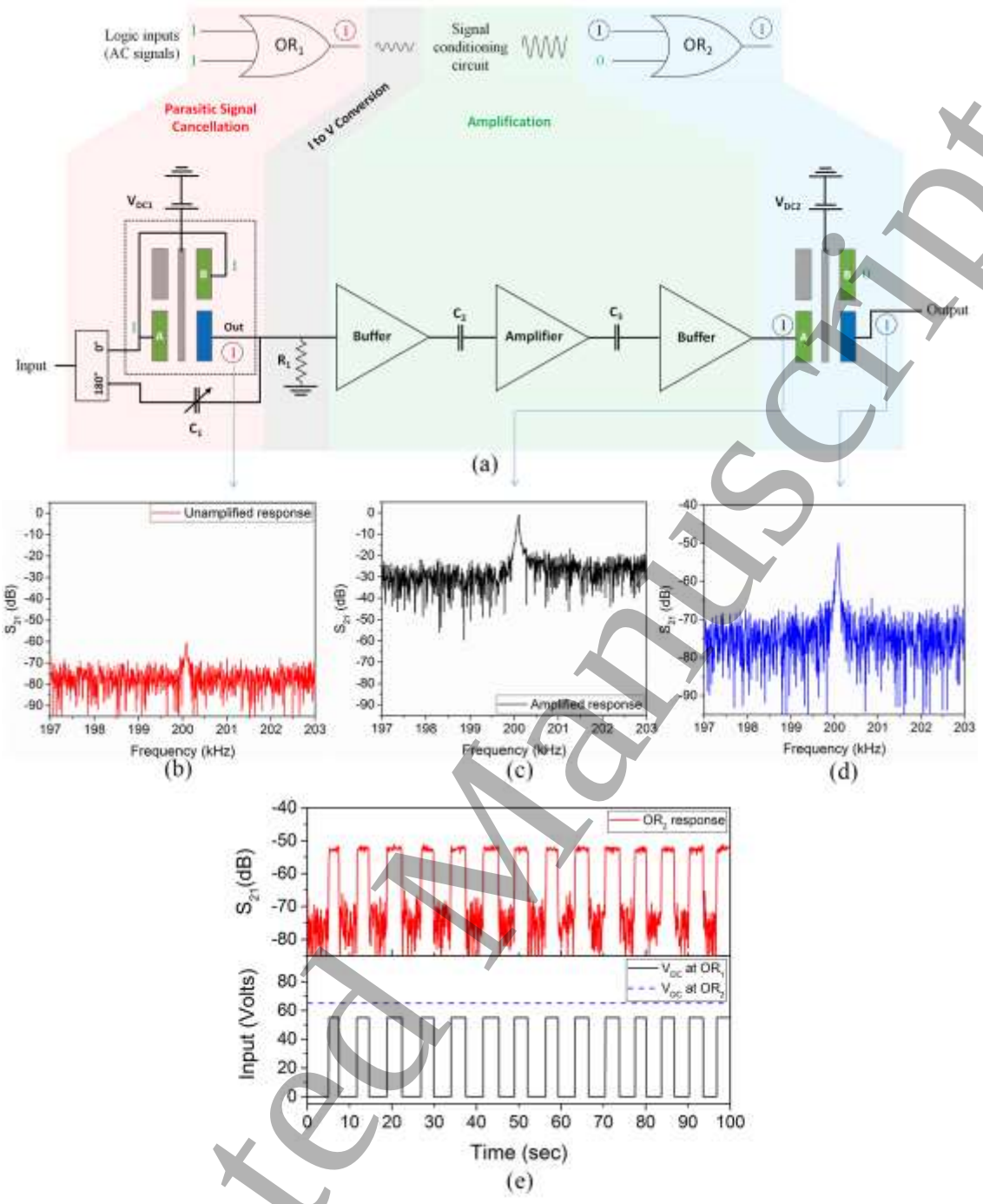
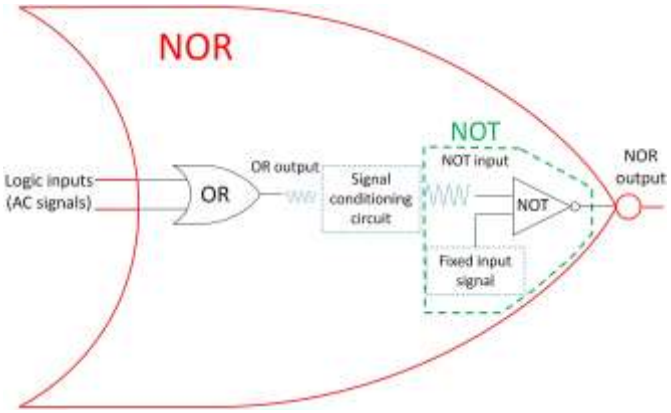


Figure 3. Cascading microresonators. (a) Schematic of the proposed cascading scheme showing the conditioning circuit and its comprising components. Network analyzer is used to provide the input to the first resonator and detect the output from the second resonator. A case study of cascading two OR gates are demonstrated as an example. (b) Response of the first resonator for (1,1) logic input condition. The output is then amplified via the signal conditioning circuit. (c) Amplified response of the resonator after the signal conditioning. This output signal is then applied to the next resonator logic device (OR_2) as "1" logic input. (d) Response of OR_2 to a logic input of (10), where the input "1" is the output of OR_1. All responses are recorded through backward frequency sweeps to ensure operation in the monostable regime. (e) Switching response of cascaded microresonators operating at ~200.074 kHz. The experimental parameters are V_{DC} (OR_1) = 55V, V_{DC} (OR_2) = 65V, V_{AC} (logic inputs) = -30 dBm (0.007 V_{RMS}), P=20 mTorr, and T=25^0 C.



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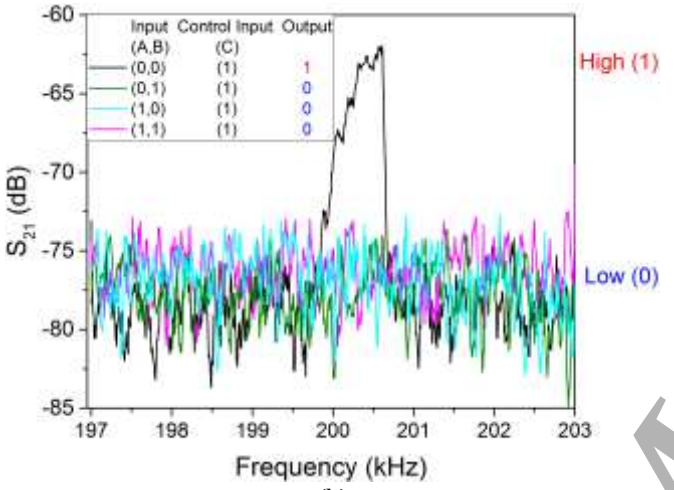


(b)

Figure 4. Demonstration of NOR operation. (a) Schematic of the experimental setup and interconnect scheme to perform the universal NOR logic operation. (b) Response of the resonator under various input logic conditions. A Low (0) response is recorded for all the cases except for A=0, B=0, for which a High (1) response is recorded. The experimental parameters are V_{DC} (OR) = 55V, V_{DC} (NOT) = 65V, V_{AC} (logic and control inputs) = 14.14 mV (RMS), P=20 mTorr, and T=25^0 C.

Figure 3(c) shows the conditioned signal, ready to drive the next blocks. Figure 3(d) shows the response of the second resonator to that signal. As discussed before, it is necessary to have the same resonance frequencies of the individual microresonators. Although the resonators were designed to be identical, due to fabrication imperfections, their resonance frequencies had to be finely tuned using a DC bias voltage. In order to further confirm and verify the cascading of the two OR logic units, a time sweep, shown in Fig. 3(e), at the maximum amplitude frequency ~200.074kHz of Fig. 3(d) is performed, under similar experimental conditions. In this case the AC input signals are provided all time while the respective DC biases of the resonators are controlled to activate and deactivate each resonator. The second resonator is kept active at all time by keeping its DC bias ON. However, the first resonator is activated and deactivated by switching its respective DC bias ON and OFF. We notice from Fig. 3(e) that whenever the OR_1 is OFF, a "0" output is passed onto the OR_2 resulting in a Low (0) off-resonance response of the second resonator. However, when the OR_1 is ON, a "1" output is passed onto the OR_2 resulting in High (1) response of the second resonator. The High and Low levels of the output responses are comparable to the response of Fig. 3(d) at 200.074 kHz. This experiment confirms that the first resonator logic device is capable of driving the second resonator logic device and a successful cascading of two logic devices (OR) is achieved.

As a second case study, using a similar experimental setup as in Fig. 4, we demonstrate the universal NOR logic gate by cascading an OR with a NOT gate, as shown in Fig. 4(a). A forward sweep is used, Fig. 4(b). This is due to the fact that the overall output signal of the resonator logic device working as a NOT gate is smaller due to the lower anti-symmetric force. This causes the backward sweep response (mono-stable) to be buried in noise. This issue can be addressed by optimization of the geometry of the device, for example, by reducing the gap between the excitation/detection electrodes with the microbeam.

6. Discussion

Among the key aspects for alternative logic elements are the maximum operation speed and energy consumption per logic operation. The logic operation speed for the current devices is limited by the mechanical transition time (Q/f) [28], which is around ~167 Hz, for Q~1200 at 20 mTorr. The operation speed of the device needs significant improvement for practical applications. The transition time could be reduced by decreasing the quality factor and increasing the resonance frequency. However, decreasing Q beyond a certain range will adversely affect the signal-to-noise ratio (SNR). Hence, a more logical choice would be to increase the resonance frequency of devices with proper choice of structural materials and down-scaling of the device dimensions. With NEMS resonators reaching GHz frequency range, operation speed in tens of MHz range is not principally out of reach [29].

For the proposed device depicted in Fig. 3(a), we focus on the energy consumption in the microresonator circuit. The energy per logic operation can be estimated conservatively using equation (1)

$$E_{Logic} = \frac{V_{AC}^2}{Z} \cdot t_s \quad (1)$$

$$Z = Z_p || R_M + R_1 \quad (2)$$

where Z is the total impedance in the circuit at resonance, comprising of a parasitic impedance Z_p in parallel with the microresonator motional resistance R_M, and a series resistor of R_1 (used as the terminating resistor at the buffer input, Fig. 3(a), and t_s is the switching time. To estimate the parasitic impedance Z_p we measure the insertion loss while providing no bias voltage to the resonator, V_{DC} = 0V, and terminate the sensing electrode directly to the network analyzer input port (load of 50Ω) without the LNA. Based on the measured insertion loss (~67 dB) and using $Z_p = 50\Omega \times 10^{\frac{S_{21}}{20}}$, Z_p is estimated to be ~112 kΩ at 200 kHz [30]. Similarly, to estimate R_M, we extract the pure motional signal at V_{DC} = 40V, and from the measured insertion loss of around 90 dB, the R_M is estimated to be ~1.6 MΩ. Thus, as per equation (2), E_{Logic} of ~120 fJ is calculated for V_{AC} = 14.14 mV (RMS), Z = 10.104 MΩ, and t_s = 6 ms.

Table 1. Performance parameters for MEMS, NEMS, and CMOS technology

	Current device	Proposed NEMS device	CMOS technology
Operating frequency	200 kHz	1.02 GHz	
Quality factor	1200	100	
Switching speed	~6 ms[28]	0.1 µs	
Energy/logic operation	~120 fJ	~0.2 fJ	0.6 fJ (45nm node) [31], 0.06 fJ (7nm node) [32]

Table 1 summarizes performance parameters of the current device, proposed NEMS resonator, and existing CMOS technology. The simulations for the proposed NEMS resonator are carried out for a Si clamped-clamped beam of length 1300nm, width 250nm, thickness 75nm, and gap 20nm. A DC voltage of 15V and an AC signal of 100mV are used. The motional resistance is estimated to be ~4MΩ [33]. It can be noticed that a device with an energy consumption as low as ~0.2fJ can be potentially achieved.

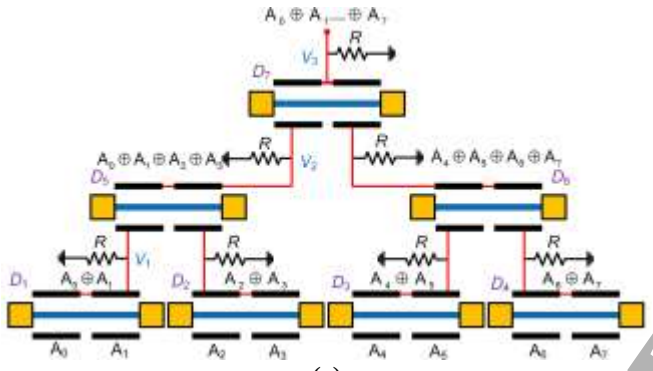
It can be observed that for the current device a large DC voltage ~50 V is required to bias the resonator, so a charge pump circuit is required. Our final goal is to optimize the device dimensions and minimize the air gap between the beam and the drive/sense electrodes. By doing that, the required DC voltage will also decrease and eventually a charge pump may not be required, or even if required, it consumes negligible energy compared to the current device, considering that the output is fully capacitive and there is no resistive load drawing current [34,35]. One possible NEMS device is proposed in Table 1.The required power to run the charge pumps is essentially used for charging and discharging the parasitic capacitances, and according to [35], with small load capacitance we expect short rise times and very small charges required for maintaining the voltage. For the current device, the total power required in the steady state, assuming bias voltage of 50 V, input voltage of 3 V, optimal stages and total charge pump capacitance of 50 pF, load capacitance of 19.5 fF, charge pump frequency of 50 KHz, and parasitic to branch capacitance ratio of 0.1, is approximately 2.85 nW. While this is a relatively large power consumption figure for device, we should point out that the entire circuit is fed by a single charge pump, and so long as the total load is reasonably smaller than the capacitance of the charge pump, the power consumption does not increase substantially [35]. As an example, if the VLSI application requires 1000 devices, the total load, including the interconnects, will increase to ~22pF, and the power of the charge pump increases to 3.15 nW. This leads to an average energy/op of only 18 fJ for each device, even for the current speed of 167 Hz. Obviously, with device optimization, the required DC voltage decreases and operation speed increases, both leading to a dramatic drop in effective energy/op attributed to the charge pump.

It is noteworthy that the implementation of logic circuits with microresonators is significantly less complex and utilizes fewer number of devices compared to CMOS. For instance, a two input XOR and OR can be implemented via a single microresonator, which otherwise would require 8 and 6 CMOS transistors, respectively. With a careful study of fan-in and fan-out limitations and development of standard cell libraries tailored for microresonators, this technology can potentially achieve one order of magnitude saving in device count and energy cost. Furthermore, a small AC voltage juast enough to achieve a viable response above thermomechanical noise should be used to achieve even lower energy cost per operation. Similarly, due to the dependence of energy cost on switching speed, increasing the switching frequency also will greatly improve the energy cost in NEMS resonator based logic devices. Despite their limitations in terms of operation speed, these devices can be attractive alternatives as low power deployable data processors in industrial, domestic, quality control, and other embedded and smart systems applications, where high speed computation is not as crucial.

To implement complex digital circuits, the microresonator logic elements must be cascaded, which may require preconditioning (amplification) of the output AC signal of each stage before it can be used as the input signal for the next stage. This will demand additional circuitry and increased energy consumption. For the current device and switching speeds, the required energy/operation of the signal conditioning blocks can be estimated around 100 pJ if standard on-chip nanowatt amplifiers are used. With careful device engineering and improvement of switching speed, in

addition to optimized amplifier design, the energy cost can be reduced by 2-3 orders of magnitude.

Another important challenge toward cascading is the frequency mismatch in a logic array caused due to the variations in the fabrication process. The resonance frequency curve overlap between the two subsequent logic devices should fall within the 3-5db bandwidth for accurate logic operation. This value is found out to be ~210 Hz for the current device. Ideally, a low quality factor device is desired which not only results in increased speed of operation for a fixed frequency, but also allows larger deviation tolerances among the resonance frequencies of two consecutive resonators.



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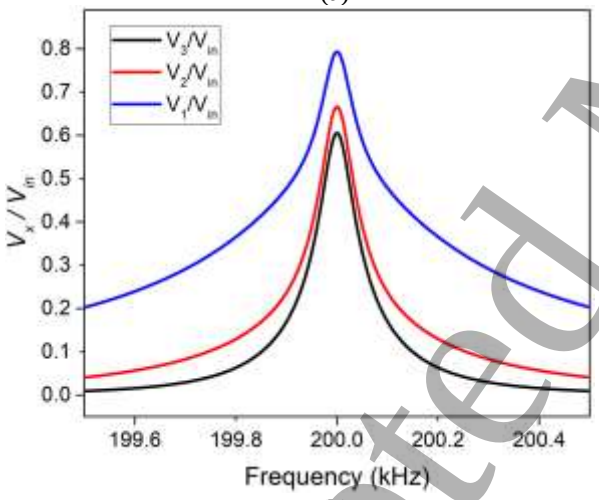

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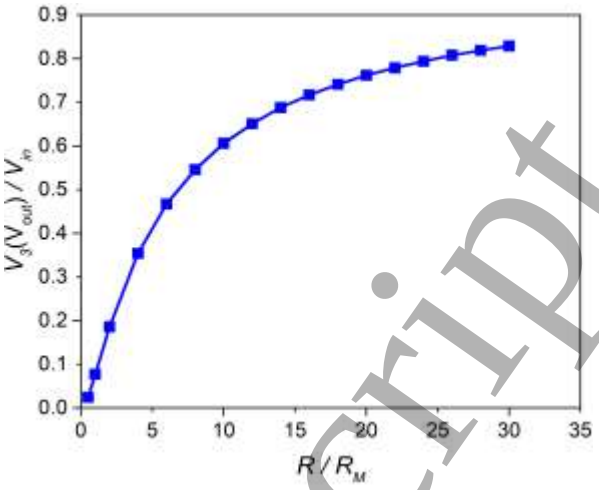

(c)

Figure 5. Proposed 8-input XOR gate (8-bit parity checker). (a) Schematic of the implementation of the 8-input XOR gate. (b) Simulated frequency response of the cascaded chain of M/NEMS resonators for R/R_M =10, and considering A_0=1and A_1 … A_7=0. Values of the ratio between the node voltages (V_1, V_2, V_3) with respect to the input voltage (V_{in}) are shown. (c) The ratio between output voltage (V_3) and input voltage (V_{in}) for different values of R/R_M for an input AC signal frequency of 200 kHz (resonance frequency). For the first stage resonators, V_{in} = 14.14 mV (RMS) represents the logic input 1. Although this value falls to 8.56 mV (RMS) at the output stage (V_3), for R/R_M =10, it is still enough to be considered as logic 1 input for subsequent logic blocks.

Table 2. Performance parameters for MEMS, NEMS, and CMOS technology for 8-input XOR gate

	Current device	Proposed NEMS device	CMOS technology
No of devices used	7	7	68
Energy/logic operation	~850 fJ	~1.4 fJ	3.7 fJ (45nm node) [31], 1 fJ (7nm node) [32]
Layout area	0.024 mm^2	4.65 µm^2	18.8 µm^2 (45nm Node-2 input XOR)[36]

To fully capitalize the potential of NEMS resonator logic devices and to be competitive with standard CMOS in terms of energy cost, the number of CMOS amplifiers/buffers in complex digital circuits must be minimized. This might be achieved by using circuit design techniques optimized and tailored for this technology and developing standard cell libraries accordingly. An example is an 8-input XOR gate (also known as 8-bit parity checker), depicted in Fig. 5(a). Although the circuit is composed of three cascaded stages, no intermediate CMOS amplifiers/buffers are required for its

functionality. Fig. 5(b) shows the simulated frequency response of the cascaded chain of M/NEMS resonators for R/R_M =10, and considering A_0 = 1and A_1 … A_7 = 0. For this simulation, we have considered motional inductance, L_M = 11 kH, and motional capacitance, C_M = 57.6 aF, typical for these kinds of microresonators [37]. The ratio between the node voltages (V_1, V_2, V_3) with respect to the input voltage (V_{in}) in the cascaded chain are shown. Fig. 5(c) shows the ratio between the output voltage, V_3 and input voltage, V_{in} for different values of R/R_M. For the first stage resonators, V_{in} = 14.14 mV (RMS) represents the logic input 1. At resonance, 200 kHz, (AC input signal frequency) this value falls to 8.56 mV (RMS) at the output stage, V_3 for R/R_M =10, which is several orders above the onset of thermomechanical noise floor (~1μV) for these devices and acceptable as an input for the following stages. This enables us to construct circuits with moderate logic depth and complexity, without any need for CMOS signal conditioning sub-circuits. Note that the proposed parity checker circuit can be implemented with only 7 microresonators, while the standard CMOS counterpart requires 68 transistors and other micro-electromechanical logic technologies, such as MEM relays, can implement the same function with 12-20 devices [38,39]. For R_M =1.6MΩ, the circuit in Fig. 5(a) is estimated to consume ~ 850 fJ per logic operation for the current device, and only ~ 1.4 fJ for a scaled NEMS resonator of Table 1. As summarized in Table 2, this is significantly smaller than the energy per operation of a CMOS based 8-bit parity checker built in 45 nm (3.7 fJ) and 7 nm (1 fJ) technology nodes [31].

It is worth mentioning that using a large load resistor (10MΩ) along with the parasitic capacitance form a low pass filter (f_{LP}~100-300 kHz) at each node, which will reduce the actual operation speed. One possible solution is to decrease the value of R_m by proper device design (decreasing the air gap and in general increasing the electromechancial coupling coefficient, increasing the beam bias). By decreasing R_m, the required load resistor will be smaller and hence the cut-off frequency will be higher. Also, while the parasitic capacitance is going to be large for n-well resistors or MOS resistors, optimized P^+/P^- non-silicide resistors in advanced technology nodes can easily achieve >1kΩ/sq, with parasitic capacitances well below 50-70 aF/μm^2 [38-39], limiting the total parasitic capacitance to <10fF level and increasing f_{LP} to values >>1GHz.

Note that DC modulated NEMS resonator based logic devices [13] consume relatively less energy to perform the switching operation, however, a constant source of energy dissipation still exists in the form of the activation energy applied as an AC voltage to the resonator. This in other words is analogous to the leakage in CMOS based logic devices. Also, other relevant works on microresonator based devices [16-20] suffer from slow response time and high energy cost due to the used electrothermal actuation. The work presented here eliminates such issues.

A final note is the down scaling of the proposed mechanical logic platform. Scaling such device configuration down to the NEMS regimes is well documented in the literature [9, 21]. Fundamentally, the working principle demonstrated in this work, based on electrostatically actuated structure, is applicable for Nano devices made with different materials, such as Carbon nanotubes [40], MoS_2 and Graphene membranes [41, 42]. The ultimate scaling limit of these devices remains an open research topic and warrants further investigation.

7. Conclusions

In this work we have proposed a conceptual and experimental platform for cascadable electromechanical logic devices. The proposed logic technology uses the selective activation and deactivation of second mode of vibration of a clamped-clamped microbeam to perform logic operations. Furthermore, we demonstrated for the first time cascading two electromechanical logic devices in series, operating at the same frequency, and showed the realization of a cascadable universal NOR logic gate by cascading an OR and a NOT gate, hence, building a functionally complete logic set. The proposed scheme unifies the input and output signal waveforms and realizes different logic operations at the same operating frequency. These characteristics make such a device a natural candidate for cascading logic gates in order to eventually perform complex computing operations. Even though this technique removes major hurdles in the way of developing resonator based cascaded logic gates, ideally, it is crucial to eliminate dependency on CMOS for signal amplification and/or provide electrical isolation between two logic blocks to reduce overall energy cost in the system. The signal conditioning circuit used to demonstrate cascading operation in this work was necessary due to the fact that the amplitude of the output signal through capacitive detections was low, unable to drive subsequent resonator logic devices connected in series. This issue can be addressed by using other alternative methods for amplification. An active front of research is currently focused on solving such issues [37,45-47]. For example, an active transistor resonator element was recently shown in [48] that can potentially eliminate the use of CMOS based circuits for signal amplification. Similarly, transfer of mechanical modes to neighbouring resonator via coupling elements can also be explored [49,50]. Design techniques that lower the number of external components used for signal conditioning and amplification in large circuits was also proposed. The demonstration of cascadable fundamental logic gates, such as, OR, NOT and a universal logic gate NOR is believed to set the stage can pave the way for more aggressive research

on the development of such technology for an alternative ultra-low power computing paradigm.

Acknowledgements

Authors acknowledge Mr. Ren Li from Integrated Circuits and Systems Group, CEMSE Division, KAUST for his help with energy cost analysis for CMOS. This publication is based upon work supported by the King Abdullah University of Science and Technology (KAUST) office of sponsored research OSR under Award No. OSR-2016-CRG5-3001.

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