# Cascade-Free Model Predictive Control for Single-Phase Grid-Connected Power Converters

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***Abstract*—In a conventional FCS-MPC formulation, active and reactive power control loops rely on the predictive controller while the dc-bus voltage is usually governed by a PI-based control loop. This comes from fact that the dynamic equations for describing the predictions of these variables are heavily coupled. In this paper, a cascade-free finite control set model predictive control (FCS-MPC) for single-phase grid-connected power converters is presented. The proposed control algorithm is formulated in terms of established dynamic references design, which was originally proposed to directly govern active and reactive power, and dc-voltage in three-phase power converters. In this work, the dynamic reference design concept is extended to control single-phase grid-connected power converters. The proposed control algorithm does not use instantaneous ac-power calculations; instead it directly formulates the optimal control problem on the grid-current in the original stationary reference frame. The experimental results obtained with a single-phase grid-connected Neutral Point Clamped (NPC) converter confirm a successful design, where system constraints, e.g. maximum power and weighted switching frequency, are easily taken into account.**

***Index Terms*—Predictive models, control design, predictive control, finite control set, converters, DC-AC power converters, smart grids, power quality, reactive power.**

## I. Introduction

SINGLE-PHASE grid-connected power converters play a key role in applications such as integration of renewable energies, and particularly high-power applications, such as high-speed railway electrical traction systems [1]. The popularity of these converters, technically called Active Front End (AFE) rectifiers, lies in their ability to allow bidirectional power exchange between ac and dc output terminals while maintaining high power quality in terms of Power Factor (PF) and Total Harmonics Distortion (THD) on the ac-side [2], [3].

The main control objectives for single-phase grid-connected power-converters are: to self-support the dc-bus voltage under load and grid-voltage variations, and to draw sinusoidal grid-current while maintaining the reactive power level around its reference. The available literature shows that for classic pulse width modulation (PWM) control methods, such as voltage-oriented control (VOC), the design procedure is 100% related to tuning proportional-integral (PI) controllers in both dc-bus voltage and grid-current loops [4]–[7]. The other widely accepted method is direct power control (DPC), which uses hysteresis comparators and look-up tables. Recently, a model based adaptive DPC [8] for three-phase grid-connected power converters has been proposed that avoids system parameter uncertainties, while improving the overall behavior of the system compared with both standard PI and hysteresis-based controllers.

For the purpose of explicitly considering the converter switching effects, the so-called Finite-Control-Set Model Predictive Control (FCS-MPC) has been introduced to govern power converters [9]. The main advantage of FCS-MPC is that offers the possibility to manage various control objectives in only one cost function and, at the same time, can handle system constraints with ease. Although more than one control objective can be used, traditional MPC-based control algorithms either for grid-connected and electrical-drives power-converters use the classical cascaded structure of an outer PI based dc-bus voltage/speed loop which delivers the power(current)/torque(current) reference to an inner MPC active-reactive power/torque(current) loop. As a consequence, the overall system performance is still influenced by the linear controller-based outer loop, which may present poor dynamic or overshoot in the outer loop [10].

A model predictive direct speed control (MP-DSC) which overcomes limitations of cascade linear controllers, was presented in [11]. This control is mainly based on the use of an attraction region defined by the MTPA (Maximum Torque per Amp) trajectory, which is used to give importance to secondary control objectives during transient conditions. In the same direction, a cascade-free predictive speed control for electrical drives, that uses a simplified equivalent *double integrator* model for representing the dynamic behavior of the motor was proposed in [12]. In that case, it was proved that the proposed equivalent model was able to successfully represent the expected machine behavior. For grid-connected power converters, a soft-constrained MPC formulated as a single optimization problem was proposed in [13] to avoid the use of PI controllers. However, there is no fixed design procedure in the soft-constrained MPC to set the upper and lower bounds, and the weighting factor of each control variable included in the cost function. In the same direction, a three-phase AFE rectifier governed by a cascade-free MPC-based Direct Power Control (MPC-DPC) was presented in [14]. The major advantage of this strategy, called *dynamic references design*, is its capability to provide suitable references for the grid active power

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and the dc-bus voltage, while maintaining active and reactive power decoupled. The concept have been described in detail in [14], however their applicability has not been demonstrated for single-phase AFE rectifiers. In essence, [14] formulates the cost function for a three-phase system in terms of the three-phase instantaneous active/reactive power definitions. In that case, the definition of the three-phase instantaneous *predicted powers* is directly considered for designing both the dynamic references and the cost function. Since the *predicted powers* are instantaneous powers in the time domain which does not have oscillations (mainly free of second harmonic), they can be directly used on the cost function formulation. However, for the particular case of single-phase grid-connected power converters, the instantaneous power calculation is not free of second harmonic. Thus, a straightforward implementation of [14] on single-phase systems is not possible.

The work at hand presents the design, implementation and evaluation of a cascade-free FCS-MPC strategy for single-phase grid-connected power-converters that address the issues outlined above. The key novelty of this approach is the compatible reference design, which allows the controller to transfer the required dc-power from the grid while regulating the dc-voltage and imposing a desired power factor by only control the grid-current. To accomplish this, the dynamic reference design concept which was originally proposed to govern three-phase power converters [14] is adopted and extended to single-phase converters. Nevertheless, the optimal control problem is directly formulated on the grid-current in the original stationary reference frame. As an illustrative example, the proposed method is used to govern a single-phase NPC converter working as an AFE rectifier.

Additionally, two different cost function formulations to evaluate the effectivenesses of the proposed algorithm in terms of obtaining a spread and imposed grid-current harmonic spectrum are adopted [15].

## II. Single-Phase Grid-Connected Power-Converter Model

In general, single-phase grid-connected power-converters can be modeled as a four-port power module where its terminals describe the respective ac-side (grid) and dc-side connections, as shown in Fig. 1. Depending on the topology of the internal circuit, the ac-side terminals can behave as a multilevel-converter that fulfills the needs for low total harmonic distortion (THD) with reduced $\frac{dv}{dt}$. On the other hand, the dc-side terminals can behave either as an electrical load or power source. In order to control all the required power converter variables, a control block external to the converter enforces the desired behavior.

The work at hand focuses on the control of a single-phase converter which is connected to the grid by means of a $L$ filter ($r$ represents the parasitic resistor of $L$). The dc-side is connected to a dynamic load as shown in Fig. 2. As a study case, a single-phase NPC converter is considered in this work. Thus, it is required to control not only the continuous-time variables grid-current, $i_g$, and the dc-voltage, $v_{\rm dc}$, but also the internal capacitor voltages $v_{C_1}$ and $v_{C_2}$.

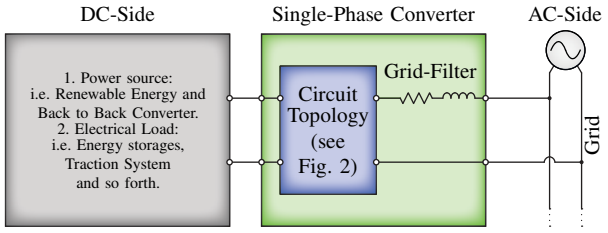


Fig. 1. Generalized circuit diagram of a single-phase grid-connected power-converter as interface to power sources or electrical loads.

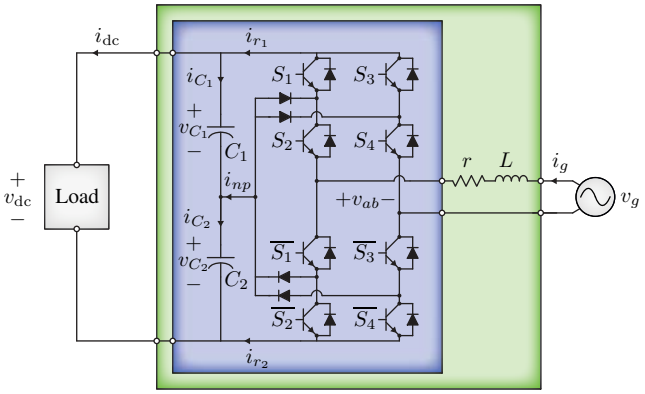


Fig. 2. Circuit topology of the single-phase grid-connected NPC converter.

By analyzing the schematic circuit shown in Fig. 2 it is possible to describe the continuous-time dynamic of the injected grid-current, $i_g$, via:

$$\frac{di_g}{dt} = \frac{1}{L}(v_g - ri_g - v_{ab}), \tag{1}$$

where $v_g$ stands for the grid-voltage and $v_{ab}$ represents the single-phase inverter voltage. On the other hand, the dynamic equations for the capacitor voltages are given by:

$$\begin{aligned} \frac{dv_{C_1}}{dt} &= \frac{1}{C_1} i_{C_1} = \frac{1}{C_1}\left(i_{r_1} - i_{\rm dc}\right), \\ \frac{dv_{C_2}}{dt} &= \frac{1}{C_2} i_{C_2} = \frac{1}{C_2}\left(-i_{r_2} - i_{\rm dc}\right). \end{aligned} \tag{2}$$

where $i_{C1}$ and $i_{C2}$ are the associated capacitor currents, $i_{r1}$ and $i_{r2}$ are internal currents of the NPC converter and $i_{\rm dc}$ is the dc-side current.

Thus, (1) can be transformed into discrete-time form by using the well known classical forward Euler method that exhibits enough precision to enable the controller to predict the future value of the grid-current, i.e.,:

$${i_g}^{k+1} = \left(1 - \frac{T_s r}{L}\right) {i_g}^k + \frac{T_s}{L}\left({v_g}^k - {v_{ab}}^k\right), \tag{3}$$

where $T_s$ is the sampling period, and the converter output voltage $v_{ab}$ can be expressed in terms of switching states (see Table I) as follows:

$${v_{ab}}^k = {v_{C_1}}^k (S_1 - S_3) + {v_{C_2}}^k (S_2 - S_4). \tag{4}$$

Therefore, based on the MPC requirements, the present values of $i_g$, $v_g$, $v_{C_1}$ and $v_{C_2}$ are needed to properly forecast the future behavior of $i_g$.

Since the regulation of $v_{C_1}$ and $v_{C_2}$ is also a control objective, the discrete-time form of (2) is obtained following the same procedure as used for (3), i.e.,:

$$\begin{aligned} {v_{C_1}}^{k+1} &= \frac{T_s}{C_1}{i_{r_1}}^k - \frac{T_s}{C_1}{i_{\mathrm{dc}}}^k + {v_{C_1}}^k, \\ {v_{C_2}}^{k+1} &= -\frac{T_s}{C_2}{i_{r_2}}^k - \frac{T_s}{C_2}{i_{\mathrm{dc}}}^k + {v_{C_2}}^k. \end{aligned} \tag{5}$$

To avoid unnecessary measurements of $i_{r_1}$ and $i_{r_2}$ it is convenient to define the direct relation between the switching states of the NPC converter and $i_g$ as [16]:

$$\begin{aligned} {i_{r_1}}^k &= \frac{S_A\left(S_A+1\right) - S_B\left(S_B+1\right)}{2}{i_g}^k, \\ {i_{r_2}}^k &= \frac{S_A\left(S_A-1\right) - S_B\left(S_B-1\right)}{2}{i_g}^k. \end{aligned} \tag{6}$$

Consequently, (3) and (5) can be used by the controller to obtain estimated values for the predictions of the grid-current and the capacitor voltages respectively.

## III. MPC for a Single-Phase Grid-Connected Power Converter

In this section, the proposed cascade-free FCS-MPC algorithm for a single-phase grid-connected power converter is derived. The procedure can be divided in three main parts: cost function formulation, stationary reference frame grid-current definition and grid-current *dynamic references design*. First, the control targets, grid-current tracking in the stationary reference frame and voltage balancing, are set into the cost function. Then, a definition of the grid-current in the stationary reference frame by means of the required active and reactive power is also derived. The resulting expression along with the *dynamic references design* concept is used to define the grid-current reference in the stationary reference frame and the dc-voltage references.

TABLE I
Switching States* of the Single-phase Full-bridge NPC Converter

| $j$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_A$ | $S_B$ | $v_{ab}$ |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 0 | 1 | -1 | $v_{C1}+v_{C2}$ |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | $v_{C1}$ |
| 2 | 0 | 1 | 0 | 0 | 0 | -1 | $v_{C2}$ |
| 3 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 4 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 5 | 0 | 0 | 0 | 0 | -1 | -1 | 0 |
| 6 | 0 | 1 | 1 | 1 | 0 | 1 | $-v_{C1}$ |
| 7 | 0 | 0 | 0 | 1 | -1 | 0 | $-v_{C2}$ |
| 8 | 0 | 0 | 1 | 1 | -1 | 1 | $-v_{C1}-v_{C2}$ |

*: only selected states.

### A. Cost Function Formulation

In general, a single control loop over the grid-current injected by the converter is enough to control the active and reactive power in the grid-side. However, for this particular converter, it is also required to regulate the dc-voltage, $v_{\mathrm{dc}}$, while keeping the capacitor voltage balance, i.e., $v_{C_1} = v_{C_2} = \frac{v_{\mathrm{dc}}}{2}$. It is important to emphasize the fact that both variables are heavily coupled, thus a compatible reference design is necessary in order to include both control targets (grid-current tracking and dc-voltage regulation) into the MPC grid-current reference. Therefore, the proposed cost function for the single-phase grid-connected NPC converter is:

$$\begin{aligned} J^k = &\left({i_g}^{\star k+1} - {i_g}^{k+1}\right)^2 + \\ &\frac{\overline{i_g}^2}{\left(\frac{\overline{v_{\mathrm{dc}}}}{2}\right)^2}\left({v_{C_1}}^{k+1} - {v_{C_2}}^{k+1}\right)^2, \end{aligned} \tag{7}$$

where $\overline{i_g}$ and $\frac{\overline{v_{\mathrm{dc}}}}{2}$ are rated values used to normalize the tracking errors. Notice that the dc-voltage control loop is not explicitly included in (7). This is due to the proposed controller that includes a static expression for the dc-voltage reference embedded in the computation of the optimal state $S_x^{\mathrm{opt}}$, $\forall\, x \in \{1,2,3,4\}$. For that reason, the design of the grid current reference ${i_g}^{\star k+1}$ which is directly related with the dc-voltage reference ${v_{\mathrm{dc}}^{\star}}^{k+1}$ is explained in detail in the following subsections.

### B. Stationary Reference Frame Grid-Current Definition

Clearly, the dc-side power can be obtained as follows:

$$\begin{aligned} {p_{\mathrm{dc}}}^k &= {p_{C_1}}^k + {p_{C_2}}^k + {p_{Z_{\mathrm{dc}}}}^k, \\ &= {i_{r_1}}^k {v_{C_1}}^k - {i_{r_2}}^k {v_{C_2}}^k, \end{aligned} \tag{8}$$

where $i_{r_1}$ and $i_{r_1}$ are taken from (6).

Regarding the ac-side, the instantaneous active ($p^k$) and reactive ($q^k$) power can be calculated by [17]:

$$\begin{aligned} p^k &= \frac{1}{2}\left(v_{\mathrm{d}}^k i_{\mathrm{d}}^k + v_{\mathrm{q}}^k i_{\mathrm{q}}^k\right), \\ q^k &= \frac{1}{2}\left(v_{\mathrm{q}}^k i_{\mathrm{d}}^k - v_{\mathrm{d}}^k i_{\mathrm{q}}^k\right), \end{aligned} \tag{9}$$

where $v$ and $i$ are any pair of voltage and current in a given common point expressed in their $\mathrm{dq}$ components. In this work, the synchronous frame is aligned to the grid-voltage, $v_g$, is considered as the direct component. Thus, the quadrature component of the grid-voltage is null, i.e., $v_{g_{\mathrm{d}}} = \hat{v}_g$ and $v_{g_{\mathrm{q}}} = 0$. Therefore, the grid-side active and reactive power can be expressed as follows:

$${p_g}^k = \frac{1}{2}\left(v_{g_{\mathrm{d}}}^k i_{g_{\mathrm{d}}}^k\right), \tag{10}$$

$${q_g}^k = -\frac{1}{2}\left(v_{g_{\mathrm{d}}}^k i_{g_{\mathrm{q}}}^k\right). \tag{11}$$

Finally, by utilizing (10) and (11), the expression for the grid-current in the stationary reference frame is obtained by multiplying each $\mathrm{dq}$ current component of ${i_g}^k$ by $\sin(\omega t)$ and $\cos(\omega t)$, i.e.,:

$${i_g}^k = \frac{2{p_g}^k}{v_{g_{\mathrm{d}}}^k}\sin(\omega t) + \frac{-2{q_g}^k}{v_{g_{\mathrm{d}}}^k}\cos(\omega t). \tag{12}$$

From (12), it is possible to confirm that by governing the injected grid-current, $i_g$, the active and reactive power injected to or absorbed from the grid can be handled. Note that this step is only an intermediate step that aims to find an equivalent mathematical expression for the grid-current. As will be elucidated, the *dynamic references design* concept will allow to define suitable references for active and reactive power in order to find the equivalent one-step ahead grid-current reference that matches with the form of (12).

### C. Grid-Current Dynamic Reference Design

A power balance on both power converter's terminals is used to obtain a compatible reference for both dc and ac control targets. However, it is not possible to instantaneously compare both ac- and dc-power. For instance, when $S_A$=$S_B$, the rectified currents $i_{r_1}$ and $i_{r_2}$ in (6) becomes zero, yielding to a null dc-power, i.e., $p_{\rm dc} = 0$, while the ac-power may not have a value equal to zero, i.e., $p_g \neq 0$. For this reason a so-called average dc-power reference, $\widetilde{p}^{\star}_{\rm dc}$, and average ac active power reference, $\widetilde{p}^{\star}_{g}$, are analytically derived to produce an average power balance in the power converter. Firstly, it follows that

$$\widetilde{p}_g^{\star k+1} = \widetilde{p}_r{}^{k+1} + \widetilde{p}^{\star}_{\rm dc}{}^{k+1}, \tag{13}$$

where $\widetilde{p}_r$ stands for the filter resistor power loss.

Since $\widetilde{p}^{\star}_{\rm dc}$ cannot be directly obtained as per (8), it is necessary to use average values for each term in (8). It is important to recall that each capacitor voltage can only be adjusted by their capacitor current, which takes energy from the grid. To achieve the power balance while maintaining a desired behavior in the capacitor voltages, a reference prediction horizon $N^{\star}$ is introduced [14]. The value of $N^{\star}$ allows the controller to take enough power from the grid in order to reach $v^{\star}_{\rm dc}{}^{k+1}$ in $N^{\star}$ steps, while limiting each capacitor current increment by $\frac{1}{N^{\star}}$ of the total current required to lead the dc-voltage reference. Thus, the average next-step capacitor voltage references are given by:

$$\begin{aligned}\widetilde{v}^{\star}_{C_1}{}^{k+1} &= v_{C_1}{}^{k} + \frac{1}{N^{\star}}\Big(v^{\star}_{C_1}{}^{k} - v_{C_1}{}^{k}\Big)\\ \widetilde{v}^{\star}_{C_2}{}^{k+1} &= v_{C_2}{}^{k} + \frac{1}{N^{\star}}\Big(v^{\star}_{C_2}{}^{k} - v_{C_2}{}^{k}\Big),\end{aligned} \tag{14}$$

where $v^{\star}_{C_1}{}^{k} = v^{\star}_{C_2}{}^{k} = \frac{v^{\star}_{\rm dc}{}^{k+1}}{2}$.

Therefore, the required average capacitor currents to achieve these voltage references are:

$$\begin{aligned}\widetilde{i}^{\star}_{C_1}{}^{k+1} &= \frac{C_1}{T_s}\big(\widetilde{v}^{\star}_{C_1}{}^{k+1} - v_{C_1}{}^{k}\big)\\ \widetilde{i}^{\star}_{C_2}{}^{k+1} &= \frac{C_2}{T_s}\big(\widetilde{v}^{\star}_{C_2}{}^{k+1} - v_{C_2}{}^{k}\big).\end{aligned} \tag{15}$$

Additionally, the required average dc-current for this set point is given by:

$$\widetilde{i}^{\star}_{\rm dc}{}^{k+1} = \frac{\widetilde{v}^{\star}_{C_1}{}^{k+1} + \widetilde{v}^{\star}_{C_2}{}^{k+1}}{\widetilde{r}^{k+1}_{\rm dc}}. \tag{16}$$

Since the actual values of $v_{C_1}{}^{k}$ and $v_{C_2}{}^{k}$ are available as measurements and the average dc-side power consumption modeled by $\widetilde{r}_{\rm dc}$ can be considered approximately constant between two consecutive steps, $\widetilde{r}^{k+1}_{\rm dc}$ can be estimated by considering the measurement of $i_{\rm dc}{}^{k}$ as:

$$\widetilde{r}^{k+1}_{\rm dc} = \frac{v_{C_1}{}^{k} + v_{C_2}{}^{k}}{i_{\rm dc}{}^{k}}. \tag{17}$$

After following the above procedure, an average dc-power reference $\widetilde{p}^{\star}_{\rm dc}{}^{k+1}$ can be defined as:

$$\begin{aligned}\widetilde{p}^{\star}_{\rm dc}{}^{k+1} = &\Big(\widetilde{i}^{\star}_{\rm dc}{}^{k+1} + \widetilde{i}^{\star}_{C_1}{}^{k+1}\Big)\,\widetilde{v}^{\star}_{C_1}{}^{k+1}\\ &+ \Big(\widetilde{i}^{\star}_{\rm dc}{}^{k+1} + \widetilde{i}^{\star}_{C_2}{}^{k+1}\Big)\,\widetilde{v}^{\star}_{C_2}{}^{k+1}.\end{aligned} \tag{18}$$

Proceeding accordingly and recalling that grid-connected single-phase converters present a large second-order harmonic component in the dc-side variables, the latter $\widetilde{p}^{\star}_{\rm dc}{}^{k+1}$ is then filtered with a notch-filter[1] centered at 100 Hz ($2f$). Furthermore, the use of the notch-filter output as a reference $\big\langle \widetilde{p}^{\star}_{\rm dc}{}^{k+1} \big\rangle^{-2f}$ provides a current reference $i_g^{\star k+1}$ free of third harmonic in the stationary frame.

To account for the filter inductor loss it is necessary to estimate the resistor power loss. Thus, it follows that:

$$\begin{aligned}\widetilde{p}_r^{\star k+1} &= \frac{1}{2} r \left(\hat{i}_g{}^{k+1}\right)^2\\ &= \frac{2r}{\big(\hat{v}_g{}^{k+1}\big)^2}\Big(\big(\widetilde{p}_g^{\star k+1}\big)^2 + \big(q_g^{\star k+1}\big)^2\Big)\end{aligned} \tag{19}$$

Here, $\hat{v}_g{}^{k+1} \approx \hat{v}_g^{k}$ and $\hat{i}_g{}^{k+1}$ are the peak values of grid-voltage and current respectively.

Now, it is possible to transfer power from the ac-side by considering (13), (18) and (19). Thus, the total power balance (13) becomes a quadratic equation in $\widetilde{p}_g{}^{k+1}$ ($a^2+bx+c=0$) as:

$$\begin{aligned}\frac{2r}{\big(\hat{v}_g^{k}\big)^2}\big(\widetilde{p}_g^{\star k+1}\big)^2 - \widetilde{p}_g^{\star k+1} + \big\langle \widetilde{p}^{\star}_{\rm dc}{}^{k+1} \big\rangle^{-2f} +\\ \frac{2r}{\big(\hat{v}_g^{k}\big)^2}\big(q_g^{\star k+1}\big)^2 = 0,\end{aligned} \tag{20}$$

where

$$a = \frac{2r}{\big(\hat{v}_g^{k}\big)^2}, \quad b = -1, \quad c = \big\langle \widetilde{p}^{\star}_{\rm dc}{}^{k+1} \big\rangle^{-2f} + \frac{2r}{\big(\hat{v}_g^{k}\big)^2}\big(q_g^{\star k+1}\big)^2.$$

Given that $\widetilde{p}_g^{\star k+1}$ has two distinct roots, the solution that minimizes the power is equal to $\frac{-b-\sqrt{b^2-4ac}}{2a}$, i.e.,:

$$\widetilde{p}_g^{\star k+1} = \frac{\rho^k}{2}\left(1-\sqrt{1 - \frac{4}{\rho^k}\left(\big\langle \widetilde{p}^{\star}_{\rm dc}{}^{k+1} \big\rangle^{-2f} + \frac{(q_g^{\star k+1})^2}{\rho^k}\right)}\right), \tag{21}$$

where $\rho^k = \frac{\left(\hat{v}_g^{k}\right)^2}{2r}$.

Consequently, after following this procedure, the final expression for the current reference, $i_g^{\star k+1}$, which also takes into account the dc-voltage regulation, is given by:

$$i_g^{\star k+1} = \frac{2\widetilde{p}_g^{\star k+1}}{\hat{v}_g^{k}}\sin(\omega t) + \frac{-2q_g^{\star k+1}}{\hat{v}_g^{k}}\cos(\omega t). \tag{22}$$

[1]A discrete form of the notch-filter can be easily designed as: $y^k = x^k b_1 + x^{k-1}b_2 + x^{k-2}b_3 - y^{k-1}a_2 - y^{k-2}a_3$, where $a_1 = 1$, $a_2 = -1.9555$, $a_3 = 0.9565$, $b_1 = a_2$, $b_2 = -1.9555$ and $b_3 = 0.9782$ for $T_s$ = 50$\mu$s.

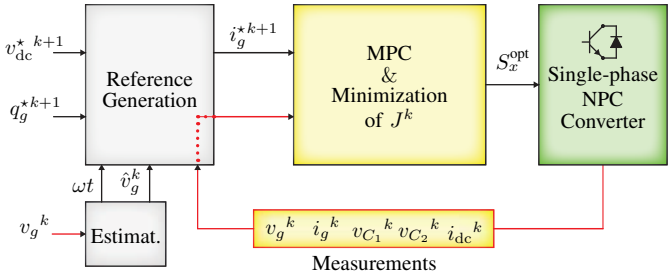


Fig. 3. Block diagram of the proposed cascade-free FCS-MPC algorithm.

Finally, the block diagram of the proposed MPC algorithm is shown in Fig. 3. The desired dc-voltage reference $v_{\rm dc}^{\star\ k+1}$ and the reactive power reference $q_g^{\star k+1}$ are first set and fed into the *reference generation* block. This block also receives the main grid parameters, i.e., peak voltage $\hat{v}_g^k$ and angle $\omega t$ from a demodulation based single-phase grid-voltage fundamental *estimation block*[2]. With this information and the measured values of $v_g{}^k$, $i_g{}^k$, $v_{C_1}{}^k$, $v_{C_2}{}^k$, and $i_{\rm dc}{}^k$ at the actual instant $k$, the reference generation block provides the future current reference, $i_g^{\star k+1}$, to transfer the required dc-power from the grid while regulating the dc-voltage. Moreover, a desired power factor is achieved by including the reactive power reference, $q_g^{\star k+1}$, into $i_g^{\star k+1}$. Then, this current reference $i_g^{\star k+1}$ is sent to the MPC block. Here, the cost function $J^k$ described in (7), which includes the current tracking error and the capacitor voltage balance, is minimized at each sampling instant $k$. Thus, the optimal switching combination $S_x^{\rm opt}$, which minimizes $J^k$, is applied at the next instant $k+1$.

## IV. Results

Simulation results have first been used to show the influence of the reference prediction horizon $N^\star$. Then, experimental results have been conducted by focusing the attention on six particular operating conditions: voltage sag in the grid, dc-load step change, volt-ampere reactive (VAR) tracking performance, dc-voltage tracking performance, cost function evaluation and uncertainties evaluation. The results presented in this section have been obtained using the following parameters: Grid voltage $v_g$ = 230 V, grid frequency $f$ = 50 Hz, dc-voltage ref. $v_{\rm dc}^\star$ = 360 V, dc-capacitors $C_{1,2}$ = 4450 $\mu$F, dc-load $r_{\rm dc}$ = 69 $\Omega$, filter inductor $L$ = 3.43 mH (0.056 pu), filter resistance $r$ = 0.1 $\Omega$, ref. pred. hor. $N^\star$ = 200, sampling period $T_s$ = 50 $\mu$s, $V_{base}$ = 230 V and $S_{base}$ = 2.75 kVA.

### A. Simulation Results

Simulated results have been obtained by means of MATLAB-Simulink and PLECS. The MPC algorithm was programmed using C-code within an S-function block. Thus, the simulated algorithm can be easily later implemented in a digital control platform for experimental validation. The single-phase NPC converter presented in Fig. 2 was tested with a linear load rated at 2.75 kW. Simulations were performed

[2]The interested reader is referred to [18] for further information about single-phase grid-voltage fundamental parameter estimation methods.

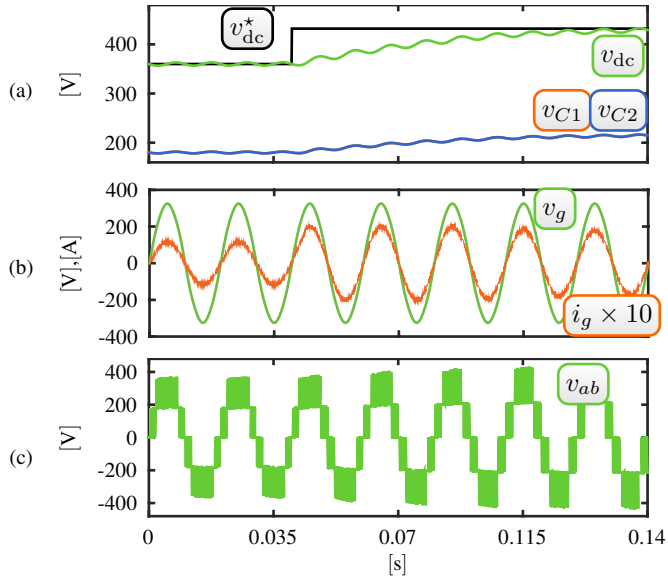


Fig. 4. Simulation results under dc-voltage step change from 360V to 432V. (a) DC-side voltages, (b) grid-voltage and grid-current and (c) converter output voltage.

considering $N^\star$ equal to $\frac{1}{2fT_s}$ which amounts to allowing the converter to reach $v_{\rm dc}^{\star\ k+1}$ approximately in a half of the fundamental period as explained in [14]. Besides the selection of $N^\star$ it is also important to define constraints such as maximum power to be extracted from the grid when any disturbance in the system is introduced. The selection of this maximum power allows the controller to reach the desired voltage reference while avoiding overshoots. In this case, $\widetilde{p}_g^{\star k+1}$ is limited in eq. (22) according to $\left|\widetilde{p}_g^{\star k+1}\right| \leq p_{g_{\max}}$, where $p_{g_{\max}}$ can be selected as the maximum power extracted from the grid.

Figure 4 details the effect of choosing $N^\star$ and $p_{g_{\max}}$ equal to 200 and 3252 W respectively. As can be clearly appreciated, the dc-voltage exhibits an inherent second harmonic component in steady state while its dynamic behavior during the step change in $v_{\rm dc}^{\star\ k+1}$ is governed by the selection of $N^\star$ and the 20 A peak saturation imposed by $p_{g_{\max}}$. Notice that due the saturation imposed by $p_{g_{\max}}$, the controller decides to limit the grid-current until the dc-voltage reach the desired voltage reference approximate in three fundamental periods. Also, both capacitor voltages maintain the same behavior. Henceforth, due to the good performance obtained, both factors will be kept at these values in the remaining experimental tests.

For comparison purpose, the same step change is performed when the NPC converter is governed by a traditional cascaded FCS-MPC and a traditional Resonant-Proportional Controller (RPC) adopted from [19] and [20] respectively. The close loop performance obtained when using the proposed algorithm considering $N^\star$ equal to 20 in order to obtain a fast dynamic response is shown in Fig. 5(a). The sub-indexes $u$ and $c$ stand for application of unconstrained and constrained active power references respectively. Results for FCS-MPC with a bandwidth (BW) equal to 70 Hz and a damping factor ($\zeta$) of 0.707 are depicted in Fig. 5(b). Here, it can be observed that large BW produces fast dynamic response but with overshoots

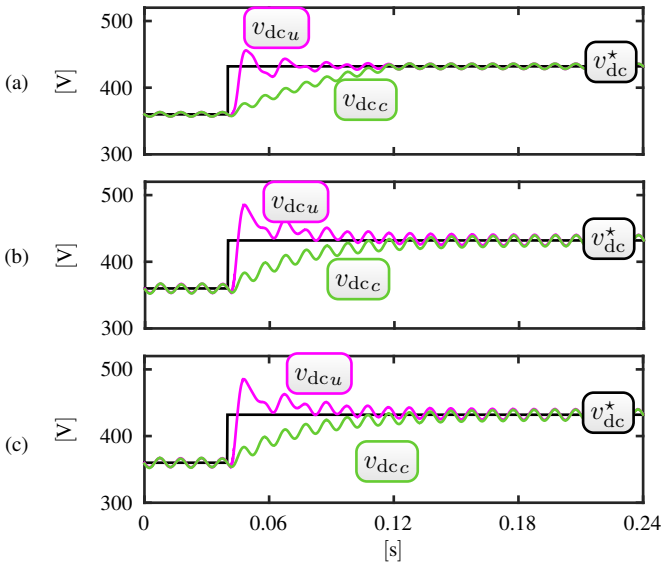


Fig. 5. Simulation results under dc-voltage step change from 360V to 432V. (a) cascade-free FCS-MPC, (b) cascaded FCS-MPC (PI-based with BW = 70 Hz and $\zeta$ = 0.707) (c) PI-based with BW = 70 Hz plus RPC with BW = 1.5 kHz and $\zeta$ = 0.707.

if the PI controller is not limited. To mitigate this, the PI is limited by the maximum allowed current to be extracted from the dc-side. In that case, the PI controller behaves slightly slower than the proposed algorithm. Note that in practice, no limitations on the references signals and/or PI controller outputs may lead in high overcurrents. Finally, a RPC current controller along with a PI controller is tested. Since the switching frequency of the RPC current controller is set to 6 kHz and the BW to 1.5 kHz, the behavior of the dc-voltage loop remains similar with cascaded FCS-MPC as shown in Fig. 5(c). Clearly, an optimization of the PI controller may be carried out to improve the dynamic response. However, the proposed method presents the capability of including several control objectives in the same cost function while easily handling system constraints. The details about the PI design have been omitted for the sake of brevity, but can be found in [20].

Additionally, Fig. 6 depicts the changes in settling time (s.t.) under the same dc-voltage step change for dc-capacitance $C_{1,2}$ variations. It can be noticed that as $C_{1,2}$ decreases, the controller is able to provide faster settling times. However, there is a trade-off between how many times the actual value of $C_{1,2}$ is smaller than its nominal value and the amount of steady state second harmonic component in $v_{\rm dc}$ ($v_{\rm dc}{}^{(2f)}$). This trade-off limits the operation of the controller to be inside a range where $v_{\rm dc}{}^{(2f)}$ takes a desired value, i.e. tolerable $v_{\rm dc}$ ripple. For that reason, besides the controller tolerates this change without knowing the actual $C_{1,2}$ value, most of single-phase converters still use bulky dc-side capacitors that reduce $v_{\rm dc}{}^{(2f)}$.

### B. Experimental Results

The effectiveness of the proposed MPC algorithm is tested in a 2.75 kVA single-phase experimental setup. The parameters of the setup are same as used in simulations. Since the

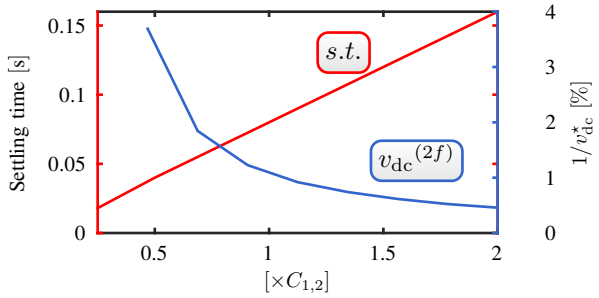


Fig. 6. Sensitivity analysis for settling time (s.t.) under dc-voltage step change from 360V to 432V and steady state second harmonic component ($v_{\rm dc}{}^{(2f)}$) with respect to dc-capacitances $C_{1,2}$.

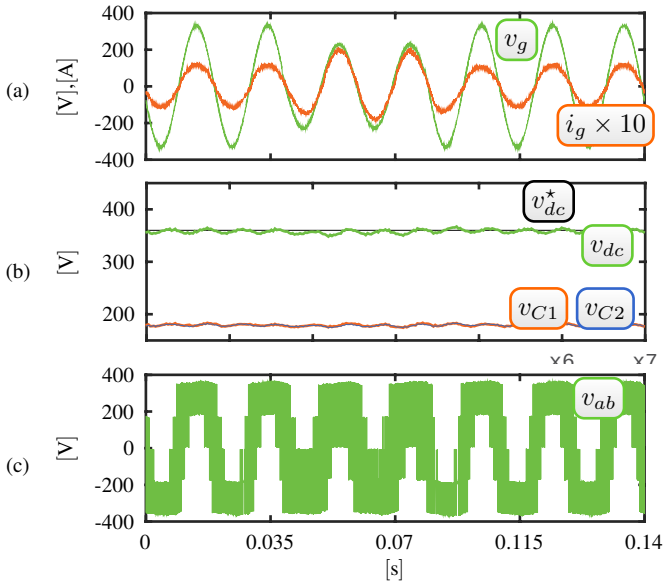


Fig. 7. Experimental results under grid-voltage sag of 30% during 40$ms$. (a) Grid-voltage and grid-current, (b) dc-side voltages and (c) converter output voltage.

proposed controller was developed for $k+1$, it is necessary to apply delay compensation for practical implementation. Although delay compensation using estimated values for $k+1$ and predictions in $k+2$ was applied, this step was intentionally omitted for the sake of brevity. For this case, the complete control loop is executed by the controller every 50 $\mu$s, while the optimal switching state is computed in 12 $\mu$s. An average switching frequency of 4.67 kHz was obtained.

*1) Grid-voltage Sag:* First, the NPC converter is operated at rated conditions with unity power factor ($q^{\star}_g = 0$), low total harmonic distortion (THD$_i$ = 3.6%) and balancing for both capacitor voltages. The normal condition is suddenly altered, by changing peak value of the grid $\hat{v}_g$ from 100% to 70% during 40$ms$. Figure 7 shows that the grid-current present an increment to compensate the variation on $v_g$ while keeping the dc-voltage around its reference.

*2) Load Step Change:* Second, a load step change from $r_{\rm dc} = 69\ \Omega$ to $r_{\rm dc} = 47\ \Omega$, equivalent to increasing the active power from 1.64 kW to 2.75 kW was produced to evaluate the dynamic behavior of $v_{\rm dc}$. As observed in Fig. 8(b) the proposed controller is able to maintain the desired value of $v_{\rm dc}$, despite the load disturbance. Moreover, the capacitor voltages remain balanced.

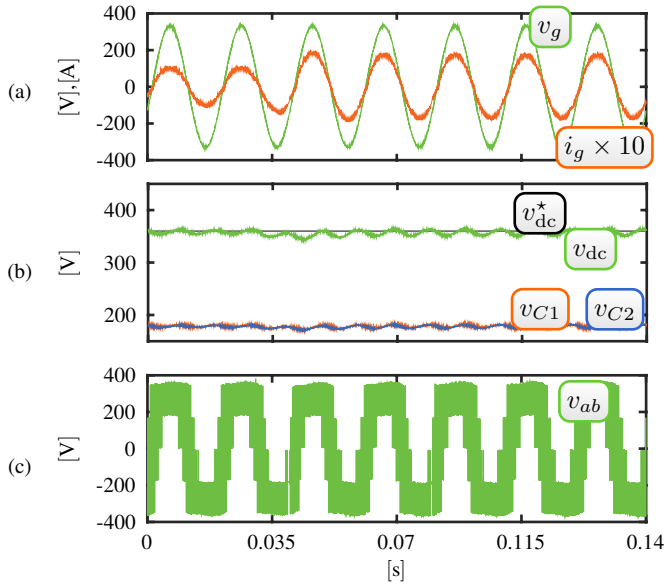


Fig. 8. Experimental results under load step change from $r_{\rm dc} = 79\ \Omega$ to $r_{\rm dc} = 47\ \Omega$. (a) Grid-voltage and grid-current, (b) dc-side voltages and (c) converter output voltage.

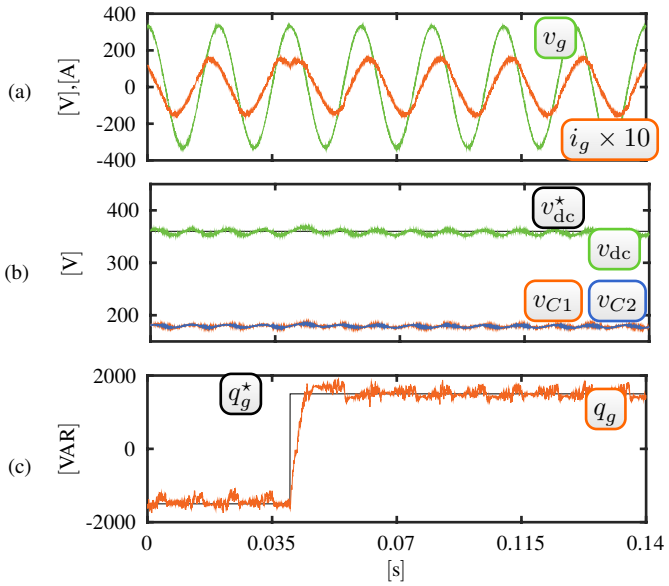


Fig. 9. Experimental results under VAR step change from $-1500$ VAR to $1500$ VAR. (a) Grid-voltage and grid-current, (b) dc-side voltages and (c) reactive power.

*3) VAR Tracking Performance:* Next, one test was performed to evaluate the tracking performance of the VAR reference. Fig. 9 depicts the experimental results under $q_g^\star$ step change from $-1500$ VAR to $1500$ VAR. Consequently, the grid-current changes from lagging the grid-voltage to leading it while maintaining the dc-voltage around its reference. Especially, Fig. 9(a) shows that the phase angle of the grid-current quickly turns $180°$ at $t = 0.04$ s, barely affecting the capacitor voltage balance.

*4) DC-voltage Tracking Performance:* A step change in the $v_{\rm dc}$ reference was produced from $360$ V to $432$ V which is equivalent to increase the active power by a factor of $1.44$. As can be clearly appreciated in Fig. 10(b), the proposed controller reaches the desired voltage reference as expected.

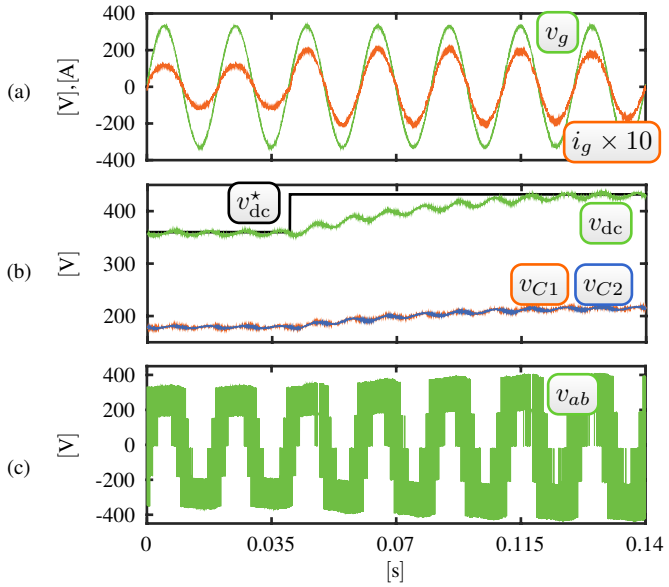


Fig. 10. Experimental results under dc-voltage step change from $360$V to $432$V. (a) Grid-voltage and grid-current, (b) dc-side voltages and (c) converter output voltage.

*5) Cost Function Evaluation:* As mentioned in the introduction, suitable cost function formulations can be adopted to permit the operation with spread and imposed grid-current harmonic spectrum. The proposed algorithm was formulated using a typical quadratic error cost function as per eq. (7) which gives a non-fixed harmonic spectrum as shown in Fig. 11(c). However, the cost function proposed in eq. (7) can be transformed into eq. (23) as explained in [15] to obtain a nearly fixed harmonic spectrum.

$$J_w^k = F(k)\left(\left(i_g^{\star k+1} - {i_g}^{k+1}\right)^2\right) + \frac{\overline{i_g}^2}{\left(\frac{v_{\rm dc}}{2}\right)^2}\left({v_{C_1}}^{k+1} - {v_{C_2}}^{k+1}\right)^2. \quad (23)$$

The function $F(k)$ is a band-stop filter which is designed to fix the harmonic spectrum of the grid-current around a desired frequency. Results obtained using the so-called frequency weighted cost function $J_w^k$ centered at 2250 Hz are shown in Fig. 11(b). Notice that due to the reduction of the switching frequency the value of $L$ was increased twice to decrease the ripple in the grid-current. Here, the corresponding spectrum (see Fig. 11(d)) shows that a nearly fixed frequency can be achieved without manipulating the equations that belong to the proposed systematic approach, i.e. $i_g^{\star k+1}$, ${v_{C_1}}^{k+1}$ and ${v_{C_2}}^{k+1}$.

Additionally, the same test used to evaluate the dc-voltage tracking performance was performed to confirm the flexibility to adopt different cost functions. In this case, a step change in the $v_{\rm dc}$ reference was produced from 360 V to 432 V. As can be clearly appreciated in Fig. 12(b), the proposed controller reaches the desired voltage reference while imposing a nearly fixed switching frequency which produces an improved waveform of the converter output voltage as shown in Fig. 12(c).

*6) Sensitivity Analysis:* Finally, a set of filter inductance value variation tests were performed to experimentally examine the tracking capabilities. These tests were carried out

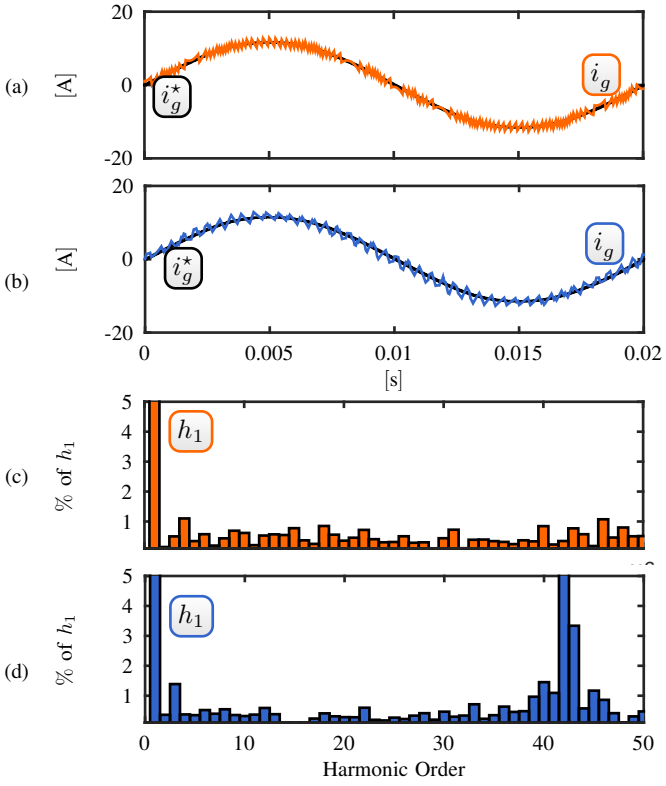


Fig. 11. Steady state evaluation for different cost functions: (a) Grid-current for a typical quadratic error cost function (see eq. (7)), (b) grid-current for a frequency weighted cost function centered at 2250 Hz (see eq. (23)), (c) grid-current harmonic spectrum for (a) and (d) grid-current harmonic spectrum for (b).

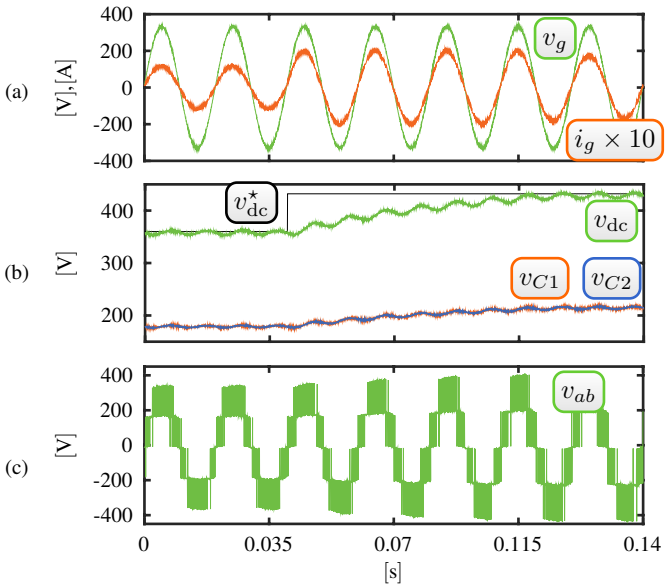


Fig. 12. Experimental results under dc-voltage step change from 360V to 432V using a frequency weighted cost function centered at 2250 Hz. (a) Grid-voltage and grid-current, (b) dc-side voltages and (c) converter output voltage.

to verify the converter limits which produces a maximum permissible steady state distortion index of the grid-current created from unknown filter parameters. Three well-known distortion indexes were evaluated – average tracking error $\overline{e}_{i_g} = |\overline{i}_g^\star - \overline{i}_g|$, $\text{THD}_{50}$ and WTHD – as shown in Fig. 13. In

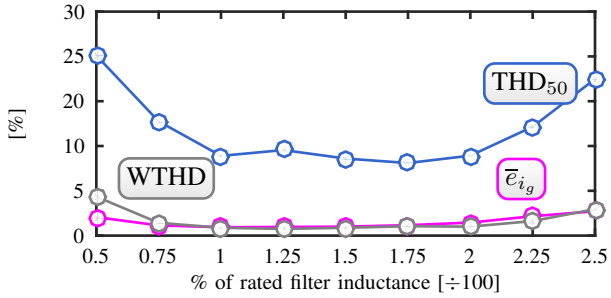


Fig. 13. Steady state distortion indexes of the grid-current under filter inductance value ($L$) variation.

this case it is recommended to avoid uncertainties greater than 2.25 or less than 0.75 times the rated value in order to maintain e.g. a $\text{THD}_{50}$ below 5%. The effect of $L$-variations over the close-loop dynamic performance remains unaltered. In these cases, the MPC saturates its output forcing $i_g$ to follow the dynamic of the plant, which behaves as a pure integrator due to $r << X_L$. Since, the variation of the $r$ value did not represent a problem for the proposed controller, these variations where not registered.

## V. Conclusion

A cascade-free FCS-MPC algorithm to govern single-phase grid-connected power converters has been presented and analyzed. The key novelty of this approach is the compatible reference design that directly allows to formulate the optimal control problem using the grid-current in the original stationary reference frame. As a result of the design procedure, no cascaded control loops are required, making the proposed cascade-free FCS-MPC algorithm easy to implement in practice. Compared with traditional implementations such as cascaded FCS-MPC, the proposed algorithm presents the capability of including several control targets in the same cost function while easily handling system constraints. Simulation and experimental results have shown that the grid-current, dc-voltage and capacitor voltages are kept around their references despite changes in the operating conditions.

## References

[1] A. Youssef, S. El Khil, and I. Slama-Belkhodja, "State observer-based sensor fault detection and isolation, and fault tolerant control of a single-phase pwm rectifier for electric railway traction," *IEEE Trans. Power Electron.*, vol. 28, DOI 10.1109/TPEL.2013.2257862, no. 12, pp. 5842–5853, Dec. 2013.

[2] C.-H. Chang, Y.-H. Lin, Y.-M. Chen, and Y.-R. Chang, "Simplified reactive power control for single-phase grid-connected photovoltaic inverters," *IEEE Trans. Ind. Electron.*, vol. 61, DOI 10.1109/TIE.2013.2271600, no. 5, pp. 2286–2296, May. 2014.

[3] M. Monfared, S. Golestan, and J. M. Guerrero, "Analysis, design, and experimental verification of a synchronous reference frame voltage control for single-phase inverters," *IEEE Trans. Ind. Electron.*, vol. 61, DOI 10.1109/TIE.2013.2238878, no. 1, pp. 258–269, Jan. 2014.

[4] Z. Yao and L. Xiao, "Control of single-phase grid-connected inverters with nonlinear loads," *IEEE Trans. Ind. Electron.*, vol. 60, DOI 10.1109/TIE.2011.2174535, no. 4, pp. 1384–1389, Apr. 2013.

[5] S. Xu, J. Wang, and J. Xu, "A current decoupling parallel control strategy of single-phase inverter with voltage and current dual closed-loop feedback," *IEEE Trans. Ind. Electron.*, vol. 60, DOI 10.1109/TIE.2011.2161660, no. 4, pp. 1306–1313, Apr. 2013.

[6] M. Vasiladiotis and A. Rufer, "Dynamic analysis and state feedback voltage control of single-phase active rectifiers with dc-link resonant filters," *IEEE Trans. Power Electron.*, vol. 29, DOI 10.1109/TPEL.2013.2294909, no. 10, pp. 5620–5633, Oct. 2014.
[7] M. Karimi-Ghartemani, S. A. Khajehoddin, P. Jain, and A. Bakhshai, "A systematic approach to dc-bus control design in single-phase grid-connected renewable converters," *IEEE Trans. Power Electron.*, vol. 28, DOI 10.1109/TPEL.2012.2222672, no. 7, pp. 3158–3166, Jul. 2013.
[8] S. Vazquez, A. Marquez, R. P. Aguilera, D. Quevedo, J. I. Leon, and L. G. Franquelo, "Predictive optimal switching sequence direct power control for grid-connected power converters," *IEEE Trans. Ind. Electron.*, vol. 62, DOI 10.1109/TIE.2014.2351378, no. 4, pp. 2010–2020, Apr. 2015.
[9] S. Vazquez, J. I. Leon, L. G. Franquelo, J. Rodriguez, H. A. Young, A. Marquez, and P. Zanchetta, "Model predictive control: A review of its applications in power electronics," *IEEE Ind. Electron. Mag.*, vol. 8, DOI 10.1109/MIE.2013.2290138, no. 1, pp. 16–31, Mar. 2014.
[10] W. Song, J. Ma, L. Zhou, and X. Feng, "Deadbeat predictive power control of single phase three level neutral-point-clamped converters using space-vector modulation for electric railway traction," *IEEE Trans. Power Electron.*, vol. 31, DOI 10.1109/TPEL.2015.2400924, no. 01, pp. 721–732, Jan. 2016.
[11] M. Preindl and S. Bolognani, "Model predictive direct speed control with finite control set of pmsm drive systems," *IEEE Trans. Power Electron.*, vol. 28, DOI 10.1109/TPEL.2012.2204277, no. 2, pp. 1007–1015, Feb. 2013.
[12] E. Fuentes, D. Kalise, J. Rodrguez, and R. M. Kennel, "Cascade-free predictive speed control for electrical drives," *IEEE Trans. Ind. Electron.*, vol. 61, DOI 10.1109/TIE.2013.2272280, no. 5, pp. 2176–2184, May. 2014.
[13] K. G. Pavlou, M. Vasiladiotis, and S. N. Manias, "Constrained model predictive control strategy for single-phase switch-mode rectifiers," *IET Power Electron.*, vol. 5, DOI 10.1049/iet-pel.2010.0253, no. 1, pp. 31–40, Jan. 2012.
[14] D. E. Quevedo, R. P. Aguilera, M. A. Perez, P. Cortes, and R. Lizana, "Model predictive control of an afe rectifier with dynamic references," *IEEE Trans. Power Electron.*, vol. 27, DOI 10.1109/TPEL.2011.2179672, no. 7, pp. 3128 –3136, Jul. 2012.
[15] P. Cortes, J. Rodriguez, D. E. Quevedo, and C. Silva, "Predictive current control strategy with imposed load current spectrum," *IEEE Trans. Power Electron.*, vol. 23, DOI 10.1109/TPEL.2007.915605, no. 2, pp. 612–618, Mar. 2008.
[16] B.-R. Lin and D.-J. Chen, "Single-phase neutral point clamped ac/dc converter with the function of power factor corrector and active filter," *IEE Proceedings - Electric Power Applications*, vol. 149, DOI 10.1049/ip-epa:20020023, no. 1, pp. 19–30, Jan. 2002.
[17] H. Akagi, E. H. Watanabe, and M. Aredes, *Instantaneous power theory and applications to power conditioning*. John Wiley & Sons, 2007, vol. 31.
[18] M. Reza, M. Ciobotaru, and V. G. Agelidis, "A modified demodulation technique for single-phase grid voltage fundamental parameter estimation," *IEEE Trans. Ind. Electron.*, vol. 62, DOI 10.1109/TIE.2014.2366720, no. 6, pp. 3705–3713, Jun. 2015.
[19] P. Acuna, L. Moran, M. Rivera, R. Aguilera, R. Burgos, and V. G. Agelidis, "A single-objective predictive control method for a multivariable single-phase three-level npc converter-based active power filter," *IEEE Trans. Ind. Electron.*, vol. 62, DOI 10.1109/TIE.2015.2393556, no. 7, pp. 4598–4607, Jul. 2015.
[20] P. Lezana, C. A. Silva, J. Rodriguez, and M. A. Perez, "Zero-steady-state-error input-current controller for regenerative multilevel converters based on single-phase cells," *IEEE Trans. Ind. Electron.*, vol. 54, DOI 10.1109/TIE.2007.891994, no. 2, pp. 733–740, Apr. 2007.

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